# A Time-to-Digital Converter Based on a Multiphase Reference Clock and a Binary Counter With a Novel Sampling Error Corrector

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***Abstract*—A new type of sampling error corrector for a time-to-digital converter (TDC) having a multiphase reference clock and a binary counter is demonstrated. With this corrector, sampling errors caused by asynchronous TDC inputs are corrected without requiring additional counters or reclocking circuits. A TDC having the corrector is implemented in 90-nm CMOS logic technology. It has 13.6-ps/least significant bit resolution and 13-bit input dynamic range. It consumes 18 mW from a 1.2-V supply and occupies a $100 \times 210$ $\mu$m$^2$ chip area.**

***Index Terms*—Counter, multiphase clock, sampling error correction, time-to-digital converter (TDC).**

## I. Introduction

A time-to-digital converter (TDC) is widely used in many applications such as nuclear experiments for locating single-shot events, laser range finders, and space science instruments. Recently, it has been employed for phase measurement in all-digital phase-locked loops (ADPLLs) [1], [2]. ADPLLs are expected to replace traditional analog phase-locked loops (PLLs) because they do not require large on-chip capacitors and do not suffer from the capacitor leakage current problem, which can seriously degrade PLL jitter performance [3]. Furthermore, ADPLLs are more immune to external noises and process parameter, voltage, and temperature (PVT) variations since many ADPLL building blocks are realized with pure digital logic circuits. However, deterministic jitters are generated in ADPLLs from quantization noises due to digitization of analog phase/frequency signals. In order to minimize these, TDC resolution should be very fine. At the same time, the TDC input dynamic range should be large in order for the ADPLL to respond to large phase errors during the PLL pull-in process.

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The conventional TDC architecture is based on a series-connected delay line (DL), including samplers [4]. In this architecture, TDC resolution is limited by the delay of a single buffer. In [5], the resolution was improved using the delay difference between unequal delay cells called vernier DL (VDL). In [6], a time amplifier and a VDL were adopted together for subpicosecond per least significant bit (LSB) resolution.

However, with the above approaches, too many delay cells and samplers are required, resulting in a large chip area if a wide input dynamic range is desired. Furthermore, since many buffers and samplers can operate all together in a narrow time window, supply currents can fluctuate, resulting in large supply noises. The circuit complexity due to the thermometer-to-binary decoder having many input bits is also a drawback. For reducing these, two-step TDC architecture was reported in [7], which employs DL-TDC as a coarse TDC and VDL-TDC as a fine TDC in order to achieve both fine resolution and wide input dynamic range. However, because the linearity of this TDC can be damaged by the mismatch between coarse TDC LSB resolution and the total range for the fine TDC, additional calibration circuits are required, which increase power consumption and chip area.

In [8]–[11], another type of TDC architecture having a multiphase reference clock as a fine TDC and a binary counter as a coarse TDC was reported, which can have a very wide input dynamic range, high resolution, good linearity, and reduced supply noise generation. However, when two TDC input signals (i.e., Start and Stop) are asynchronous to the counter clock (= the reference clock), the counter value can be erroneously sampled if input signals arrive while the counter value is changing. In order to prevent this error, two counters triggered with two different phases of the reference clock are used in [8] and [9]. However, power consumption of an additional counter can be a problem when the reference clock frequency is high. On the other hand, if a reclocking circuit is used, which synchronizes the TDC input signals to the reference clock as shown in [10] and [11], several additional D flip-flops (DFFs) triggered with the reference clock are required, which also cause a concern for increased power consumption.

In this brief, a new type of sampling error corrector (SEC) for the TDC having a multiphase reference clock and a binary counter is demonstrated. It can eliminate the counter sampling error with the addition of delay buffers and two counter samplers that operate on TDC input signals instead of TDC reference clock. This scheme can save power consumption

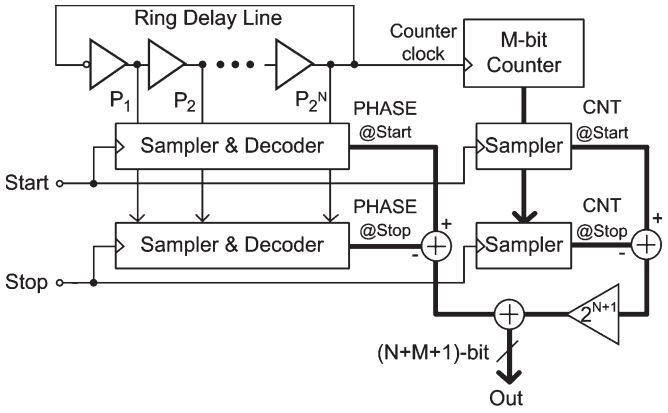


Fig. 1. TDC architecture using an RDL and a binary counter.

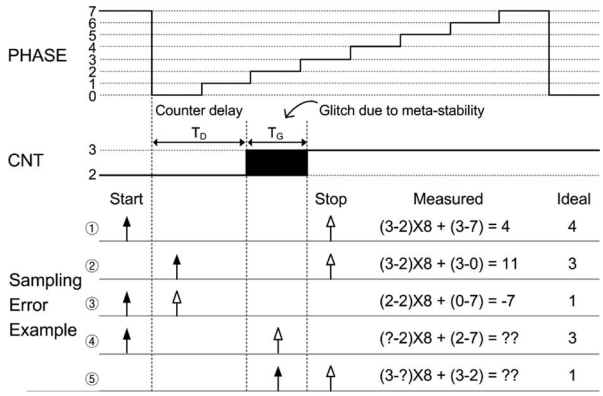


Fig. 2. Examples of possible sampling errors.

compared with the previously reported structures, particularly for ADPLL applications in which the frequency ratio between TDC reference clock and TDC input signal is large, as is the case for [10]. For feasibility demonstration of the new SEC scheme, a TDC circuit, including SEC, is fabricated and tested.

This brief is organized as follows. Section II briefly reviews the TDC architecture based on a multiphase reference clock and a binary counter. Section III explains our new SEC. Details of circuit implementation are given in Section IV. Measurement results of the fabricated chip are given in Section V. Finally, Section VI summarizes and concludes our works.

## II. TDC Using a Multiphase Reference Clock and a Binary Counter

Fig. 1 shows the TDC architecture having a multiphase reference clock and a binary counter. Although the multiphase reference clock for TDC can be realized with a ring DL (RDL) [8], [10], or a phase interpolator based on a delay-locked loop [9], [11], we will consider the architecture having the RDL for verifying the proposed SEC simply because our SEC can be adopted regardless of the multiphase generation method. RDL output signals $(P_1, P_2, \ldots P_{2^N})$ are sampled and binary decoded with $(N+1)$ bits so that RDL phase values (PHASE) at the rising edge of Start signal can be saved. PHASE is sampled again at the rising edge of Stop signal, and the PHASE increment during Start to Stop represents the quantized time difference. Higher resolution can be realized with higher RDL oscillation frequency and more phases.

The RDL dynamic range is equal to the RDL oscillation period. In order to extend this, an $M$-bit binary counter is added, which counts the number of RDL rotation. The counter output (CNT) is saved at each rising edge of Start and Stop signals. Because the period of the counter increment is $2^{N+1}$ times the RDL resolution, 1 CNT is equal to $(2^{N+1}) \times$ PHASE. Consequently, TDC output has CNT increment as the most significant bit (MSB) and PHASE increment as the LSB. With this, the dynamic range is extended $2^M$ times while TDC resolution remains the same. As a result, this architecture allows very short DL and reduces circuit complexity, chip area, and supply noise generation. Furthermore, there is not much degradation in linearity by device mismatch as the MSB of the TDC output comes from the counter that operates with the fixed frequency.

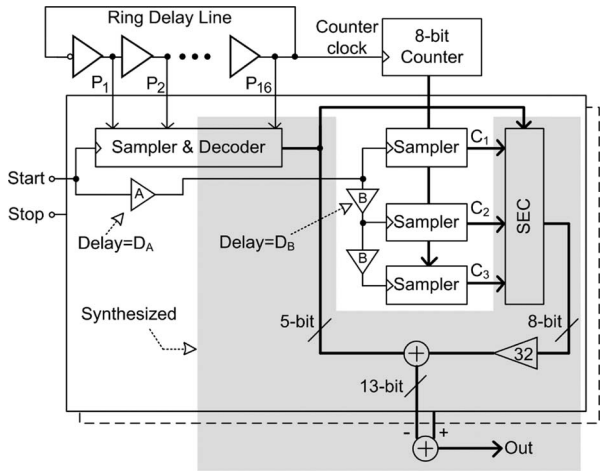


Fig. 3. Modified TDC architecture, including proposed SEC.

## III. SEC

Unfortunately, because input signals (i.e., Start and Stop) and RDL are not synchronized, the counter output can be erroneously sampled. Fig. 2 shows examples of sampling errors for the case of a four-stage RDL. The black and white arrows indicate the rising edges of Start and Stop signals, respectively. If both of two inputs are not in the counter clock-to-output delay region having time interval $T_D$ nor in the counter glitch region having time interval $T_G$ as shown in Fig. 2, there is no error (case ①). On the other hand, if one input is in the counter delay region, there is an error of $\pm 8$ for the measured output (cases ② and ③). If any input is in the glitch region, the output becomes ambiguous due to counter metastability (cases ④ and ⑤). These error probabilities are not negligible for high-performance TDC having RDL with a high oscillation frequency or a large-bit counter.

We modified the TDC architecture to prevent the sampling error, as shown in Fig. 3. A delay buffer having delay $D_A$ (see buffer A in Fig. 3) is added in front of the counter sampling clock for compensating $T_D$, and two delay buffers having delay $D_B$ (see buffer B in Fig. 3) and two counter samplers are added in order to avoid the counter glitch.

Fig. 4 explains our correction method using a timing diagram. $P_{\mathrm{RDL}}$ indicates the RDL oscillation period. Since it is not possible to fix $D_A$ at the exactly desired value $T_D$, $D_A$ is intentionally set a little smaller than $T_D$. With $T_{DC} =$

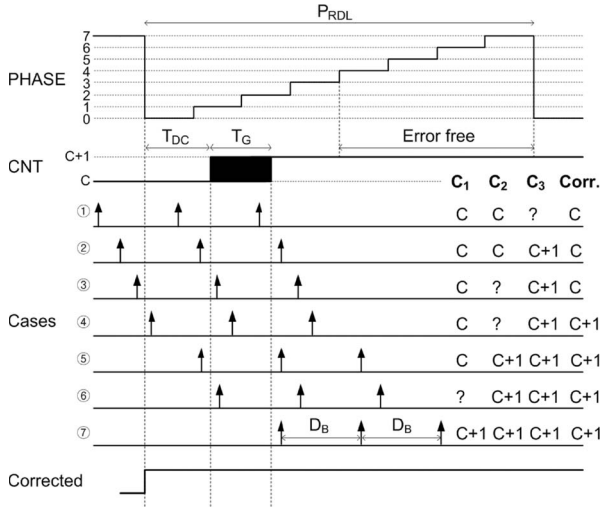


Fig. 4. Error correction examples when $N = 2$.

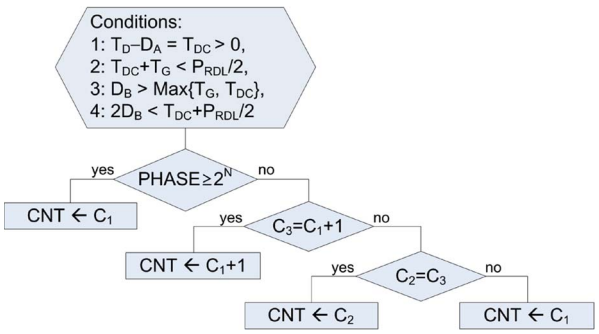


Fig. 5. Proposed simple SEC algorithm and conditions.

$T_D - D_A$ and assuming that $T_{DC} + T_G < P_{\mathrm{RDL}}/2$, there is no sampling error, as shown in Fig. 4, when the sampling point is in the second half of $P_{\mathrm{RDL}}$ where PHASE $\geq 2^N$. On the other hand, if the sampling point is in the first half of $P_{\mathrm{RDL}}$, there is a possibility for wrong CNT. In order to avoid this, the counter output is sampled three times $(C_1, C_2, C_3)$ with time interval $D_B$, where $D_B$ must satisfy the following three conditions. First, $D_B > T_G$ so that only one of three samples can be ambiguous. Second, $D_B > T_{DC}$ so that we can observe if the first sampling point is in the $T_{DC}$ region. Finally, $2 \times D_B < T_{DC} + P_{\mathrm{RDL}}/2$ so that the last sampling point cannot be in the $T_G$ region when the first sampling point is in the first half of $P_{\mathrm{RDL}}$. With these conditions, correct CNT values can be determined by the following algorithm, as shown in Fig. 4: If PHASE $\geq 2^N$, $C_1$ is correct regardless of $C_2$ and $C_3$ (cases ①, ②, and ③). If $C_3 = C_1 + 1$, $C_3$ is correct (cases ④ and ⑤). If $C_2 = C_3$, $C_2$ is correct (cases ⑤, ⑥, and ⑦). In any other cases, $C_1$ is correct. Thus, by adding two $M$-bit samplers and three delay buffers, we can always eliminate any sampling errors and obtain correct CNT values. Fig. 5 summarized the above correction algorithm.

Table I compares the required logics for our SEC with those of previously reported results. The counter and the DFF are triggered with the reference clock, and the counter sampler is triggered with TDC input signals. As can be seen, our SEC does not require logics such as additional counters and DFFs that operate with the reference clock speed. This can result in less power consumption, particularly when TDC input signals are slower than the reference clock. In [10], the TDC reference clock and input frequencies are 4 GHz and 78 MHz, respectively, and an 8-bit counter is used. With this as an example, the number of DFF triggering for a second can be determined as $10 \times 4$ GHz (8-bit counter and two reclocking DFFs) $+16 \times 78$ MHz (two 8-bit samplers) $= 41.25$ GHz. On the other hand, with our scheme, the number of operation is $8 \times 4$ GHz $+ 24 \times 78$ MHz $= 33.87$ GHz.

TABLE I
REQUIRED LOGICS FOR COUNTER SAMPLING

| | # of counter | # of DFF | # of counter sampler |
|---|---|---|---|
| **[8]** | 2 | 0 | 2 |
| **[9]** | 2 | 0 | 2 |
| **[10]** | 1 | 2 | 2 |
| **[11]** | 1 | 3 | 1 |
| **This work** | 1 | 0 | 3 |

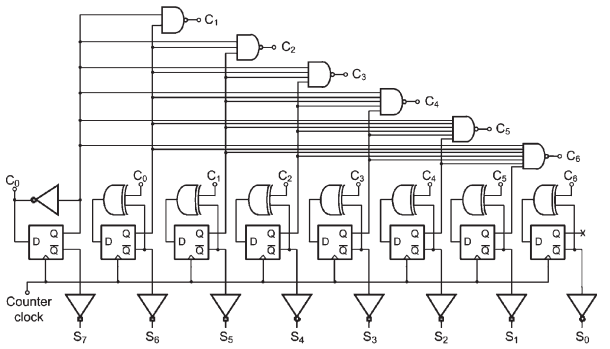


Fig. 6. Schematic of 8-bit carry-look-ahead counter.

## IV. IMPLEMENTATION

RDL oscillation frequency is restricted by the maximum operation speed of the binary counter. For our implementation, the binary counter is custom designed using an 8-bit carry-look-ahead adder circuit shown in Fig. 6. DFFs are designed using a true single-phase clocked (TSPC) DFF circuit [12] without reset function because the counter initial condition is not important. The XOR gate is designed with transmission gates. The designed counter is verified in a postlayout simulation with up to 3.3-GHz clock and 1.2-V supply.

The schematic of RDL is shown in Fig. 7. It has a ring oscillator, buffers, dummy nMOS capacitors, an operational transconductance amplifier (OTA), and an inverter. The unit delay of the delay cell in the ring oscillator should be small for high-resolution TDC, and the duty cycle error should be minimized for phase accuracy. A current-mode logic (CML)-type fully differential buffer is used as a delay cell, which has 0.4-V voltage swing and 13.6-ps delay. Because RDL oscillation frequency is inversely proportional to the number of stages and restricted by 3.3 GHz, the ring oscillator consists of 16-stage delay cells. It has a 2.3-GHz oscillation frequency and 32-level phases, resulting in total TDC output of 13 bits. Sixteen small-size CML-type buffers are connected in parallel in order to isolate output nodes from the ring oscillator. An OTA and an inverter are used to extract the single-mode full-swing clock

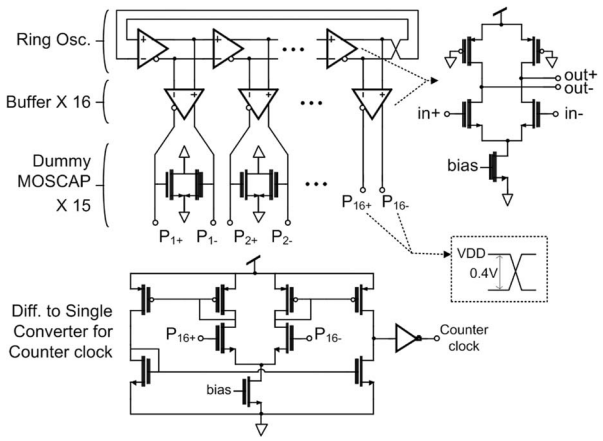


Fig. 7. Schematic of RDL.

signal from differential-mode ring oscillator outputs, i.e., $P_{16+}$ and $P_{16-}$, for the binary counter. Fifteen nMOS capacitor pairs having the same size as the nMOS input pair in the OTA are connected with the first 15-pair outputs in order to equalize the output fan-out.

Delay buffers (i.e., buffers A and B) for the SEC are made up with an inverter chain. The size of each inverter is adjusted to satisfy $D_A$ and $D_B$ determined by spice simulation in the following manner. First, $T_D$, $T_G$, and $P_{\mathrm{RDL}}$ are determined from counter circuit simulation. Then, $D_A$ is optimized to be close to $T_D - T_G$ because small $D_A$ (large $T_{DC}$) increases the lower bound of acceptable $D_B$ range, and large $D_A$ degrades the timing margin required for condition $D_A < T_D$. Finally, $D_B$ is optimized to be half of the acceptable range $\max(T_G, T_{DC}) \sim (T_{DC} + P_{RDL}/2)/2$ in order to maximize the timing margin. In our implementation, buffer A has six inverters and buffer B has four inverters.

Fig. 8 shows the postlayout simulation results of the timing margins for delay buffers with PVT variation. We simulated $T_D$, $T_G$, $P_{\mathrm{RDL}}$, $D_A$, and $D_B$ with three process corners (i.e., FF, TT, and SS) and three supply voltages (1.1, 1.2, and 1.3 V) at three temperatures ($-40$ °C, 30 °C, and 100 °C). As shown in the figure, the delay conditions are satisfied for all the cases with enough margins. Since all time variables are influenced in the same direction by PVT variation, the timing margin is maintained as all the time variables maintain their relative sizes. For example, when $T_G$ increases due to PVT variation, $D_B$ also increases, maintaining $D_B > T_G$.

Since phase sampler input signals supplied from the RDL do not have full swing, sense-amplifier-based DFFs [4] are used for the sampler, which takes differential-mode input and produces full-swing output signals. Counter samplers are designed using TSPC DFFs for low power consumption and small chip area. The phase decoders, SEC, adders, and a multiplier shown in the shaded area in Fig. 3 are synthesized using standard digital logic cells. By the postlayout simulation, we estimate that two counter samplers consume 257.8 fJ and delay buffers consume 163.8 fJ with 1.2-V supply voltage per one TDC input. Our estimation is done for energy values rather than power values since power consumption depends on TDC input frequency.

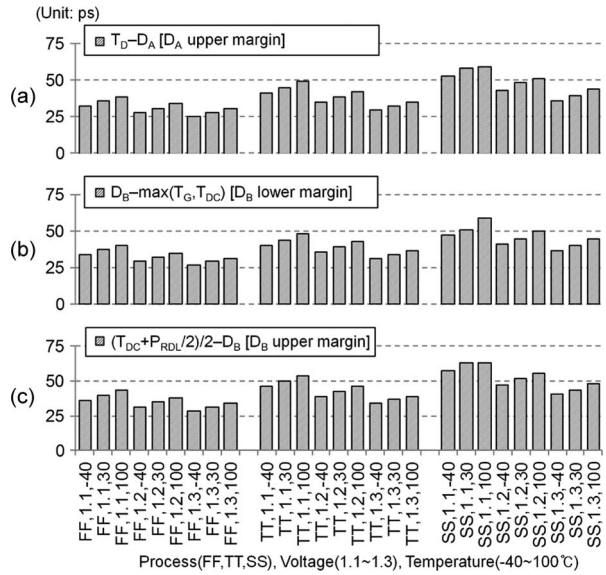


Fig. 8. Time margins of delay buffers with PVT variation (postlayout simulation results). (a) Upper margin of $D_A$. (b) Lower margin of $D_B$. (c) Upper margin of $D_B$.

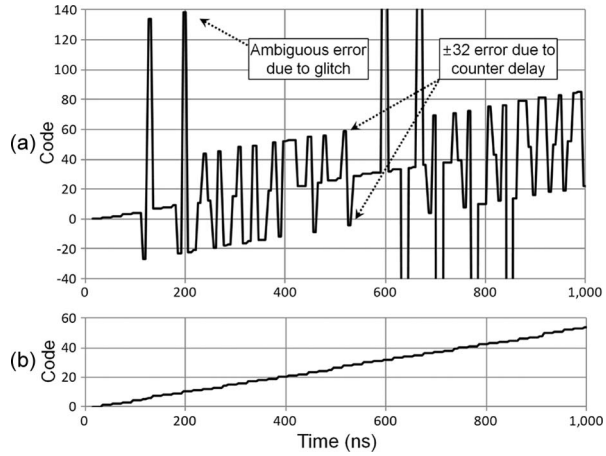


Fig. 9. TDC simulation results (a) without SEC and (b) with SEC.

Fig. 9 shows the simulation results for TDC with and without the SEC. In this simulation, Start and Stop signals having rectangular pulses of 9.995- and 10-ns periods, respectively, are used. In Fig. 9(a), two types of errors can be observed. One is due to the glitch of the counter, and the other is due to the counter delay. SEC successfully corrects these errors, as shown in Fig. 9(b). The designed TDC circuit is fabricated using a 90-nm CMOS logic process. Fig. 10 shows the microphoto of the prototype chip. The TDC chip size is $100\ \mu\mathrm{m} \times 210\ \mu\mathrm{m}$.

## V. Measurement Results

Fig. 11 shows the measurement setup. Two pattern pulse generators (PPGs) for Start and Stop signals are synchronized and connected to a PC through IEEE-488 general-purpose interface bus cables. The time difference $\Delta_T$ between Start and Stop signals, both having 3.9 MHz, is controlled by a Labview program with a 1-ps delay step. Receiving two pulse signals from two PPGs, the TDC chip measures the time difference and produces a 13-bit digital code. The code is serialized using an

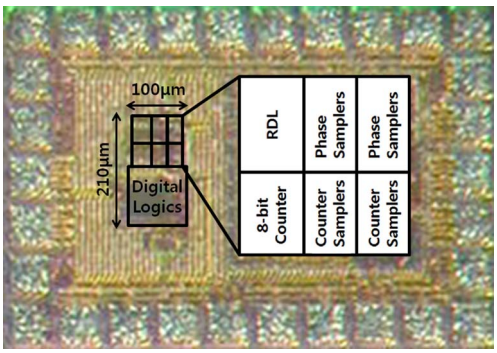


Fig. 10. Microphoto of fabricated chip.

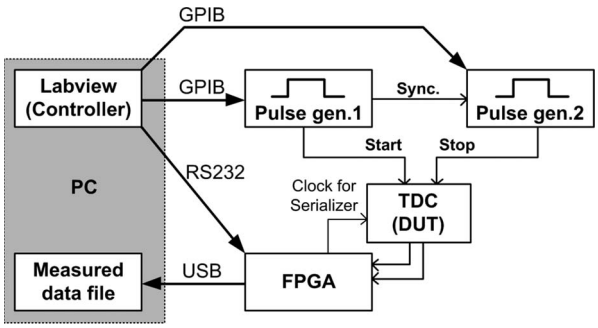


Fig. 11. Measurement setup.

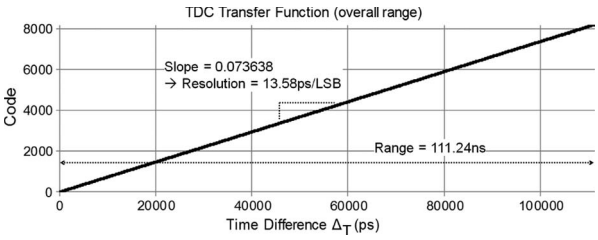


Fig. 12. Measured TDC transfer function with 1.2-V supply.

external clock from a field-programmable gate array (FPGA) and delivered to the FPGA. The FPGA parses the device under test output and passes it to the PC through a universal serial bus cable. Finally, the measured data are stacked in the PC.

The TDC consumes 18 mW from a 1.2-V supply. The measured TDC transfer function with 1.2-V supply is shown in Fig. 12. The resolution is 13.58 ps/LSB, and the maximum input dynamic range is 111.24 ns. From these results, we can confirm that RDL oscillation frequency is 2.3 GHz $(1/(2 \times 16 \times 13.58 \text{ ps}))$ and the 8-bit counter, as well as the SEC, successfully operates. The dependence of the TDC transfer function on supply voltage is shown in Fig. 13. As can be seen, our SEC successfully operates with supply voltages from 1 to 1.4 V.

## VI. Conclusion

This brief has presented a new type of simple SEC for TDC having an RDL and a binary counter. Using our SEC, the counter value can be sampled without any ambiguity although the sampling clock is not synchronized with the counter clock.

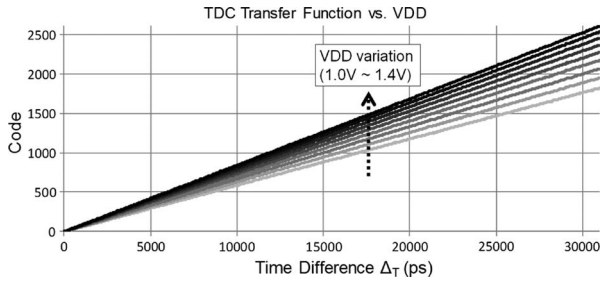


Fig. 13. Measured TDC transfer function on supply voltage.

A TDC circuit, including SEC, is successfully demonstrated. The circuit has 13.6-ps/LSB resolution, 13-bit input dynamic range, consumes 18 mW from a 1.2-V supply, and has a $100 \times 210$ $\mu$m$^2$ chip area. It is expected that our simple SEC can be useful for many applications that desire asynchronous counter sampling.

## Acknowledgment

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## References

[1] R. B. Staszewski, D. Leipold, C. M. Hung, and P. T. Balsara, "TDC-based frequency synthesizer for wireless applications," in *Proc. IEEE RFIC*, Jun. 2004, pp. 215–218.

[2] M. Song, Y. Kwak, S. Ahn, W. Kim, B. Park, and C. Kim, "A 10 MHz to 315 MHz cascaded hybrid PLL with piecewise linear calibrated TDC," in *Proc. IEEE CICC*, Sep. 2009, pp. 243–246.

[3] R. Holzer, "A 1 V CMOS PLL designed in high-leakage CMOS process operating at 10-700 MHz," in *Proc. IEEE ISSCC*, Feb. 2002, pp. 272–466.

[4] R. B. Staszewski, S. Vemulapalli, P. Vallur, J. Wallberg, and P. T. Balsara, "1.3 V 20 ps time-to-digital converter for frequency synthesis in 90-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 3, pp. 220–224, Mar. 2006.

[5] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a vernier delay line," *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, Feb. 2000.

[6] M. Lee and A. A. Abidi, "A 9 b, 1.25 ps resolution coarse–fine time-to-digital converter in 90 nm CMOS that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, Apr. 2008.

[7] C. Hwang, P. Chen, and H. Tsao, "A high-precision time-to-digital converter using a two-level conversion scheme," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 4, pp. 1349–1352, Aug. 2004.

[8] T. Watanabe, Y. Makino, Y. Ohtsuka, S. Akita, and T. Hattori, "A CMOS time-to-digital converter LSI with half-nanosecond resolution using a ring gate delay line," *IEICE Trans. Electron.*, vol. E76-C, no. 12, pp. 1774–1779, Dec. 1993.

[9] M. Mota, J. Christiansen, S. Débieux, V. Ryjov, P. Moreira, and A. Marchioro, "A flexible multi-channel high-resolution time-to-digital converter ASIC," in *IEEE Nucl. Sci. Symp. Conf. Rec.*, Oct. 2000, vol. 2, pp. 9/155–9/159.

[10] K. Takinami, R. Strandberg, P. C. P. Liang, G. G. Mercey, T. Wong, and M. Hassibi, "A distributed oscillator based all-digital PLL with a 32-phase embedded phase-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2650–2660, Nov. 2011.

[11] A. Mäntyniemi, T. Rahkonen, and J. Kostamovaara, "A 9-channel integrated time-to-digital converter with sub-nanosecond resolution," in *Proc. IEEE Int. MWSCAS*, Aug. 1997, vol. 1, pp. 189–192.

[12] Q. Huang and R. Rogenmoser, "Speed optimization of edge-triggered CMOS circuits for gigahertz single-phase clocks," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 456–465, Mar. 1996.