A Tissue Impedance Measurement Chip for Myocardial Ischemia Detection

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Abstract—In this paper, the design of a specific integrated circuit for the measurement of tissue impedances is presented. The circuit will be part of a multi-micro-sensor system intended to be used in cardiac surgery for sensing biomedical parameters in living bodies. Myocardium tissue impedance is one of these parameters which allows ischemia detection. The designed chip will be used in a four-electrode based setup where the effect of electrode interfaces are cancelled by design. The chip includes a circuit to generate the stimulus signals (sinusoidal current) and the circuitry to measure the magnitude and phase of the tissue impedance. Several integrated circuits have been designed, fabricated and tested, in a 0.8-μm CMOS process, working at 3 V of power supply. Some of them including building blocks, and other with the whole measurement system. Experimental tests have shown the circuit feasibility giving expected results for both in-vitro and in-vivo test conditions.

Index Terms—Analog integrated circuits, G_m-C filters, impedance measurement circuits, myocardial ischemia detection.

I. INTRODUCTION

IMPEDANCE is a useful parameter for determining the properties of biological tissues because they are electrically conductives. Based on this parameter, physiological events can be monitored, in particular those related with human body performance. Advantages of microelectronics systems applied to health care solutions are to provide small size devices, possibility to avoid wires for telemetry transmission of signal and power, easy portability, long time implant for low power circuits and the possibility of improving the sensing of weak signals (in the order of milivolts) by taking them out *in-situ*[1]–[4].

This paper presents the design and experimental results of an integrated circuit for tissue impedance measurement. In the case of myocardium tissue, it has been shown that when heart ischemia is going to be produced, the myocardium impedance suffers changes both in magnitude and phase. Fig. 1 illustrates a typical evolution of the heart tissue impedance magnitude when occlusion of the coronary artery is done [5]. The occlusion starts in $t = 0$, and after one hour, the magnitude of impedance becomes 100% higher than the initial value. The herein proposed

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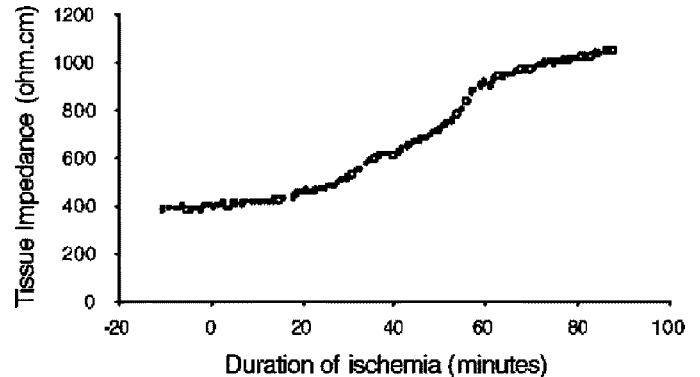
Fig. 1. Evolution of the tissue magnitude impedance under ischemia conditions [6].
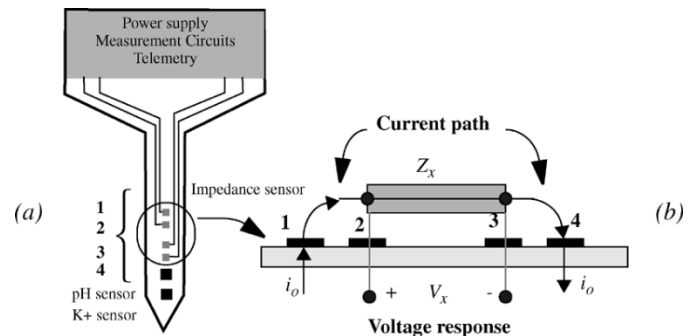

Fig. 2. (a) System proposal for measurement of myocardial tissue impedance, [*pH*] and [K^+]. (b) Four-wire scheme for Z_x impedance measurement. (Terminals 1 and 4 are for excitation and terminals 2 and 3 are for measure.)

fully-integrated impedance measurement circuit allows to acquire and process data *in-situ*, and to transmit them by telemetry or wires. Output data will be acquired by a computer in order to be post-processed. The circuit is part of a multi-micro-sensor system developed in the context of a multidisciplinary project[1] for ischemia monitoring. The idea of the measurement system is a needle (Fig. 2) containing four electrodes, together with other specific silicon integrated sensors to obtain *pH* and K^+ concentrations [6].

The paper is organized as follows. Section II gives a general overview of the whole measurement system and introduces the impedance measurement scheme, its more relevant problems to be solved, and the required circuits. Main circuit blocks, their design specifications and trade-offs, are described in Section III. A chip in a 0.8-μm CMOS process working at 3 V of
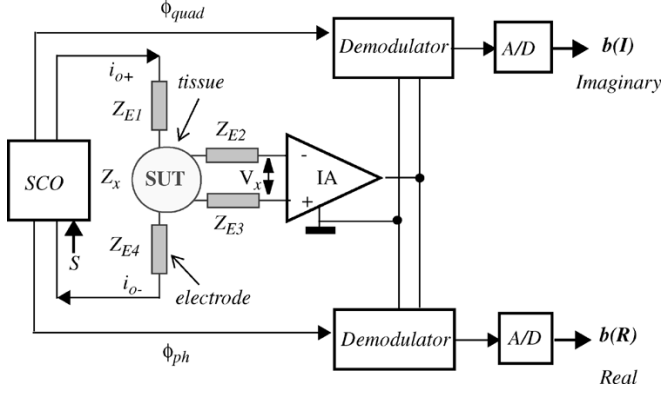
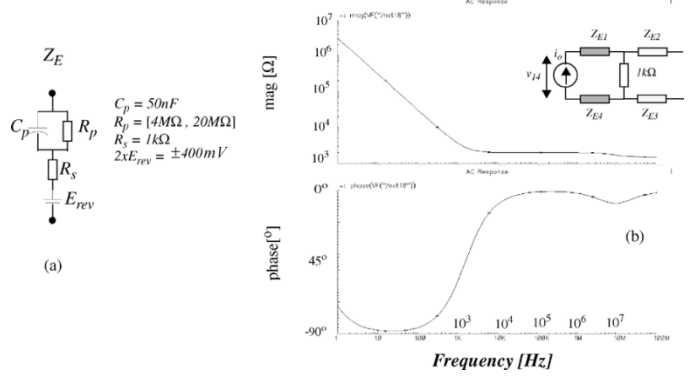Fig. 3. Blocks involved in the impedance measurement system and its connection to the four wires system.

Fig. 4. (a) Electrode model. (b) Frequency response: ac-magnitude and phase of the input impedance of the four-wires system applied to a 1-kΩ load.

power supply was designed to validate these blocks; some experimental results of the blocks are also reported in Section III. The whole impedance measurement system was also fabricated and its experimental results, in several test conditions, will be shown in Section IV. Conclusions are highlighted in Section V.

II. SYSTEM DESCRIPTION

The proposed measurement method is based on a four-electrodes system (Z_{E1}[2] to Z_{E4}) shown in Fig. 3. A reference current i_o (denoted as i_{o+} and i_{o-} in practical situations) is injected through two electrodes (Z_{E1}, Z_{E4}) to stimulate the tissue sample (SUT) of unknown impedance Z_x. The other two electrodes (Z_{E2}, Z_{E3}) take out the SUT voltage response, V_x, whose value is related to the magnitude and phase of Z_x. This voltage response is processed to obtain the real and the imaginary parts of Z_x. Two circuits are necessary to do that: 1) stimulation circuit for current generation and 2) signal processing circuits, for voltage response sensing and impedance parameters extraction (real and imaginary components of Z_x).

The excitation part consists of an oscillator delivering a sinusoidal current signal of different frequencies [sinusoidal current generation (SCO) in Fig. 3]. The maximum amplitude and optimal frequencies for this current are imposed by medical safety conditions. Frequency selection is done by means of a digital control signal, S. The signal acquisition circuitry is composed by an instrumentation amplifier (IA) for V_x measurement, two demodulators for real and imaginary components of Z_x extraction, and two analog- to-digital converters (ADCs) to deliver the imaginary and real parts in digital domain.

Accurate methods for impedance measurements have been already developed [7]–[9]. Our circuit is based on the two-phase reference coherent demodulation method [9], which gives simultaneously the real ($\mathrm{Re}(Z_x)$) and imaginary ($\mathrm{Im}(Z_x)$) components of a complex impedance, Z_x. For that, two demodulators with the corresponding clock phases, ϕ_{ph} and ϕ_{quad}, in quadrature of phase are required. The outputs of the circuit are two digital signals $b(R)$ and $b(I)$, corresponding to the digital representation of the real and imaginary parts of the tissue impedance Z_x.

[2]We will refer electrode 1 as Z_{E1}, that is, the electrode whose impedance is Z_{E1}.

The whole system must fulfill the following general specifications. For safety conditions, the excitation current must be always below 5 μA_{rms}, with frequency in the range 1 to 20 kHz [5]. The expected range of magnitudes to be measured go from 100 Ω to 10 kΩ, while the phase is in the range of [0,30°]. However, the main objective is not to obtain precise values of these parameters, but to detect large changes (see Fig. 1). The effects of the electrodes should be considered in the design of each block. In this sense, the fabricated electrodes included in the Si-based needle were characterized and a model for them was developed. This model was validated with results obtained measuring the electrodes in a saline solution (0.9%NaCl solution). Details of this model are given in Fig. 4, together with its validation in an application example (a 1-kΩ resistance measurement). As it can be seen, the magnitude and phase of the electrode impedance are frequency dependent. The magnitude takes a high value for low frequencies, while it is nearly constant ($2R_s$) at the frequency range of interest. In these conditions, care must be taken in defining the SCO output impedance because any offset in i_o will cause an excessive output voltage.

Mismatch in contact potential of the electrode model (E_{rev}) could occur but this has been considered in the values taken for the $2 \times E_{\mathrm{rev}}$ range (± 400 mV) for the four wire electrodes model [Fig. 4(b)]. This range will define the common-mode input range of the IA.

III. CIRCUIT DESIGN

In this section, the design in CMOS technology of the set of circuits introduced in Section II will be described.

A. Signal Excitation Circuit

This circuit drives a sinusoidal current to the SUT. The objective is to produce a voltage response when the current i_o passes through the load. For a heart tissue, the specifications are the following. The current must be always below 5 μA_{rms}, over an expected load range of 100 Ω–10 kΩ. For that, the output resistance of the SCO must be high enough to reduce load effects. Three different frequencies 1, 8, and 16 kHz are generated according to a 2-bit digital word S.

The SCO block diagram is shown in Fig. 5(a). It uses a g_m-C ramp integrator and a second-order bandpass filter to generate the sinusoidal output current. Both were implemented as proposed in [10]–[13], and their schematics are shown in Fig. 5(b)
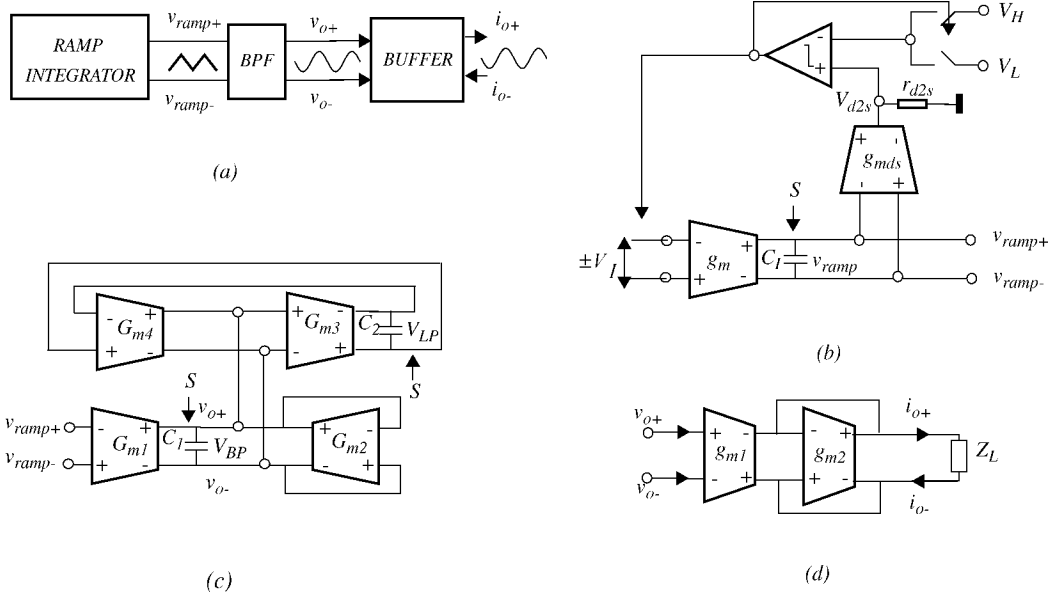
Fig. 5. (a) Circuit blocks for SCO. (b) Ramp generator. (c) Second-order bandpass filter. (d) Output buffer with load.

and (c), respectively. A buffer to adapt the SCO output stage to the load specifications of the four-electrode system is also designed [Fig. 5(d)]. The oscillation frequencies generated by the circuit are given by

$$f_{\text{osc}} = \frac{g_m \cdot V_I}{2(V_H - V_L)C_I} \tag{1}$$

where V_I is a constant reference voltage generated on-chip, g_m is the transconductance of the operational transconductance amplifier (OTA), C_I the integrating capacitor, and $(V_H - V_L)$ the voltage swing allowed for the integrator output. Input S is the digital control signal that selects three different values for C_I, making possible the generation of three frequencies (1, 8, and 16 kHz) by programming a capacitor bank. The OTAs have been designed with transistors working in weak inversion region to fulfil the circuit specifications with low power consumption [10].

The biquad filter in Fig. 5(c) [14] generates the bandpass function $(V_{\text{BP}}/V_{\text{in}})$, given by

$$\frac{V_{\text{BP}}(s)}{V_{\text{in}}(s)} = -\frac{s \cdot \frac{G_{m1}}{C_1}}{s^2 + s \cdot \frac{G_{m2}}{C_1} + \frac{G_{m3}G_{m4}}{C_1 C_2}}. \tag{2}$$

All the OTA transconductances are equal $G_{mi} = G_m$ ($i = 1,2,3,4$) as well as the integrating capacitors $C_1 = C_2 = C$. This means that the cutoff frequency is $f_o = G_m/2\pi C$ and $Q = 1$. For the case of $f_o = 1$ kHz, and a $C = 15$ pF, a G_m of around 100 nS for each OTA is required. For transistors in weak inversion, a current of 10 nA is employed to bias the input differential pair.

The output buffer is a V/I converter that defines and limits the amplitude of the current oscillator, reducing also the load effects derived from the electrodes electrical performance. Considering a Z_L load composed by the series of two electrodes and the tissue to be measured, the buffer we propose has a high-pass output impedance. That is, it has a low output impedance at low frequencies (near dc and below the band of interest) and a high and constant output impedance in the 1- to 20-kHz frequency
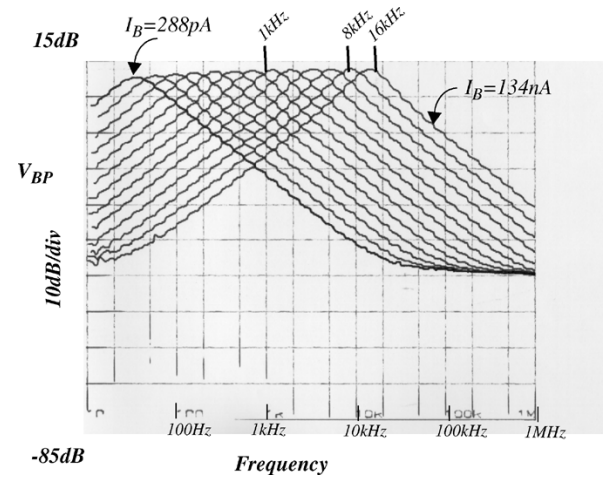

Fig. 6. Experimental bandpass filter transfer functions showing the f_o programming.

band. This allows to minimize the effects of any offset in the V_{BP} differential signal [13]. This solution is more compact and requires less area than classical approaches that employ discrete highpass networks for this purpose [2].

Some experimental results from a chip that was designed, in a 0.8-μm CMOS process working at 3 V of power supply, to validate these blocks appear in Fig. 6 (the filter response for different bias currents) and in Fig. 7 (the SCO output current for different frequencies). High precision in bias currents is not always required for this application in order to generate the excitation frequencies, because they do not need to be precisely generated. What is important is the good matching between the oscillation frequencies of the ramp generator and the cutoff frequencies of the bandpass filters. It can be observed in Fig. 7 that when frequency increases, the amplitude of the SCO output decreases. This is due to some mismatch between the frequency of the ramp signal and the filter central frequency. A tuning mechanism would be necessary to correct this effect; however in the
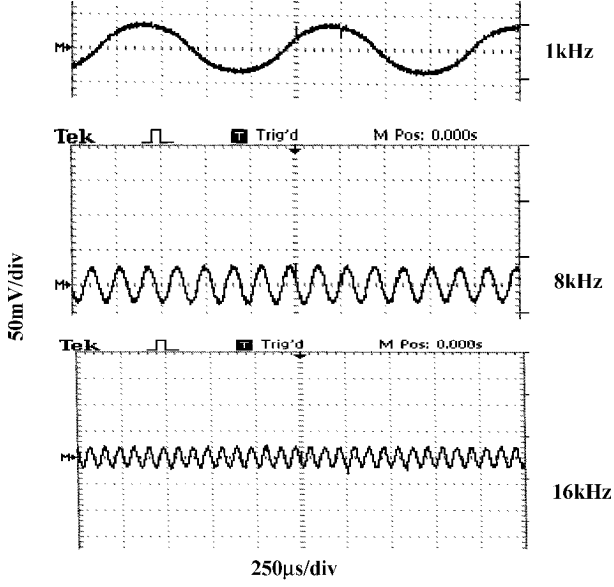
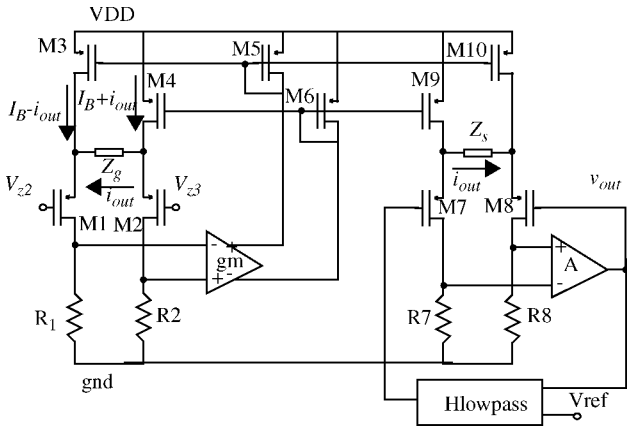Fig. 7. SCO current output over a load of 10 kΩ.

Fig. 8. IA circuit schematic.

present circuit it was no included and hence we have had to calibrate the experimental measurements performed at different frequencies, with the whole system. The calibration procedure will be explained in Section IV.

B. IA

Specifications for the IA are specially strong due to the input voltage levels coming from the electrodes. In particular, the contact potential in the interface electrode-tissue, E_{rev}, will cause a high swing of the input common-mode voltage, and even a large differential dc voltage level. The dc levels imposed by contact potentials are in the ± 400-mV range, and they are significantly larger than the signals to be amplified (from 0.5 to 50 mV as maximum). We have selected a 20-dB gain for the amplifier, and a dynamic range of 74 dB. The CMRR required is of 110 dB. The circuit designed as amplifier is based on that reported in [15]. Its schematic is shown in Fig. 8. It relies on V-I and I-V conversions using linearization circuits at the input and output stages. It has a bandpass-type transfer function hence filtering low frequency noise and the dc differential level from the electrodes.
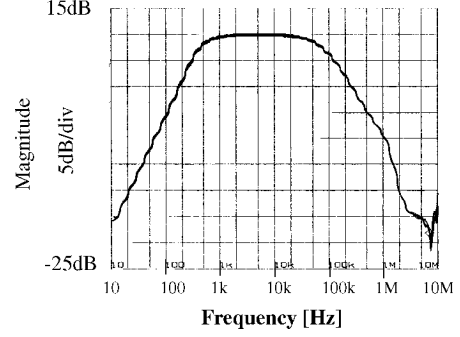

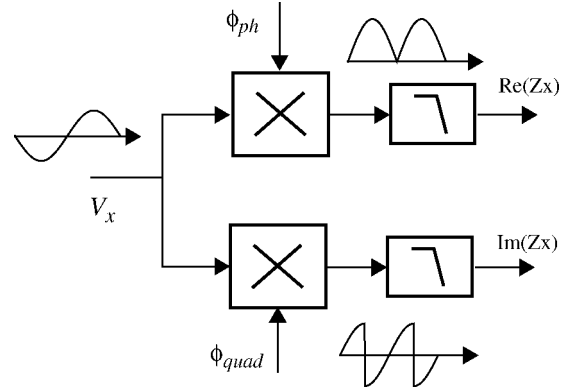Fig. 9. IA experimental frequency response.

Fig. 10. Demodulation principle.

Low-pass filtering is performed by Z_s, while the highpass function is implemented by feedback with the *Hlow-pass* block.

In Fig. 9, the bandpass frequency response of the implemented IA is shown. The measured common-mode range was 586 mV, the differential dc range was 524 mV, and the bandwidth is from 980 Hz to 19.7 kHz.

C. Impedance Measurement Circuit

From the IA, a sinusoidal waveform with amplitude and phase proportional to the impedance, Z_x, of the tissue is obtained. Two phase reference coherent demodulation method is employed for extracting the value of the magnitude and phase of Z_x [7]–[9]. Its operational principle is illustrated in Fig. 10. This method requires two clocks signals in-quadrature (ϕ_{ph}, ϕ_{quad}) to perform the modulation operation. For a given phase shift α between i_o and V_x, the dc levels obtained at the demodulator outputs are proportional to the $\cos(\alpha)$ and $\sin(\alpha)$ functions, being these the real and imaginary components of Z_x

$$\text{Re}(Z_x) = \frac{2V_{xo}}{\pi} \cdot \cos\alpha \qquad (3)$$

$$\text{Im}(Z_x) = \frac{2V_{xo}}{\pi} \cdot \sin\alpha \qquad (4)$$

where V_{xo} is the amplitude of the IA output. A fourth-order lowpass filter (40-dB/dec attenuation), with low cutoff frequency around 200 Hz is necessary to select these dc signals and maintain the ripple errors below 1% at 2-kHz frequency. This filter has been implemented by cascading two biquad circuits, with input pair transistors working in weak inversion [10]. In order to reduce the capacitor area, bias currents of 2 nA have been used to obtain low transconductance to capacitance ratios.
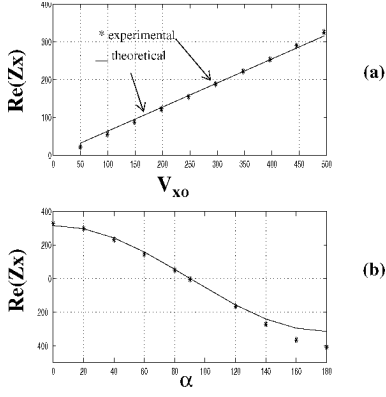
Fig. 11. Demodulator response obtained: (a) changing the input amplitude [mV] with phase $\alpha = 0°$ and (b) changing the input phase with amplitude of $V_{xo} = 349$ mV.
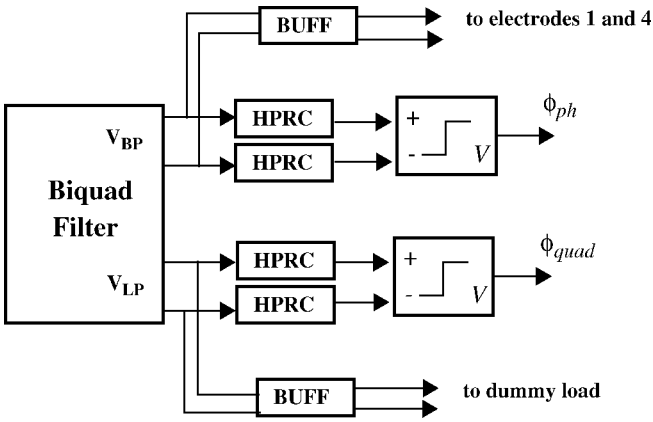

Fig. 12. Quadrature signals generation.

Fig. 13. Measured in-quadrature signals.
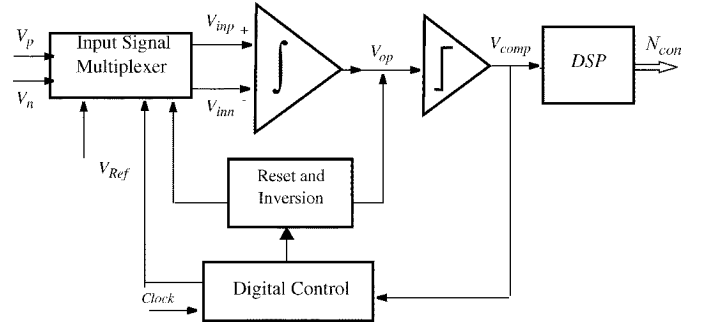
Fig. 14. Conceptual schematic of the incremental ADC.

Fig. 11 shows the experimental results taken at the $\mathrm{Re}(Z_x)$ output. Using a clock generator triggered by a differential signal controlling the phase shift between them, the effects of a R and a *RC* loads have been emulated. For the first situation, the results represented in Fig. 11(a) have been measured by changing the input amplitude for zero phase conditions. On the other hand, Fig. 11(b) shows the evolution of the output, in the *RC* load case, for a phase change in the range of [0,180°] and a constant input voltage of 349 mV. The frequency in both cases was 1 kHz.

D. Clock Phases Generation Circuit

As said before, implementing the coherent demodulation requires two 90° delayed square signals. We generate these signals using the two output voltages (V_{LP} and V_{BP}) of the filter in the SCO [Fig. 5(b)] that are 90° shifted. The block diagram of this generator is shown in Fig. 12. Any offset has been eliminated by a first-order high-pass passive filter (HPRC) in each channel. Each *C-R* filter is composed by a capacitor $C = 10.8$ pF and two saturated MOS transistors in weak inversion working as a resistor, with a bias current of 1 nA. A buffer has been also included at the low-pass output in order to make equal the load conditions in the low-pass (V_{LP}) and bandpass (V_{BP}) filter outputs. Two differential comparators [16] are used to finally obtain the ϕ_{ph} and ϕ_{quad} signals. Fig. 13 illustrates the two in-quadature signals obtained experimentally at 1 kHz.
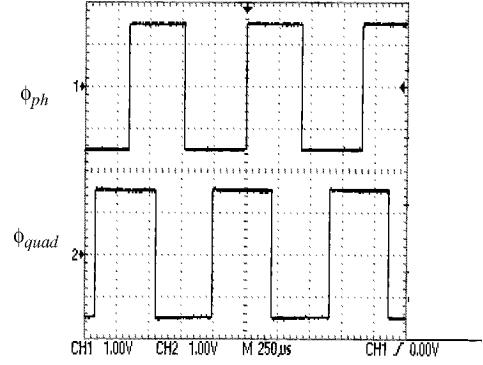
The accuracy in the generation of the in-quadrature signals ϕ_{ph} and ϕ_{quad} is affected by the mismatches between the highpass filters and the comparators. Considering a $\Delta\theta$ deviation of the $\pi/2$ nominal value and making a Taylor series approximation, the real and imaginary parts of the impedance will be given as

$$\mathrm{Re}(Z) = |Z_x| \cdot \cos\alpha \qquad (5)$$
$$\mathrm{Im}(Z) \approx -|Z_x| \cdot \sin\alpha \cdot (1 + \Delta\theta). \qquad (6)$$

Both (5) and (6) can be used for the calculus of the new magnitude and phase

$$\mathrm{Magnitude}' \approx |Z_x| \cdot \sqrt{1 + \sin\alpha^2 \cdot 2\Delta\theta} \qquad (7)$$
$$\mathrm{Phase}' \approx \mathrm{atan}(\tan\phi \cdot [1 + \Delta\theta]). \qquad (8)$$

This means that for a maximum phase angle of $\alpha = 30°$, and $\Delta\theta = 5°$, the errors are of a 1.08% in magnitude and 2.11° in phase (for $\Delta\theta = 10°$, 2.5% and 4.14° are obtained, respectively). Errors in clock signals below 5° should be obtained by design.

E. ADC

The specifications for the targeted ADC are 12 bits, a 50-kHz clock, and an input range of ± 0.5 V. A first-order incremental ADC [17] has been chosen because it gives good accuracy for low frequency conversion rates. A continuous-time implementation was realized, in which the integration function is performed by using the OTA-C technique [18], [19]. The general block diagram of the ADC converter is shown in Fig. 14, and the diagram of its analog part is in Fig. 15. It includes a controlled two-input integrator and a comparator. The input *mux* block is
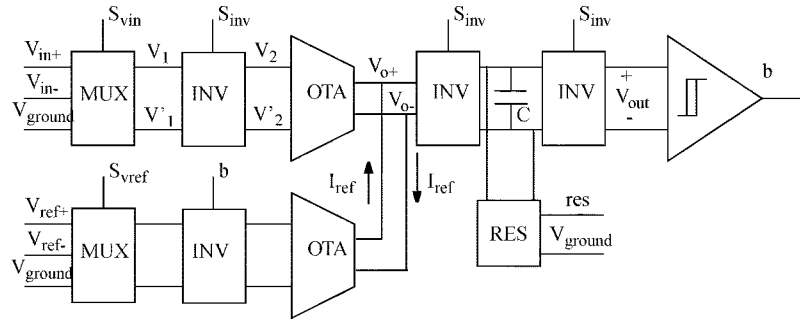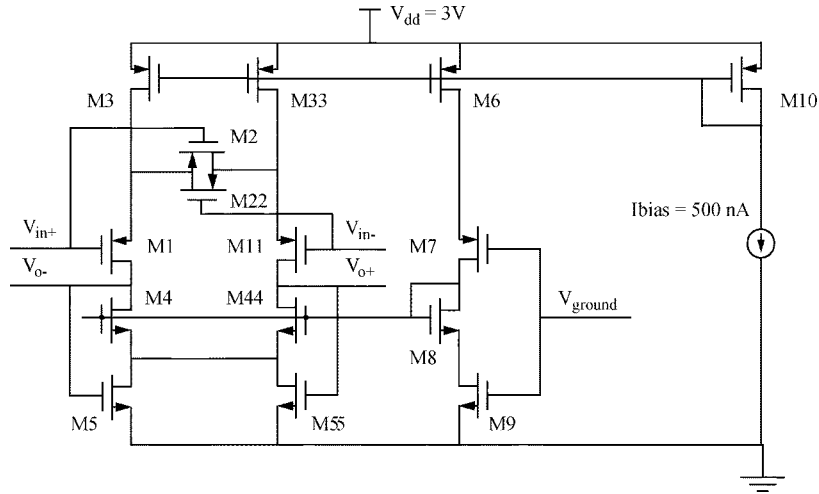
Fig. 15.   ADC analog blocks.
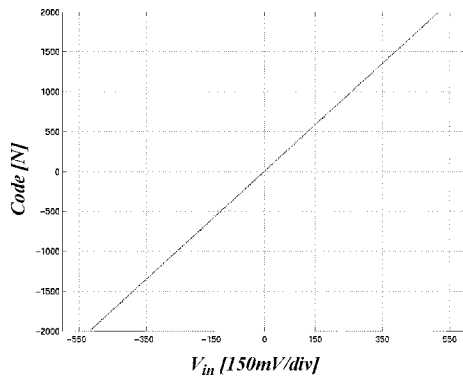

Fig. 16.   Schematic of the OTA.

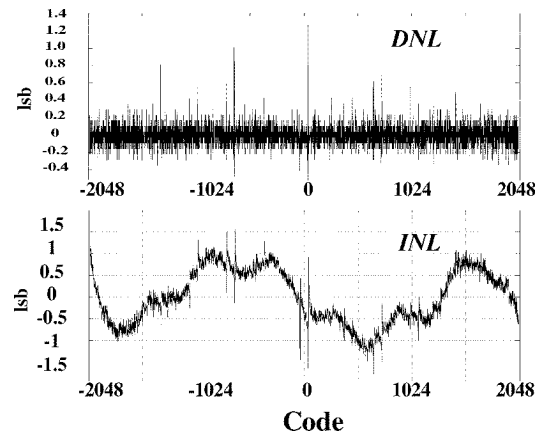Fig. 17.   Experimental transfer function for $n = 12$ bits, and $V_{\mathrm{Ref}} = 500\,\mathrm{mV}$.

Fig. 18.   DNL and INL for $n = 12$ bits, $V_{\mathrm{Ref}} = 500\,\mathrm{mV}$ and $f_C = 50\,\mathrm{kHz}$.

Fig. 19.   Micro photograph of the IC prototype.

controlled by the S_{vin} digital signal, which selects when the integrator has to process the ADC input or a zero input. The INV block applies signal inversions. Both blocks are implemented with CMOS analog switches, whose on-resistance must be optimized. The RES block discharges the capacitor when the conversion finishes. For the reference signal integration the same OTA than for the input is used, whose operation is now controlled by the S_{vref} digital signal, sourcing/sinking current at the integrating capacitor C. The more challenging analog block is the OTA; a linearized architecture has to be used due to the required input range. We have employed the circuit reported in [18] which allows to increase the input linear range by properly designing M2 and M22 transistors. Its schematic including the common-mode feedback circuit is shown in Fig. 16. In order to guaranty the linearity of the OTA-C integrator, the selection

of the transconductance value is realized taken into account the integrator capacitor value, the OTA output resistance, and the
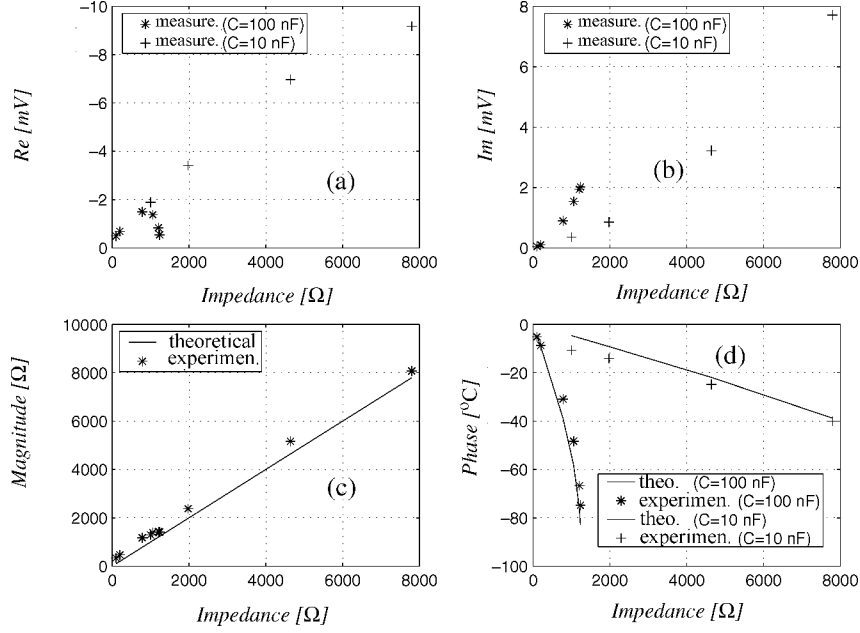
Fig. 20. Experimental results for the parallel *RC* load case. (a)-(b) real and imaginary components, and (c)-(d) magnitude and phase at 1 kHz of signal excitation versus several values of *R* and *C* loads.

integration time. For a maximum input value of $V_{\text{Ref}} = 0.5$ V, a $C = 15$ pF and a $g_m = 0.338\,\mu$S result for the integrator.

A prototype of the ADC was integrated in the 0.8-μm CMOS process. The experimental transfer function, the differential nonlinearity (DNL*)* and the integral nonlinearity (INL*)* graphics for 12 b, an input range of ±500 mV, and $V_{\text{Ref}} = 500$ mV are shown in Figs. 17 and 18, respectively. An implicit advantage of continuous time implementations is the good frequency scaling behavior since the clock drives the conversion time but not the ADC resolution. This has been proved on the same prototype, testing it at 2-MHz clock frequency with equal performance.

IV. EXPERIMENTAL RESULTS

In this section, the experimental results obtained from the whole impedance measurement system are reported. Several set of measurements are given for the system using different kind of loads and setups. A test chip was fabricated in a 0.8-μm CMOS process, including the main measure functionality circuits (this prototype do not include the two ADCs required by the system). A voltage supply of 3 V was chosen in order to be battery powered. The chip photograph is shown in Fig. 19. The core area is 6.95 mm^2. It includes the biasing circuits, with a bandgap reference circuit. The total current consumption is 700 μA. The characterization of the system was performed in the following setup and load conditions: 1) with passive *RC* loads and without using the needle. To emulate the electrode effect a $R = 2$ kΩ was used; 2) with the needle, and measuring in saline solutions with different concentrations (*in vitro*) and 3) with the needle, and using rat kidney as load (*in vivo*). The obtained results are explained in the following.

1) The chip was tested in the lab for a parallel *RC* load configuration, and for the full range of magnitude and phase. Fig. 20(a) and (b) represents the real and imaginary parts for different values of *C* and *R*. The magnitude and phase

derived from them are in Fig. 20(c) and (d). The measurements have been calibrated in order to eliminate the setup effects. Results show a good agreement with the expected data, being possible to detect changes in both magnitude and phase. Calibration has been done following the next steps.

a) A load (i.e., a resistance of 100 Ω) is taken as reference.

b) The real and imaginary components are measured with the system.

c) Deviations from ideal values (100 Ω, 0°) are taken as offset errors.

d) These errors are corrected in all the measures performed later.

e) This process is repeated for each work frequency.

2) *In vitro* experimentation was performed using the fabricated needle and several NaCl saline solutions as loads. The aim is to validate the correctness of the chip-needle system for the use *in vivo* measurements. A 0.9% NaCl solution (1:1) was taken as reference, whose impedance magnitude is around 200 Ω. The other loads were concentrations at 1:5, 1:10, 1:20 and 1:40, being more diluted, more resistive. In Fig. 21(a) and (b), the magnitude and phase responses for the five solutions are shown, for three test frequencies. Several effects can be observed.

a) For constant test frequency, the magnitude of impedance increases when concentration are more diluted (1:1 to 1:40). Also, it can be observed how the magnitude is nearly constant, for every concentration. This agrees with the expected results.

b) In the phase response we obtain two main performances: i) for a given frequency, phase decreases when increases dilution; ii) for a given solution, phase decreases when increases frequency. This means a more elaborated frequency dependence
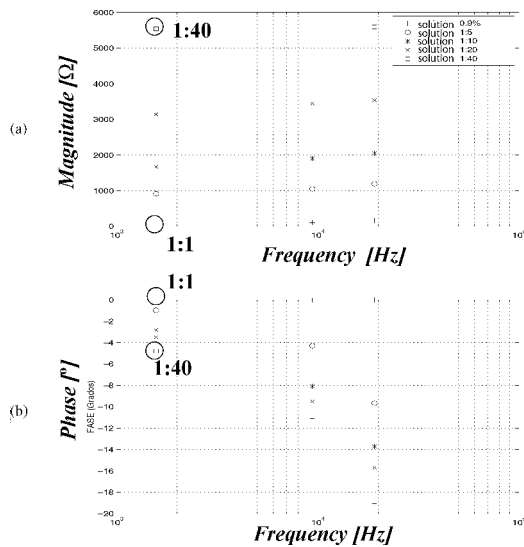
Fig. 21. *In-vitro* experimental (a) magnitude and (b) phase for 1, 8 and 16 kHz of signal excitation for five values of NaCl concentrations.
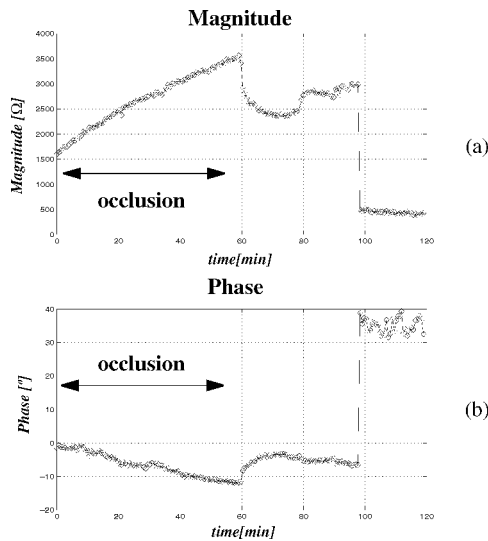

Fig. 22. *In-vivo* experimental magnitude (a) and phase (b) obtained in rat kidney at 1 kHz of signal excitation during the occlusion period of 60 min.

of the electrode-to- solution interface model than shown in Fig. 4(a), probably a concentration-dependent model for the electrode.

3) Finally, after performing electrical and *in vitro* tests, an *in vivo* test was carried out in a rat kidney subjected to acute ischemia. The study was conducted under the supervision of the Instituto de Investigaciones Biomédicas (IIBB) ethics commission and conformed to the EU guidelines for handling and care of laboratory animals. The rat kidney was subjected to 60 minutes ischemia. The impedance probe was orthogonally inserted into the kidney by direct puncture. The penetration depth of the center of the electrode array was *5 mm*. Fig. 22 shows the magnitude and phase responses measured in this experiment. The impedance module increases according to the severity of the ischemic damage while the phase decreases. Both results agree with the expected, and prove that the integrated circuit proposed predicts the same

evolution for magnitude and phase impedance than where measured with conventional instrumentation [20], [21].

V. CONCLUSION

A microelectronic system for impedance measure applications in medical and biological environments, such as heart surgery, organ transplant, and tissue characterization, has been proposed, designed and tested. Specifications and proposed solutions for basic building blocks have been discussed and pointed out, making special emphasis on system performance. Integrated circuits for basics blocks and the impedance measurement system have been reported with experimental results, proving the correct detection of magnitude and phase impedance evolution in several load conditions. The chip for tissue impedance measurements includes the excitation and the data acquisition circuitry and it could form part of a wireless system to be used during heart surgery. It has been designed for 3-V battery power supply, taking into account the specifications given by the impedance range to be measured and by the electrical electrode model used at the four wires system. The test performed *in vivo* conditions showed the feasibility of the system as an useful integrated circuit option for *in situ* data measure and acquisition in tissue impedance sensors.

ACKNOWLEDGMENT

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