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A Topology Generation and Synthesis Method for Boost Converters Based on Inductive Volt-Second Balance Theory

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Abstract: In this paper, a comprehensive method is proposed to derive the boost DC–DC converter from a given gain formula. The given gain formula is obtained by analyzing, generalizing, and summarizing previous boost structures in the literature. The analysis is based on the volt-second balance theory of inductors. Thus, the gain formula is only related to two elements, the connection between components and the duty cycle of the switches. Therefore, the topology corresponding to the gain can be derived and synthesized according to the connection of the inductors and the capacitor components during the commutation of the switch to meet the demand for different boost converters in different applications. Meanwhile, all the three-order gain formulas generated by this method are analyzed and three of them are selected for topology simplification and focus analysis, and the correctness of the selected topologies is verified by the simulation results and experimental results.

Keywords: volt-second balance theory; DC–DC converter; topology generation; boost structure

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1. Introduction

With the rapid development of technology in today's society, all kinds of equipment and systems in industry or in life are increasingly inseparable from electricity [1,2]. Therefore, how to design circuits to meet the needs of different devices is always a key research direction. DC–DC converters, as the most critical power supply module in various systems, can change the input voltage to the required output voltage, which is the most critical performance [3]. In the traditional DC–DC converter design, engineers design the DC–DC converter based on the basic DC–DC boost unit, such as boost structure, switching capacitor, switching inductor, and cascade structure, etc., through organic combination. The theoretical voltage gain of the designed converter is then derived by applying volt-second balance theory.

In the traditional circuit design, many design solutions are developed from the six most basic circuit topologies, such as buck, boost, and buck–boost, and the most current design solutions are to add switched capacitors, switched inductors, coupled inductors, and interleaved structures to the topology [4–7]. A major drawback of this design approach is that when the engineer designs a circuit and does not know what the specific gain of the circuit is, it is difficult to obtain the circuit topology that best fits the application conditions more quickly. At the same time, only one topology is generated by this method, which cannot meet the application of different occasions. In order to solve this problem, a variety of family circuits have been proposed [8–11]. These family circuit topologies are generated by designing a single-order boost structure first that meets the requirements, and then expanding this circuit to the Nth order by cascading this structure while simplifying the

topology of the circuit, which results in a series of circuits with similar performance and different boost capabilities. However, the higher-order topologies generated by this method have lower conversion efficiency, due to the gradual increase in components, so only a few circuits can actually be used. In [12–16], another new idea for circuit generation based on the three-port network is provided. Firstly, a three-port network with voltage conversion capability is designed and then, a variety of circuit topologies are obtained by using each of the three ports as input and output in different arrangements. This method is able to generate multiple topologies with a limited number of components, thus solving the problem of increasingly low conversion efficiency when generating topologies by cascading. However, the number of topologies generated by this method is limited; none of them have the same circuit properties and conversion capability; the topologies generated are both boost and buck types. In addition, it still does not solve the problem of not knowing the gain of the circuit at the beginning of the design.

A circuit synthesis method based on the inductive volt-second balance theory is then proposed, which quantifies the connections between components and substitutes them into the equations of the inductive volt-second balance theory to obtain a general equation for the voltage gain [17–19]. In the design of a circuit, the desired voltage gain can be found by using the general equation to reverse the connection of the components in the circuit and obtain the topology of the circuit. This method completely solves the problem of not knowing the specific gain form at the beginning of the design process, and it can generate a large number of topologies for different scenarios. However, this method still has some drawbacks, which are as follows:

(1). The general formula for voltage gain requires a very complex mathematical derivation, and it is difficult to derive a unified gain formula when the circuit is higher than two orders.
(2). The resulting circuit topologies have many of the same properties and they are not clearly classified.

In this paper, an improved generation and synthesis method based on inductive volt-second balance theory is proposed to specifically generate boost-type converters with specified gain. This method can be adapted to various application scenarios, and while it is easier to generate the specified topology, the least number of switches can be selected by analysis after synthesis. The proposed method in this paper is further studied on the basis of the method described in [17–19], which eliminates some meaningless forms in the process of topology generation through the analysis of the connection coefficient. Furthermore, the complexity of topology generation is simplified based on [20]. Through the combination of theoretical derivation and program designing, the proposed method can generate a series of topological structures with the same characteristics under specific conditions, which is beneficial to researchers in the process of selecting and analyzing required circuit. In Section 2, the voltage gain general formula is finally derived based on inductive volt-second balance theory for the three-order boost converter. In Section 3, the generation theory proposed in this paper is programmed to find all possible connections and corresponding gain formulas. Section 4 then shows how to select the corresponding topologies for the specified gain conditions, using the three-order boost converter and the specific gain conversion selected in this paper as examples. The topology generated by the proposed method is verified by simulation and experimentation in Sections 5 and 6, respectively.

2. Topological Synthesis Derivation

In a DC–DC converter, the boost or buck of the output voltage is mainly determined by the connection between the components in the circuit and the duty cycle of the switches. Therefore, if the connection between the components is quantified, the voltage gain of the circuit can be calculated by using the volt-second balance theory of inductors and Kirchoff voltage law (KVL). The connection between the power supply/capacitor and the inductor is defined as K, where $K = -1$ means reverse connection to the inductor, $K = 1$ means

forward connection to the inductor, and $K = 0$ means disconnected. In addition, to simplify the analysis process, the following is assumed:

(a) The circuit works in continuous conduction mode (CCM).
(b) All used components are ideal.
(c) One can define the number of inductors as the order of the circuit topology. Then, Equation (1) can be listed for a first-order circuit.

$$< V_L >_{T_S} = D(K_1 V_{IN} + K_2 V_o) + (1 - D)(K_3 V_{IN} + K_4 V_o) = 0 \quad (1)$$

Equation (1) can be simplified to obtain the general equation of voltage gain at this time, as shown in Equation (2), where $G = \frac{V_o}{V_{in}}$.

$$G = -\frac{(K_1 - K_3)D + K_3}{(K_2 - K_4)D + K_4} \quad (2)$$

When K_1, K_2, K_3 and K_4 adopt different values, the voltage gain G has many forms. In order to find all forms of voltage gain, all possible cases are listed by the developed program. The general formula makes the following constraint in order to subtract the meaningless and repetitive cases.

(a) The gain cannot always be 1 or -1, so K_1, K_2 cannot be 0 at the same time, and K_3, K_4 cannot be 0 at the same time, and the cases of $K_1 = K_3$ and $K_2 = K_4$ should also be excluded.
(b) The gain cannot always be 0 or infinity, so K_1, K_3 cannot be 0 at the same time; K_2, K_4 cannot be 0 at the same time.
(c) For $G = \frac{1}{(1-D)}$ and $G = -\frac{1}{(1-D)}$, which are mutually opposite gain forms, they are regarded as the same case because they have the same voltage change capability, and only the output is opposite.

After programming with the above constraints and sorting out all the possible gain forms, there are 12 possible gain forms. Among them, three boost forms, three buck forms, and six buck–boost forms are listed in Table 1. The present study will be carried out for all boost converters so the three gain forms in the last row of Table 1 are selected and the coefficients of these three gain forms can be obtained by back propagation, as shown in Equation (3).

$$\begin{pmatrix} K_1 \\ K_2 \\ K_3 \\ K_4 \end{pmatrix} = \begin{pmatrix} 1 \\ -1 \\ 1 \\ 0 \end{pmatrix} or \begin{pmatrix} 1 \\ 0 \\ 1 \\ -1 \end{pmatrix} or \begin{pmatrix} 1 \\ 1 \\ 1 \\ -1 \end{pmatrix} \quad (3)$$

Table 1. All possible gain forms of DC–DC converter.

Gain Form of First-Order DC–DC Converter			
Gain form		G	
Buck type	$1-2D$	D	$1-D$
Buck–boost type	$\frac{1-2D}{D}$ $\frac{1-D}{D}$	$\frac{D}{1-2D}$ $\frac{1-D}{1-2D}$	$\frac{D}{1-D}$ $\frac{1-D}{1-2D}$
Boost type	$\frac{1}{1-D}$	$\frac{1}{1-2D}$	$\frac{1}{D}$

It can be observed from Equation (3) that in either case, the values of K_1 and K_3 are 1, so the equation can be further simplified for a boost type converter. For an N-order DC–DC converter, if the number of inductors and capacitors is assumed to be equal, the voltage of capacitor C_1 is boosted in the first link through inductor L_1 with the voltage gain G_1. Inductor L_2 can then be connected to the power supply and capacitor C_1, and the voltage of capacitor C_2 is boosted in the second link through inductor L_2 with the voltage gain G_2. Similarly, the N-order generalization in Equation (4) can be obtained. Vi represents the

input at each level, which can take one or more of the cells that already have energy in the session.

$$\begin{gathered} < V_{Li} > T_S = D(A_i V_{i1} + K_{i1} V_o) + (1-D)(B_i V_{i2} + K_{i2} V_o) = 0 \\ A_i = (a_{i1}, a_{i2} \ldots a_{ii}) \\ B_i = (b_{i1}, b_{i2} \ldots b_{ii}) \\ V_{i1} = \begin{pmatrix} V_{in} \\ V_{C1} \\ \cdots \\ V_{C(i-1)} \end{pmatrix} \\ V_{i2} = \begin{pmatrix} V_{in} \\ V_{C1} \\ \cdots \\ V_{C(i-1)} \end{pmatrix} \end{gathered} \tag{4}$$

The voltage gain equation of the DC–DC converter of N-order is obtained by solving Equation (4). The gain equation for each order is determined by the previous $N-1$ order equation. Since there are more parameters in the formula, and each parameter in the formula is operated by different polynomials, each polynomial is defined as a new variable in the general formula, and the detailed cross-relations are shown in Table 2.

$$G_1 = \frac{V_{C1}}{V_{in}} = \frac{1}{(K_{12} - K_{11})D - K_{12}} \tag{5}$$

$$G_n = \frac{V_{Cn}}{V_{in}} = \frac{N_{n1} + N_{n2} G_1 + \cdots + N_{ni} G_{i-1} + \cdots + N_{nn} G_{n-1}}{M_n} \tag{6}$$

Table 2. Polynomial label.

Polynomial Label	Polynomial
M_i	$(K_{i2} - K_{i1})D - K_{i2}$
N_{ij}	$(a_{ij} + b_{ij})D + K_{ij}$

The next step in the analysis of this paper will study the three-order DC–DC converter as an example and program it in the next section in order to find all the topologies that can operate. Based on the aforementioned analysis, the equation for the three-order converter can be simplified to the form of Equations (7)–(9).

$$D(V_{IN} + K_{11} V_{C1}) + (1-D)(V_{IN} + K_{12} V_{C1}) = 0 \tag{7}$$

$$D(a_{21} V_{IN} + a_{22} V_{C1} + K_{21} V_{C2}) + (1-D)(b_{21} V_{IN} + b_{22} V_{C1} + K_{22} V_{C2}) = 0 \tag{8}$$

$$D(a_{31} V_{IN} + a_{32} V_{C1} + a_{33} V_{C2} + K_{31} V_{C3}) + (1-D)(b_{31} V_{IN} + b_{32} V_{C1} + b_{33} V_{C2} + K_{32} V_{C3}) = 0 \tag{9}$$

The gain Equation (10) can be obtained by simplifying the inductive volt-second balance equation of the three-order DC–DC converter, with the help of the polynomial representation in Table 2.

$$G = \frac{V_{C3}}{V_{in}} = \frac{N_{31} + N_{32} G_1 + N_{33} G_2}{M_3} \tag{10}$$

$$\begin{aligned} G_1 &= \frac{V_{C1}}{V_{in}} = \frac{1}{M_1} \\ G_2 &= \frac{V_{C2}}{V_{in}} = \frac{N_{21}+N_{22}G_1}{M_2} \\ M_1 &= (K_{12}-K_{11})D - K_{12} \\ M_2 &= (K_{22}-K_{21})D - K_{22} \\ M_3 &= (K_{32}-K_{31})D - K_{32} \\ N_{21} &= (a_{21}+b_{21})D + K_{21} \\ N_{22} &= (a_{22}+b_{22})D + K_{22} \\ N_{31} &= (a_{31}+b_{31})D + K_{31} \\ N_{32} &= (a_{32}+b_{32})D + K_{32} \\ N_{33} &= (a_{33}+b_{33})D + K_{33} \end{aligned} \tag{11}$$

3. Topology Programming

Based on the analysis in Section 2, the general form of the voltage gain of a three-order boost DC–DC converter is obtained. There are a total of 8 dependent variables in Equation (10), which in turn are determined by 16 independent variables (K_{ij}, a_{ij}, b_{ij}; i = 0, 1, 2, 3; j = 0, 1, 2, 3). Therefore, according to the analysis in Section 2, thousands of possible circuit topologies will be generated. In order to analyze these topologies efficiently, in this section, an algorithm is deduced to find all the possible voltage gains of any order of the boost circuit and to record the connections corresponding to these gains, so that the best circuit topology can be selected for synthesis and application when a certain gain is needed.

Figure 1 shows the flowchart of the program, starting with an exhaustive list of all the connection methods, followed by a preliminary screening of the listed connections according to the constraints analyzed in Section 2 to obtain the parameters that allow the correct synthesis of the circuit. After that, the corresponding gain formula is chosen according to the order of the circuit to be synthesized, and since the three-order converter will be used as an example in this paper, all possible results are substituted into Equation (10). In this way, the gain formulas corresponding to all possible results are obtained, and these formulas are stored in the list G. After every calculation, it is judged whether the newly calculated coefficients are already stored in the list G. If they do exist, the secondary connection method is stored in the array G_j of the list G. If they do not exist, the newly appeared gain form is stored in the list G. Finally, after all possible cases have been calculated, all available gain forms and their corresponding multiple connection methods are obtained.

According to the final output of the program, a total of 938 different forms of gain can be obtained. Equations (7)–(9) show that when the gain formula includes $1-2D$, if $D > 0.5$, then there will be a possibility of voltage gain $G < 1$. Therefore, all the generated circuit topologies can be divided into two categories, the first one must have a boost capability in the duty cycle range of $D < 0.5$; the second one must have a boost capability in the duty cycle range of $0 < D < 1$. The gain images of these two different circuits are shown in Figures 2 and 3, where the x-axis represents the duty cycle D, the y-axis represents the Ith gain curve, and the z-axis represents the gain.

Figure 2 shows all the DC–DC converters with a boost capability at $D < 0.5$, for a total of 596 different gain forms, each gain curve is represented by a different color to distinguish. By observing the curves in Figure 2, it can be observed that all curves have an asymptote of $D = 0.5$. Moreover, most of these curves slightly change in the range of $D < 0.5$, so they will have good stability if applied to real circuits.

Figure 3 shows all possible gain curves that must have a boost capability in the duty cycle range of $0 < D < 1$, each gain curve is represented by a different color to distinguish. There are a total of 342 curves corresponding to 342 different gain forms. Firstly, the growth rate of these curves is generally high, so that the synthesized converter has a high voltage gain. Secondly, some of these curves have a slight change in the range of $0.3 < D < 0.7$, so it is easy to control and its stability is good, while the voltage gain of these curves are all more than 10 times higher, which means these converters have the characteristics of high gain.

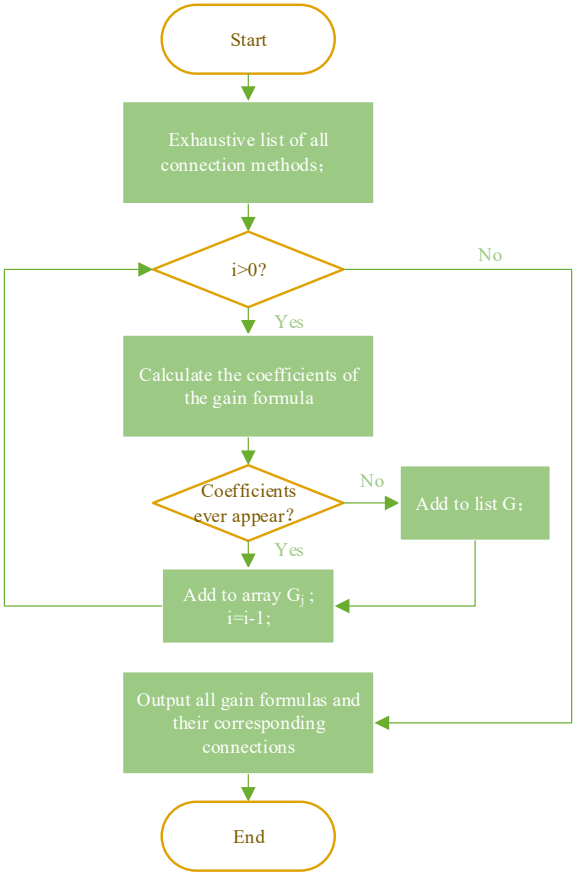


Figure 1. Flowchart of the developed program to calculate all different forms of gain.

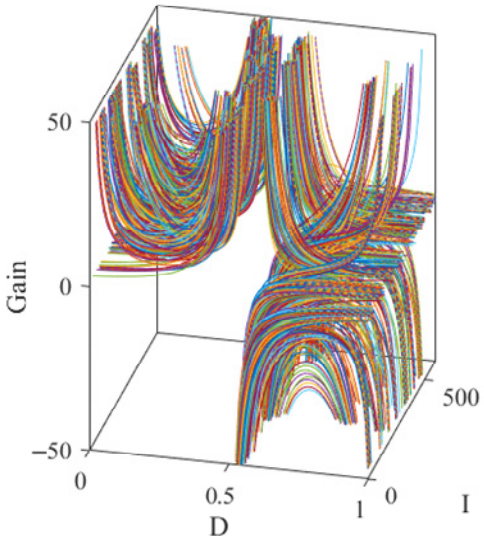


Figure 2. All possible gain curves that must have a boost capability in the duty cycle range of $D < 0.5$.

As shown in Table 3, the topologies of the four typical voltage gains are generated by using the proposed generation and synthesis method in this paper. For each gain, three topological structures with a small number of switches are generated and displayed, and all the twelve topologies listed are numbered from 1 to 12. The value of the connection factor corresponding to each topology is also listed in Table 3. In the next section, the No. 1 and No. 4 topologies are analyzed in detail and verified by simulations and experiments. The 10–12 topology synthesized in this paper has been verified in [21], which proves the feasibility of this topology.

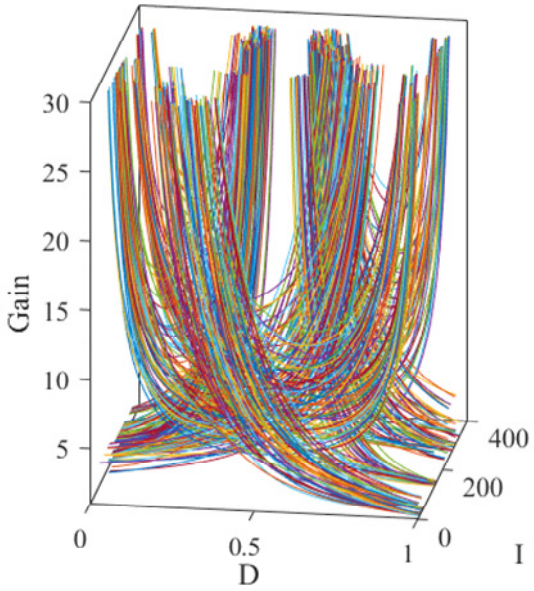
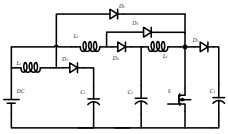
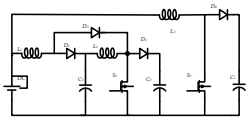
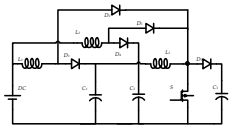
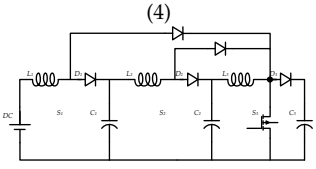
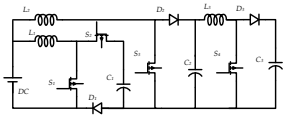
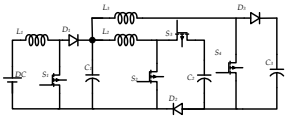
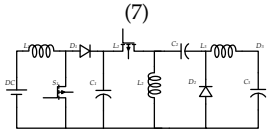
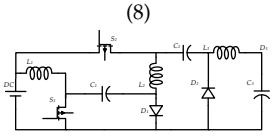
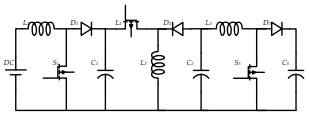
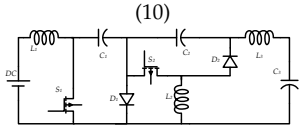
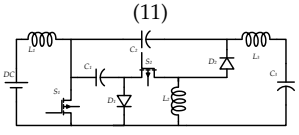
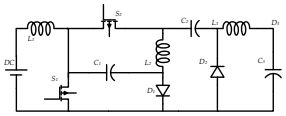


Figure 3. All possible gain curves that must have a boost capability in the duty cycle range of $0 < D < 1$.

Table 3. Obtained topologies for four different voltage gains.

Connection Factor	$K_{11}, K_{12}, K_{21}, K_{22}, K_{31}, K_{32}, a_{21}, a_{22}, a_{31}, a_{32}, a_{33}, b_{21}, b_{22}, b_{31}, b_{32}, b_{33}$		
Value	0, −1, 0, −1, 0, −1, 1, 0, 0, 0, 1, 1, 0, 0, 0, 1	0, −1, 0, −1, 0, −1, 0, 1, 1, 0, 0, 0, 1, 1, 0, 0	0, −1, 0, −1, 0, −1, 1, 0, 0, 1, 0, 1, 0, 0, 1, 0
Gain	$1/(1-D)^2$		
Topology	(1) 	(2) 	(3) 
Value	0, −1, 0, −1, 0, −1, 0, 1, 0, 0, 1, 0, 1, 0, 0, 1	0, −1, 0, −1, 0, −1, 1, 1, 0, 0, 1, 1, 0, 0, 0, 1	0, −1, 0, −1, 0, −1, 0, 1, 0, 1, 1, 0, 1, 0, 1, 0
Gain	$1/(1-D)^3$		
Topology	(4) 	(5) 	(6) 
Value	0, −1, 0, −1, 0, −1, 0, 1, 1, 1, 0, 0, 0, 0, 1, 1	−1, 0, 0, −1, 0, −1, 0, 1, 1, 0, 1, 0, 1, 0, 0, 1	−1, 0, 0, −1, 0, −1, 0, 1, 1, 0, 1, 1, 0, 0, 1, 1
Gain	$D/(1-D)^2$		
Topology	(7) 	(8) 	(9) 
Value	−1, 0, 0, −1, 0, −1, 1, 0, 1, 0, 1, 1, 1, 0, 0, 1	−1, 0, 0, −1, 0, −1, 0, 1, 1, 0, 1, 1, 0, 0, 1, 1	0, −1, 0, −1, −1, 0, 1, 1, 0, 1, 1, 0, 1, 0, 1, 0
Gain	$D^2/(1-D)^2$		
Topology	(10) 	(11) 	(12) 

4. Topology Generation

In Section 3, a large number of gain curves and the corresponding connections for different DC–DC converters are obtained. The next step in topology synthesis is to select a gain curve that meets the actual requirements, and then find the parameters corresponding to it by using the above programming. The circuit diagram is then drawn in reverse and the circuit is filtered and simplified.

In this paper, a typical three-order boost converter is chosen to verify the correctness of the theory. According to the image of the gain curve obtained in Figure 3, there are several curves with higher gain. In order to verify the correctness of the theory, a group of coefficients $\{-1, 3, -3, 1, 0, 0, 0, 1\}$ are chosen, where $G = \frac{1}{(1-D)^3}$. Then, through the program design in the previous section, all the connection methods corresponding to the chosen coefficient can be found in the list G. In the program, there is only one connection method $\{K_{11}, K_{12}, K_{21}, K_{22}, K_{31}, K_{32}, a_{21}, a_{22}, a_{31}, a_{32}, a_{33}, b_{21}, b_{22}, b_{31}, b_{32}, b_{33}\} = \{0, -1, 0, -1, 0, -1, 0, 1, 0, 0, 1, 0, 1, 0, 0, 1\}$ that corresponds to the desired form of gain, so that is the connection method used for synthesis. The first step is to substitute the coefficients of the connection method into the Equations (7)–(9) to obtain the following equation:

$$\begin{cases} DV_{in} + (1-D)(V_{IN} - V_{C1}) = 0 \\ DV_{C1} + (1-D)(V_{C1} - V_{C2}) = 0 \\ DV_{C2} + (1-D)(V_{C2} - V_{C3}) = 0 \end{cases} \tag{12}$$

Therefore, according to Equation (11), the two operation modes shown in Figure 4 can be obtained. In the DTs phase circuit, such as the one shown in Figure 4a, the input source DC charges inductor L_1, capacitor C_1 charges inductor L_2, and then capacitor C_2 charges inductor L_3. In the $(1 - D)$ Ts stage, the power supply is connected in series with inductor L_1 charging capacitor C_1, while capacitor C_1 is connected in series with inductor L_2 charging capacitor C_2. However, at this time, capacitor C_1 is in a charged state and cannot discharge to other components. Thus, in the actual circuit, there is an input source DC in series with inductors L_1 and L_2 to supply power to C_2. Similarly, the capacitor C_3 is charged by the input source DC in series with inductors L_1, L_2, and L_3. These results are shown in Figure 4b.

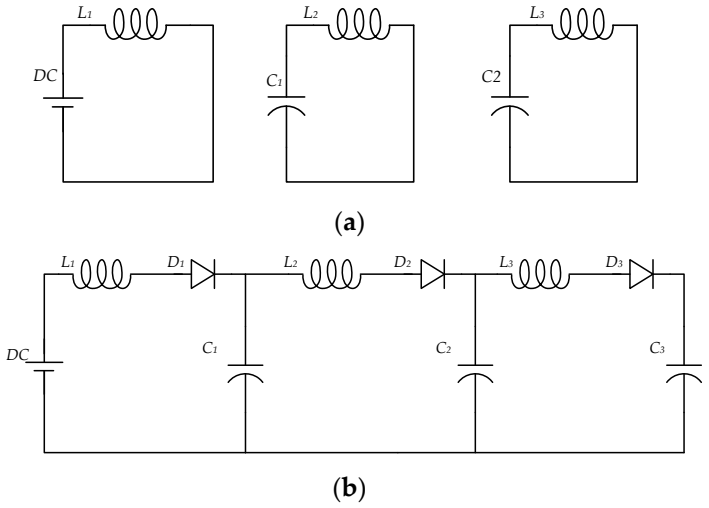


Figure 4. Connection method in DTs and $(1 - D)$ Ts of three-order boost converter. (**a**) Mode I, (**b**) Mode II.

Once two modes of topology are available, the topology of the two states can be combined by adding switches to convert all the different connection paths in each state, as shown in Figure 5.

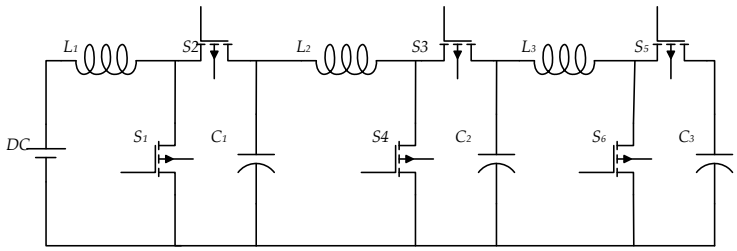


Figure 5. Topology after combination of three-order boost converter.

Then, after analyzing the voltages of all switches in the circuit at different stages of operation, it is determined whether the switch can be replaced by a diode. If it can be replaced by a diode, then the circuit can be simplified. Furthermore, as it can be observed from Figure 5, the circuit topology has switches S_1, S_4, and S_6, all of which are connected to the negative terminal of the power supply and have the same on-time and off-time, so the circuit can be further simplified to obtain the single switch form, as shown in Figure 6. The synthesis of the circuit topology is now complete, and the traditional design for this topology can then be applied to the specified scenario.

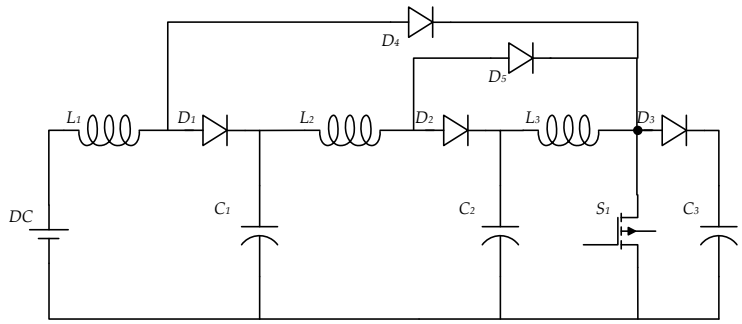


Figure 6. The final simplified synthesized circuit of three-order boost converter.

As shown in Figure 7, the proposed generation and synthesis method also generates a circuit topology that provides a dual output with one voltage gain $\frac{1}{(1-D)^2}$ and the other output voltage $\frac{1}{1-D}$ of capacitor C_1, so it can be used in applications that require two different voltage outputs at the same time. The circuit can still be synthesized by applying the above method, but since all the switches are on at the same time and connected to the negative terminal of the power supply after the connection method is determined, all the switches can be replaced by one switch to simplify the circuit. The final circuit is shown in Figure 8.

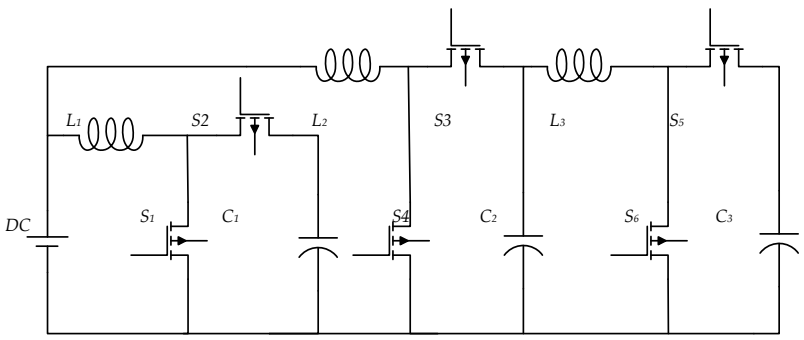


Figure 7. Dual output converter after synthesis.

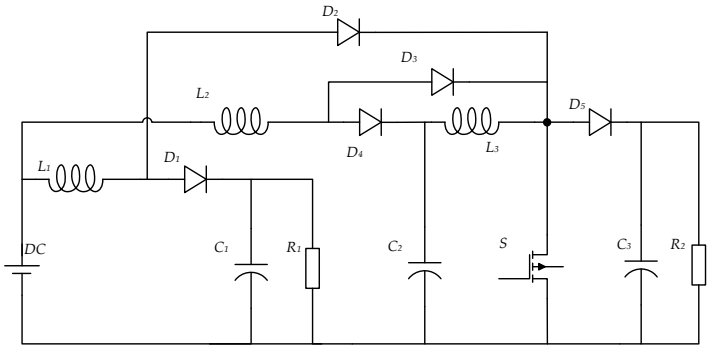


Figure 8. The final simplified synthesized circuit of the dual output converter.

5. Circuit Simulation

In the previous section, a circuit structure with a high voltage gain and a circuit structure with multiple outputs are used as examples for topology generation. In this section, simulations in MATLAB will be performed to verify the feasibility of this circuit structure. Both circuits use a closed-loop control method for the output voltage.

Based on the derived gain equation, it is known that when a PWM signal with a duty cycle of 0.6 is fed to the switch, the boost factor of this high gain converter is 15. In this paper, the input voltage of 10 V and a PWM signal with a duty cycle of 0.6 are chosen for the converter. When all the inductors are in continuous conduction mode, as shown in Figure 9, this topology will result in an output voltage of 150 V. The output voltage of this circuit is shown in Figure 10. Since the ideal device is used in the simulation and the closed-loop control is applied, the final voltage is stabilized at 150 V, which is the same as the theoretical calculation, proving that there is indeed a circuit with high boost capability in the topology generated by this synthesis method.

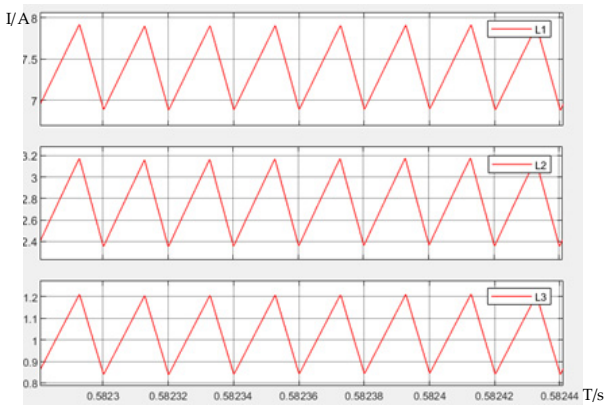


Figure 9. Current through high gain converter inductors.

The proposed converter with dual outputs is also verified by simulation, in which the input voltage is set to 10 V, and the control signal is a PWM signal with a duty cycle of 0.5 and a frequency of 10 kHz. Figure 11 illustrates the output voltage of the dual output converter. The first output is the voltage output across capacitor C_1, and the second output is the voltage output across capacitor C_3; both are consistent with the theoretical $V_{C1} = \frac{V_{IN}}{(1-D)}$ and $V_{C3} = \frac{V_{IN}}{(1-D)^2}$, and are 20 V and 40 V, respectively, at an input of 10 V. Therefore, the feasibility of the topology generated using this method can be demonstrated.

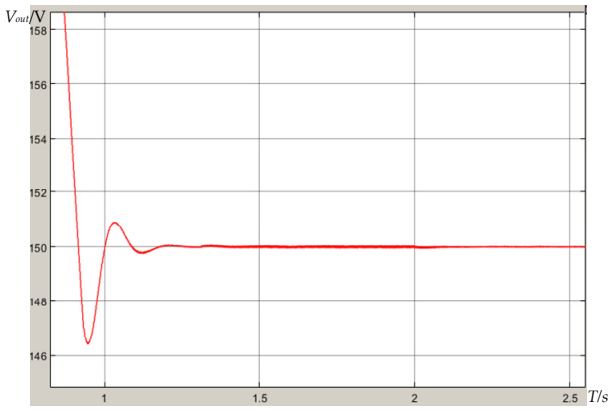


Figure 10. Output voltage across high gain converter.

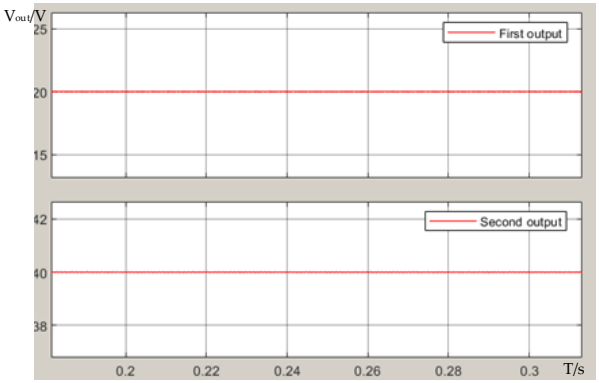


Figure 11. Output voltage of the dual output converter.

6. Experimental Verification

In order to verify the correctness of the proposed method, an actual circuit of the three-order boost converter is assembled and tested in the laboratory. The hardware prototype of the three-order boost converter is shown in Figure 12. Component parameters are the same as the MATLAB simulation, and the input voltage is 10 V. Figure 13 shows the PWM control signals and output voltage of the three-order boost converter. The green waveform indicates the output voltage of the converter, and the yellow waveform indicates the PWM control signal, where the duty cycle is chosen to be 0.5, and the frequency is chosen to be 20 kHz. According to the theoretical analysis in Section 3, the final output should be 80 V, while the output voltage of the circuit in Figure 13 is 79.5 V. The actual output of the circuit is slightly lower than the theoretical value, due to the losses in the actual circuit. After the simulation and experiment, it is proved that the circuit topology generated by the topology generation and synthesis theory proposed in this paper is feasible and has boosting capability. If all components are ideal, the actual output of the circuit generated by the proposed method is exactly the same as the theoretical analysis.

Figure 12. Hardware prototype of three-order boost converter.

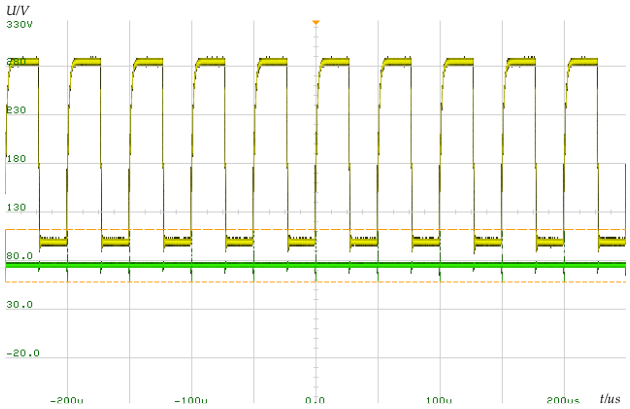


Figure 13. PWM control signals and output voltage of three-order boost converter.

7. Conclusions

This paper presents a method for generating and synthesizing topologies with a boost function based on the volt-second balance theory of inductors, and synthesizing circuit topologies with boost capability by knowing the gains in advance. Moreover, an adapted program algorithm is designed for this method to find all possible forms of gain and the circuit connections corresponding to all forms of gain. The topologies found by applying this topology generation method have the following advantages: all generated topologies must have boost capability at a certain duty cycle. It is easier to extend the order of the circuit to N-order to find topologies with higher boost functions. In addition, since the combination of theory and program greatly improves the work efficiency of topology generation and the number of available topologies with the same operation characteristics, it shortens the development cycle of the project. The circuit generated by the proposed method is assembled and tested in the laboratory. Therefore, the proposed method is also feasible in actual production. In the process of theoretical researching, designing a high-performance topology with high boost capability has always been a hot research topic, and the theory proposed in this paper also makes it possible to design new boost structures.

The proposed generation and synthesis method is able to generate most of the desired boost converters, but there are still a few problems. For the same gain formula, there are multiple circuit connections, and the proposed method cannot find the best circuit among them and it is necessary to analyze each circuit, one by one.

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