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Abstract

The design of a Time Projection Chamber (TPC) detector with complete pad coverage is presented. The TPC will allow the measurements of high multiplicity ($\approx$ 200 tracks) relativistic nucleus-nucleus collisions initiated with the heaviest, most energetic projectiles available at the LBL BEVALAC accelerator facility. The front end electronics, composed of over 15,000 time sampling channels, will be located on the chamber. The highly integrated, custom designed, electronics and the VME based data acquisition system are described.

1 Introduction

Studies with 4π detectors at the Bevalac (the Streamer Chamber [1] and the Plastic Ball [2]) have opened a major new field of nuclear physics - the study of the dynamics of nuclear matter under extreme conditions. Such investigations are of fundamental interest and are also essential for an understanding of supernova explosions and of neutron star structure. The experimental results obtained from existing detectors have contributed vastly to the understanding of the reaction mechanisms. The important discovery of the collective flow and squeeze-out phenomena, as predicted by theoretical models, has lead to the experimental observation of compressed nuclear matter - a necessary condition before one can study in detail the nuclear equation of state and search for phase transitions.

Much of the interesting work remains to be done and experience has shown that it will be necessary to make the simultaneous observation of a variety of phenomena which is beyond the capabilities of the existing 4π detectors. A new detector with a large solid angle acceptance, particle identification, and momentum measurement for all the charged particles is required.

This paper describes a Time Projection Chamber under construction at LBL designed to study relativistic heavy ion collisions and to cope with the high multiplicity and high particle density environment typical of such reactions.

2 Mechanical Design

The HISS TPC, sketched in Figure 1, is in the shape of a single rectangular box centered in the HISS dipole magnet and is designed to operate at one atmosphere pressure. The detector is configured as a drift volume enclosed with field cage panels on the sides and a single proportional wire chamber - pad plane on the bottom. The active drift volume is 150 cm long in the beam direction, 96 cm wide in the bending direction and 75 cm high in the drift direction. A 15 cm high rigid I-beam box structure between the pad plane and the magnet pole tip maintains the pad plane uniformity and provides the support structure for the TPC. Each box compartment will contain four zero insertion force (ZIF) connectors which provide the electrical connection to the rows of pads and the plumbing for water cooling. The electronics will be mounted on a double sided printed circuit board which will slip into the ZIF connector from the open side. An optical platform within the TPC bulkhead supplies the laser beam tracks for calibration. The detector is encased in a relatively light weight skin for gas containment and thermal isolation. Multiple scattering is kept small so that the TPC can be operated in combination with other detectors.

2.1 Pad Plane Design

The pad plane is a single panel with an array of 1.2 cm $\times$ 0.8 cm pads covering a 96 cm by 150 cm rectangle (15,360 pads total). As shown in Figure 2 the three wire planes over these pads will be essentially the same as in the
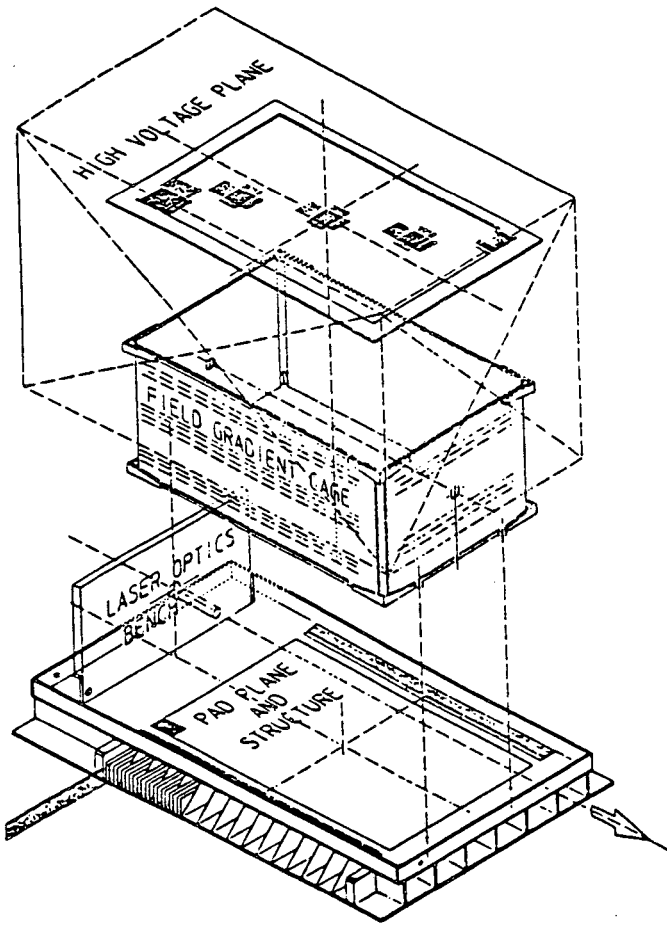
Figure 1: Exploded View of the HISS TPC detector

Figure 2: HISS TPC Wire and Pad Plane layout

PEP4 [3] and TOPAZ [4] detectors: the first plane consists of alternating field and anode wires, the next plane is an isolation grid, and the third plane is a gating grid. The latter passes drifting electrons for the accepted events only and thereby limits positive-ion build-up in the drift volume.

Construction of the wire planes in the HISS TPC configuration will be simpler than other TPC's since the wire termination can be located well away from the active region, thus avoiding difficulties with gain variations over the pads. The anode wires will normally be operated at approximately 1170 volts to give a gas gain of 3000, but they will be divided among 16 separate power supplies to permit sections to be operated at reduced gas gain for analysis of tracks from heavier, more strongly ionizing particles. We do not intend to record the wire signals directly due to the high multiple hit rate. Instead, the pad array has 100% coverage for complete three dimensional read-out unlike other existing TPC detectors. Table 1 lists some of the TPC design parameters.
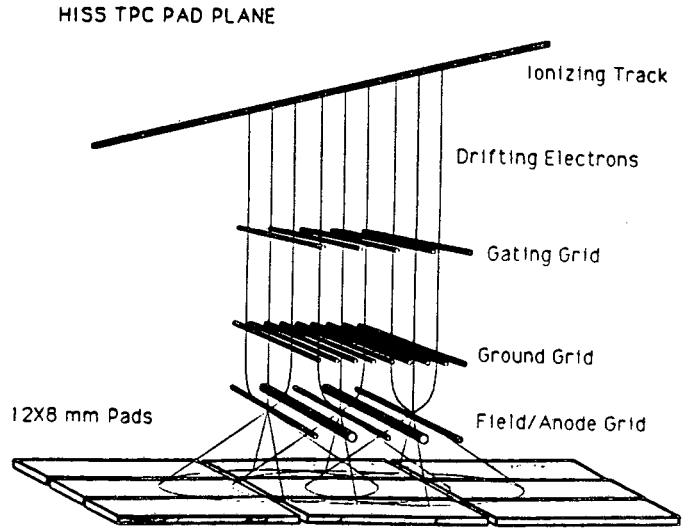
2.2 Field Cage

The design of the field cage is derived from that of the ALEPH [5] detector. It will be fabricated using kapton clad on both sides with copper strips. The copper strips alternate such that the thin exposed bands of kapton are backed on the opposite side with copper. Prototype tests are in progress exploring the possibility of forming panels from two of these kapton/copper sheets with a Rohacell core. The cage will be constructed from four of these light weight panels set back about 5 cm from the active pad region, thus avoiding the local field distortions near the surfaces of the cage. In the low beam intensity configuration thin entrance and exit windows will be provided for the beam. In the high beam intensity configuration the field cage-box will be divided into two separate cages on either side of the beam.

The drift field for 90% Ar plus 10% CH_4 (P10) at atmospheric pressure is 120 V/cm. Thus a total bias of 9 KV will be required for the field cage.

2.3 Laser Calibration System

There will be static distortions in the electron drift path due to the curving B field lines. The laser system will produce straight line ionized tracks through the active volume of the TPC. These tracks will be used to calibrate the routines that are needed to remove the B-field distortions and alignment errors. With the aid of the laser system it will also be possible to monitor and perhaps correct for time dependent distortions due to positive ion build up and long term variations in drift velocity due to ambient pressure changes.

The design is based on the ALEPH TPC laser system and uses 266 nm wavelength UV light from a frequency

HISS TPC Characteristics	
Pad Plane Area	1.5m × 1.0m
Number of Pads	15360 (120 × 128)
Pad Size	12mm × 8mm
Drift Distance	75 cm
Time Sampling Freq.	10 MHz
Signal Shaping Time	250 ns
Electronic Noise	700 e
Gas Gain	3000
Gas Composition	$90\% Ar + 10\% CH_4$
Pressure	1 Atmosphere
B Field	13 kG
E Field	120 V/cm
Drift Velocity	$5cm/\mu s$
Event Rate	10-80 events/ 1 sec spill
dE/dx range	$Z = 1-8, \Lambda, \pi, p, d, t, He, Li - O$
Two Track Resolution	2.5cm
Multiplicity Limit	≈ 200

Table 1: TPC detector specifications

quadrupled Nd-Yag laser. The laser system has optics for remotely adjusting the intensity, position and angle of the laser beam entering the TPC. The laser beam is split into 18 paths in the active volume. This is accomplished with a system of beam splitters placed on a vertical optical bench located in front of the field cage. A large aperture in the center of the optical bench allows the particle beam to pass through.

3 Electronics

3.1 Performance

Two requirements drive the specification for noise and dynamic range of the pad read out electronics. Good position resolution for minimum ionizing particles is the first requirement. Position measurement is achieved by fitting a pad response function to the signals from two or more pads. This procedure places demands on both noise and digital resolution. The second requirement is a large dynamic range in dE/dx to include measurements of highly ionizing particles. To accommodate these two requirements the system has been designed with the maximum practical dynamic range and the TPC will be operated with the minimum gas gain required to achieve the desired position resolution. The planned operating parameters and the electronics specifications bearing on this issue are summarized in Table 2.

The signal on a pad for a minimum ionizing track passing directly over the pad center is 11,000 electrons. This number corresponds to the most probable value in the dE/dx distribution when a gas gain of 3000 is used. The expected noise on the preamp is 600 electrons rms and the final sys-

tem noise is 700 electrons. This yields a most probable minimum ionizing signal/noise of 16:1 which is adequate to achieve a 300 micron position resolution.

The dynamic range (maximum signal/noise) of the complete electronics system is 1400:1, that is the maximum signal is 90 × the most probable minimum ionizing signal. As shown in Figure 3 this dynamic range will allow dE/dx measurements for ions with charges as high as oxygen. The figure gives dE/dx values for a variety of ions as a function of their kinetic energy per nucleon and shows the range of dE/dx values covered for two different gas gains. By running sections of the chamber at a gas gain of 33 it will be possible to span a range in dE/dx from minimum ionizing to Au ions at 1 GeV per nucleon. Saturation of the gas gain will extend this range even further.
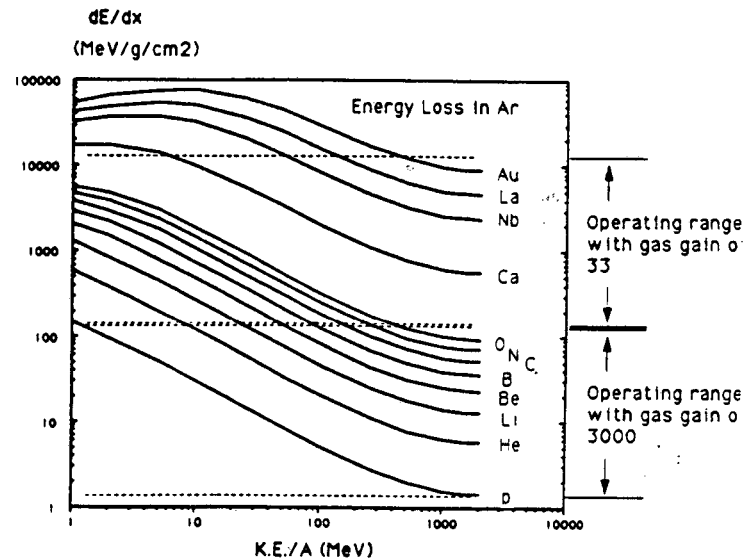

Figure 3: dE/dx versus kinetic energy per nucleon for a variety of ions. The dynamic range of the TPC electronics is shown for two different gas gains

3.2 Configuration

The electronic system for 15,360 pads cannot be constructed in the traditional way, where the preamplifier resides on the detector and the signals are transferred individually by cable off the detector for further processing. Recent progress in analogue VLSI electronics encouraged us to choose a different design for the HISS TPC that would have a number of significant advantages. The principal advantage of our scheme is the ability to accomplish amplification, shaping, analogue storage, a high degree of multiplexing and digitization immediately on the pad plane. The resulting cabling reduction saves valuable vertical space between the pole tips. The remainder of the electronics can be contained in one or two racks, thus

(3)

Pad Signal for a Centered Minimum Ionizing Particle	
dE/dx (eV/cm)	1250
Pad Length (cm)	1.2
Electrons/eV loss	26
Gas Gain	3000
Efficiency of charge collection due to the integration time	0.4
Wire-Pad Coupling	0.16
Pad Signal (e)	11000

Electronics Specifications							
Device	Gain	Device Noise	Cumulative Noise		Min I Signal	Device Maximum	
			e	mV	mV	mV	Min I's
Preamp	0.32 μV/e	600 e	600	0.192	3.5	2000	570
Shaper Amp	6.5	0.5 mV		1.3	23	2000	90
CCD	1.0	0.6 mV	700	1.4	23	2000	90

Table 2: Operating parameters and electronic specifications

avoiding the need for additional housing and greatly reducing installation and maintenance problems and overall cost. Figure 4 shows a block diagram of the electronic system that will read out and process the data from 15,360 pads.

The connections between the pads and the preamplifiers are kept as short as possible in order to obtain an optimal signal to noise ratio. This is achieved by mounting the electronic components on a mother board, called a "stick", which is inserted into a zero insertion force edge card connector located on the pad plane. A schematic view of a stick is shown in Figure 5. Each stick services two rows of pads (a total of 120 pads) across half of the width of the chamber. 15 hybrid circuits are mounted on each side of the board. A hybrid will contain an integrated circuit 4-channel preamplifier and four discrete shaper-amplifiers. The shapers are designed to restore the baseline of the signals with a time constant of about 250 ns and to compensate for the tails generated by the slow drift of the positive ions. The hybrid occupies a height of about 10 cm between the pad plane and the pole face of the HISS magnet. In a multi-layered printed circuit board structure the output signals of the shapers are guided to the end of the stick where they are written into a 256-cell deep analogue store (Switched Capacitor Array SCA or Charge Coupled Device CCD) at a rate of 10 MHz. Thus each cell contains information about a drift space of 5 mm (100 ns). All 256 cells of the 60 analogue storage devices on each side of the stick are multiplexed and digitized by a common ADC with a frequency of 1.0 MHz. The digital information from the two ADC's is sent off the detector via a 100 Mbits/s optical link for further processing.

3.3 Preamplifier

The charge integrating preamplifier is the most important component of the readout electronics with regard to noise performance and dynamic range. The noise generated in the input stage of the amplifier is the dominant source of accuracy degradation in charge measurement and limits the dynamic range. The special requirements of HISS TPC detector called for a high performance, low noise integrated preamplifier. The calculated signal to noise ratio is 16:1 for minimum ionizing particles (Min I's) for a noise charge of 600 e_{rms} (ENC referred to the input). The dynamic range is set at 4200:1 to match that of the analogue storage device and the ADC resolution. However, in order to accommodate multiple tracks in the time domain, the preamplifier is designed to saturate at 3 times the maximum signal. This implies that the maximum useable signal is 90 times minimum ionizing particle or a 1400:1 dynamic range and the particle identification range as shown in Figure 3.

A custom CMOS integrated preamplifier has been designed [6]. and is shown schematically in Figure 6. In designing this preamplifier, it was clear from the outset that oscillations that are normally associated with such high gain-bandwidth circuits is a problem. Such instabilities are observed when the preamplifier is reset because either the output signal is saturated or a forced abort condition exists. For these reasons, a novel reset scheme based on auxiliary transconductance amplifiers in the feedback loop was used to quickly return the output signal to baseline.
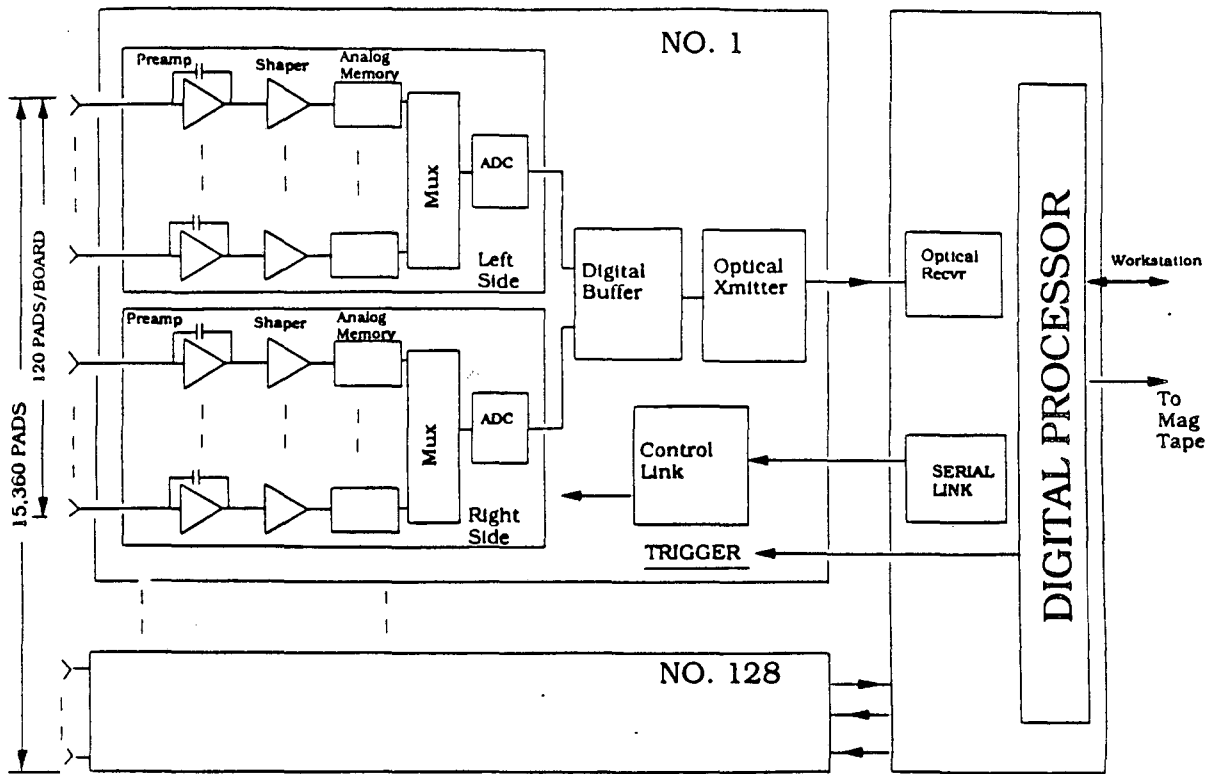
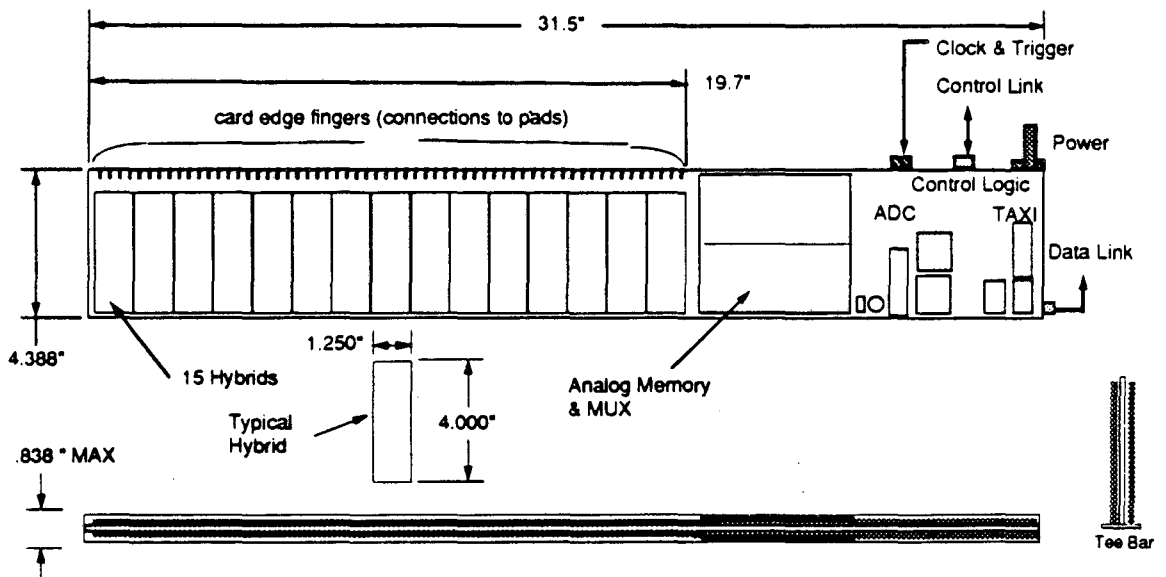Figure 4: Block diagram of the front end electronics

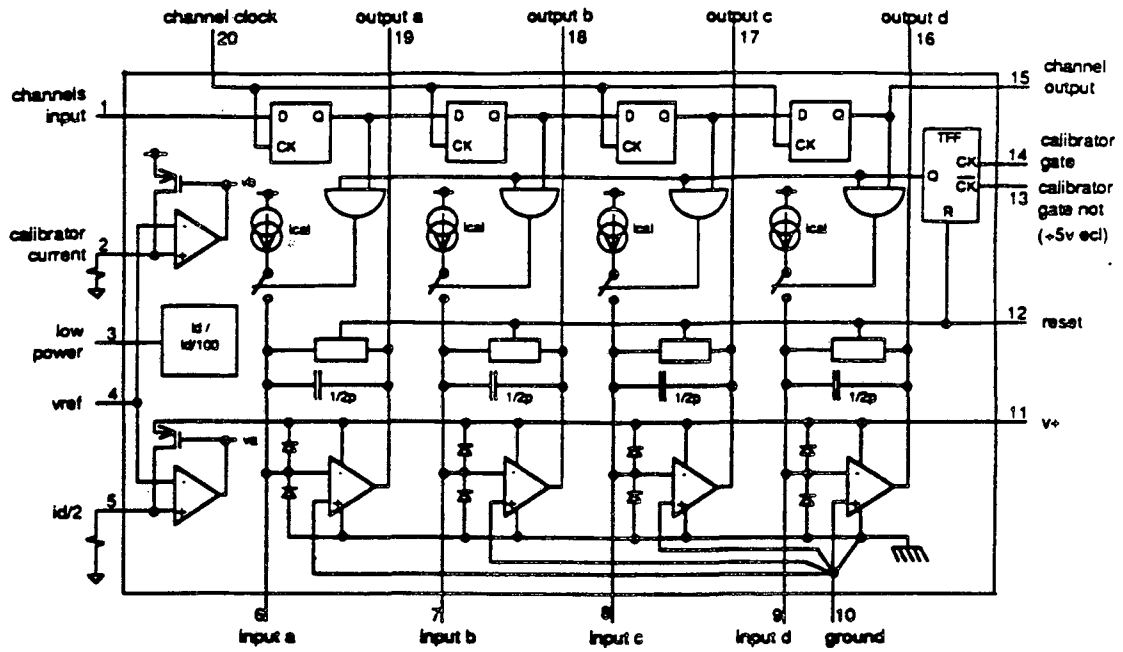Figure 5: Schematic layout of electronics on a stick

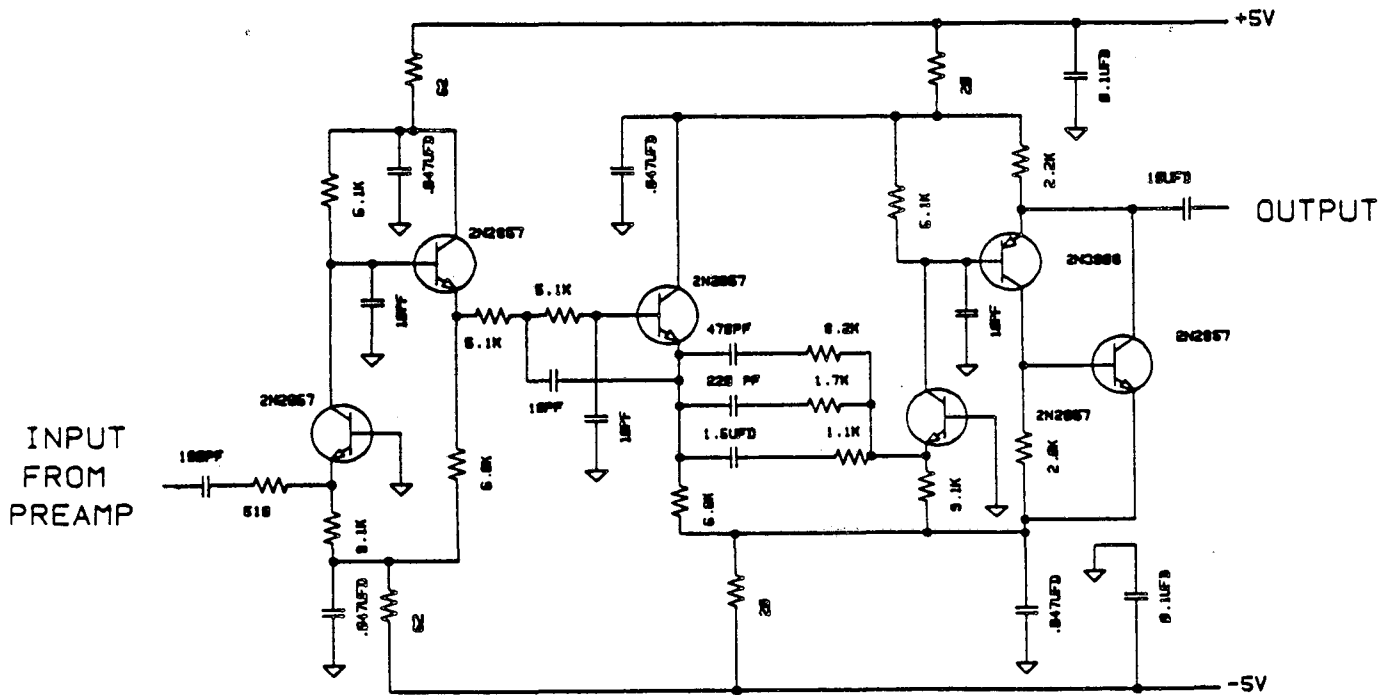Figure 6: Block diagram of the integrated circuit preamplifier

Figure 7: Shaper circuit diagram

To meet the channel-to-channel gain matching requirement of better than 5%, an on-chip calibrator is used. In principle, a known current is gated into an unknown capacitor for a known time. The accuracy is determined by the timing characteristics of the current pulse and for that reason the pulse is derived from a fast ECL switch. In addition, each channel can be pulsed individually for diagnostic and electronic gain calibration purposes.

3.4 Shaper

The shaper amplifier circuit, shown in Figure 7, is fabricated using hybrid surface mount technology. The primary design consideration was to minimize the component count, thereby keeping the hybrid surface area and the power dissipation at their lowest possible values. For simplicity the shaper circuit has no overall feedback loop. However, the resultant $\leq 3\%$ non-linearity easily meets requirements.

The shaper contains six transistors which have a moderately high f_t to avoid intrinsic bandwidth limitation. A common base input stage was selected to minimize the noise. The input signal is differentiated and filtered using an active 4-pole integrator. In addition, the 1/T tail cancellation is accomplished with three parallel RC networks. The output transistors drive the line capacitance and the switched capacitor array input impedance. Satisfactory results have been obtained from a discrete component version of the shaper. A noise of value of less than $0.5mV_{rms}$ was measured.

A prototype hybrid layout which includes a discrete preamplifier has been completed. The preamplifier is essentially identical to the PEP4 [7] design except for the introduction of a reset switch across the feedback capacitor and a simple calibration circuit at the input. Prototypes have been fabricated and tests are currently in progress.

3.5 Analogue Memory

The shaper analogue signal is time sampled at 10 MHz and read out at 50kHz. We have investigated the merits of using CCDs and a integrated circuit switched capacitor array (SCA) designed at LBL which is described in detail in a separate contribution to these proceedings [8].

The SCA device is fabricated using the two micron, double metal, double polysilicon CMOS process which permits low power dissipation ($\approx 15mW$/channel of standby power) and a high degree of integration. There are 16 channels per chip, each containing 256 samples. The dynamic range has been measured to be 8000:1 at 10% non-linearity and better than 4000:1 at the 1% level. The spatial noise is comparable to CCDs and better than 0.6 mV rms. The signal bandwidth is limited by a 16ns integra-

tion time constant, which is primarily determined by the input MOSFET switch resistance and the effective sampling capacitance. The time constant is, however, short compared with the sampling time and consequently there is little signal distortion. Tests have shown that the cell to cell signal variation due to all effects (e.g. time constant) over the sampling capacitors is 0.4% with a 50ns acquisition window (0.1 % using a 80ns window) which is sufficiently below the 6.5% uniformity requirement for the HISS TPC. The SCAs can be reset by discharging all the sampling capacitors for $10\mu s$.

An interleaved multiplexing scheme is used for read out to accommodate the $30\mu s$ settling time of the SCA. In the HISS TPC application, the read out rate of the SCA's using the on-chip multiplexing and interleaving 4 SCA chips is sustainable at 1 MHz.

CCDs have at most two channels per chip and require a greater number of transport clock drivers capable of supplying large peak currents into a relatively large capacitive load $\approx 35 - 85\ pF$. In addition, CCDs dissipate substantially more standby power ($\approx 60 - 150$ mW/Channel depending on the CCD vendor) than the SCA. Other important concerns are the dark current build up, the temperature stability, input bias and output offsets.

At this time, the advantages of using the SCAs make it the most suitable candidate for the analogue memory device. We plan to test a batch of SCAs under the exact timing conditions and readout scheme devised for the HISS TPC. Most of the TPC logic functions are generated efficiently in a small amount of space using high-density Xilinx programmable Logic Cell Arrays (LCAs) [9]. A Xilinx chip is being programmed to produce the HISS TPC logic signals for the stick electronics. This will provide a working prototype for carrying out tests.

4 Data Acquisition

Data rates are a major concern when implementing a data acquisition system for a detector of this size. Simulations with events with 200 tracks (central collisions of 1 GeV Au on Au) show that between 10-20 % of the pixels in the TPC volume will contain signals above threshold. Allowing two bytes per recorded pixel and including required addressing information, these events will be approximately 0.5-1.0 Mbytes in length. Combining the expected data rate of 10 events per spill with the expected spill rate of one spill per 6 seconds, we reach an aggregate recorded data rate of 1-2 Mbyte per second. Current large volume storage media (e.g. 8mm digital tape) will operate at sustained rates of approximately 250 Kbytes/second. Operating a number of these devices in parallel (5-10 units) will yield the desired recording speeds.

The TPC data acquisition system acquires data from the TPC detector and its dedicated on-chamber electronics. Since the TPC is a very large and complex system, there will be a great deal of interaction between its various detector system components, e.g embedded processors, real time kernels, detector electronics, interconnections, graphics etc. To keep things simple and achieve the necessary data throughput we will use a VME-based system to read out, format and record events onto 8mm digital tape. Where ever possible, the system will utilize commercial components.

The general arrangement of hardware components is shown schematically in Figure 8. There are six interconnected VME crates. Four of these VME crates, identified as the Front End Processors (FEPs), will operate in parallel - each receiving and processing data from a different portion of the chamber. The remaining two VME crates are the Event Builder Processors (EBPs) whose task will be to collect and package data from FEPs and feed events to workstations, and to tape drives. Every VME crate will have a CPU processor running the VxWorks real time operating system [10]. This system will control the execution of the tasks residing in these processors and will provide some common tools for program development, remote procedure calls (RPC) and network file access.

Pad signals are amplified, shaped, stored and digitized by the detector electronics located above the pad plane. The resulting data are then transmitted over optical fiber to the FEPs located in an adjacent experimental area. The FEPs consist of eight custom designed VME interfaces boards which receive and and store the data in local memory buffers. A receiver board has four Motorola 58001 digital signal processors (DSPs) each dedicated to an optical fiber link. The DSPs compress the data and apply a simple gain correction. After suitable digital filtering, the DSPs move the data into dual-ported memory buffers which are connected to the VME bus backplane. EBPs collect and assemble the data into larger event buffers. These event buffers are subsequently sorted and organized in such a way that events which belong to a particular beam spill are stored together on one of the many 8mm cassette tape drives. Additionally, the EBPs provide configuration and consistency checks to ensure the integrity of data presented to the event builder. Every data packet from each stick contains configuration data and a unique event I.D number for each event which can be used to verify proper synchronization of all 128 data sources.

Since scientific workstations currently offer substantially better computational performance than larger minicomputer systems, we plan to use workstations to perform on-line analysis. The high quality video subsystems on these systems will provide the required data display capabilities. On-line analysis programs will obtain events or, more typically, selected portions of events, via an eth-
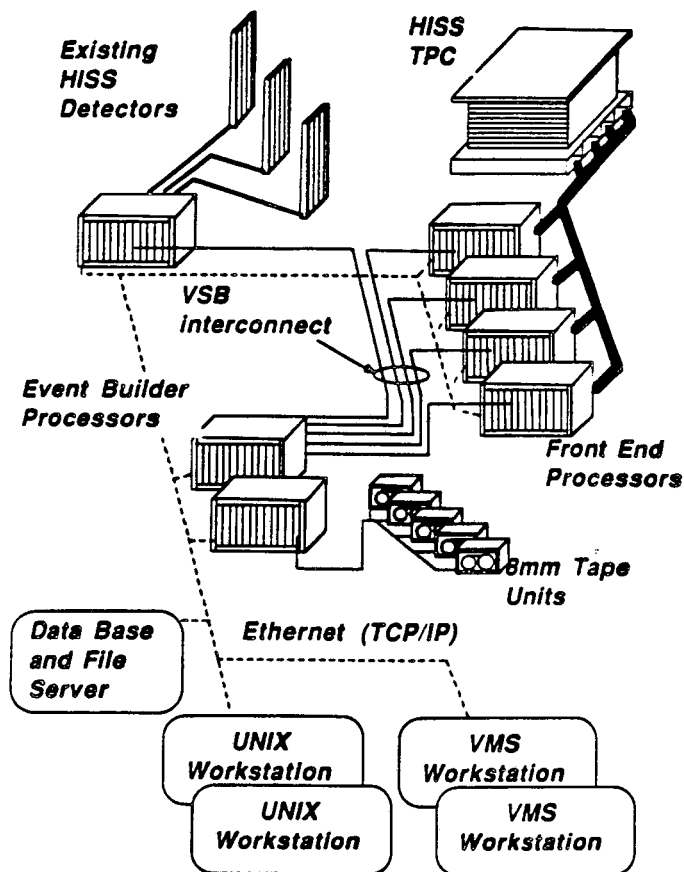

Figure 8: Data acquisition system hardware overview

ernet link that interconnects all of the processors in the system. During data taking, events waiting to be taped will be available for selection and analysis by a number of workstations.

5 Summary

The HISS TPC will greatly expand detector capabilities at the Bevalac. It will provide the capability to completely measure most charge particles emitted from heavy ion collisions. Three dimensional tracking will allow the unfolding of high multiplicity events with as many as 200 charged particles. Good tracking resolution in the HISS dipole field and dE/dx information provide momenta and particle identification for most of the charged particles of interest.

In addition, the detector will make a significant step towards the complete integration and miniaturization of electronics needed in detectors that are being planned for future experiments.

Acknowledgments

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