# A Transformer–less Static Synchronous Compensator Employing a Multi–level Inverter

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***Abstract*— This paper examines the application of a high voltage multi–level inverter in a 13.8 kV distribution system Static Synchronous Compensator SSC. Equations are developed for the component MVA of the multi–level inverter. Trends in component MVA as a function of the number of inverter voltage levels and the modulation strategy are identified. Control of the dc bus capacitor voltages during phase voltage imbalance is identified as a problem. A method is described whereby the multi–level inverter's dc bus capacitor voltages are actively controlled without using additional power components. The operation of the capacitor voltage control loop is demonstrated through EMTP simulations of an SSC responding to single phase and three phase load variations in a model distribution system.** **Keywords: SSC, STATCOM, Inverter and Static Var Compensation.**

## I. INTRODUCTION

Var compensation can be achieved by using a controlled synchronous voltage source which is connected to the power system through a small reactor. If the voltage source is produced by a static power converter, the system is called a Static Synchronous Compensator (SSC). The benefits of a SSC for reactive power compensation have been broadly examined in [1]. In [2], it was demonstrated that the use of a SSC permits fast control of the voltage as well as a potential for reduction in the system footprint. In [3], a SSC has been placed in service for stabilizing the transmission system and in [4] it has been studied for its use in regulating voltage at the distribution level.

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This paper investigates the use of a multi–level inverter in a transformer–less SSC operating at the 13.8 kV distribution level. The multi–level inverter can produce a high output voltage without a step–up transformer. Eliminating the transformer could result in further reduction of the system footprint. Direct transformer–less connection of the twelve pulse inverter can not be done since it relies on the transformer phaseshift for the cancellation of harmonics. In addition, it is difficult to obtain an inverter output voltage much greater than the voltage rating of an individual GTO when using the standard inverter bridge configuration.

To increase the output voltage from a standard inverter bridge configuration, the dc bus voltage must be raised and switching devices placed in series to hold off the additional voltage. The series connection of Gate Turn Off thyristors (GTOs) leads to significant problems with voltage sharing among devices during turn–on and turn–off [3]. This has limited the number of devices that can be successfully placed in series to three GTOs in [3] and five GTOs in [5]. The utilization of the GTO's voltage rating can be particularly poor when devices are connected in series. Methods for improving voltage sharing include over–snubbing of each device and active control of gate signal timing [6].

The problem of voltage sharing in series connected devices can be avoided when a multi-level inverter is employed. The voltage stress on each GTO in a multi-level inverter is well controlled and is much less than the dc bus voltage [7]. As the dc bus voltage is raised, the voltage stress on each GTO can be held constant by adding more levels to the inverter. As more voltage levels are added to the inverter, the harmonic performance improves without increased switching loss and the filter size also can be reduced. The increase in dc bus voltage also increases the MVA rating of the system.

The use of a multi–level inverter has been previously suggested in [8] where use of a transformer coupled multi-level inverter for an SSC was explored. The focus in [8] was evaluation of multi-level PWM strategies. This paper builds upon the work of [8] by 1) showing the component MVA requirements for the MLI 2) showing how component ratings are a function of the number of voltage levels and the modulation strategy 3) comparing these ratings to a twelve pulse inverter and highlighting differences.

Furthermore, this paper identifies the difficulty with controlling capacitor voltages in a multi-level inverter when

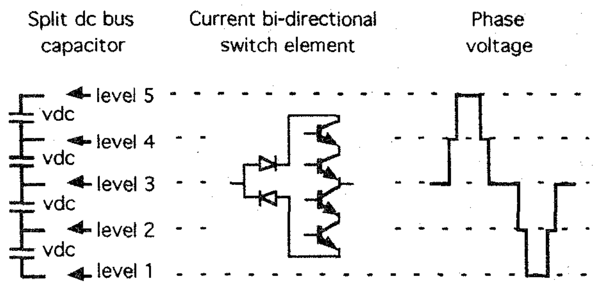


Figure 1. Elements of a multi–level inverter.

the system voltages are unbalanced. EMTP simulations are used to show that the voltages on the dc bus capacitor can drift when imbalance is present. The presence of single phase loads in a distribution system can result in phase voltage imbalance. A control method to mitigate the problem is described. The operation of the proposed capacitor voltage control method is simulated using EMTP for a five–level inverter SSC in a simplified distribution system model.

## II. DESCRIPTION OF THE MULTI–LEVEL INVERTER STRUCTURE

This section describes the composition and features of the multi–level inverter. Fig. 1 shows the elements of the inverter. The dc bus capacitor is split into sections. Splitting the capacitor provides tap points which are at different voltage levels. By splitting the capacitor into more sections, more voltage levels become available. The next converter element is a set of diodes and force commutated switches (IGBTs or GTOs). The diodes and switches together form a switching group which is bi–directional in current and uni–directional in voltage. One such switch group is connected to each tap point along the dc capacitor. As each switch group is turned on, inverter output is connected to a different voltage level as shown on the right side of Fig. 1.

The operation of the inverter is such that switch groups can share transistors. This results in the appearance of interleaved switch groups within each phase leg of the three phase inverter in Fig. 2. With this switch arrangement, the added diodes serve to clamp the off–state voltage stress seen by the main devices. The dc bus capacitor in Fig. 2 is split into four sections which yields five available voltage levels hence it is called a five–level inverter.

The task of keeping equal voltages on each of the dc bus capacitors is referred to as the voltage balancing problem. In [9], it is shown that if the modulation index of the inverter for each voltage level is properly constrained, capacitor voltage can be maintained under ideal balanced conditions.

## III. FEATURES OF THE MULTI–LEVEL APPROACH

The two main features of the multi–level inverter are the low harmonic content of the output voltage and the fact that the force commutated switches experience a voltage stress that is a fraction of the total dc bus voltage. The step–like nature

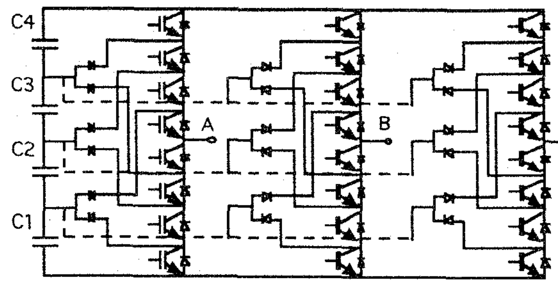


Figure 2. Three Phase Five–level Inverter

of the output voltage results in lower harmonics than a square wave pulse. The width of each step in the waveform can be varied to result in elimination of selected harmonics. A five–level inverter can eliminate the $5^{th}$ and $7^{th}$ harmonics, while using only fundamental frequency switching. A nine–level inverter can eliminate the $5^{th}$, $7^{th}$, $11^{th}$, and $13^{th}$ harmonics.

From a performance perspective, increasing the number of voltage levels a multi–level inverter results in 1) lower harmonics, 2) decreased device voltage stress or equivalently a higher dc bus voltage for the same switch voltage and 3) potentially higher inverter voltage and thus power rating.

The reliability and availability of the inverter is a significant issue for utility applications. Fault modes and protection methods for the multi–level inverter are discussed in [10].

## IV. COMPONENT MVA OF MULTI–LEVEL INVERTER

Equations are now developed for the MVA ratings of the inverter components by examining the voltage and current stresses on the clamp diodes, GTOs, and capacitors

### *A. Assumptions*

Component ratings are given in per unit. The component rating equations are developed using the SSC's MVA rating as the base power. The base voltage is the zero to peak value of the system's phase voltage. Peak phase current is used for determining the rating of GTO devices based on their turn–off limitations. Each GTO is assumed to be paired with an antiparallel diode of the usual rating. Deratings are not applied. They can readily be applied to the final equations if desired. A 10%p–p ripple on the dc bus voltage is used to balance capacitor size with semiconductor device ratings. A 10% reactance is assumed to connect the inverter to the network.

In the multi–level inverter, many of the component ratings are dependent upon the modulation angles of the inverter. A set of harmonically optimized modulation angles is chosen and used for the analysis. Figure 3 illustrates the definition of the modulation angles for the five–level inverter.

### *B. MVA Ratings*

The calculation of the inverter component MVA is done in the following order. Given the inverter MVA rating and voltage rating, the required dc bus voltage is determined

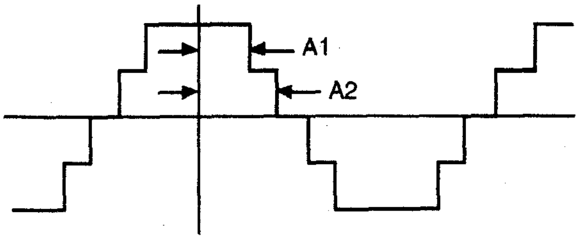


Figure 3. Definition of modulation angles A1 and A2 for five-level waveform.

assuming a linking reactance of 10%. Next, the inverter rated phase current is determined. The GTO and clamp diode MVA are then derived from the dc bus voltage and phase current. A sizing method for the dc bus capacitors is presented which keeps the peak to peak dc bus voltage ripple to 10% for rated inverter current.

The maximum dc bus voltage is that voltage required to produce rated leading current into rated system voltage:

$$V_{dc(max)} = \left\{\frac{2}{k_i}\right\} \{V_{base} (X_{l(pu)} + 1.0)\} \qquad (1)$$

where $k_i$ is the modulation index of the inverter and $X_{l(pu)}$ is the value of the linking reactance in per unit.

The modulation index for a set of switching angles, $A_n$, is

$$k_i = \frac{4}{\pi}\,\frac{1}{m}\sum_{n=1}^{m} \sin(A_n). \qquad (2)$$

where m is the number of switching angles = $(N_{levels}-1)/2$.

The peak dc bus voltage is $V_{dc(max)}$ plus ripple:

$$V_{dc(peak)} = \left\{1 + \frac{\%V_{ripple}}{2}\right\} V_{dc(max)} \qquad (3)$$

or, $$Vdc(peak) = K_1\ Vbase \qquad (4)$$

where

$$K_1 = \left\{1 + \frac{\%V_{ripple}}{2}\right\}\left\{\frac{2}{k_i}\right\}(X_{l(pu)}+1.0) \qquad (5)$$

and $\%V_{ripple}$ is the peak to peak voltage ripple on the dc bus.

*1) GTO MVA Rating:* The voltage stress on each GTO is equal to the dc bus voltage divided the number of levels minus one.

$$V_{GTO} = \frac{V_{dc(peak)}}{N_{levels} - 1} \qquad (6)$$

Each GTO must be sized to handle the peak phase current. The peak of the inverter phase current is:

$$I_{phase(peak)} = 2\left\{\frac{MVA_{inv}}{3\ V_{base}}\right\} \qquad (7)$$

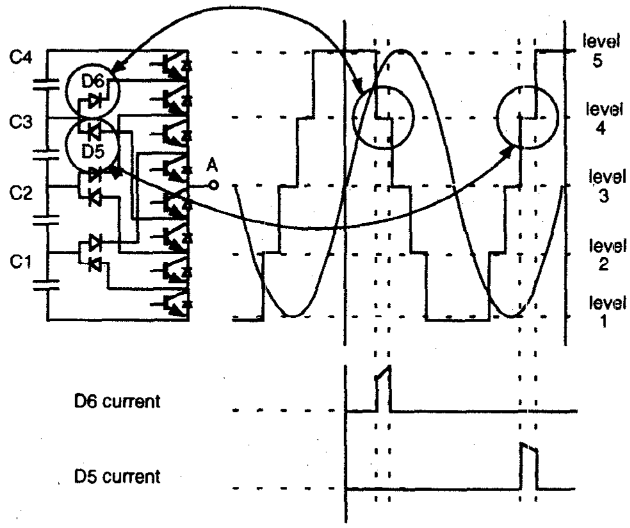


Fig. 4 Using the phase voltage to determine the current in each clamp diode. Illustrated are the clamp diode currents in D5 and D6 when the phase voltage is at level 4.

where $MVA_{inv}$ is the MVA rating of the SSC. The MVA rating of each GTO is $V_{GTO}$ times $I_{GTO}$:

$$MVA_{perGTO} = \frac{V_{dc(peak)}}{N_{levels} - 1}\left\{\frac{2\ MVA_{inv}}{3\ V_{base}}\right\} \qquad (8)$$

The number of GTO's in an N-level inverter is:

$$N_{GTO} = 6\,(N_{levels} - 1) \qquad (9)$$

The total MVA of GTOs is then, after simplification,

$$MVA_{GTO} = 4\,K_1\ MVA_{inv}. \qquad (10)$$

This formula shows that the MVA of GTOs required is independent of the number of voltage levels.

*2) Clamp Diode MVA:* The voltage rating of each clamp diode depends upon its connection points in the N-level inverter. In each phase leg, there are two diodes that each see reverse voltage stress of:

$$V_{diode} = \left\{\frac{N_{levels} - 1 - k}{N_{levels} - 1}\right\} \times V_{dc(peak)} \qquad (11)$$

where k goes from 1 to $(N_{levels} - 2)$

Applying this formula over the indicated range of k gives the voltage stress on each of the diodes of the phase leg. Note that the highest voltage stress seen by a clamp diode approaches $V_{dc(peak)}$ as the number of voltage levels becomes large. The equation for clamp diode voltage stress can be simplified by noting that for any pair of clamp diodes (e.g. D6 and D5 in figure 4), the total voltage stress is $V_{dc}$ (e.g. 3/4 $V_{dc}$ + 1/4 $V_{dc}$). The number of clamp diode pairs in each phase leg is:

$$N_{diodepairs} = 3 \times (N_{levels} - 2) \qquad (12)$$

resulting in the total clamp diode voltage stress per phase leg being:

$$V_{diodes(per\ phase)} = 3 \times (N_{levels} - 2)\, V_{dc(peak)}. \quad (13)$$

The average current in each clamp diode is a function of the modulation angles and the diode's connection points in the inverter. Figure 4 illustrates how the current in a particular clamp diode is related to the phase current.

In figure 4, diode D6 sees the phase current for the time interval from switching angle A1 to switching angle A2. The average current in the diode can be calculated from:

$$I_{avg} = I_{phase(peak)} \frac{1}{2\pi} \int_A^B \sin(\emptyset)\, d\emptyset \quad (14)$$

Applying this formula to all of the clamp diodes in a phase leg of the inverter and combining the results yields the average current through all the clamp diodes in a phase leg:

$$I_{avgdiode} = I_{phase(peak)} \frac{1}{\pi} \{-\cos(\pi - A1) + \cos(A1)\} \quad (15)$$

This equation shows that the average current that goes through the clamp diodes depends only on the first modulation angle. The distribution of this average among the various clamp diodes, however, depends upon the whole set of modulation angles.

Combining the voltage and current ratings, the clamp diode MVA is:

$$V_{dc}\, (N_{levels} - 2)\, I_{phase(peak)} \frac{3}{\pi} (-\cos(\pi - A1) + \cos(A1)) \quad (16)$$

which simplifies to:

$$K_1\, (N_{levels} - 2)\, MVA_{inv} \frac{2}{\pi} (-\cos(\pi - A1) + \cos(A1)). \quad (17)$$

This equation shows that the clamp diode MVA increases with the number of voltage levels used and is also a function of the modulation angles.

*3) Dc Bus Capacitor MVA:* The dc bus capacitors are sized to limit the voltage ripple on the dc bus. The formula for the capacitance is $C = \Delta Q_{p-p} / \Delta V_{p-p}$, where $\Delta Q_{p-p}$ is the deviation in charge on the capacitor which depends upon the capacitor current waveform.

The current wavefrom through each capacitor is a function of the modulation angles. Figure 5. shows the current waveform for the innermost capacitor in a five-level inverter.

The change in charge on the capacitor is the area under the curve over the indicated interval. For the example waveform of figure 5, the peak to peak change in charge is:

$$\Delta Qi_{p-p} = \frac{2}{2\pi 60} I_{phase(peak)} (1 - \cos(120\text{-}A2)). \quad (18)$$

If A2 is less than 60° then the following formula is used:

$$\Delta Qi_{p-p} = \frac{2}{2\pi 60} I_{phase(peak)} (1 - \cos(A2)). \quad (19)$$

For the outer capacitor, A2 is replaced with A1 in the above formula. For a higher number of levels, the substitution is extended. Using a more complex modulation can lead to

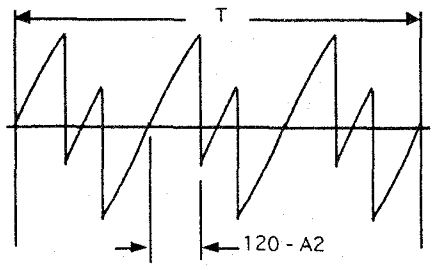


Figure 5. Current in innermost dc bus capacitor (C2) of five-level inverter (for A2>=60 degrees).

different equations for $\Delta Q$, but such advanced modulation techniques are not evaluated in this paper.

An acceptable peak to peak voltage ripple is 10% as determined by a trading off increasing voltage stress on the semiconductors against increased capacitor size. The capacitor size required to keep the voltage ripple at 10% is:

$$C_{level} = \frac{\Delta Q_{p-p}}{\left\{\frac{10\% \times V_{dc}}{N_{levels} - 1}\right\}} \quad (20)$$

This capacitance value must be determined for each voltage level. It can be noted from the symmetry of the converter that the capacitance values are symmetric about the middle of the dc bus.

From the capacitance value, the MVA of capacitance is determined by equating the peak dc voltage across the capacitor to the peak of a fundamental frequency sinewave. The capacitor MVA is then (for each level):

$$MVA_{cap(per\ level)} = \frac{1}{2} (2\pi 60)\, C_{level}\, \frac{1}{2} \left\{\frac{V_{dc}}{N_{levels} - 1}\right\}^2 \quad (21)$$

Combining this equation with the formula for $C_{level}$ and noting that the number of capacitors equals $N_{levels} - 1$ results in the total capacitor MVA being:

$$MVA_{total} = \frac{1}{3}\, \Delta Q_{avg}\, K_1\, MVA_{inv} \left\{\frac{100\%}{\%V_{ripple}}\right\} \quad (22)$$

Where the different capacitor current waveforms are accounted for in the term $\Delta Qavg$, which equals:

$$\Delta Q_{avg} = \frac{\sum_{\substack{n=1 \\ A_n > 60°}}^{m} \{1 - \cos(120 - A_n)\} + \sum_{\substack{n=1 \\ A_n < 60°}}^{m} \{1 - \cos(A_n)\}}{m} \quad (23)$$

where m is the number of switching angles = $(N_{levels} - 1) / 2$.

Note that the total capacitor MVA is independent of the number of voltage levels. The $\Delta Q_{avg}$ term does not necessarily increase with the number of levels. The total capacitor MVA is, however, a function of the modulation strategy through $K_1$ and $\Delta Q_{avg}$.

TABLE I.
PER UNIT MVA OF INVERTER COMPONENTS

| Number of levels | GTO MVA | Diode MVA | Capacitor MVA | Transformer MVA | Mod. index |
|---|---|---|---|---|---|
| 5[a] | 7.8 | 3.8 | 2.2 | – | 1.18 |
| 7[b] | 7.9 | 7.4 | 2.0 | – | 1.17 |
| 9[c] | 8.8 | 16.6 | 2.1 | – | 1.05 |
| 12-pulse | 7.26 | – | 0.21 | 1.0 | 1.27 |

[a] switching angles: a1=59, a2=85
[b] switching angles: a1=54, a2=74, a3=83
[c] switching angles: a1=32, a2=56, a3=72, a4=81

### C. Discussion of Ratings

Table I shows the per unit component MVA of five–level through nine–level inverters as well as for a twelve–pulse inverter. The twelve–pulse is used for reference because it has harmonic performance similar to the five–level inverter when fundamental frequency switching is used. The component ratings are discussed below.

*1) GTO MVA:* GTO MVA is relatively unchanged from the twelve–pulse to the five–level and seven–level inverters. The GTO MVA is higher for the nine–level inverter only because the modulation index of the inverter is lower than for the seven– and five–level inverters. The reduced modulation index is due in part to the elimination of additional harmonics from the waveform as the number of voltage levels is increased.

*2) Capacitor MVA:* Capacitor MVA is relatively constant among the five–, seven–, and nine–level inverters but is much greater than for the twelve–pulse inverter. The split capacitor of the multi–level inverter combined with the modulation method make it difficult to suppress dc bus voltage ripple. Dc bus ripple is well suppressed in the twelve pulse inverter because it has a single common dc bus capacitor into which ripple current flows.

*3) Clamp diode MVA:* Table I shows that the clamp diode MVA increases with the number of voltage levels.

*4) Effect of Number of Levels on MVA Ratings:* There are direct and indirect penalties associated with increasing the number of voltage levels. Clamp diode MVA increases strongly with the number of voltage levels. The force commutated device MVA increases slightly because of the reduction in modulation index for a higher number of levels. Capacitor MVA is virtually unaffected by the number of voltage levels.

*5) Effect of Modulation Strategy:* The switching angles of the modulation switching angles have a large effect on the capacitor MVA and clamp diode MVA. The dc bus capacitor ripple is highest when the modulation angles are near 60°. Reduction of the capacitor MVA may be combined with the minimization of harmonics in the design of the modulation strategy. Changes in modulation index will also weakly affect the GTO MVA.

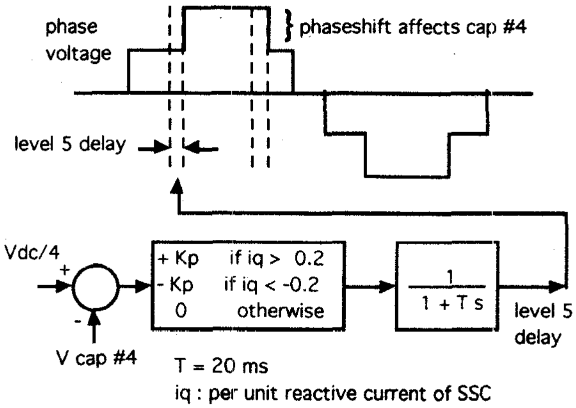


Figure 6. Controller for individual capacitor voltages.

## V. CAPACITOR VOLTAGE BALANCING

The three phase five–level inverter shown in Fig. 2 has four distinct dc bus capacitors labelled C1 through C4. To control the inverter's fundamental component voltage these capacitors must be charged or discharged to alter the total dc bus voltage. The charging current of each capacitor is controlled by the modulation strategy and the inverter ac side currents. The voltage change on each capacitor is the combined effect of the capacitor size and and the charging current.

For normal operation with balanced inverter voltages and balanced inverter currents, the size of each capacitor can be determined so that the voltage on each capacitor will change equally when the total dc bus voltage is adjusted. Such a capacitor sizing scheme is discussed in [9].

However, the capacitor voltages can become unequal when unbalanced inverter currents are flowing. Unbalanced inverter currents can arise from disturbances in the ac power system such as phase voltage imbalance. The presence of many single phase loads in the distribution system can cause unbalanced voltages. If the capacitor voltages drift apart and become unequal, the voltage stress on the switching devices will increase and the inverter voltages will become distorted as well. If the capacitor voltage drift is excessive, the switch ratings may be exceeded resulting in failure.

An algorithm has been developed that provides active control over each capacitor's voltage and permits equalizing of the capacitor voltages when the ac system voltage becomes unbalanced.

The capacitor voltage balancing controller for one of the four capacitors is shown in Fig. 6. The capacitor voltage is compared to the one quarter of the total dc voltage generating an error signal which is filtered and used to phase shift a specific portion of the inverter's output voltage. The direction of the phase shift depends upon whether the SSC is producing leading or lagging vars. In Fig. 6, the controller phaseshifts the level 4 to level 5 section of the waveform to control capacitor C4. The capacitor controller is disabled when the SSC's current output is very low in magnitude. If balancing

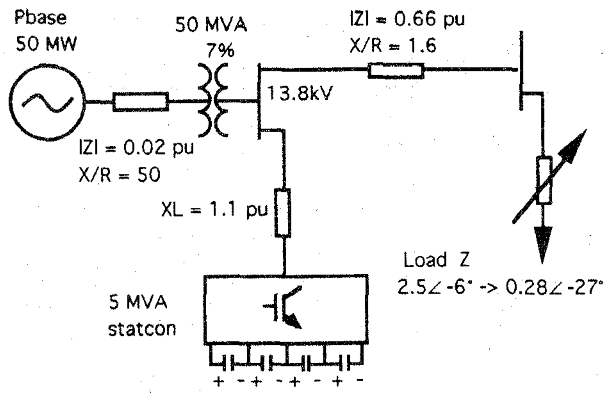


Figure 7. Distribution system model for EMTP simulation

control is desired at very low current levels, a modified algorithm can be employed. Long term drift is prevented by grading resistors across the capacitors.

## VI. EMTP SIMULATION MODEL AND RESULTS

The operational performance of a five–level inverter based SSC was evaluated using EMTP. A model distribution system is shown in figure 7 which includes a SSC directly coupled to a substation bus. A remote varying load is connected through a distribution feeder.

A five–level inverter rated at 5 MVA, 13.8 kV is chosen for analysis. This system rating is comparable in rating to other systems studied for distribution system application [4]. To avoid any series connection of devices, more than five–levels would need to be used in the inverter. Instead of increasing the number of voltage levels, series connection of a small number of devices is assumed. This is not a major concern since it is has been demonstrated that a small number of devices may be successfully put in series.

In Fig. 8, the voltage at the SSC regulated bus is shown when a step increase in three phase load is applied. The system voltage drops by 16 % and is restored in two cycles.

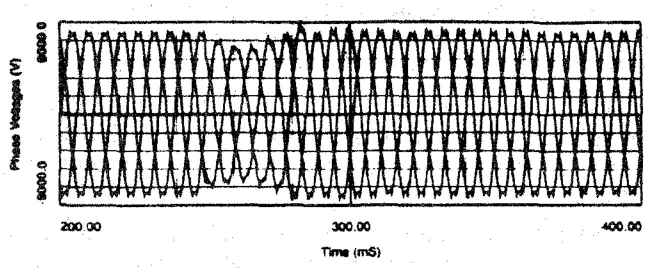


Figure 8. Response of regulated bus voltage to step increase in three phase load.

Fig. 9 shows the voltage on each of the four dc bus capacitors for a three phase load increase. The capacitor voltages track each other and do not drift apart.

When an unbalanced load is applied at the load bus, the phase voltages become unbalanced. Fig. 9 shows the phase voltages at the regulated bus. The compensator controls used in this simulation only regulate the total three phase substation voltage so the phase imbalance persists. The compensator detects an overall reduced voltage and thus adds in leading current resulting in two of the phase voltages being high by 5 % and one phase low by 10 %.

Fig. 11 shows the voltages on each of the dc bus capacitors when the unbalanced voltages are present and the capacitor balancing control is disabled. The presence of voltage unbalance causes the capacitor voltages to deviate from their desired values. If the voltage drift is allowed to continue to grow, the inverter will eventually stop functioning. Fig. 12 shows the capacitor voltages remaining equal when the balancing control is enabled for the same unbalanced load as in Fig. 11.

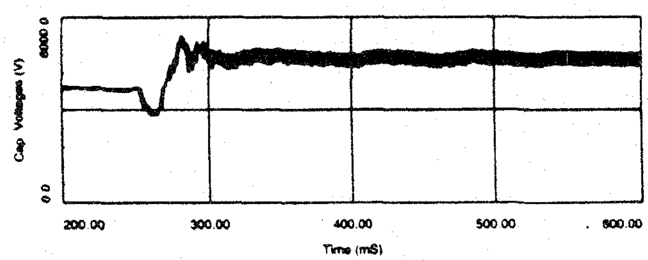


Figure 9. Voltage on each dc bus capacitor during step increase in three phase load.

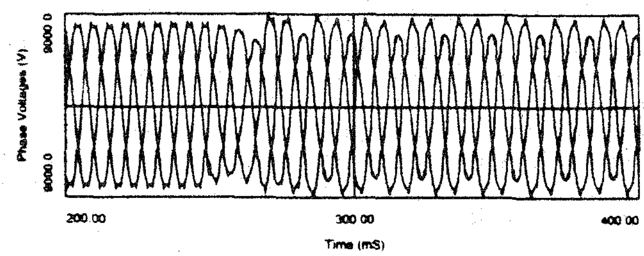


Figure 10. Response of regulated bus voltage to application of an unbalanced load.

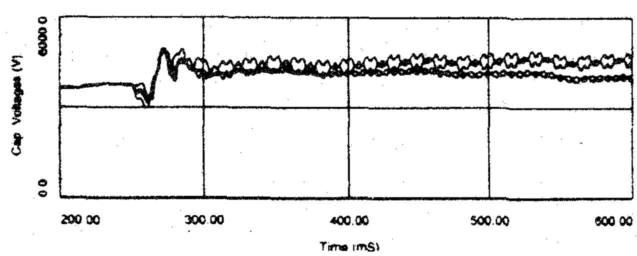


Figure 11. Voltage drift on the capacitor voltages arising from application of an unbalanced load. Capacitor voltage balancing controller is disabled.

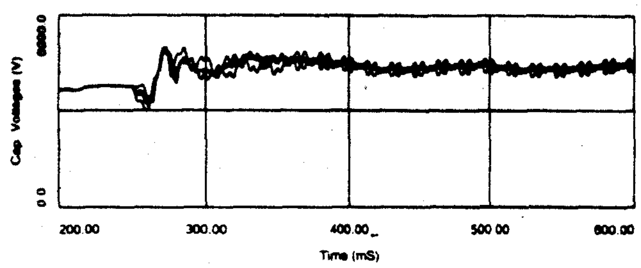


Figure 12. Drift of the capacitor voltages arising from application of an unbalanced load is eliminated when the capacitor voltage balancing controller is active.

## VII. DISCUSSION OF CAPACITOR BALANCING

The capacitor balancing algorithm has been observed to be effective in EMTP simulations. The method does not require additional power conversion components. A small amount of distortion is introduced into the waveform as a result of the phaseshifting of individual sections of the inverter voltage. The distortion occurs only under abnormal conditions such as when the system voltages are greatly unbalanced. In the case of balanced system voltages, the speed of response of the compensator is affected by the size of the dc bus capacitors and the linking reactance.

## VIII. CONCLUSIONS

The capability of the multi–level inverter to limit device voltage stress makes it suitable for high voltage power conversion. Equations developed for the component MVA of the multi–level inverter show that: 1) GTO MVA and capacitor MVA are relatively independent of the number of voltage levels, 2) clamp diode MVA increases strongly with the number of voltage levels, 3) the switching angles of the modulation strategy have a strong effect on capacitor MVA and clamp diode MVA, and 4) the capacitor MVA in the multi–level structure is much larger than in a twelve pulse inverter.

Increasing the number of levels solely to improve harmonic performance may not be justified because of the additional component MVA required. However, increasing the number of levels may still be worthwhile to enable the converter to work within the voltage ratings of available switching devices without using series connected devices.

A capacitor voltage balancing controller has been presented which maintains operation of the multi–level inverter SSC under conditions of phase voltage imbalance is possible and EMTP simulations have been presented to verify that capacitor voltages can be held equal using the described control method.

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