A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation

Mohammad Al-Shyoukh, Hoi Lee, *Member, IEEE*, and Raul Perez, *Member, IEEE*

***Abstract*—This paper presents a low-dropout regulator (LDO) for portable applications with an impedance-attenuated buffer for driving the pass device. Dynamically-biased shunt feedback is proposed in the buffer to lower its output resistance such that the pole at the gate of the pass device is pushed to high frequencies without dissipating large quiescent current. By employing the current-buffer compensation, only a single pole is realized within the regulation loop unity-gain bandwidth and over 65° phase margin is achieved under the full range of the load current in the LDO. The LDO thus achieves stability without using any low-frequency zero. The maximum output-voltage variation can be minimized during load transients even if a small output capacitor is used.**

The LDO with the proposed impedance-attenuated buffer has been implemented in a 0.35-μm twin-well CMOS process. The proposed LDO dissipates 20-μA quiescent current at no-load condition and is able to deliver up to 200-mA load current. With a 1-μF output capacitor, the maximum transient output-voltage variation is within 3% of the output voltage with load step changes of 200 mA/100 ns.

***Index Terms*—Linear regulator, load transient response, low-dropout regulator (LDO), pass device, power management integrated circuits, voltage buffer.**

I. Introduction

POWER management is essential in all battery-powered portable devices such as cellular phones and PDAs in order to reduce the standby power and prolong the battery runtime. Low-dropout regulators (LDOs) are one of the most critical power management modules, as they can provide regulated low-noise and precision supply voltages for noise-sensitive analog blocks. With the widespread proliferation of modern portable devices, ever more stringent performance requirements of the LDO are needed. First, low dropout voltage across the pass device of the LDO is required provide high power efficiency. In addition, the increased level of integration in portable devices not only demands the LDO to deliver high load current, but also requires the no-load quiescent current of the LDO to be minimized for improving the current efficiency [1]. Good load transient response with small output-voltage variation including overshoots and undershoots upon load switching is critical to prevent an accidental turn off or resetting of the portable device. These four major performance requirements of the LDO, including low dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots and overshoots are, however, difficult to achieve simultaneously.

In LDO design, the ability to source high load current while achieving low dropout voltage requires the use of a large size pMOS transistor as the pass device [1]. In addition to the low-frequency dominant pole generated by the output capacitor, the large gate capacitance of the pMOS pass device creates another low-frequency non-dominant pole within the unity-gain frequency of the regulation loop, thereby degrading stability. Different approaches have been reported to address this issue [1]–[5]. In [1], an emitter-follower has been adopted as a voltage buffer to drive the pMOS pass device. The low output resistance of the emitter-follower allows the pole at the gate of the pass device to be pushed beyond the unity-gain frequency of the LDO regulation loop. The reported LDO dissipates low quiescent current, while sourcing the maximum load current of 50 mA [1]. However, if the LDO is required source a larger load current (e.g., 100 mA or more), a much larger pass device with larger gate capacitance is needed. The current dissipation of the emitter-follower thus needs to be greatly increased to further lower its output resistance at the gate of the pass device for maintaining loop stability. Instead of dissipating large quiescent current in the voltage buffer to achieve loop stability, the approach of creating a low-frequency left-half-plane (LHP) zero has been widely employed, which provides positive phase shift to compensate for the negative phase shift due to the low-frequency non-dominant pole [2]–[5]. The low-frequency LHP zero can be generated by either adding a resistor in series with the output capacitor (or the intrinsic equivalent series resistor (ESR) of the output capacitor), namely ESR zero [2]–[4], or relying on frequency compensation through a voltage-controlled current source [5]. However, the exact pole-zero cancellation within the unity-gain frequency of the LDO regulation loop is difficult to achieve under the full range of the load current. The incomplete pole-zero cancellation may lead to instability of the LDO in the worst condition. Small pole-zero frequency mismatch within the unity-gain frequency can degrade the quasi-linear transient settling behavior [6], [7] of the LDO upon load switching. Even worse, if the ESR zero approach is adopted, the resistor leads to large output overshoots and undershoots during massive load-current step changes especially when a low-value output capacitor C_L of micro-farad range is used.

Manuscript received November 10, 2006; revised April 12, 2007. This work was supported by Texas Instruments Inc.

M. Al-Shyoukh is with Texas Instruments Inc., Dallas, TX 75243 USA, and also with the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX 75083-0688 USA (e-mail: mshyoukh@ti.com).

H. Lee is with the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX 75083-0688 USA (e-mail: hoilee@utdallas.edu).

R. Perez is with Fyrestorm Inc., Sunnyvale, CA 94085 USA.

Digital Object Identifier 10.1109/JSSC.2007.900281

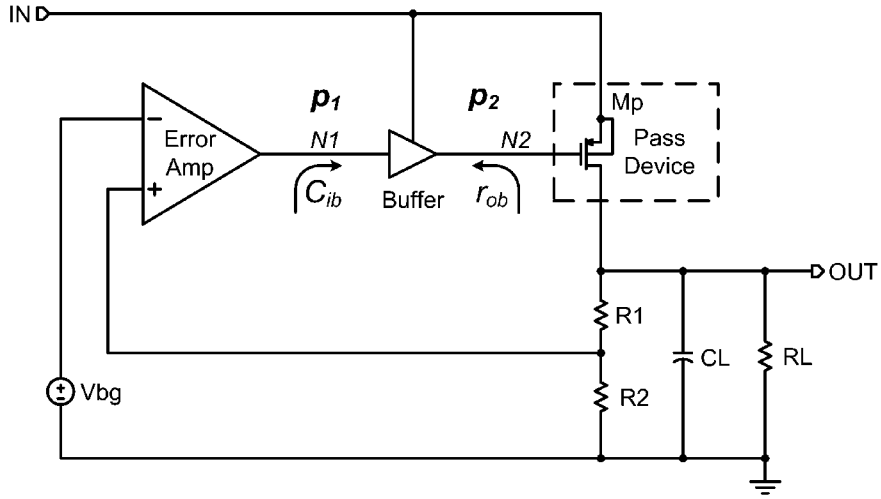

Fig. 1. Typical structure of a low-dropout regulator with an intermediate buffer stage.

In order to further improve LDO performances, buffer impedance attenuation technique (BIA) is first proposed to realize an intermediate stage for driving the pMOS pass device. The proposed BIA technique greatly reduces the output resistance of the buffer through dynamically-biased shunt feedback. As a result, the pole at the gate of the pass device is pushed far beyond the unity-gain frequency of the LDO regulation loop under the entire load current range even if a huge pass device is used for achieving low dropout voltage and sourcing high load current. The BIA technique thus allows the LDO to dissipate low quiescent current. By employing current-buffer compensation in the LDO, only a single pole is realized within the unity-gain frequency and a good phase margin is achieved for the entire load current range with a small compensation capacitor. The LDO thus achieves stability without using any low-frequency zero. Moreover, the LDO can have good transient settling behavior and small output-voltage variation even if a small output capacitor is used.

This paper is organized as follows. Section II presents the operational principle of the proposed BIA technique, while different design considerations including the stability analysis of the LDO using current-buffer compensation and details of LDO circuit implementation are discussed in Section III. Finally, Sections IV and V provide the measurement results of the proposed LDO and the conclusions, respectively.

II. Proposed Impedance-Attenuated Buffer

Fig. 1 shows a typical structure of a low-dropout regulator, which consists of an error amplifier comparing a scaled-down output signal to a bandgap voltage V_{bg}, a pMOS pass transistor M_p, and an intermediate buffer stage driving M_p. There are three poles in the LDO structure located at the output of the error amplifier (N_1), the output of the buffer (N_2), and the output of the LDO (V_{out}). In particular, these poles are given by

$$p_{1\,|\,N_1} = 1/(r_{o1}C_1) \tag{1}$$

$$p_{2\,|\,N_2} = 1/(r_{ob}C_p) \tag{2}$$

$$p_{o\,|\,V_{\text{out}}} = 1/(R_{oeq}C_L) \tag{3}$$

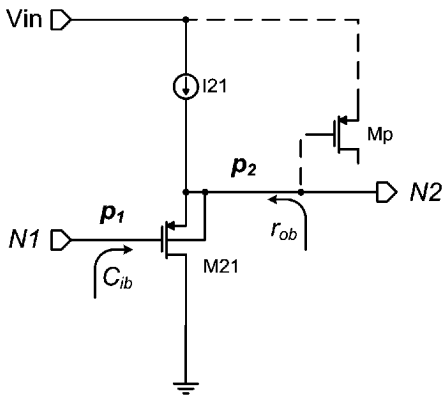

Fig. 2. Source-follower implementation of the intermediate buffer stage.

where r_{o1} is the output resistance of the error amplifier, C_1 is the equivalent capacitance at N_1 which is dominated by the input capacitance of the buffer C_{ib}, r_{ob} is the output resistance of the buffer, C_p is the input capacitance of M_p, and R_{oeq} is the equivalent resistance seen at the output of the LDO. Ideally, both C_{ib} and r_{ob} should be very small in order to achieve single-pole loop response by locating both p_1 and p_2 at frequencies much higher than the unity-gain frequency of the regulation loop.

In order to construct the required intermediate buffer stage, a simple pMOS source-follower is first considered to implement the buffer and its structure is shown in Fig. 2. The pMOS source-follower can provide near complete shutdown of the pass device under light-load conditions. Since the output resistance r_{ob} of the source-follower is given by $1/g_{m21}$, it is necessary to increase g_{m21} in order to decrease the value of r_{ob} and allow p_2 to be located at frequencies much higher than the unity-gain frequency of the LDO regulation loop. Transconductance g_{m21} can only be increased either through using a larger W/L ratio of transistor M_{21}, or through increasing the DC biasing current I_{21} through M_{21}, or both. Increasing I_{21} would, however, increase the total quiescent current of the LDO, thereby degrading the current efficiency of the LDO. Using a larger W/L ratio of M_{21} would increase the input capacitance C_{ib} of the buffer, which in turn pushes p_1 to a lower frequency and the stability can be

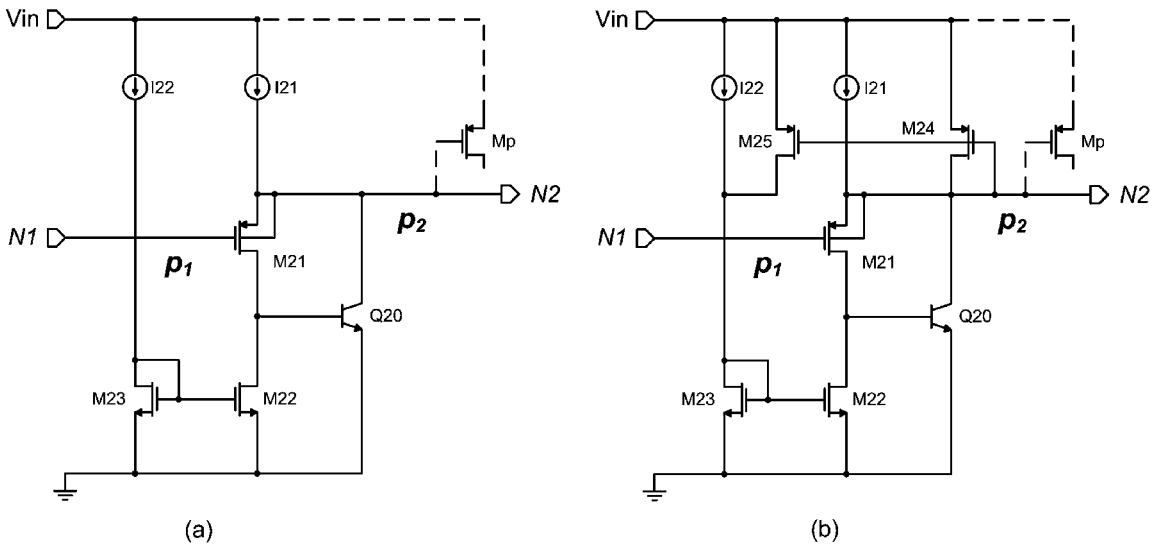

Fig. 3. (a) Source-follower with shunt feedback and (b) proposed buffer with dynamically-biased shunt feedback for output resistance reduction under different load currents.

poorly affected. A simple pMOS source-follower is, therefore, not a suitable implementation of the intermediate buffer stage in the LDO.

To minimize W/L ratio of M_{21} and the quiescent current required to reach a given r_{ob}, the source-follower with negative feedback shown in Fig. 3(a) is used. In particular, the npn transistor Q_{20} is the feedback device connected in parallel to the output of the source-follower M_{21} in order to reduce r_{ob} through shunt feedback. From a qualitative standpoint, when the input voltage at N_1 is constant and the output voltage increases, the magnitude of the drain current of M_{21} also increases, which in turn increases the base current of Q_{20}. As a result, the collector current of Q_{20} increases, reducing the output resistance r_{ob} by increasing the total current that flows into the output node. The output resistance looking into the follower is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta)}. \tag{4}$$

Equation (4) shows that the output resistance of the follower is reduced by the current gain β of the shunt feedback device Q_{20}. For example, when an npn transistor with $\beta \approx 10$ is used, the value of r_{ob} would be decreased by about 10 times and the frequency of p_2 at the gate of the pass device is then pushed to a decade higher. As a result, the quiescent current needed through M_{21} is greatly reduced to realize g_{m21} for a given r_{ob}. Similarly, the transistor size of source-follower M_{21} required is also reduced. The input capacitance of the buffer C_{ib} is then decreased, which allows p_1 given in (1) to be located at a higher frequency without dissipating additional quiescent current.

It should be noted that the shunt feedback device Q_{20} can also be implemented by a nMOS transistor in single-well technologies to achieve a similar reduction in the output resistance [8]. Since inexpensive twin-well technologies with large feature size (0.35 μm and larger) are widely used for integrated power ICs and vertical parasitic npn structures with $\beta > 10$ are available in twin-well technologies, the shunt feedback device is implemented by the vertical parasitic npn transistor in our design.

Since the unity-gain frequency of the LDO regulation loop increases with the load current, the output resistance of the buffer should decrease when the load current increases in order to maintain p_2 far beyond the unity-gain frequency under the entire load current range. Fig. 3(b) shows the proposed structure of the buffer, in which two pMOS transistors M_{24} and M_{25} and the npn transistor Q_{20} realize dynamically-biased shunt feedback to decrease r_{ob} under different load current conditions. The output resistance of the proposed buffer is then given by

$$r_{ob} = \frac{1}{g_{m21}(1+\beta) + g_{m24}} \tag{5}$$

where g_{m24} is the transconductance of the diode-connected transistor M_{24}. As shown in Fig. 3(b), when the load current flowing through the pass device M_p increases, both voltages at N_1 and N_2 decrease. The gate-source voltage of M_{24} is increased and hence more current flows through M_{24}. This current then mirrors through M_{25} such that the current through the follower device M_{21} dynamically increases with the load current. This boosts the value of g_{m21}, thereby further reducing the output resistance of the buffer according to (5). In addition, the increase in g_{m24} with the load current can reduce the value of r_{ob}. This effect is significant under heavy load current conditions. Moreover, when the load current increases, part of the dynamically-increased current through M_{21} flows into the base of Q_{20} and increases its collector current. The current gain β of the vertical parasitic npn transistor slightly increases with the collector current, which also helps on reducing the value of r_{ob} when the load current increases.

The proposed buffer also improves the slewing of the gate drive at N_2 during load transients. During the transition from no load to full load, the decrease in the voltage at N_1 causes an increase in the transient current through M_{21}, which flows through the base of Q_{20}. The collector current of Q_{20} then increases to discharge the large gate capacitance of the pass device C_p and the voltage at N_2 decreases with a faster slewing. It should be noted that I_{21} is designed to be larger than I_{22} such that Q_{20} is always on under different load currents. Similarly,

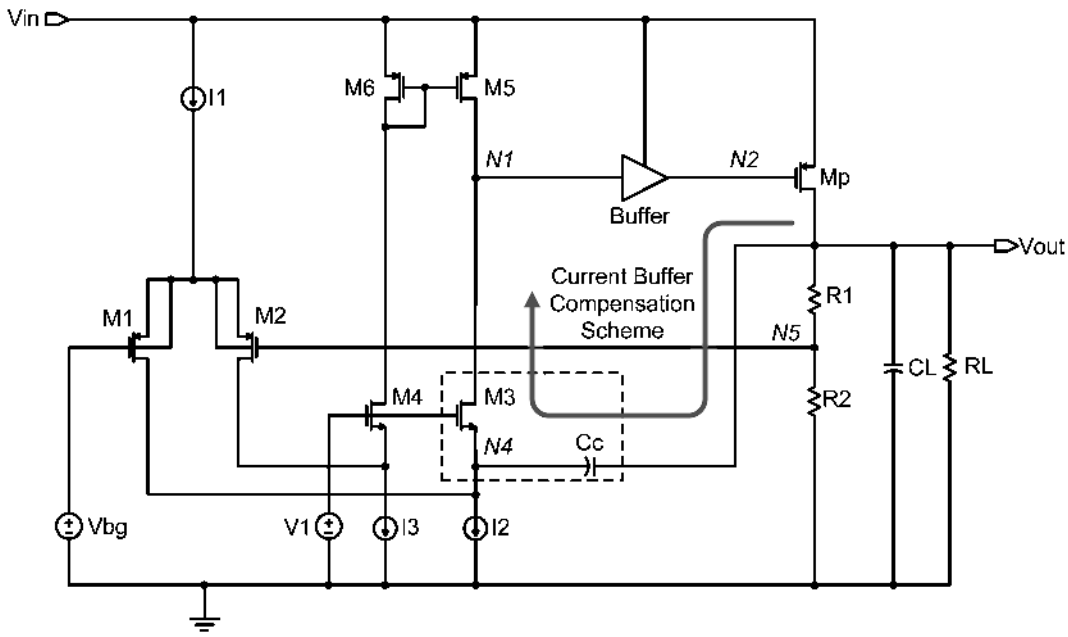

Fig. 4. Structure of the proposed LDO using current-buffer compensation scheme.

when the voltage at N_1 increases, transistor M_{24} provides extra transient current to charge C_p and increase the voltage at N_2 to follow the voltage change at N_1 with a faster slewing during the transition from full load to no load.

In short, the proposed buffer with dynamically-biased shunt feedback reduces both the input and output impedance of the buffer by decreasing the values of C_{ib} and r_{ob}, respectively. In particular, the reduction in the value of r_{ob} increases with the load current. As a result, p_2 is located at sufficiently high frequencies under different load currents, while the LDO only dissipates low quiescent current at no-load condition. The benefit of having a smaller C_1 by using a smaller size of source-follower device in the proposed buffer also improves the stability of the LDO, which will be further clarified in the next section.

III. Design of the Proposed LDO

In the proposed LDO structure shown in Fig. 4, the error amplifier is realized by a single-stage folded-cascode structure with transistors M_1–M_6. As discussed in the previous section, the pole p_2 at the output of the buffer is pushed to sufficiently high frequencies under different load currents by employing dynamically-biased shunt feedback. The pass device M_p realizes a common-source gain stage and constitutes the second gain stage in the LDO. Accordingly, the resulting LDO structure can be viewed as a two-stage amplifier driving a large capacitive load with two poles located at N_1 and the LDO output. The large capacitive load is due to the use of a micro-farad range off-chip output capacitor C_L. This LDO structure can be stabilized using current-buffer (or cascode-Miller) frequency compensation, which is a pole-splitting compensation designed for splitting two poles p_1 at N_1 and p_o at the LDO output in order to achieve stability in the full range of the load current. In two-stage amplifier design, the use of the current-buffer compensation scheme allows the amplifier to achieve wider unity-gain frequency and improved stability by removing the right-half-plane zero and enhance PSRR [9]–[15]. In the proposed LDO, current-buffer compensation also removes the right-half-plane zero and improves PSRR. Additionally and more importantly, this compensation allows the LDO to achieve stability over the entire load current range by using only a small compensation capacitor. In Fig. 4, the current-buffer compensation in the LDO is realized by C_c and the common-gate transistor M_3 [15]. The details of the stability using the current-buffer compensation are discussed in the following subsection.

A. Stability Analysis

The stability of the proposed LDO is studied using the loop-gain transfer function $T(s)$ of the regulation loop. Fig. 5 is the small-signal block diagram representation of the circuit in Fig. 4 for analyzing the loop-gain transfer function. Here, g_{m1}, g_{m3} and g_{mp} represent the transconductances of input differential stage M_1/M_2, current buffer stage M_3 and pass device M_p, respectively. In addition, B is the feedback factor $R_2/(R_1 + R_2)$. As mentioned before, since the output of the buffer N_2 is a low impedance node and p_2 is located at a very high frequency under the full range of the load current, the capacitive loading at N_2 is neglected in the analysis. The loop-gain transfer function is derived based on the following considerations.

1) C_L, C_c are much larger than C_1.
2) Transconductance g_{mp} and output resistance R_{oeq} provide the gain of the pass device $A_p = g_{mp}R_{oeq}$ and A_p varies with the load current I_L. In particular, g_{mp} (R_{oeq}) decreases (increases) with the load current and $A_p = g_{mp}R_{oeq}$ is inversely proportional to $\sqrt{I_L}$.

Based on the above, the loop-gain transfer function of the proposed LDO is given as

$$T(s) = \frac{T_{\text{out}}}{T_{\text{in}}} = \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}\left(1 + s\frac{C_c}{g_{m3}}\right)}{1 + as + bs^2 + cs^3} \tag{6}$$

$$a = R_{oeq}(C_L + g_{mp}r_{o1}C_c) \tag{7}$$

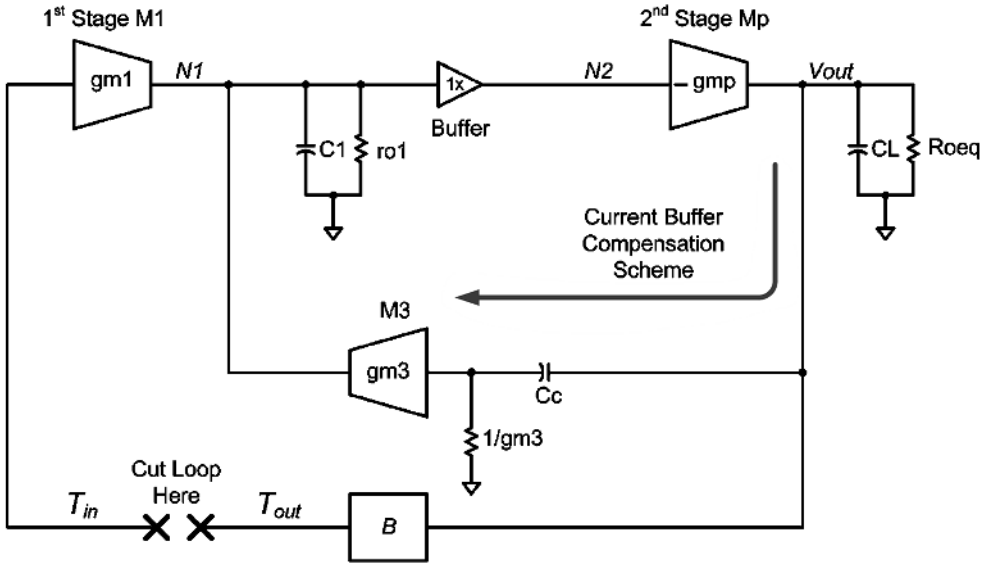

Fig. 5. Small-signal block diagram of the proposed LDO with current-buffer compensation scheme.

$$b = C_1 C_L r_{o1} R_{oeq} \tag{8}$$

$$c = \frac{C_1 C_c C_L r_{o1} R_{oeq}}{g_{m3}}. \tag{9}$$

From (6), the loop gain is negative due to the negative feedback established for output voltage regulation. In addition, the numerator of $T(s)$ indicates that a LHP zero $z_b = g_{m3}/C_c$ exists, while the third-order polynomial of the denominator implies that the system has three poles. According to (7)–(9), locations of poles vary under different load currents due to the existence of R_{oeq} and g_{mp}. As a result, the loop gain transfer function should be studied for different load current conditions.

When $I_L = 0$, the current drain from the pass device is $V_{\rm out}/(R_1 + R_2)$, which is around 1–3 μA. Hence, g_{mp} is at its minimum and $C_L R_{oeq} \gg g_{mp} r_{o1} C_c R_{oeq}$ in (7). As a result, $T(s)$ in (6) can be approximated to

$$\begin{aligned} T(s)\,|_{I_L=0} &\approx \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}\left(1+s\frac{C_c}{g_{m3}}\right)}{1+sC_LR_{oeq}+s^2C_1C_Lr_{o1}R_{oeq}+s^3\frac{C_1C_cC_Lr_{o1}R_{oeq}}{g_{m3}}} \\ &\approx \frac{-Bg_{m1}g_{mp}r_{o1}\left(1+s\frac{C_c}{g_{m3}}\right)}{(1+sC_LR_{oeq})(1+sC_1r_{o1})\left(1+s\frac{C_c}{g_{m3}}\right)} \\ &= \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{(1+sC_LR_{oeq})(1+sC_1r_{o1})} \\ &= \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{\left(1+\frac{s}{p_{-3\rm dB}\,|\,I_L=0}\right)\left(\frac{s}{p_{\rm nd}\,|\,I_L=0}\right)} \end{aligned} \tag{10}$$

where $p_{-3\rm dB}\,|\,I_L=0 = 1/(C_L R_{oeq})$ and $p_{\rm nd}\,|\,I_L=0 = 1/(C_1 r_{o1})$ are dominant and non-dominant poles of $T(s)\,|_{I_L=0}$. As indicated in (10), the system is designed to have three separate poles and the third pole is canceled by the LHP zero, resulting in a second-order system. In particular, $p_{-3\rm dB}\,|\,I_L=0 = p_o$ and $p_{\rm nd}\,|\,I_L=0 = p_1$ indicate that no pole splitting occurs during $I_L = 0$ and both the dominant and non-dominant poles are located at the LDO output and the output of the error amplifier, respectively. With the proposed buffer-impedance attenuation technique, the value of C_1 can be minimized due to the smaller source-follower device. The small C_1 allows $p_{\rm nd}\,|\,I_L=0$ to be much higher than the unity-gain frequency of the loop-gain transfer function, which guarantees the proposed LDO to achieve good phase margin under $I_L = 0$.

When the load current significantly increases, g_{mp} becomes much larger. Hence, $g_{mp} r_{o1} C_c R_{oeq} \gg C_L R_{oeq}$ in (7), and $T(s)$ in (6) is approximated to

$$\begin{aligned} T(s)\,|_{I_L\gg 0} &\approx \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}\left(1+s\frac{C_c}{g_{m3}}\right)}{1+sg_{mp}C_cr_{o1}R_{oeq}+s^2C_1C_Lr_{o1}R_{oeq}+s^3\frac{C_1C_cC_Lr_{o1}R_{oeq}}{g_{m3}}} \\ &\approx \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}(1+s\frac{C_c}{g_{m3}})}{\left(1+s\frac{1}{g_{mp}C_cr_{o1}R_{oeq}}\right)\left(1+s\frac{C_1C_L}{g_{mp}C_c}\right)\left(1+s\frac{C_c}{g_{m3}}\right)} \\ &= \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{(1+sg_{mp}C_cr_{o1}R_{oeq})\left(1+s\frac{C_1C_L}{g_{mp}C_c}\right)} \\ &= \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{\left(1+\frac{s}{p_{-3\rm dB}\,|\,I_L\gg 0}\right)\left(\frac{s}{p_{\rm nd}\,|\,I_L\gg 0}\right)}. \end{aligned} \tag{11}$$

Equation (11) shows that the loop gain transfer function has also two poles under $I_L \gg 0$, where $p_{-3\rm dB}\,|\,I_L\gg 0 = 1/(g_{mp}C_c r_{o1} R_{oeq})$ and $p_{\rm nd}\,|\,I_L\gg 0 = (g_{mp}C_c)/(C_1 C_L)$ are the dominant and non-dominant poles of $T(s)\,|_{I_L\gg 0}$. Under this condition, the maximum unity-gain frequency of the loop-gain transfer function is achieved ($\omega_{u,\max} = g_{m1}/C_c$), which is fixed with respect to the load current change. Since $p_{\rm nd}\,|\,I_L\gg 0$ is always larger than $\omega_{u,\max}$, only a single pole exists within the unity-gain frequency of the regulation loop. In addition, $p_{\rm nd}\,|\,I_L\gg 0$ increases with the load current, which implies that the phase margin and stability of the LDO improve with the load current.

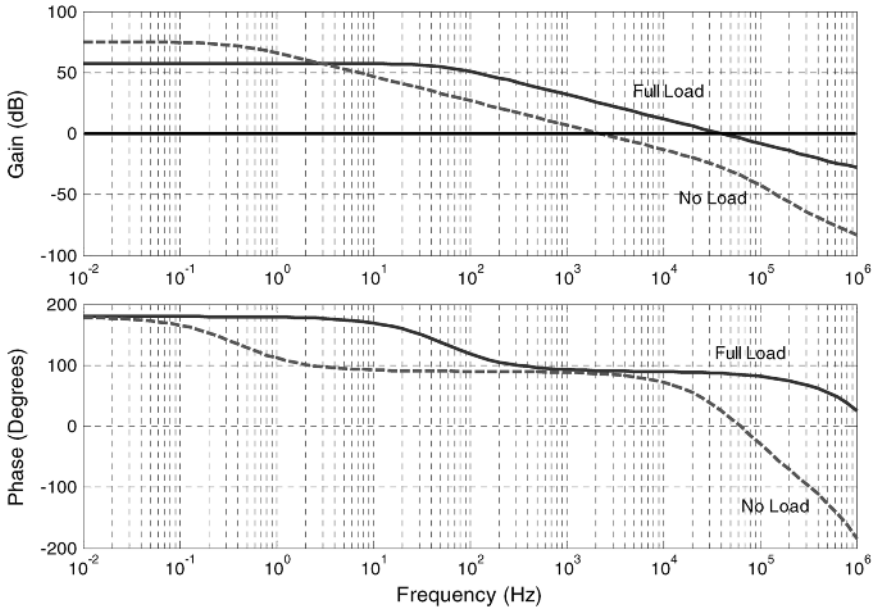

Fig. 6. Simulated loop-gain transfer function of the proposed LDO with a 1 μF output capacitor.

Similar to the derivation in (10) and (11), the loop-gain transfer function of the proposed LDO using current-buffer compensation is actually a second-order system under the full range of the load current and $T(s)$ from (6) can then be simplified as

$$\begin{aligned} T(s) &\approx \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{1+sR_{oeq}(C_L+g_{mp}r_{o1}C_c)+s^2C_1C_Lr_{o1}R_{oeq}} \\ &\approx \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{[1+sR_{oeq}(C_L+g_{mp}r_{o1}C_c)]\left(1+s\frac{C_1C_Lr_{o1}}{(C_L+g_{mp}r_{o1}C_c)}\right)} \\ &= \frac{-Bg_{m1}g_{mp}r_{o1}R_{oeq}}{(1+p_{-3\mathrm{dB}})(1+p_{\mathrm{nd}})}. \end{aligned} \tag{12}$$

Equation (12) can be used to find out the worst-case stability of the LDO under different load currents such that the value of the compensation capacitor C_c can be designed to ensure the stability of the LDO in the entire load current range. The worst-case stability occurs at the minimum phase margin of the second-order system. The phase margin (PM) of a compensated two-pole system is given by

$$\mathrm{PM} = 90^\circ - \arctan\frac{\omega_u}{p_{\mathrm{nd}}} \tag{13}$$

where ω_u is the unity-gain frequency. The larger the ratio p_{nd}/ω_u is, the better the PM of the system can achieve. As a result, F_{PM} is defined to evaluate the separation between p_{nd} and ω_u under different load currents, which is given as

$$F_{\mathrm{PM}} = \frac{p_{\mathrm{nd}}}{\omega_u} = \frac{\omega_{p_{\mathrm{nd}}}}{A_{\mathrm{DC}}\cdot p_{-3\mathrm{dB}}} \tag{14}$$

where A_{DC} is the DC loop-gain magnitude given by $Bg_{m1}g_{mp}r_{o1}R_{oeq}$. By substituting $p_{\mathrm{nd}}, p_{-3\mathrm{dB}}$ and A_{DC} from (12) into (14) and setting $B=1$ [$B=1$ corresponds to the worst-case feedback factor for stability as it maximizes the denominator of (14)], F_{PM} can be rewritten as

$$F_{\mathrm{PM}} = \frac{(C_L+g_{mp}\cdot r_{o1}C_c)^2}{g_{mp}\cdot(g_{m1}C_1C_Lr_{o1}^2)}. \tag{15}$$

If we differentiate F_{PM} with respect to g_{mp} and set the derivative to zero, the minimum value of F_{PM} can be found, at which the minimum phase margin occurs. The resulting minimum $F_{\mathrm{PM,min}}$ is given by

$$F_{\mathrm{PM,min}} = \frac{4}{g_{m1}r_{o1}}\cdot\frac{C_c}{C_1}. \tag{16}$$

By substituting (16) into (13), the minimum phase margin $\mathrm{PM}_{\mathrm{min}}$ is given as

$$\mathrm{PM}_{\mathrm{min}} = 90^\circ - \arctan\left(\frac{g_{m1}r_{o1}}{4}\cdot\frac{C_1}{C_c}\right) \tag{17}$$

and from (17), the C_c can be designed as

$$C_c = \frac{g_{m1}r_{o1}}{4\cdot\tan(90^\circ-\mathrm{PM}_{\mathrm{min}})}\cdot C_1. \tag{18}$$

From (18), C_c is proportional to small parasitic capacitance C_1. Accordingly, the impedance-attenuated buffer which results in a small C_1 reduces the required value of C_c. In our design, a C_c of 10 pF is sufficient for the LDO to be stable under the full range of the load current. This capacitance can be easily integrated in CMOS technologies.

The simulated loop gain transfer functions of the proposed LDO with $C_L = 1$ μF under no-load and full-load conditions are shown in Fig. 6. Simulated results validate the existence of only a single pole within the unity-gain frequency and a good phase margin of approximately 90° is achieved under both conditions. In addition, Fig. 7 shows the simulated phase margin of the loop-gain transfer function under different load currents. The minimum phase margin is always larger than 65° for the entire range of the load current. This simulation result further verifies that a small C_c of 10 pF is sufficient to ensure unconditionally stability under the full range of the load current.

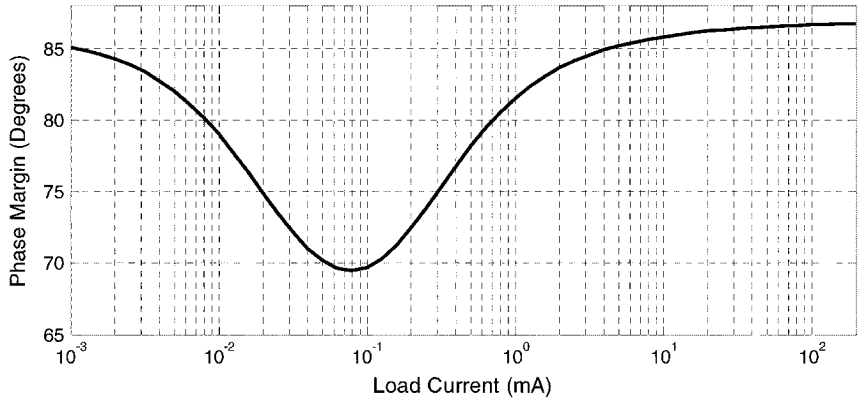

Fig. 7. Phase margin of the proposed LDO loop-gain transfer function under different load currents with a 1-μF output capacitor.

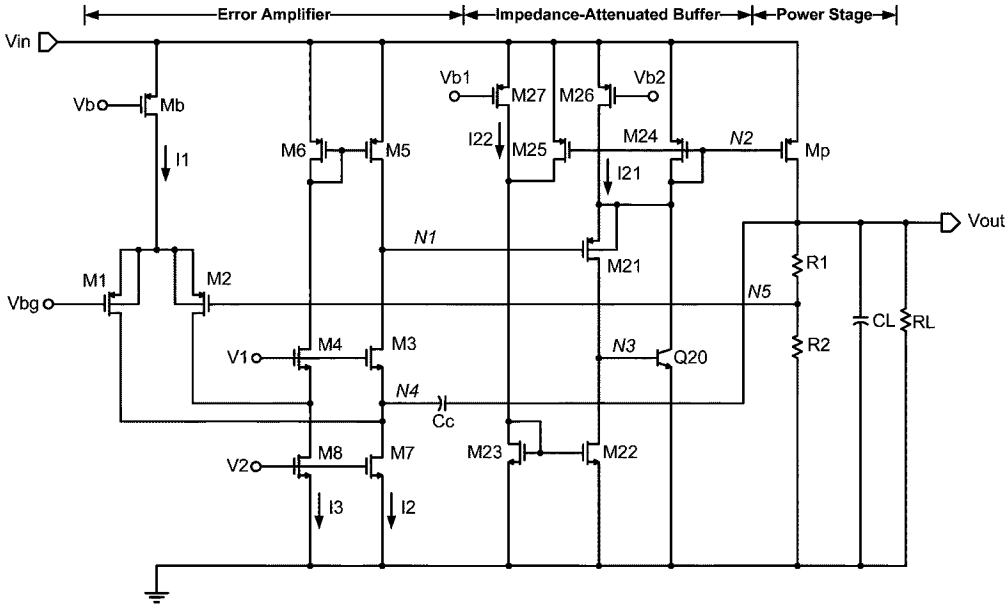

Fig. 8. Schematic of the proposed LDO.

B. Circuit Design

The schematic of the proposed LDO is shown in Fig. 8 [16]. A 1-V bandgap voltage reference is integrated together with the LDO to provide the reference voltage V_{bg} to the input of the error amplifier. In the single-stage folded-cascode error amplifier, a simple diode-connected active load using transistors M_5 and M_6 is adopted. The simple diode-connected active load results in a smaller output resistance of the error amplifier r_{o1} as compared to a cascode load, which helps reduce the value of compensation capacitor C_c to achieve a particular phase margin according to (18). In the proposed LDO, the gain of the error amplifier is equal to $g_{m1}r_{o1}$ and can always be greater than 50 dB under the entire load current range.

Moreover, the use of a pMOS transistor to implement the source-follower in the proposed buffer is extremely critical to minimize the quiescent current at no-load condition. Under no-load condition, the pass device M_p is almost turned off, as it only provides current for the feedback resistors R_1 and R_2. The current is equal to $V_{\text{out}}/(R_1 + R_2)$, and the gate-source voltage V_{sg} required for M_p to minimize the amount of current can be around 100 mV. In order to allow the error amplifier to maintain its gain, the DC voltage level at the output of the error amplifier needs to be at least an overdrive voltage $V_{ov} \approx$ 200 mV below V_{in}. If the buffer stage has no level shifting toward the input supply, V_{sg} of the pass device would need to be increased under no-load condition in order to allow the DC voltage at N_1 to be within the output swing of the error amplifier. As a result, both R_1 and R_2 need to be reduced to accommodate the required increase in V_{sg} of M_p, which results in an undesirable increase in the quiescent current in the LDO under no-load condition.

IV. Experimental Results and Discussions

In order to verify the proposed buffer impedance attenuation technique, the LDO shown in Fig. 8 was fabricated in a 0.35-μm twin-well 7-V CMOS process. Fig. 9 shows the die micrograph of the proposed LDO, which was fabricated as part of an integrated power IC. The effective die area of the LDO is 0.264 mm^2. It should be noted that the output voltage of the LDO is bonded with only a single bonding wire from the pad to the pin in order to minimize the cost.

The input voltage range of the LDO is designed from 2.0 V to 5.5 V for portable applications using lithium-ion batteries. This

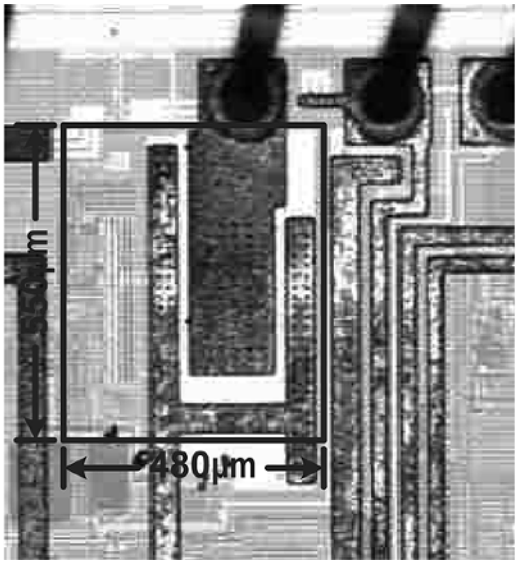

Fig. 9. Micrograph of the proposed LDO.

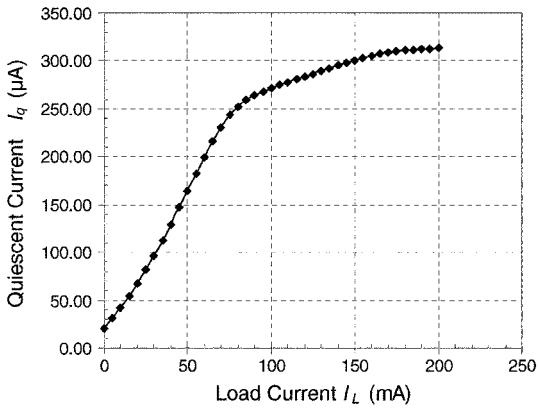

Fig. 10. Measured quiescent current under different load currents.

covers the widest lithium-ion battery variation, which ranges from 2.5 V to 5.5 V. The output voltage of the LDO has programmable steps with a step size of 50 mV and the minimum output voltage is 1.8 V. When $V_{\rm out} = 1.8$ V, the LDO can deliver up to 200 mA with a dropout voltage of 0.2 V. The output capacitor range is from 1 μF to 100 μF. Fig. 10 shows the measured quiescent current I_q under different load currents I_L. The figure indicates that the quiescent current increases with I_L, which validates the dynamic increase in current realized by transistors M_{24} and M_{25} to lower the output resistance of the intermediate buffer stage. In addition, from Fig. 10, the LDO consumes small quiescent current of 20 μA under no-load condition, while the quiescent current of 320 μA is dissipated at full-load condition. It should be noted that the maximum quiescent current seen over multiple samples at full load is 340 μA, which corresponds to the worst-case current efficiency of 99.8% in the proposed LDO. Table I provides the detailed measurement results.

Fig. 11(a) shows the transient response of the proposed LDO when the load current is pulsating between 1 mA and 200 mA with pulse rise and fall time of 100 ns. With the use of a 1-μF output ceramic capacitor, the maximum output-voltage variation is less than 40 mV when $V_{\rm out}$ is at 1.8 V, which includes

TABLE I
PERFORMANCE SUMMARY OF PROPOSED LDO

Full Load Current	200mA
Output Capacitor	1μF
I_q (no-load)	20μA
I_q (full-load)	340μA
Dropout Voltage $V_{\rm do}$	0.2V
DC Load Regulation 0 - 200mA	34mV = 170μV/mA (single bondwire)
DC Line Regulation	2mV/V ($\Delta V_{\rm in}$ = 3.5V)
PSRR (0-20kHz)	> 45dB
Transient Response 0 - 200mA Step	Undershoot < 1.1% C_L = 1μF
Transient Response 1 - 200mA Step	Undershoot < 0.9% C_L = 1μF
Die Area	0.264mm^2
Technology	0.35μm CMOS

output undershoots, overshoots and variations due to load regulation. This 40-mV total output variation corresponds to slightly more than 2% of $V_{\rm out}$. The total output undershoots and overshoots are less than 15 mV above and below the steady-state $V_{\rm out}$, which amounts to less than 1% of the output voltage. With the same output capacitor, when the LDO is tested with full-load steps pulsating between 0 and 200 mA, Fig. 11(b) shows that the maximum output-voltage variation is 54 mV, which corresponds to 3% of $V_{\rm out}$. The transient undershoot of 20 mV only accounts for 1.1% of $V_{\rm out}$. Fig. 12 shows the measured load transient response when output voltage of the LDO is changed to 3.15 V. In this case, the maximum output voltage variation is 65 mV, which is 2% of $V_{\rm out} = 3.15$ V. The transient undershoot for this condition is 25 mV, which only corresponds to 0.8% of $V_{\rm out}$.

Based on measured results shown in Figs. 11(a) and (b) and 12, transient overshoots and undershoots only occupy a small portion of the total output-voltage variation under massive load-step changes even when a small output capacitor of 1 μF is used. This is because both the proposed impedance-attenuated buffer and current-buffer compensation allow the LDO to achieve stability without relying on any low-frequency ESR zero. Moreover, the well-behaved transient settling behavior of the output voltage further justifies large phase margin achieved in the LDO by using the proposed techniques.

As mentioned before, the LDO output is bonded with a single bonding wire to the pin in our design and the resistance of the bondwire varies from 50 mΩ to 100 mΩ. The IR drop across the bondwire can then be as high as 20 mV when the load current is 200 mA. This accounts for almost 60% of the total DC load regulation error of 34 mV in Fig. 11(b). This error can be reduced if multiple bonding wires are used to decrease the bondwire resistance. As a result, both the DC load regulation and the total output-voltage variation during transient can be minimized.

The measured line transient response of the proposed LDO is shown in Fig. 13 in order to evaluate the effect of battery voltage

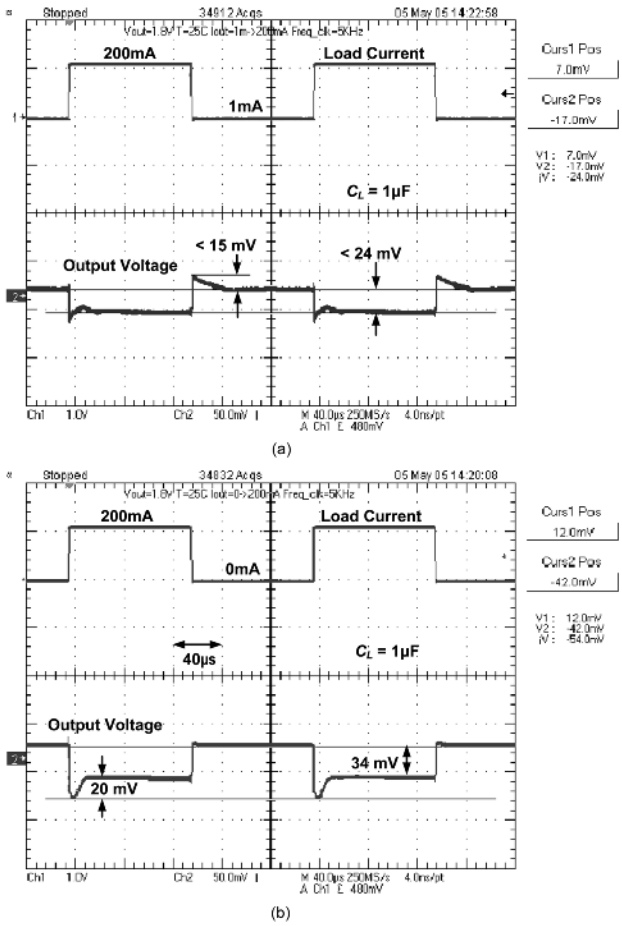

Fig. 11. Measured load transient response of the proposed LDO for a load step pulsating (a) between 1 mA and 200 mA and (b) between 0 and 200 mA with rise and fall time of 100 ns and $V_{\rm out} = 1.8$ V.

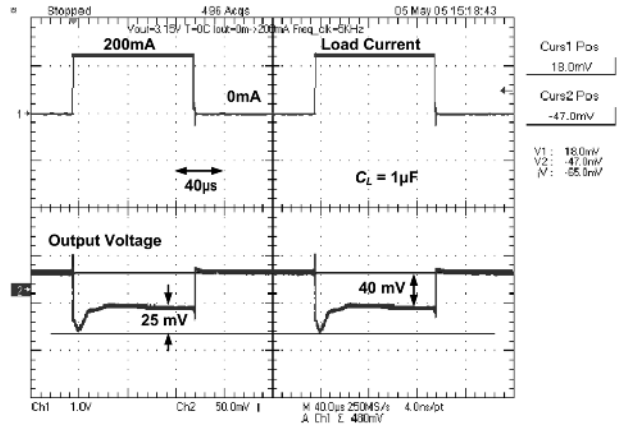

Fig. 12. Measured load transient response of the proposed LDO for a load step pulsating between 0 and 200 mA with rise and fall time of 100 ns and $V_{\rm out} = 3.15$ V.

changes on the LDO output voltage. When the change in the input supply of the LDO is 1 V with rise and fall time of 40 μs, the output voltage changes by less than 3 mV at $I_L = 1$ mA.

In order to provide a clearer picture of the performance improvement in the proposed LDO resulting from the impedance-attenuated buffer and current-buffer compensation, a comparison of some reported LDOs is given in Table II.

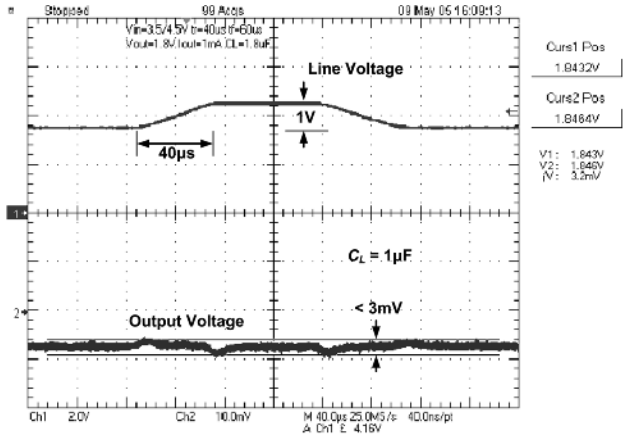

Fig. 13. Measured line transient response of the proposed LDO for a line step change of 1 V.

A figure of merit FOM $= T_r(I_q/I_{L,\max})$ [17] is adopted to compare the transient response of different LDOs by evaluating the tradeoffs between the response time T_r, the quiescent current I_q and the maximum load current $I_{L,\max}$. T_r of the LDO is given by $T_r = (C_L \Delta V_{\rm out})/I_{L,\max}$, where $\Delta V_{\rm out}$ is the maximum transient output-voltage variation (the peak-to-peak output-voltage change due to overshoots, undershoots and load-regulation error during load transient). The smaller the FOM, the better the transient response the LDO achieves. From Table II, the proposed LDO achieves the smallest FOM compared with other reported LDOs. As the proposed LDO is designed for portable applications, the FOM achieved by the proposed LDO is much smaller than other reported LDOs for the same applications [1], [3]–[5] by at least one order of magnitude. It should be noted that the LDO for embedded microprocessor applications [17] dissipates much larger quiescent current in full-load condition, as compared to other LDOs for portable applications. Hence, the current efficiency of the LDO in [17] is much lower. Current efficiency above 99% is critical if the LDO is designed for portable applications as the current efficiency determines the battery lifetime.

V. Conclusion

In this paper, a low-dropout regulator based on the proposed buffer-impedance attenuation (BIA) technique with dynamically-biased shunt feedback has been presented. The BIA technique enables the realization of an intermediate pass-device driving stage with minimal capacitive loading to the preceding error amplifier stage, and minimal output resistance driving the pass device. The parasitic pole at the gate of the pass device can be pushed to sufficiently high frequencies under different load currents, while the LDO only dissipates low quiescent current. In addition to the BIA technique, current-buffer compensation allows the LDO to achieve only a single pole within the unity-gain bandwidth of the regulation loop and a good phase margin with a small compensation capacitor. The LDO is thus stable under the full range of the load current without any requirement for a low-frequency zero. Good transient response of the LDO with small undershoots and overshoots is achieved even if an inexpensive low-value

TABLE II
PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED LDOS

	1998 [1]	2000 [3]	2003 [4]	2004 [5]	2005 [17]	**This Work**
Technology (μm)	2.0	1.0	0.6	0.5	0.09	**0.35**
$V_{\rm do}$ (V)	0.3	N.A.	0.2	N.A.	0.3	**0.2**
$I_{L,\max}$ (mA)	50	200	100	160	100	**200**
I_q (mA)	0.023	0.03	0.038	0.025	6	**0.02**
Current Efficiency at $I_{L,\max}$ (%)	99.5	N.A.	N.A.	N.A.	94.3	**99.8**
$\Delta V_{\rm out}$ (mV)	19	220	130	200	90	**54**
T_r (μs)	1.8	1.1	2	2.75	0.00054	**0.27**
C_L (μF)	4.7	1	10	2.2	0.00060	**1**
ESR Zero Required	No	Yes	Yes	No	No	**No**
FOM (ns)	8.2	0.165	4.9	0.43	0.032	**0.027**

output capacitor is used. The LDO is able to achieve low dropout voltage of 200 mV and deliver 200-mA load current for portable power management applications with lithium-ion batteries. This work is verified on silicon and comparisons with the previous reported work on low-dropout regulators are also presented.

ACKNOWLEDGMENT

The authors would like to thank D. Aksin, M. Martins, and G. Balachandran for their useful input throughout the implementation of this work.

REFERENCES

[1] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[2] G. A. Rincon-Mora and P. E. Allen, "Optimized frequency-shaping circuit toplogies for LDO's," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 6, pp. 703–708, Jun. 1998.

[3] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.

[4] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control-frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[5] C. K. Chava and J. Silva-Martinez, "A frequency compensation scheme for LDO voltage regulators," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 6, pp. 1041–1050, Jun. 2004.

[6] B. Y. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 347–352, Dec. 1974.

[7] C. T. Chuang, "Analysis of the settling behavior of an operational amplifier," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 74–80, Feb. 1982.

[8] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001.

[9] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 629–633, Dec. 1983.

[10] R. Reay and G. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 591–594, May 1995.

[11] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," *IEEE Trans. Circuits Syst. I, Fundam. Theory Applicat.*, vol. 44, no. 3, pp. 257–262, Mar. 1997.

[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, Inc., 2001.

[13] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE J. Solid-State Circuits*, vol. SC-19, no. 12, pp. 919–925, Dec. 1984.

[14] R. Hogervorst, J. P. Tero, and J. H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.

[15] H. Lee, K. N. Leung, and P. K. T. Mok, "Low-voltage analog circuit techniques using bias-current reutilization, self-biasing and signal superposition," in *Proc. IEEE Int. Conf. Electron Devices and Solid-State Circuits*, 2005, pp. 533–536.

[16] M. Al-Shyoukh, R. A. Perez, and H. Lee, "A transient-enhanced 20-μA-quiescent 200 mA-load low-dropout regulator with buffer impedance attenuation," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2006, pp. 615–618.

[17] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, Apr. 2005.

Mohammad Al-Shyoukh received the B.Sc. degree from the electrical and computer engineering Department, Jordan University of Science and Technology, Irbid, Jordan, in 1997, and the M.Sc. degree from the Electrical and Computer Engineering Department, The Ohio State University, Columbus, OH, in 1999. He is currently working toward the Ph.D. degree in electrical engineering at the University of Texas at Dallas.

In 2000, he joined Tezzaron Semiconductor as an analog and mixed-signal IC designer where he worked on memory and stacked memory development, ultra-low-power linear voltage regulators, opamps, and SAR converters. Since late 2002, he has been with Texas Instruments Inc., Dallas, TX, working in the Mixed Signal Automotive and later the Wireless Terminals organizations. He has been involved in the development of wide range of power ICs for automotive and handheld applications. His research interests include linear and power IC design, and ultra-low-power data converters.

Hoi Lee (S'00–M'05) received the B.Eng. (First Class Honors), M.Phil., and Ph.D. degrees in electrical and electronic engineering from the Hong Kong University of Science and Technology, Hong Kong, in 1998, 2000, and 2004, respectively.

In January 2005, he joined the Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX, as an Assistant Professor. His current research interests include power management integrated circuits, integrated systems for cochlear and neural prostheses and low-voltage low-power analog and mixed-signal circuit techniques.

Dr. Lee was the recipient of the Best Student Paper Award at the 2002 IEEE Custom Integrated Circuits Conference. He serves as a member of the Technical Program Committee of IEEE Asian Solid-State Circuits Conference (A-SSCC) and the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society.

Raul Perez (M'06) received the B.S.E.E. degree from the University of Puerto Rico, Mayaguez Campus, and the M.S.E.E. degree from the University of Texas at Dallas in 2000 and 2005, respectively.

In 2000, he joined the Wireless Terminals group at Texas Instruments Inc., Dallas, TX, where he worked on power and linear IC design. His design expertise includes low-dropout regulators (LDOs), low-power, low voltage and low noise analog design, single-ended and fully-differential amplifier architectures, and voltage and current references references in CMOS, BiCMOS and BCD technologies. He developed several products for the major wireless phone vendors, as well as the catalog and consumer electronics markets. In 2006, he moved to Fyrestorm Inc., Sunnyvale, CA, where he is currently Senior Analog and Power IC Designer and team lead. His technical interests include DC/DC converters, Class-D amplifiers and silicon carbide ICs for hybrid electric vehicle applications. He currently holds four U.S. patents with three more pending, all in linear and power IC design.