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# A Tree-Based Architecture for High-Performance Ultra-Low-Voltage Amplifiers

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**Abstract:** In this paper, we introduce a novel tree-based architecture which allows the implementation of Ultra-Low-Voltage (ULV) amplifiers. The architecture exploits a body-driven input stage to guarantee a rail-to-rail input common mode range and body-diode loading to avoid Miller compensation, thanks to the absence of high-impedance internal nodes. The tree-based structure improves the CMRR of the proposed amplifier with respect to the conventional OTA architectures and allows achievement of a reasonable CMRR even at supply voltages as low as 0.3 V and without tail current generators which cannot be used in ULV circuits. The bias currents and the static output voltages of all the stages implementing the architecture are accurately set through the gate terminals of biasing transistors in order to guarantee good robustness against PVT variations. The proposed architecture and the implementing stages are investigated from an analytical point of view and design equations for the main performance metrics are presented to provide insight into circuit behavior. A 0.3 V supply voltage, subthreshold, ultra-low-power (ULP) OTA, based on the proposed tree-based architecture, was designed in a commercial 130 nm CMOS process. Simulation results show a dc gain higher than 52 dB with a gain-bandwidth product of about 35 kHz and reasonable values of CMRR and PSRR, even at such low supply voltages and considering mismatches. The power consumption is as low as 21.89 nW and state-of-the-art small-signal and large-signal FoMs are achieved. Extensive parametric and Monte Carlo simulations show the robustness of the proposed circuit to PVT variations and mismatch. These results confirm that the proposed OTA is a good candidate to implement ULV, ULP, high performance analog building blocks for directly harvested IoT nodes.

**Keywords:** body-driven; ultra-low-voltage; ultra-low-power; operational transconductance amplifier; IoT



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## 1. Introduction

The continuous evolution of electronic systems and the ever increasing symbiotic relationship between humans and electronic devices characterize the era of Internet of Things (IoT) [1,2]. Smart and portable devices, such as laptops, smartphones, smartwatches, fit-trackers and so on, are used more and more often for checking emails, banking management, counter services and the like. Indeed, most of these electronic apparatuses have changed the way we work, study or play.

This IoT revolution has also driven the development of body area networks [3], which exploit implantable and wearable devices, and are widely used in healthcare monitoring and in the study of neurodegenerative diseases such as Parkinson's, Alzheimer's and so on [4–7].

The growing popularity of these electronic devices is also due to their increasing capability to work with low power consumption and low supply voltage in order to maximize battery life or employ energy harvesting techniques.

The stringent requirements in terms of ultra-low-power (ULP) and ultra-low-voltage (ULV) operation set by the above applications have brought about a revolution also in

the approach to the design of analog integrated circuits (ICs). In fact, the latter have to be reinvented to enhance the autonomy of smart devices and find a balance between performance, area footprint and power consumption at supply voltages of a few hundreds of millivolts. As such, analog interfaces are among the most challenging building blocks for IoT applications [1,8–11].

The Operational Transconductance Amplifier (OTA) stands out, among the analog building blocks, for its design complexity, especially if ULP and ULV operation are key requirements. In the last few years, there has been a growing trend in the design of ULP OTAs and a plenty of solutions have been proposed in the literature [12–14]. Most of the low voltage OTAs reported in the last decade operate with supply voltages ranging from 0.5 V to about 1 V, and are based on the conventional cascode, folded cascode, multi-stage or gain-boosting approaches, which have been successfully exploited in the past to implement high-performance amplifiers for several application scenarios [15–19]. A novel OTA architecture based on current gain stages to improve bandwidth and slew rate has been recently proposed in [20]. The OTA reported in [20] operates with a supply voltage of 1 V and exhibits state of the art small-signal and large-signal figures of merit. Unfortunately, most of these conventional amplifier topologies are not suited for applications requiring supply voltages lower than 0.5 V, and inverter-based [21–26] and pseudo-differential [27,28] architectures are preferred. However, an aggressive supply voltage scaling severely limits the swing of the control voltage, thus strongly limiting the effectiveness of body bias approaches to set the bias or the common mode current. Therefore, gate-driven amplifiers operating at supply voltages lower than 0.5 V are not able to guarantee either rail-to-rail input common mode range (ICMR) or well-defined bias currents.

The bulk-driven technique [29–31] allows rail-to-rail ICMR in ULV amplifiers at the cost of reduced gain and a resistive input impedance component. Bulk-driven amplifiers are surely one of the best alternatives to attain rail-to-rail input–output swing when a well-defined bias or common mode current is required to increase the robustness against process, supply voltage, and temperature (PVT) variations [32–42]. Indeed, the signal-free gate terminals can be used to accurately set the bias current of the different OTA stages. The bulk-driven technique combined with inverter-based topologies has also been exploited in recent papers to design ULV amplifiers [33,36,39].

A completely novel approach based on fully digital operation to the design of analog differential circuits has been introduced in [43]. Several papers dealing with the fully digital implementation of OTAs for IoT applications have been recently published [44–46]. The digital OTAs in [44,45] are based on the C-Muller element and do not require any passive component. Such digital OTAs are able to operate at supply voltages lower than 0.3 V and are very interesting from the viewpoint of the area footprint and power consumption. However, the operation of this kind of circuits can be sensitive to PVT variations and mismatch and may require suitable calibration strategies to achieve high production yield [47].

Indeed, even if bulk-driven OTAs exhibit some drawbacks with respect to gate-driven ones (higher noise, larger area and lower bandwidth) and to digital OTAs (larger area and power consumption), they can be designed to be robust against PVT and mismatch variations and still represent the best solution to attain rail-to-rail ICMR at supply voltages of the order of 0.3 V.

In this work, we present a novel OTA architecture based on a tree-like structure. This can be viewed as the ULV implementation of the OTA reported in [20], previously proposed by the authors to enhance the bandwidth efficiency. The current gains obtained by means of conventional current mirrors in [20] are not feasible in ULV conditions and have to be implemented by means of other solutions such as the one presented in [48]. In the ULV architeture proposed in this paper, the current gains are implemented by using a different approach which is based on the body-to-gate (B2G) interfaces as will be detailed in the following. The proposed architecture exploits a body-driven input stage to guarantee a rail-to-rail input common mode range and body-diode loading to avoid Miller compensation, thanks to the absence of high-impedance internal nodes. The bias currents and the static

output voltages of all the stages implementing the proposed architecture are accurately set through the gate terminals of biasing transistors in order to guarantee a good robustness against PVT variations. However, this biasing strategy results in pseudo-differential stages and therefore has a negative impact on CMRR performance. The proposed tree-like structure improves the CMRR of the OTA with respect to conventional pseudo-differential amplifiers and allows achievement of a reasonable CMRR even in ULV conditions. A 0.3 V supply voltage ULP OTA based on this architecture was designed in a 130 nm CMOS process, and simulation results show state of the art small-signal and large-signal figures of merit (FoMs).

The paper is organized as follows: Section 2 introduces the proposed OTA architecture. Circuit analysis is reported in Section 3. Section 4 deals with design and simulation results and conclusions are drawn in Section 5.

## 2. Proposed Topology

The block scheme of the proposed OTA architecture is depicted in Figure 1. This architecture of ULV OTA was derived from the OTA introduced by the authors in [20] and is a three stage, tree-like OTA, made up of the cascade of differential-to-single-ended converter stages, to maximize CMRR. Three different topologies are exploited in the three stages of the OTA to optimize the tradeoff between performance and efficiency. Each one of these stages was extensively investigated and their behavior is discussed in the next subsections. It has to be remarked that the proposed ULV OTA makes extensive use of the body terminals of MOS devices and thus it can be implemented only in CMOS technologies (such as triple-well-bulk or FDSOI), where both NMOS and PMOS transistors have available body connections. However, this is not a strong limitation, since most modern processes have available body connections for both PMOS and NMOS transistors.

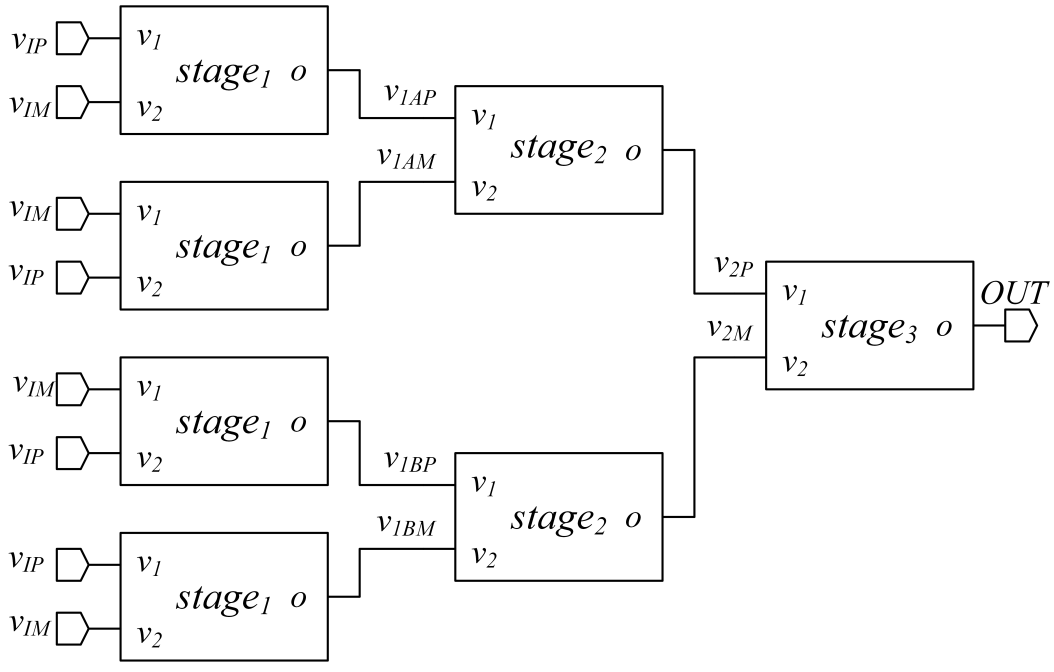


**Figure 1.** Proposed tree-like architecture of the OTA.

### 2.1. $Stage_1$

The topology of the blocks denoted as $stage_1$ in Figure 1 is reported in Figure 2, and is made up of transistors $M_{1A}$, $M_{1B}$ and $M_{2A}$, $M_{2B}$. This input stage has the same topology adopted for the OTA in [40]. It is a bulk-driven stage in which the bias current is accurately set through the $V_{GN}$ voltage applied to the gate of transistor $M_{2A}$. The bias voltage $V_{GN}$ is generated by the biasing circuit reported in Figure 3. The current flowing in $M_{2A}$ is mirrored through $M_{1A}$ and $M_{1B}$, so that the standby current of all MOS devices is accurately

set. The body terminals of transistors $M_{1A}$ and $M_{1B}$ are connected to the input voltages, $V_{IP}$ and $V_{IM}$, respectively. The output of stage $_1$ is loaded through a body–diode connection on the transistor $M_{2B}$ whose gate voltage is connected to the bias voltage $V_{GN}$, and results in an output impedance lower than the one of conventional input stages. This stage thus provides limited gain, but allows achievement of a rail-to-rail input common mode range and improvement of the bandwidth. As a consequence, noise and mismatch of the second stage contributes to the total input referred noise and offset. However, even if noise and offset performance are suboptimal, the OTA can still be designed to exhibit acceptable noise and offset, while achieving very good bandwidth efficiency.

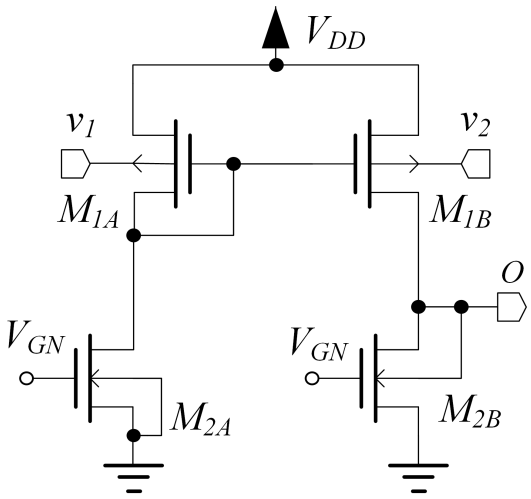


**Figure 2.** Stage $_1$ used in the proposed OTA architecture.

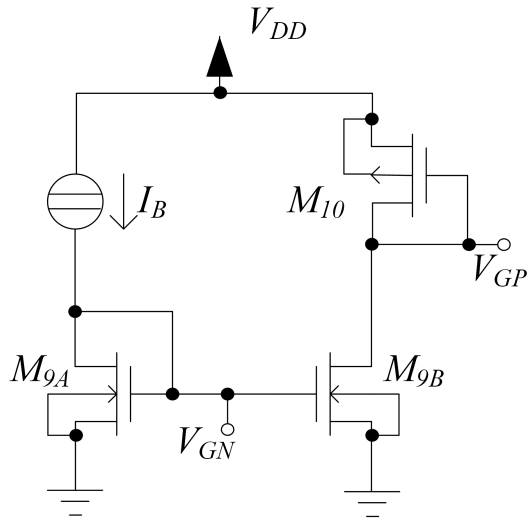


**Figure 3.** Biasing circuit used in the proposed OTA architecture.

### 2.2. $Stage_2$

The topology of stage$_2$ is shown in Figure 4. This stage converts the input differential signal to single-ended providing some gain, a well defined bias point and contributing to the overall CMRR. The input signal is applied to the gates of $M_{4A}$ and $M_{4B}$, and the bias current is set through the gates of $M_{3A}$ and $M_{3B}$ connected to the bias voltage $V_{GP}$ generated by the circuit in Figure 3. The current cancellation given by the body-to-body (B2B) current mirror (Appendix B) $M_{4A}$, $M_{4B}$ allows to attain good common mode rejection ratio as will be better shown in the next sections. Since the output is body-loaded, also this stage doesn't show any high-impedance internal node and thus does not require any internal compensation.

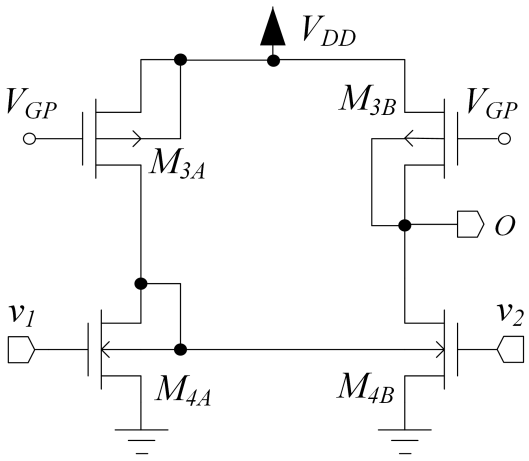


**Figure 4.** Stage$_2$ used in the proposed OTA architecture.

### 2.3. Stage$_3$

The topology of stage$_3$ is shown in Figure 5. This stage combines the signal behavior of an inverter-based pseudo-differential pair (Arbel topology) with differential-to-single-ended conversion through the body current mirror and robust biasing, and is composed by an n-input and a p-input stage similar to that of Figure 4, but without diode loading, connected together. The signal is applied to the gates of two PMOS and two NMOS devices, respectively $M_{6A}, M_{6B}$ and $M_{8A}, M_{8B}$, and the body-diode connections in $M_{6A}$ and $M_{7B}$ implement body-driven current mirrors performing differential-to-single-ended conversion and common mode current cancellation. Transistors $M_{5A}$, $M_{5B}$ and $M_{7A}$ and $M_{7B}$ act as current sources and are exploited to set the bias current in all the branches of the third stage through $V_{GP}$ and $V_{GN}$, respectively; thus, each transistor has a well-defined bias point.

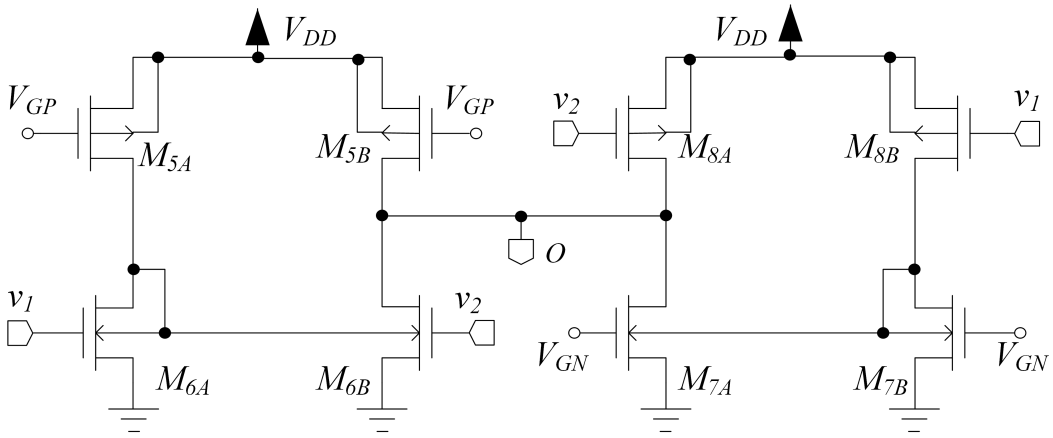


**Figure 5.** Stage$_3$ used in the proposed OTA architecture.

### 2.4. Architectural Considerations

It has to be noted that, referring to the proposed architecture, at the interfaces between stage$_1$ and stage$_2$ and between stage$_2$ and stage$_3$, we have a body-to-gate (B2G) connection. These B2G connections result in lower voltage gain with respect to the conventional drain-to-gate connections, but the lower gain allows avoidance of high-impedance internal nodes, and therefore compensation capacitors. In fact, even if each B2G interface generates a pole (as shown in Appendix A), it is placed at a much higher frequency than the one given by the output stage, which provides the dominant pole.

## 3. Circuit Analysis

In this section, the small-signal and large-signal performances of the proposed architecture are analyzed from an analytical point of view, and design equations for the

main performance parameters, such as gain, frequency response, slew-rate and noise, are presented to provide insight into circuit behavior.

### 3.1. Differential Gain

Referring to the small-signal equivalent circuits of stage$_1$, stage$_2$ and stage$_3$, the differential mode gain of the different stages was computed. Using the standard notation for small-signal parameters of MOS devices, the differential gain of the first stage can be expressed as:

$$A_{vd_1} = \frac{g_{mb_1}}{g_{mb_2}} \frac{1 + s\frac{\tau_1}{2}}{(1 + s\tau_1)(1 + s\tau_2)} \tag{1}$$

where:

$$\begin{aligned} \tau_1 &\approx \frac{2C_{gs_1} + C_{gd_1}(1 + \frac{g_{m_1}}{g_{mb_2}}) + C_{gd_2}}{g_{m_1}} \\ \tau_2 &\approx \frac{C_{gs_4} + C_{gd_4}(1 + \frac{g_{m_4}}{g_{mb_3}}) + C_{gd_2} + C_{gd_1} + C_{bs_2}}{g_{mb_2}} \end{aligned} \tag{2}$$

According to usual approximations, the pole-zero doublet in Equation (1) can be neglected.

Thereafter, the differential gain of stage$_2$ can be derived to be:

$$A_{vd_2} = \frac{g_{m_4}}{g_{mb_3}} \frac{1 + s\frac{\tau_3}{2}}{(1 + s\tau_3)(1 + s\tau_4)} \tag{3}$$

where:

$$\begin{aligned} \tau_3 &\approx \frac{2C_{bs_4} + C_{gd_3} + C_{gd_4}}{g_{mb_4}} \\ \tau_4 &\approx \frac{C_{gs_6} + C_{gs_8} + C_{gd_3} + C_{gd_4} + C_{bs_3} + \frac{g_{m_8}}{g_{out}} C_{gd_8} + \frac{g_{m_6}}{g_{out}} C_{gd_6}}{g_{mb_3}} \end{aligned} \tag{4}$$

Moreover, in this case, the pole-zero doublet in Equation (3) can be neglected.

Finally, the stage$_3$ differential gain can be computed by neglecting the pole-zero doublets given by body–diode connections of $M_{6_{A,B}}$ and $M_{7_{A,B}}$; hence, it can be expressed as:

$$A_{vd_3} = \frac{g_{m_8} + g_{m_6}}{g_{out}} \frac{1}{1 + s\frac{C_L}{g_{out}}} \tag{5}$$

where it is denoted with:

$$g_{out} = 2(g_{ds_8} + g_{ds_6}) \tag{6}$$

considering that $M_5 = M_8$ and $M_6 = M_7$.

The overall gain of the amplifier can then be expressed as:

$$A_{vd_{tot}}(s) = 4 \prod_{i=1}^{3} A_{vd_i}(s) \tag{7}$$

and rewritten as:

$$A_{vd_{tot}}(s) = 4 \cdot \frac{g_{m_8} + g_{m_6}}{g_{out}} \cdot \frac{g_{mb_1}}{g_{mb_2}} \cdot \frac{g_{m_4}}{g_{mb_3}} \cdot \frac{1}{\left(1 + s\frac{C_L}{g_{out}}\right)} \cdot \frac{1}{(1 + s\tau_2)(1 + s\tau_4)} \tag{8}$$

It is evident from Equation (8) that the output capacitance sets the dominant pole since the poles of stage$_1$ and stage$_2$ are at higher frequencies due to the body–diode connected loads and the smaller load capacitances.

Starting from the above results, the gain-bandwidth product (GBW) of the proposed OTA can be computed as:

$$\text{GBW} = \frac{g_\alpha}{2\pi \cdot C_L} \tag{9}$$

where:

$$g_\alpha = (g_{m_8} + g_{m_6}) \cdot \frac{g_{mb_1}}{g_{mb_2}} \cdot \frac{g_{m_4}}{g_{mb_3}} \tag{10}$$

The phase margin of the whole OTA can then be expressed as:

$$\varphi_m = \frac{\pi}{2} - \arctan\left(\frac{g_\alpha}{C_L} \cdot \tau_2\right) - \arctan\left(\frac{g_\alpha}{C_L} \cdot \tau_4\right) \tag{11}$$

According to Equation (11), the proposed OTA requires a minimum value of $C_L$ for stability. However, Equation (11) shows also that the desired phase margin can be set by properly designing MOS devices' size for a given load capacitor; a higher $C_L$ results in a smaller GBW and a larger phase margin.

### 3.2. Common Mode Gain

The common mode gain of stage$_1$ was found to be:

$$A_{vc_1} = -\frac{g_{mb_1}(g_{ds_1} + g_{ds_2})}{g_{mb_2} g_{m_1}} \frac{1 + s\tau_{z_1}}{(1 + s\tau_{p_{1,1}})(1 + s\tau_{p_{2,1}})} \tag{12}$$

where:

$$\tau_{z_1} = \tau_1 \frac{g_{m_1}}{g_{ds_1} + g_{ds_2}} \quad \tau_{p_{1,1}} = \tau_1 \quad \tau_{p_{2,1}} = \tau_2 \tag{13}$$

therefore, the CMRR of stage$_1$ can be expressed as:

$$\text{CMRR}_1 = \frac{g_{m_1}}{g_{ds_1} + g_{ds_2}} \tag{14}$$

The common mode gain of stage$_2$ is:

$$A_{vc_2} = -\frac{g_{m_4}}{g_{mb_4}} \frac{g_{ds_3} + g_{ds_4}}{g_{mb_3}} \frac{1 + s\tau_{z_2}}{(1 + s\tau_{p_{1,2}})(1 + s\tau_{p_{2,2}})} \tag{15}$$

where:

$$\tau_{z_2} = \tau_3 \frac{g_{mb_4}}{g_{ds_3} + g_{ds_4}} \quad \tau_{p_{1,2}} = \tau_3 \quad \tau_{p_{2,2}} = \tau_4 \tag{16}$$

whereas its CMRR amounts to:

$$\text{CMRR}_2 = \frac{g_{mb_4}}{g_{ds_4} + g_{ds_3}} \tag{17}$$

Stage$_3$ shows a common mode gain of:

$$A_{vc_3} = \frac{g_{m_8} + g_{m_6}}{2 g_{mb_6}} \frac{1 + s\tau_{z_3}}{(1 + s\tau_{p_{1,3}})(1 + s\tau_{p_{2,3}})} \tag{18}$$

where:

$$\tau_{z_3} = \frac{2C_{bs_6} + C_{gd_8} + C_{gd_6}}{g_{mb_6}} \quad \tau_{p_{1,3}} = 2\frac{2C_{bs_6} + C_{gd_8} + C_{gd_6}}{g_{ds_8} + g_{ds_6}} \quad \tau_{p_{2,3}} = \frac{C_L}{g_{ds_8} + g_{ds_6}} \tag{19}$$

and its CMRR results:

$$\text{CMRR}_3 = \frac{g_{mb_6}}{g_{ds_8} + g_{ds_6}} \tag{20}$$

Due to the body current mirror, the CMRR of these stages is reduced with respect to stage$_1$. Combining the above results, the common mode gain of the proposed tree-like architecture can be derived as:

$$A_{vc_{TOT}} = \prod_{i=1}^{3} A_{vc_i} \tag{21}$$

Finally, the CMRR of the overall OTA can be expressed as:

$$\mathrm{CMRR}_{tot} = 4 \prod_{i=1}^{3} \mathrm{CMRR}_i \tag{22}$$

therefore, the total CMRR is about:

$$\mathrm{CMRR}_{tot} = 4 \cdot \frac{g_{m_1}}{g_{ds_1} + g_{ds_2}} \cdot \frac{g_{mb_4}}{g_{ds_4} + g_{ds_3}} \cdot \frac{g_{mb_6}}{g_{ds_8} + g_{ds_6}} \tag{23}$$

By looking at Equation (22), it is evident that the CMRR in typical conditions is high, due both to the cascade of several stages and to the scaling factor of the tree architecture, and that it can be enhanced by further iterating the tree-like structure of the proposed OTA architecture. However, in ULV conditions, PVT variations and mismatch may impact on the stability of the operating point, especially in the presence of a B2G interface, and significantly degrade the CMRR$_{i\text{-th}}$ of the OTA. As a consequence, the CMRR of this architecture is more sensitive to PVT variations and mismatch than other architectures which adopt higher supply voltages and/or a more stable operating point. Anyway, to cope with this problem, design centering techniques are exploited in this work in order to increase the overall CMRR in a given range of PVT and mismatch conditions achieving a reasonable robustness. The above reported frequency analysis shows that the common mode gain presents some zeros that could appear before the unity-gain frequency (depending on the $C_L/C_{gs}$ ratio), thus reducing the CMRR at high frequency. A large load capacitance is usually required to achieve stability, therefore the resulting CMRR reduction is often limited.

### *3.3. Large-Signal Performances*

The large-signal performance of the proposed OTA has been investigated by assuming that the load capacitance $C_L$ is much larger than the other circuit capacitances. The slew-rate is thus determined by the output stage, and it can be assumed that the output voltage $v_{O2}$ of stage$_2$, which drives stage$_3$, is a rail-to-rail signal.

With reference to Figure 5, the output current is given by $I_o = I_{5B} + I_{8A} - I_{6B} - I_{7A}$; positive and negative slew-rates are given by $SR_p = I_{o_{max}}/C_L$ and $SR_m = I_{o_{min}}/C_L$, where $I_{o_{max}}$ and $I_{o_{min}}$ are the maximum positive and negative values of $I_o$.

For the current, we use the standard relationship for sub-threshold current:

$$I_{n,p} = I_{0_{n,p}}\, e^{\frac{V_{ov} - |V_{th_{n,p}}|}{n_{n,p} U_t}} \tag{24}$$

where $U_t = kT/q$ is the thermal voltage and $|V_{th_{n,p}}| = V_{th_{n,p_0}} - \alpha_{n,p}|V_{bs}|$.

For the positive slew-rate, we have $v_1 = V_{DD}$ and $v_2 = 0$, and we can assume that the body voltages of $M_{6_B}$ and $M_{7_A}$ are approximately 0. By denoting with $I_{ref}$, the quiescent current of the devices of stage$_3$, we obtain:

$$I_{o_{max}} = I_{ref}\left[1 + e^{\frac{\alpha_n |\Delta V_{BH}|}{n_n U_t}} + e^{\frac{\Delta |V_{GH}|}{n_p U_t}}\right] \tag{25}$$

where: $\Delta V_{BH} = -V_{B0}$, $\Delta V_{GH} = V_{DD} - V_{GP}$ with $V_{B0}$ and $V_{GP}$ the quiescent voltage at body and gate terminals of the NMOS and PMOS devices.

For the negative slew-rate, we have $v_1 = 0$, $v_2 = V_{DD}$ and in this case we derive:

$$I_{o_{min}} = I_{ref}\left[1 - e^{\frac{\alpha_n|\Delta V_{BL}|}{n_n U_t}}\left(1 + e^{\frac{|\Delta V_{GL}|}{n_n U_t}}\right)\right] \tag{26}$$

where: $\Delta V_{BL} = V_{DD} - V_{B0}$ and $\Delta V_{GL} = V_{DD} - V_{GN}$ with $V_{GN}$ as the quiescent voltage at gate terminals of NMOS devices. In this case, we assume that the body terminals of $M_{6_B}$ and $M_{7_A}$ are approximately $V_{DD}$. Equations (25) and (26) show that, in general, positive and negative slew-rates give different results.

### 3.4. Noise Analysis

The noise analysis has been carried out assuming that each transistor can be modelled with only one noise current generator, which includes both thermal and flicker noise. The power spectral density of the modelled current generator can be expressed as follows:

$$S_{n_i} = \overline{i_{i_w}^2} + \overline{i_{i_f}^2} \tag{27}$$

where:

$$\overline{i_{n(p)_w}^2} = 4kTn_{n(p)}\gamma g_{m_i} = 2qI_d \tag{28}$$

$$\overline{i_{n(p)_f}^2} = \frac{K_{n(p)}}{fC_{ox}}\frac{g_m^2}{WL} \tag{29}$$

Taking into account that the noise sources due to stage$_3$ can be neglected due to the high gain of the preceding stages (considering also the contribution of the tree structure), the equivalent input noise mainly results from the first two stages and can be expressed as follows:

$$S_{v_{eq}} = \frac{S_{n_1} + S_{n_2}}{2\, g_{mb_1}^2} + \frac{1}{4\, g_{m_4}^2} \cdot \frac{g_{mb_2}^2}{g_{mb_1}^2}(S_{n_3} + S_{n_4}) \tag{30}$$

As it can be observed from Equation (30), the noise performance of the amplifier is worsened by body driving, which shows a transconductance gain (i.e., $g_{mb}$) which is $n$-times lower than $g_m$. Consequently, in order to reduce the equivalent input noise, larger transistors are required. The result in Equation (30) can be written in a less concise form as:

$$S_{v_{eq}} \approx \frac{1}{16}(4S_{no1} + \frac{2S_{no2}}{A_V^2}) \tag{31}$$

where

$$S_{no1} = \frac{2}{g_{mb_1}^2}(S_{n_1} + S_{n_2}) \tag{32}$$

and

$$S_{no2} = \frac{2}{g_{m_4}^2}(S_{n_3} + S_{n_4}) \tag{33}$$

are the input-referred noise spectra for the first and second stage (contribution of the single cell). Factor 16 in the denominator of (31) accounts for the $2^{(N-1)}$ gain contribution of a N-level tree architecture, whereas the factors 4 and 2 in the numerator consider how many identical cells are present.

## 4. Amplifier Design and Simulation Results

The proposed OTA has been designed and simulated in a 130 nm CMOS process from STMicroelectronics. Small-signal and large-signal figures of merit (FoMs) were used to compare it against recently published OTAs with supply voltages lower than 0.5 V. Extensive parametric and Monte Carlo simulations were carried out in order to assess the robustness of the amplifier to PVT variations and mismatch referring to both open-loop and closed-loop simulation test benches.

### 4.1. Sizing

The transistors in the stages implementing the architecture in Figure 1 were sized as reported in Table 1. The bias voltages $V_{GN}$ and $V_{GP}$ in Figures 2, 4 and 5, are generated by the biasing circuit shown in Figure 3. Moreover, the sizing of the NMOS transistors $M_{9A}$ and $M_{9B}$ and of the PMOS transistor ($M_{10}$) of the biasing circuit are reported in Table 1. The voltages $V_{GN}$ and $V_{GP}$ propagate the bias current, $I_B = 4$ nA, through body-mirroring or gate-mirroring.

**Table 1.** Transistors' sizing.

| Transistor | Stage | Width [µm] | Length [µm] | $I_{bias}$ [nA] |
|---|---|---|---|---|
| $M_{1A}$, $M_{1B}$ | 1 | 4.465 | 1.000 | 4 |
| $M_{2A}$, $M_{2B}$, $M_{9A}$, $M_{9B}$ | 1 | 0.375 | 3.000 | 4 |
| $M_{3A}$, $M_{3B}$, $M_{10}$ | 2 | 4.465 | 1.000 | 4 |
| $M_{4A}$, $M_{4B}$ | 2 | 0.375 | 3.000 | 4 |
| $M_{5A}$, $M_{5B}$, $M_{8A}$, $M_{8B}$ | 3 | 13.390 | 1.000 | 19.67 |
| $M_{6A}$, $M_{6B}$, $M_{7A}$, $M_{7B}$ | 3 | 1.125 | 3.000 | 19.67 |

### 4.2. Circuit Simulations

The proposed OTA was simulated within the Cadence Virtuoso environment assuming a supply voltage of 0.3 V and an output load capacitance of 50 pF.

Referring to the open-loop simulation test bench the differential gain (magnitude and phase) was evaluated as reported in Figure 6. As can be observed from the figure, the phase margin is about 52.40°, whereas the gain-bandwidth product is about 35.16 kHz. Figure 6 also shows the common mode gain in typical conditions.

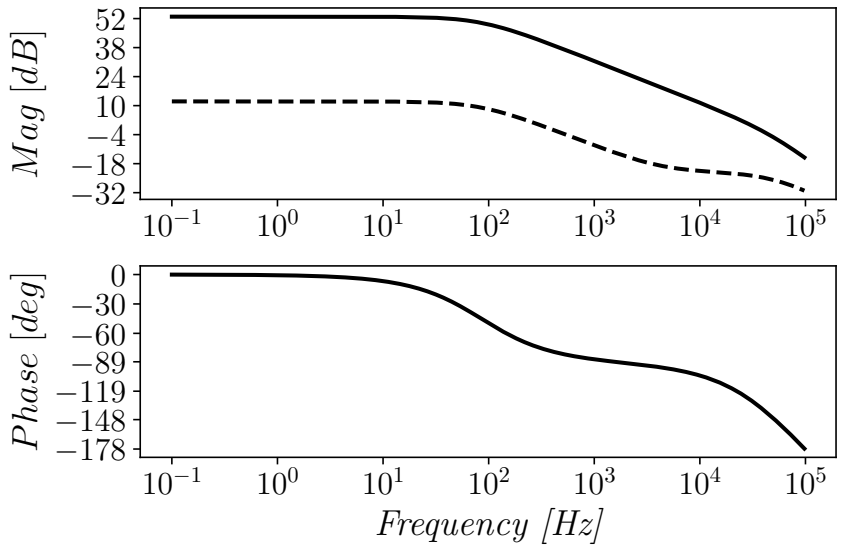


**Figure 6.** Differential (solid) and common mode (dashed) gain of the proposed OTA.

Figure 7 confirms that the bias currents of all the three stages of the OTA are accurately set and are also very stable for an input signal amplitude going rail-to-rail in closed-loop unity-gain configuration.

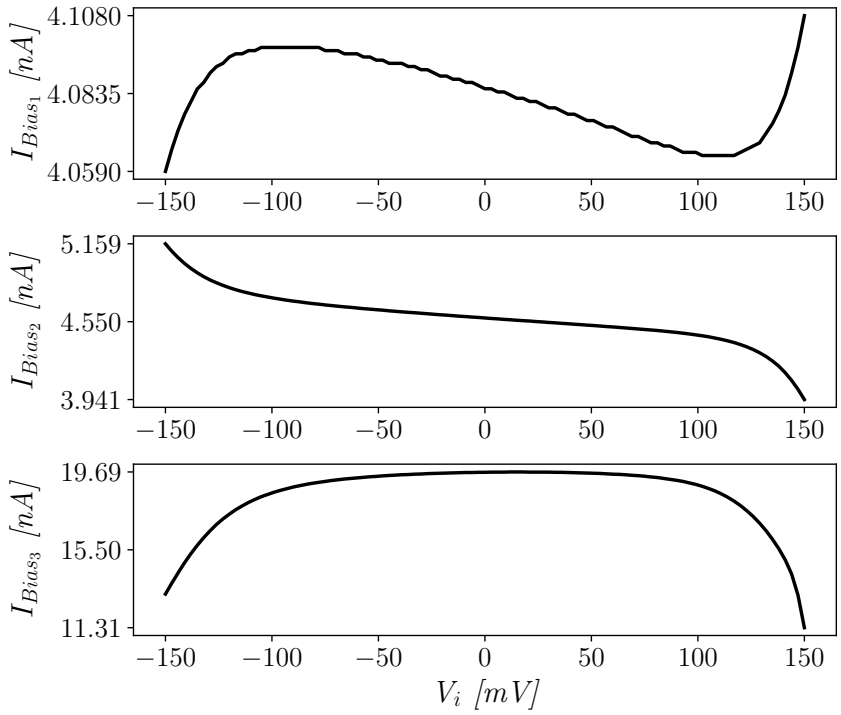


**Figure 7.** Biasing currents of the three stages vs. input common mode level.

The amplifier was then tested in unity-gain configuration and its transfer characteristic is reported in Figure 8, highlighting the rail-to-rail capabilities of the OTA.

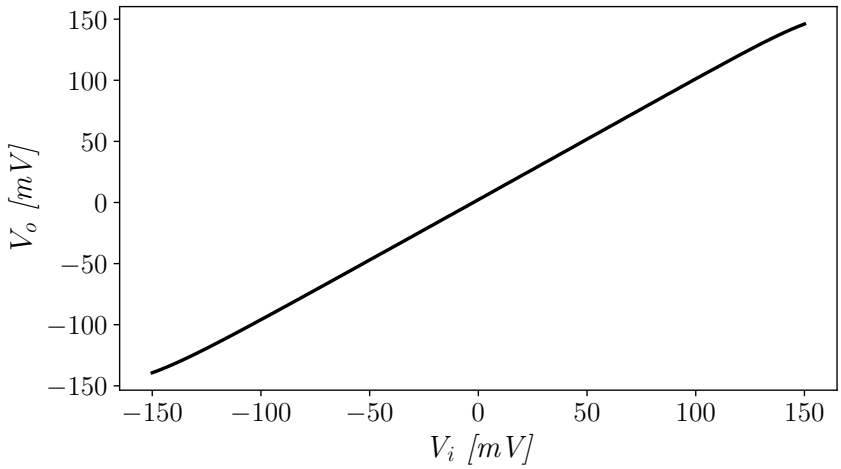


**Figure 8.** Unity-gain amplifier transcharacteristic.

Sinusoidal waves at different amplitudes and with a frequency of 200 Hz were used to excite the unity-gain amplifier and evaluate distortions. The OTA exhibits very good total harmonic distortion (THD), also with an input signal swing equal to the supply voltage (as depicted in Figure 9). As can be observed from Figure 9, when a 90% signal swing is considered, the THD is about 0.673%, whereas when a full-swing signal is used the THD is still good and equal to about 1.38%. Furthermore, to assess the slew-rate (SR) performance of the amplifier, a full range square wave was used, and results are shown in Figure 10. The amplifier shows positive and negative slew-rate ($SR_p$ and $SR_n$) equal to 18.61 and 11.51 V/ms, respectively. Though not symmetrical, the worst-case slew-rate is not much worse than the best one, hence large-signal performance is good on both signal edges.

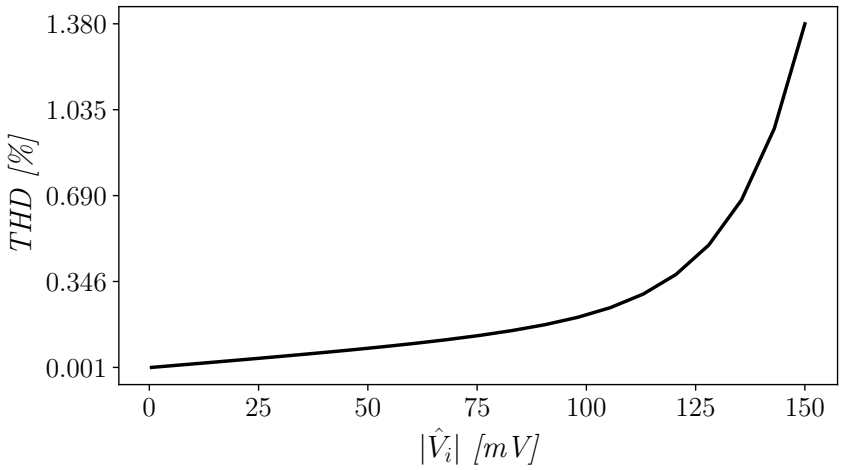


**Figure 9.** THD vs. amplitude of the input signal in unity-gain configuration.

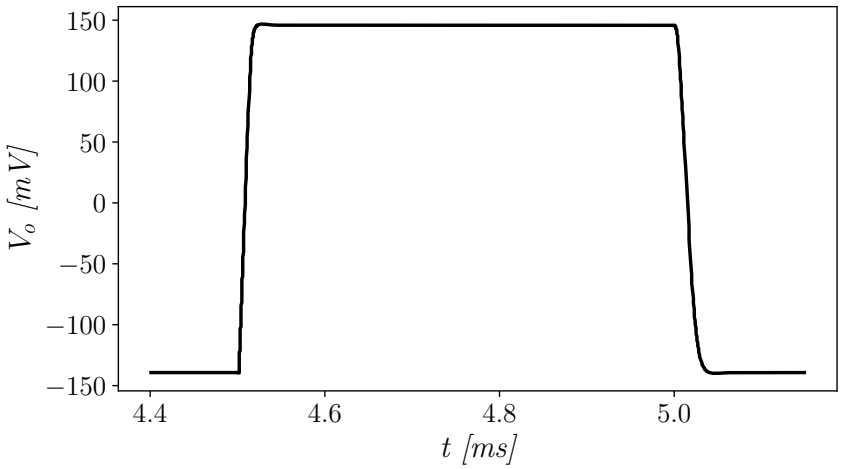


**Figure 10.** Response to square input wave.

The input-referred noise spectrum of the proposed OTA is reported in Figure 11 and shows a value of about 1.60 $\mu V/\sqrt{Hz}$ at 1 kHz.

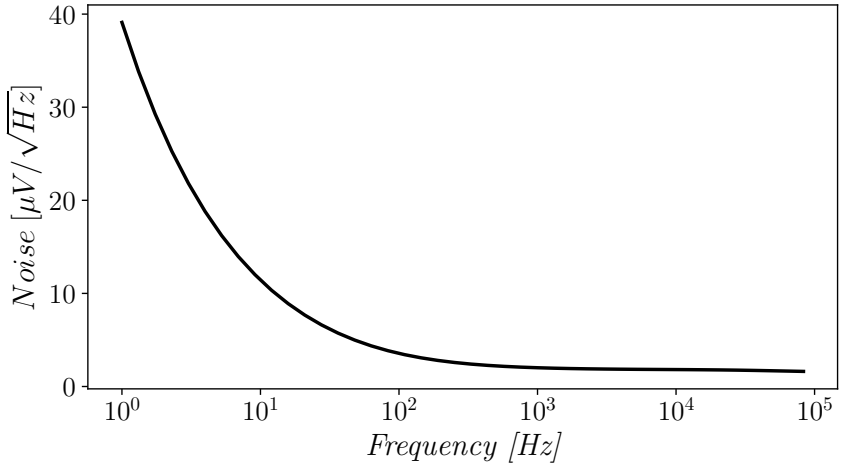


**Figure 11.** Input-referred noise of the proposed OTA.

### *4.3. Robustness to Mismatch and PVT Variations*

The OTA was then extensively tested by means of parametric and Monte Carlo simulations to demonstrate its robustness to PVT and mismatch variations. Table 2 reports

the results of 200 Monte Carlo iterations. Power dissipation ($P_D$) has a standard deviation lower than the 10% of the mean value. Large-signal performance (i.e., $SR_p$ and $SR_m$) is close to the nominal value, whereas the attained mean value of the phase margin $m_\varphi$ is about 53°. The standard deviation of the offset is relatively large, confirming the suboptimal performance in terms of noise and offset of the proposed OTA. Its value is however similar to other ULV OTAs reported in the literature.

**Table 2.** Performance under mismatch variations.

| | **Mean** | **StdDev** | **Min** | **Max** |
|---|---|---|---|---|
| $P_D$ (nW) | 20.85 | 1.44 | 16.6 | 24.34 |
| Idiss (nA) | 69.50 | 4.80 | 55.33 | 81.13 |
| Offset (mV) | 3.84 | 15.46 | −30 | 50 |
| $SR_p$ (V/ms) | 18.54 | 0.30 | 17.84 | 19.42 |
| $SR_m$ (V/ms) | 11.63 | 0.34 | 10.82 | 12.52 |
| Gain (1 Hz) (dB) | 51.48 | 1.22 | 49.59 | 56.49 |
| CMRR (dB) | 42.11 | 10.44 | 27.84 | 98.85 |
| PSRR (dB) | 56.13 | 2.12 | 48.05 | 56.39 |
| Mphi (deg) | 53.08 | 6.27 | 38.25 | 74.98 |
| GBW (kHz) | 32.72 | 8.42 | 11.54 | 49.33 |
| THD (%) | 0.74 | 0.57 | 0.51 | 2.61 |

Figure 12 reports the histogram of the CMRR that clearly shows a log-normal distribution, probably due to the sub-threshold operating condition of the circuit. The architecture exhibits a CMRR up to 98dB for some iterations (as expected from theoretical results in Section 3.2), and remains relatively high under mismatch variations, with a mean value of about 42 dB.

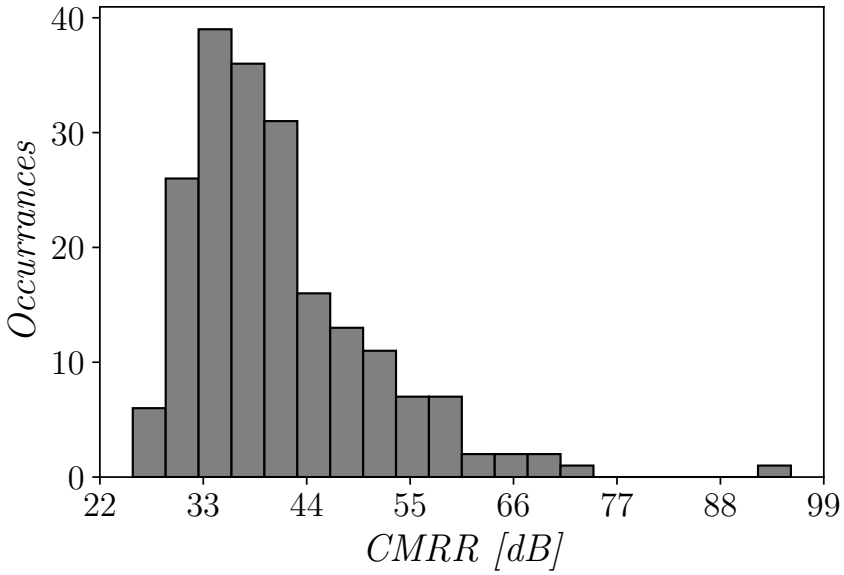


**Figure 12.** Histogram of the common mode rejection ratio (CMRR) of the proposed OTA for 200 Monte Carlo mismatch iterations.

The power supply rejection ratio (PSRR) of the proposed OTA is also quite good despite the very low supply voltage. Figure 13 reports the histogram of the PSRR, that shows a mean value of about 56.13 dB with a limited variation under mismatch.

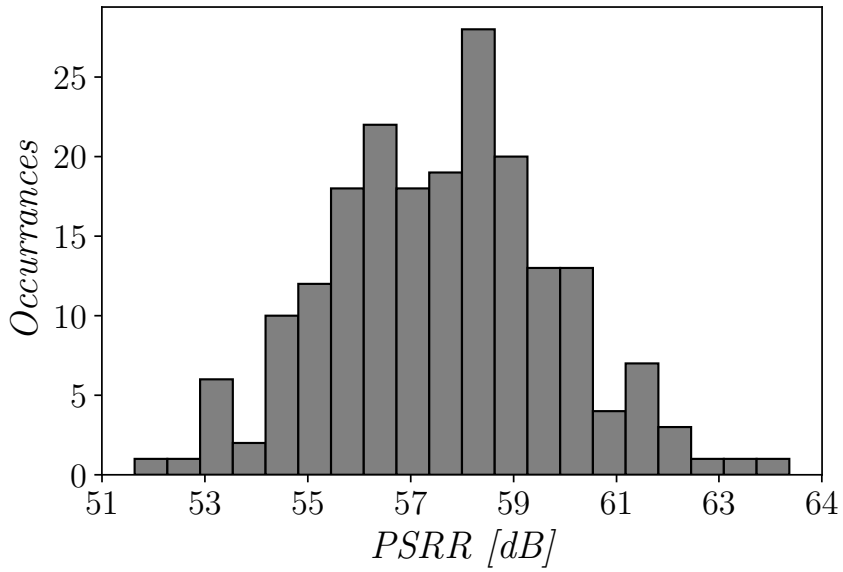


**Figure 13.** Histogram of the power supply rejection ratio (PSRR) of the proposed OTA for 200 Monte Carlo mismatch iterations.

The performance under PVT variations was investigated taking into account a ±10% supply voltage variation and a [0, 70] °C temperature range. In Table 3, the performance under temperature variations is summarized. Total power consumption, the gain-bandwidth product as well as noise and total harmonic distortion are adequately stable across the considered temperature range. However, it is evident from Table 3 that the differential gain and CMRR degrade at high temperatures; this is probably due to variations in the bias point of $stage_2$ and in particular in transistors $M_{4A}$ and $M_{4B}$ entering the triode region. A temperature-dependent current biasing approach would probably allow achievement of better results, but this has not been considered in this work. Furthermore it has to be noted that an ideal constant current source was considered: while such generator can be devised (e.g., see [49], or using a higher supply voltage for the current reference), this clearly remains a critical issue, dependent on the application environment of the OTA.

**Table 3.** Performance vs. temperature variations.

| **Temp (°C)** | **0.00** | **16.67** | **27.00** | **43.33** | **50.00** | **70.00** |
|---|---|---|---|---|---|---|
| $P_D$ (nW) | 21.48 | 21.93 | 21.89 | 20.40 | 20.54 | 21.35 |
| $I_D$ (nW) | 71.59 | 73.10 | 72.98 | 68.00 | 68.46 | 71.18 |
| $SR_p$ (V/ms) | 11.44 | 15.66 | 18.61 | 23.55 | 25.60 | 31.76 |
| $SR_m$ (V/ms) | 10.11 | 10.99 | 11.51 | 12.47 | 12.84 | 13.65 |
| Gain (1Hz) (dB) | 58.65 | 57.61 | 52 | 50.07 | 48.87 | 46.72 |
| CMRR (dB) | 64.45 | 57.56 | 44.96 | 34.31 | 32.03 | 26.66 |
| Mphi (deg) | 48.63 | 46.26 | 52.40 | 54.54 | 52.86 | 48.88 |
| GBW (kHz) | 32.85 | 39.45 | 35.16 | 30.80 | 32.16 | 37.95 |
| Noise ‡ ($\mu V/\sqrt{Hz}$) | 0.60 | 0.85 | 1.60 | 3.42 | 3.91 | 4.85 |
| THD (%) | 0.45 | 0.51 | 0.67 | 0.72 | 0.84 | 1.23 |

‡ Computed at 1 kHz.

Table 4 shows that the amplifier is stable under power supply variations, with power dissipation and slew-rate increasing significantly with the supply voltage, whereas CMRR improves at lower supply voltages due to the following design centering approach.

**Table 4.** Performance vs Voltage Variations.

| $V_{DD}$ (mV) | 270.0 | 285.0 | 300.0 | 315.0 | 330.0 |
|---|---|---|---|---|---|
| $P_D$ (nW) | 21.710 | 21.980 | 21.890 | 20.500 | 20.240 |
| Idiss (nA) | 72.370 | 73.270 | 72.980 | 68.350 | 67.460 |
| $SR_p$ (V/ms) | 8.532 | 12.750 | 18.610 | 26.500 | 36.790 |
| $SR_m$ (V/ms) | 7.147 | 9.161 | 11.510 | 14.230 | 17.210 |
| Gain (1 Hz) (dB) | 54.34 | 53.22 | 52.93 | 52.84 | 53.07 |
| CMRR (dB) | 60.340 | 53.720 | 44.960 | 38.740 | 35.450 |
| Mphi (deg) | 47.530 | 50.230 | 52.920 | 53.550 | 49.570 |
| GBW (kHz) | 34.830 | 35.230 | 35.160 | 33.470 | 36.980 |
| Noise ‡ ($\mu V/\sqrt{Hz}$) | 0.869 | 1.011 | 1.595 | 2.485 | 3.161 |
| THD (%) | 0.50 | 0.37 | 0.29 | 0.23 | 0.19 |

‡ Computed at 1 kHz.

The OTA was then tested under different process corners and results are reported in Table 5. As is evident from Table 5, the proposed OTA shows good performance, even assuming the worst case process conditions.

**Table 5.** Performance vs. corners.

| Corner | TYP | FF | SS | SF | FS |
|---|---|---|---|---|---|
| $P_D$ (nW) | 21.89 | 20.32 | 21.68 | 21.98 | 26.60 |
| Idiss (nA) | 72.97 | 67.73 | 72.27 | 73.27 | 88.67 |
| $SR_p$ (V/ms) | 18.61 | 27.32 | 12.18 | 28.77 | 11.63 |
| $SR_m$ (V/ms) | 11.51 | 15.47 | 8.62 | 9.00 | 14.43 |
| Gain (1 Hz)(dB) | 52.92 | 50.41 | 57.90 | 55.72 | 49.93 |
| CMRR (dB) | 44.96 | 33.72 | 63.31 | 53.26 | 35.5 |
| PSRR (dB) | 56.40 | 48.26 | 73.31 | 64.93 | 47.52 |
| Mphi (deg) | 52.40 | 51.37 | 48.59 | 42 | 58.59 |
| GBW (kHz) | 35.16 | 34.43 | 37.19 | 49.626 | 27.55 |
| Noise ‡ ($\mu V/\sqrt{Hz}$) | 1.60 | 3.03 | 3.03 | 3.21 | 5.16 |
| THD (%) | 0.67 | 0.25 | 0.43 | 0.95 | 0.46 |

‡ Computed at 1 kHz.

### *4.4. Discussion and Comparison with the Literature*

In order to compare the amplifier with the literature, we employ the two standard figures of merit (FOMs) for small and large-signal performance, namely $FOM_S$ and $FOM_L$. The $FOM_S$ is defined as:

$$FOM_S = \frac{\text{GBW} \cdot C_L}{P_D} \tag{34}$$

where $C_L$ is the load capacitance; the $FOM_L$ is defined as:

$$FOM_L = \frac{SR_{avg} \cdot C_L}{P_D} \tag{35}$$

where $SR_{avg}$ is the average (between the positive and negative edge) slew-rate.

However, since most works presented in the literature show an asymmetric slew-rate, it is more meaningful to consider the worst case slew-rate. Consequently, as in [40], we define the $FOM_{L_{WC}}$ as:

$$FOM_{L_{WC}} = \frac{SR_{WC} \cdot C_L}{P_D} \tag{36}$$

where $SR_{WC}$ is the worst case slew-rate between the positive and negative signal edges.

The proposed amplifier exhibits the largest small-signal *FOM* among the comparable ULV literature, with a $FOM_S$ approaching 80.29 k against the previously reported record of about 20.16 k attained by [42]. The proposed OTA outperforms gate-driven, body-driven and also digital OTAs. Large-signal performance is also very good, especially if

the worst-case $FOM$ is considered: the proposed amplifier is the best in the literature. Indeed, the $FOM_L$ is about 34.40 k; furthermore, the worst case $FOM_{L_{WC}}$ also is very good, approximately 26.30 k, which is an awesome result, also given that previous works attained in the best case $FOM_L \approx 21.00$ k and in the worst case $FOM_{L_{WC}} \approx 8.36$ k. The proposed amplifier has a small area occupation with respect to comparable body-driven designs, though the area is larger than digital and gate-driven designs (Table 6).

**Table 6.** Comparison table.

| | **This Work** * | [42] * | [45] † | [40] * | [39] * | [25] * | [37] † | [50] † | [23] † | [36] * | [51] † |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Year | 2021 | 2021 | 2021 | 2021 | 2021 | 2020 | 2020 | 2019 | 2019 | 2018 | 2018 |
| Technology (µm) | 0.13 | 0.13 | 0.18 | 0.13 | 0.13 | 0.18 | 0.18 | 0.18 | 0.13 | 0.065 | 0.18 |
| $V_{DD}$ (V) | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 |
| $V_{DD}/V_{TH}$ | 0.86 | 0.86 | 0.6 | 0.86 | 0.86 | 0.6 | 0.6 | 0.6 | 0.86 | - | 0.6 |
| $DC_{gain}$ (dB) | 52.92 | 38.07 | 30 | 40.80 | 64.6 | 39 | 98.1 | 64.7 | 49.8 | 60 | 65.8 |
| $C_L$ (pF) | 50 | 50 | 150 | 40 | 50 | 10 | 30 | 30 | 2 | 5 | 20 |
| GBW (kHz) | 35.16 | 24.14 | 0.25 | 18.65 | 3.58 | 0.9 | 3.1 | 2.96 | 9100 | 70 | 2.78 |
| $m\varphi$ (deg) | 52.40 | 60.15 | 90 | 51.93 | 53.76 | 90 | 54 | 52 | 76 | 53 | 61 |
| $SR_+$ $[\frac{V}{ms}]$ | 18.61 | 20.02 | - | 10.83 | 1.7 | - | 14 | 1.9 | - | 25 | 6.44 |
| $SR_-$ $[\frac{V}{ms}]$ | 11.51 | 8.44 | - | 32.37 | 0.15 | - | 4.2 | 6.4 | - | 25 | 7.8 |
| $SR_{avg}$ $[\frac{V}{ms}]$ | 15.06 | 14.23 | 0.085 | 21.60 | 0.93 | - | 9.1 | 4.15 | 3.8 | 25 | 7.12 |
| THD (%) | 0.673 | 1.635 | 2 | 1.4 | 0.84 | 1 | 0.49 | 1 | - | - | 1 |
| % of input swing | 90 | 80 | 90 | 80 | 100 | 23 | 83.33 | 85 | - | - | 93.33 |
| CMRR (dB) | 42.11 ‡ | 54.88 | 41 | 67.49 | 61 | 30 | 60 | 110 | - | 126 | 72 |
| PSRR (dB) | 56.13 ‡ | 51.05 | 30 | 45 | 26/28 * | 33 | 61 | 56 | - | 90/91 * | 62 |
| spot-noise $[\frac{\mu V}{\sqrt{Hz}}]$ | 1.60 | 3.16 | - | 2.12 | 2.69 | 0.81 | 1.8 | 1.6 | 0.035 | 2.82 | 1.85 |
| @freq (Hz) | 1000 | 1000 | - | 1000 | 100 | 1000 | - | - | 100,000 | 1000 | 36 |
| Power (nW) | 21.89 | 59.88 | 2.4 | 73 | 11.4 | 0.6 | 13 | 12.6 | 1800 | 51 | 15.4 |
| Mode | BD | BD | DIGITAL | BD | BD | GD | BD | BD | GD | BD | BD |
| $FOM_S$ $[\frac{MHz \cdot pF}{mW}]$ | 80.29 k | 20.16 k | 15.89 k | 10.20 k | 15.72 k | 15.00 k | 7.15 k | 7.05 k | 10.11 k | 6.86 k | 3.61 k |
| $FOM_L$ $[\frac{V \cdot pF}{\mu s \cdot mW}]$ | 34.40 k | 11.88 k | 5.40 k | 11.82 k | 4.08 k | - | 21.00 k | 9.88 k | 4.67 k | 2.45 k | 9.25 k |
| $FOM_{L_{WC}}$ $[\frac{V \cdot pF}{\mu s \cdot mW}]$ | 26.30 k | 7.04 k | - | 5.93 k | 4.52 k | - | 6.30 k | 4.52 k | - | 2.45 k | 8.36 k |
| Area $[mm^2]$ | 0.0052 ★ | 0.0027 | 0.000982 | 0.0036 | 0.0036 | 0.00047 | 0.0098 | 0.0085 | - | 0.003 | 0.0082 |

* Simulated; † Measured; ‡ Monte Carlo mean-value; * $PSRR_+/PSRR_-$ [dB]; ★ area estimated accounting for the minimum distances due to deep N-Wells for body connections.

## 5. Conclusions

In this work, we propose a novel tree-based OTA architecture that exploits body-driven stages to achieve rail-to-rail ICMR, and body-diode loads to avoid Miller compensation, improving the bandwidth efficiency. A ULV ULP OTA exploiting this approach was designed in a 130 nm CMOS process from STMicroelectronics. Simulation results show a dc gain higher than 52 dB, a gain-bandwidth product of about 35.16 kHz with nominal CMRR and PSRR, respectively, equal to 42.11 dB and 56.13 dB. Large-signal characteristics are also very good both in terms of THD and slew-rate. Due to the very limited power consumption of about 21.89 nW, the OTA exhibits state-of-the-art small-signal and large-signal FoMs. Summarizing, the overall performance of the proposed OTA shows record-breaking small-signal and large-signal performance, relatively large DC gain and reasonable PSRR and CMRR performance. The OTA exhibits good stability and robustness against PVT and mismatch variations.

**Author Contributions:** Conceptualization, F.C., R.D.S. and G.S.; data curation, R.D.S.; investigation, F.C., R.D.S., P.M. and G.S.; software, R.D.S.; validation, R.D.S.; supervision, F.C. and G.S.; writing—original draft preparation, R.D.S. and P.M.; writing—review and editing, F.C. and G.S.; funding acquisition, A.T. All authors have read and agreed to the published version of the manuscript.

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## Appendix A. Body-to-Gate (B2G) Interface

This section aims to explain the body-to-gate (B2G) interface which is exploited in each stage $i$th$-1$, $i$th interface. Following the notation in Figure A1a, the current gain can be expressed as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{m_B}}{g_{mb_A}} \left( \frac{1}{1 + \frac{1}{g_{mb_A}/g_{ds_A}}} \right) \frac{1}{1 + s\frac{C_{gs_B} + C_{bs_A} + C_{gd_A} + C_{gd_B}\chi_\alpha}{g_{mb_A} + g_{ds_A}}} \tag{A1}$$

where $\chi_\alpha$ derives from Miller approximation on $C_{gd_B}$ and can be therefore expressed as:

$$\chi_\alpha = \frac{g_{m_B}}{(g_{ds_B} + g_{load})} \tag{A2}$$

where $g_{load}$ load conductance and as a consequence it could be equal to $g_{mb_{load}}$ or $g_{ds_{load}}$ (respectively, for stage$_{1,2}$ and stage$_3$). It is possible thereafter to conclude that the interface behaves as a small signal current-mirror with gain.

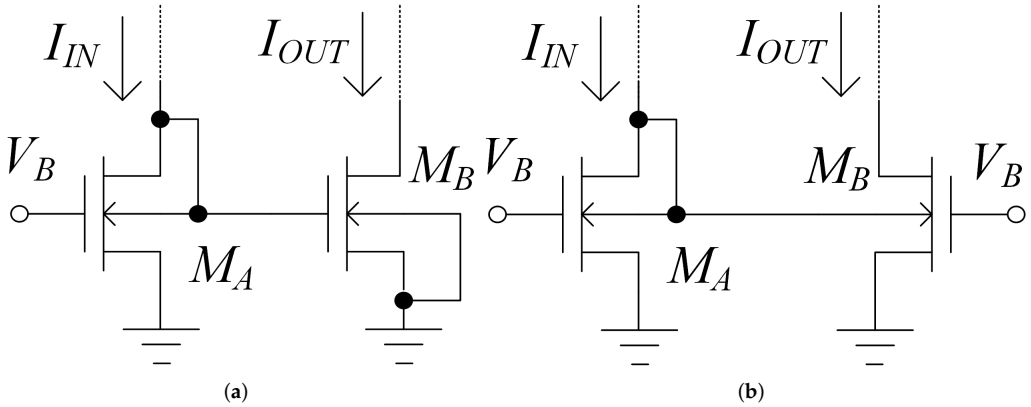


**Figure A1.** (**a**) Body-to-gate (B2G) interface; (**b**) body-to-body (B2B) mirror.

## Appendix B. Body-to-Body (B2B) Mirror

This section aims at explaining the body-to-body (B2B) interface which is exploited in each stage. Following the notation in Figure A1b, the current gain can be expressed as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{mb_B}}{g_{mb_A}} \left( \frac{1}{1 + \frac{1}{g_{mb_A}/g_{ds_A}}} \right) \frac{1}{1 + s\frac{C_{gd_A} + C_{bs_A} + C_{bs_B} + C_{bd}\chi_\beta}{g_{ds_A} + g_{mb_A}}} \tag{A3}$$

where also in this case $\chi_\beta$ denotes the Miller approximation and can be derived as:

$$\chi_\beta = \frac{g_{mb_B}}{(g_{ds_B} + g_{load})} \tag{A4}$$

Finally, it can be concluded that the interface could be considered as a B2B mirror that enables a small-signal current mirror whose gain is fixed by properly sizing $M_A$ and $M_B$.

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