A Triple-Mode Continuous-Time ΣΔ Modulator With Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver

Robert H. M. van Veldhoven

***Abstract*—Time jitter in continuous-time ΣΔ modulators is a known limitation on the maximum achievable signal-to-noise-ratio (SNR). Analysis of time jitter in this type of converter shows that a switched-capacitor (SC) feedback digital-to-analog converter (DAC) reduces the sensitivity to time jitter significantly. In this paper, an I and Q continuous-time fifth-order ΣΔ modulator with 1-bit quantizer and SC feedback DAC is presented, which demonstrates the improvement in maximum achievable SNR when using an SC instead of a switched-current (SI) feedback circuit.**

The modulator is designed for a GSM/CDMA2000/UMTS receiver and achieves a dynamic range of 92/83/72 dB in 200/1228/3840 kHz, respectively. The intermodulation distance IM2, 3 is better than 87 dB in all modes. Both the I and Q modulator consumes a power of 3.8/4.1/4.5 mW at 1.8 V. Processed in 0.18-μm CMOS, the 0.55-mm^2 integrated circuit includes a phase-locked loop, two oscillators, and a bandgap.

***Index Terms*—Mobile communication, telecommunication receiver, intermediate frequency (IF) conversion, GSM, EDGE, CDMA2000, UMTS, sigma-delta analog-to-digital converter (ADC), sigma-delta modulator, switched-capacitor (SC) digital-to-analog converter (DAC), reduced jitter sensitivity.**

I. Introduction

THE diversity in mobile communication standards requires the integration of multimode receiver architectures on silicon to reduce cost and application dimensions. In order to share analog circuits in the different modes, it is necessary to align signal levels and noise densities. The analog-to-digital converter (ADC) must adapt to the required channel bandwidth in each mode. In [1], [2] ΣΔ modulators have been demonstrated for a dual-mode receiver. This paper presents a ΣΔ modulator, which can convert the intermediate frequency (IF) signals in a GSM, EDGE, CDMA2000, and UMTS receiver into the digital domain.

The receiver architecture and the required dynamic ranges in the different modes are discussed in Section II. Although continuous-time ΣΔ modulators are known to be very power efficient, the maximum achievable signal-to-noise ratio (SNR) is limited due to their sensitivity to time jitter. The time jitter sensitivity of both a continuous-time ΣΔ modulator with switched current (SI) and switched-capacitor (SC) feedback circuit is analyzed in Section III. The implementation of the modulator circuits is described in Section IV. Section V and VI present the experimental results and the conclusions, respectively.

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The author is with Philips Research Laboratories, 5656 AA Eindhoven, The Netherlands (e-mail: robert.van.veldhoven@philips.com).

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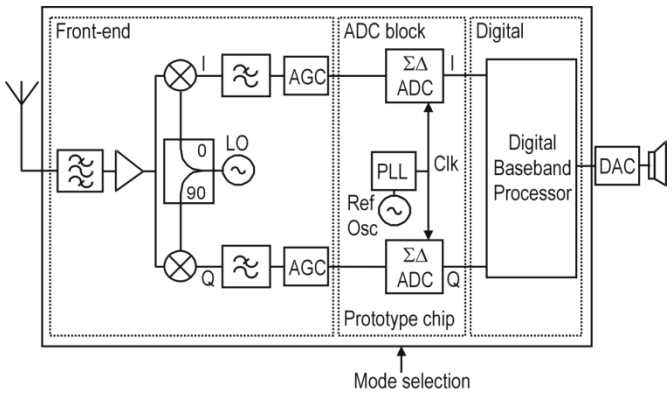


Fig. 1. Triple-mode receiver architecture.

II. Receiver Architecture and Dynamic Range of the ADC

The receiver architecture used, which is shown in Fig. 1, is similar to the structure described in [3]. An RF front-end converts the antenna signal down to the IF frequency— zero-IF for UMTS and CDMA2000 and low-IF (100 kHz) for GSM and EDGE. The IF signals are fed to an I and Q ΣΔ modulator. The dynamic range requirement of the modulator is determined by the amount of prefiltering in front of the modulator which attenuates large out-of-band interferers. To reduce the required dynamic range of the modulators, a passive first-order filter is implemented in front of the modulator. To avoid expensive discrete analog channel filters, a high dynamic range of the modulator is still required. This way, most of the channel filtering can be implemented digitally.

Table I summarizes the specifications on bandwidth and dynamic range in the different modes, from which the maximum allowed noise density can be derived. Because the modulator has to cope with the IF signals of four different systems, bandwidth and sample frequency has to be adapted to be able to achieve a high dynamic range at minimum power consumption. To assure reusability of circuits, the maximum ADC input level provided by the front-end is set to 1 $V_{\rm rms}$ differential in all modes. Furthermore, because GSM and EDGE bandwidths and dynamic ranges required are very close, it is decided to combine these two standards in one ADC mode.

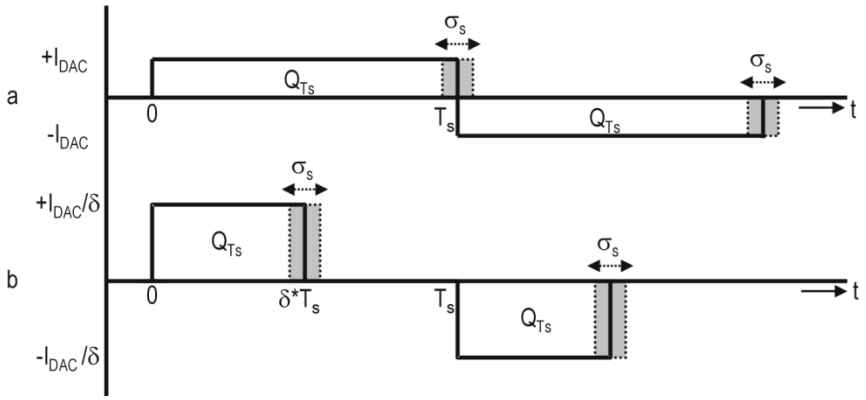


Fig. 2. SNR limitation due to jitter on the pulse width (SI).

TABLE I
ADC REQUIREMENTS IN THE DIFFERENT MODES

Mode	UMTS	CDMA2000	EDGE	GSM
Receiver topology	ZIF	ZIF	LIF	LIF
Channel bandwidth [kHz]	3840	1228	270	190
SNR Specification [dB]	70	80	87	90
Noise Density [nV/√Hz] ($V_{in,max}$=1V_{rms})	228	128	85	72
ADC Sample Frequency [MHz]	153.6	76.8	26	26
Calculated SNR Thermal [dB]	78	85	88	90
Simulated SNR Quantization [dB]	82	103	102	105
Simulated SNR Total [dB]	76	85	88	90

ADC target specification

Table I indicates that UMTS-mode has the highest bandwidth, which implies high bandwidth circuits, while GSM-mode requires the lowest noise density and determines power consumption due to the low impedances required to achieve this low noise density. Although the combination of the foregoing contradicts the low power receiver solution needed in present-day telecom terminals, the few decibels overhead in dynamic range in UMTS- and CDMA2000-mode can reduce the required analog prefiltering in front of the ADC even more, and minimize cost.

Continuous-time $\Sigma\Delta$ modulators are chosen for the ADC topology because of their high dynamic range and built in anti-alias filter. The bandwidth of these type of converters can be scaled easily by changing the coefficients and sample frequency. A major disadvantage of continuous-time modulators is their sensitivity to time jitter, which will be analyzed in the next section.

III. SNR LIMITATION DUE TO TIME JITTER IN $\Sigma\Delta$ MODULATORS

A major concern in continuous-time $\Sigma\Delta$ modulators is the degradation of the SNR due to time jitter. Imprudent design of the clock circuitry, which generates the feedback-D/A clock, will induce too much time jitter on the DAC feedback pulse and will degrade the performance of the modulator.

In this section two different ways in which time jitter influences the performance of a $\Sigma\Delta$ modulator will be discussed. First the degradation of the SNR due to time jitter on the pulse width will be calculated for an SI and an SC feedback DAC. Secondly the SNR limitation due to time jitter on the pulse position is presented.

A. Pulse Width Jitter in a Continuous-Time 1-Bit $\Sigma\Delta$ Modulator

In this subsection, the time jitter calculations on pulse width jitter in [4] will be extended. Pulse width jitter is the constantly changing integrated charge per clock cycle of the feedback pulse due to time jitter on the clock.

1) Pulse Width Jitter in a Continuous-Time 1-Bit $\Sigma\Delta$ Modulator With SI DAC: In Fig. 2(a) the waveform in an SI DAC is displayed. When there is time jitter present on the clock this will cause timing errors Δt with variance σ_s^2 causing a variation on the pulse width. The variance of the error charge σ_q^2 transferred per clock cycle T_s can be calculated by

$$\sigma_q^2 = \sigma_s^2 \cdot I_{\mathrm{DAC}}^2 \tag{1}$$

where I_{DAC} is the amplitude of the feedback current. To reduce the intersymbol interference (ISI) [4] a return-to-zero (RTZ) interval in the DAC feedback pulses can be used. In Fig. 2(b) the feedback pulse in a switched current feedback DAC of a continuous-time $\Sigma\Delta$ modulator is shown for RTZ $= 0$ (a) and RTZ $= 1 - \delta$ (b) in which δ is the non-return-to-zero (NRTZ) interval. When RTZ is used, the feedback pulse has to have an amplitude inversely proportional to δ to assure that the amount of integrated feedback charge Q_{Ts} is constant, and the gain in the feedback path is RTZ independent. This increases the magnitude of σ_q because of the $1/\delta$ times larger amplitude feedback pulses. The NRTZ interval can be added to (1) which leads to

$$\sigma_q^2 = \frac{\sigma_s^2 \cdot I_{\mathrm{DAC}}^2}{\delta^2}. \tag{2}$$

A disadvantage of the RTZ interval is the higher clock frequency needed to create the RTZ interval. When RTZ $= 0.5$, the feedback pulse is two times shorter in time, and to feedback the same amount of charge Q_{Ts}, the pulse has to be twice the amplitude. The error charge due to time jitter is expected to be two times higher compared to the RTZ $= 0$ pulses.

Formula (2) is only true when it is assumed that the time jitter on the output clock of the oscillator is independent of its output frequency. For every clock generator or oscillator [with

or without a phase-locked loop (PLL)], which generates a fixed frequency the following is true:

$$\sigma^2_{\mathrm{osc,out}} \cdot f_{\mathrm{osc,out}} = \mathrm{constant}. \tag{3}$$

If the oscillator output frequency $(\mathrm{f_{osc,out}})$ is divided by two it can be seen that the jitter $(\sigma_{\mathrm{osc,out}})$ increases with $\sqrt{2}$, assuming that the noise contribution (time jitter) caused by the divider is insignificant. In case of RTZ $= 0.5$ the feedback pulse is two times shorter in time, and to feedback the same amount of charge Q_{Ts}, the pulse has to be twice the amplitude. Intuitively one would think that the performance degradation due to time jitter would be two times higher compared to the RTZ $= 0$ pulses. However, this is not the case when looking at (3). To be able to create the RTZ $= 0.5$ pulses, a clock with twice the frequency has to be used. This clock has $\sqrt{2}$ times less time jitter, and thus it can be generally written that

$$(\sigma_{\mathrm{osc,out}} \cdot \sqrt{\delta})^2 \cdot \frac{f_{\mathrm{osc,out}}}{\delta} = \mathrm{constant}. \tag{4}$$

If the oscillator output frequency is chosen two times higher, $\sigma_{\mathrm{osc,out}}$ is multiplied by $\sqrt{\delta}$ which in this case is 0.707.

This means that (2) changes into

$$\sigma_q^2 = \frac{\sigma_s^2 \cdot I^2_{\mathrm{DAC}}}{\delta} \tag{5}$$

when the performance of the oscillator as a function of its output frequency is also taken into account in the ADC design process.

The power of a sinewave with amplitude A is $A^2/2$. The maximum signal amplitude at the input of the modulator is -3 dB compared to the DAC current levels, so $A = I_{\mathrm{DAC}}/\sqrt{2}$. The signal charge per sample period can be calculated with $q = i \cdot t$

$$Q^2_{\mathrm{signal}} = \frac{I^2_{\mathrm{DAC}} \cdot T_s^2}{4}. \tag{6}$$

The maximum SNR is the maximum signal power divided by the noise power in the signal band. Assuming that the noise power that is introduced by time jitter is white, the maximum achievable SNR due to pulse width jitter is

$$\begin{aligned}\frac{S}{N_{\mathrm{jitter,SI}}} &= 10\log\left(\frac{Q^2_{\mathrm{signal}}}{\sigma_q^2} \cdot \frac{f_s}{2f_b}\right) \\ &= 10\log\left(\frac{\delta}{16 \cdot \mathrm{OSR} \cdot f_b^2 \cdot \sigma_s^2}\right) \\ &= 10\log\left(\frac{\delta \cdot \mathrm{OSR}}{4 \cdot f_s^2 \cdot \sigma_s^2}\right).\end{aligned} \tag{7}$$

Formula (7) is extended with δ when compared to (13) and (14) presented in [4].

2) Pulse Width Jitter in a Continuous-Time 1-Bit ΣΔ Modulator With SC DAC: To reduce the degradation on the SNR due to time jitter on the clock, an SC feedback circuit can be used to implement the feedback DAC of the modulator.

The feedback current in the SC DAC is shown in Fig. 3. The integrated feedback charge Q_{Ts} is the same as in the switched current example $(Q_{Ts,\mathrm{SI}} = Q_{Ts,\mathrm{SC}})$, because the same amount of charge has to be fed back to the input to assure the same gain from input to output of the modulator.

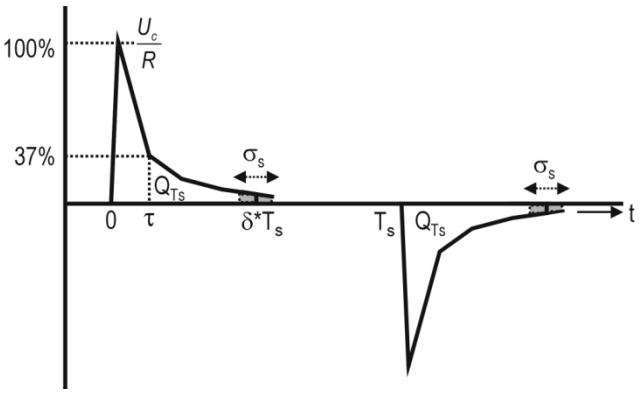


Fig. 3. SNR limitation due to jitter on the pulse width (SC).

From Fig. 3, it can be seen that the error charge due to clock jitter is now dependent on the settling-time constant τ of the DAC. When it is assumed that $\sigma_s << T_s, \tau$, the variance of the error charge transferred per clock cycle can be approximated by

$$\sigma_q^2 = \sigma_s^2 \cdot \delta \cdot \frac{U_c^2}{R^2}\left(e^{\frac{-T_s \cdot \delta}{\tau}}\right)^2 \tag{8}$$

where $\tau = R \cdot C, U_c$ is the capacitor voltage, and R is the resistance in which the capacitor is discharged. Generally R is determined by switch resistance and the equivalent input impedance of the integrator stage.

From Fig. 3, the integrated feedback charge per clock period can be calculated

$$\begin{aligned}Q_{Ts,\mathrm{SI}} &= \frac{U_c}{R}\int_0^{\delta \cdot T_s} e^{\frac{-t}{\tau}} \cdot dt = -\tau\,\frac{U_c}{R} e^{\frac{-t}{\tau}}\Big|_0^{\delta \cdot T_s} \\ &= U_c \cdot C \cdot \left(1 - e^{\frac{-\delta \cdot T_s}{\tau}}\right).\end{aligned} \tag{9}$$

The signal charge per clock period Q_{signal} can be calculated in the same way (6) is derived

$$Q^2_{\mathrm{signal}} = \frac{U_c^2 \cdot C^2}{4} \cdot (1 - e^{-\delta \cdot \alpha})^2. \tag{10}$$

With α defined as

$$\alpha = \frac{1}{\tau \cdot f_s} = \frac{T_s}{\tau} \tag{11}$$

which gives the number of settling time constants $\tau = \mathrm{RC}$ relative to T_s. Now the SNR limitation due to pulse width jitter in a modulator with SC feedback can be calculated using (8) and (10)

$$\begin{aligned}\frac{S}{N_{\mathrm{jitter,SC}}} &= 10\log\left(\frac{Q^2_{\mathrm{signal}}}{\sigma_q^2} \cdot \frac{f_s}{2f_b}\right) \\ &= 10\log\left(\frac{\mathrm{OSR} \cdot \tau^2}{4 \cdot \delta \cdot \sigma_s^2} \cdot (1 - e^{\delta \cdot \alpha})^2\right).\end{aligned} \tag{12}$$

Formula (12) can be rewritten using (11) as

$$\frac{S}{N_{\mathrm{jitter,SC}}} = 10\log\left(\frac{\delta \cdot \mathrm{OSR}}{4 \cdot f_s^2 \cdot \sigma_s^2}\left(\frac{1 - e^{\delta \cdot \alpha}}{\delta \cdot \alpha}\right)^2\right). \tag{13}$$

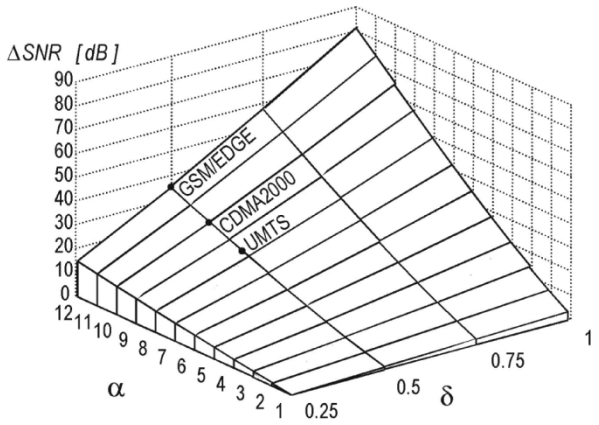


Fig. 4. ΔSNR as function of σ and δ.

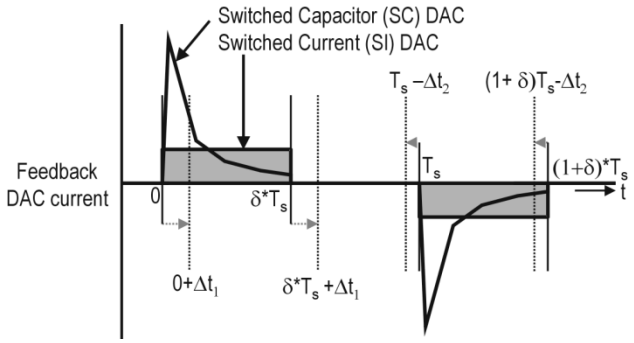


Fig. 5. SNR limitation due to jitter on the pulse position.

With constant OSR, time jitter, sample frequency and RTZ interval, the improvement from a switched current to SC feedback DAC is given by

$$\Delta\text{SNR} = \frac{S}{N_{\text{jitter,SC}}} - \frac{S}{N_{\text{jitter,SI}}} = 20\log\left(\left|\frac{(1-e^{\delta\cdot\alpha})}{\delta\cdot\alpha}\right|\right)\ \text{dB}. \tag{14}$$

The improvement is only dependent on the multiplication of δ and α, which gives the effective settling of the SC DAC. This can also be seen intuitively, because when $T_s \gg \tau \Rightarrow \alpha \to \infty$ and the SC current would settle completely. This would give an infinite improvement in achievable SNR, because pulse width jitter is eliminated completely. In the case of $\alpha = 3$ and $\delta = 1$ the improvement would be 16 dB. In Fig. 4, (14) is plotted as a function of δ and α.

B. Pulse Position Jitter in a Continuous-Time 1-Bit $\Sigma\Delta$ Modulator

In [4] it is stated that due to time jitter on the clock the position of the feedback pulse is shifted in time while keeping its integrated feedback charge Q_{Ts} constant. The effect is demonstrated in Fig. 5. The SI or SC feedback pulse is shifted over a time $\Delta t_{1,2}$ by the time jitter on the clock. The formula that can be used to calculate the degradation in SNR due to this effect is repeated here.

$$\frac{S}{N} = 10\log\left(\frac{1}{4\cdot\pi^2\cdot f_b^2\cdot\sigma_s^2}\right) \tag{15}$$

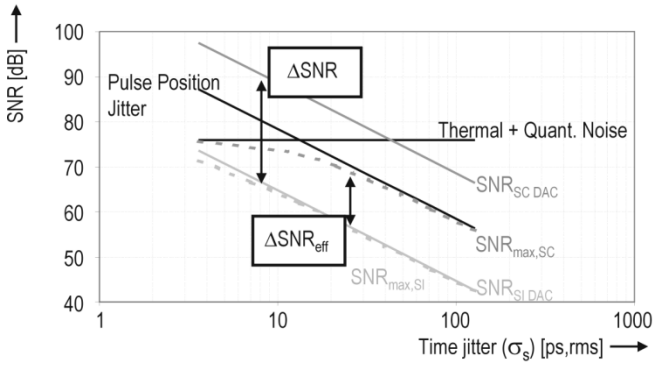


Fig. 6. SNR limitation in UMTS mode.

where f_b is the input signal frequency and σ_s is the variance of the jitter on the clock.

At high input frequencies the degradation is the most severe, so substituting the ADC channel bandwidth for f_b gives the worst case scenario. The time jitter on the clock is represented by σ_s. Pulse position jitter is assumed to have the same effect on both SI and SC feedback $\Sigma\Delta$ modulators.

C. SNR Limitations in UMTS Mode

In Fig. 6, all SNR limiting contributions are shown for UMTS mode. The solid horizontal line represents the maximum achievable SNR due to quantization and thermal noise, which are determined by the ADC design and chosen such a way that power consumption is minimized. The SNR limitation due to pulse position jitter is independent of the modulator design parameters because the bandwidth of the modulator is fixed and the time jitter is determined by the PLL and reference oscillator.

For the switched current implementation the SNR limitation ($\text{SNR}_{\text{SI DAC}}$) due to pulse width jitter is also given in Fig. 6. When thermal-, quantization- and jitter noise is added, the maximum achievable SNR ($\text{SNR}_{\text{max,SI}}$) as a function of time jitter can be calculated, which is also plotted in Fig. 6, and is dominated by the pulse width jitter at realistic time jitter values. As can be seen from the figure, time jitter values lower than 4 ps_{rms} are needed to achieve the SNR of 70 dB needed for our UMTS application.

The same calculation is done for the modulator with SC feedback DAC. The SNR limitation due to pulse width jitter ($\text{SNR}_{\text{SC DAC}}$) is beyond the pulse position SNR limitation which, in the SC feedback DAC case, limits the maximum achievable SNR ($\text{SNR}_{\text{max,SC}}$).

The difference (ΔSNR) in SNR limitation due to pulse width jitter for SC and SI is also displayed in Fig. 6, and is 24 dB using (14) with $\alpha = 8.4$ and $\delta = 0.5$. Because pulse position jitter for the SC DAC is dominant, the effective improvement when going from an SI DAC to an SC DAC is $\Delta\text{SNR}_{\text{eff}}$. The effective improvement $\Delta\text{SNR}_{\text{eff}}$ for low time jitter values is limited by the thermal and quantization noise and for high time jitter values fully dependent on the pulse position jitter.

IV. Implementation of the $\Sigma\Delta$ Modulator

Fig. 7 shows the block diagram of the $\Sigma\Delta$ modulator. A fifth-order feedforward loopfilter is implemented with two complex

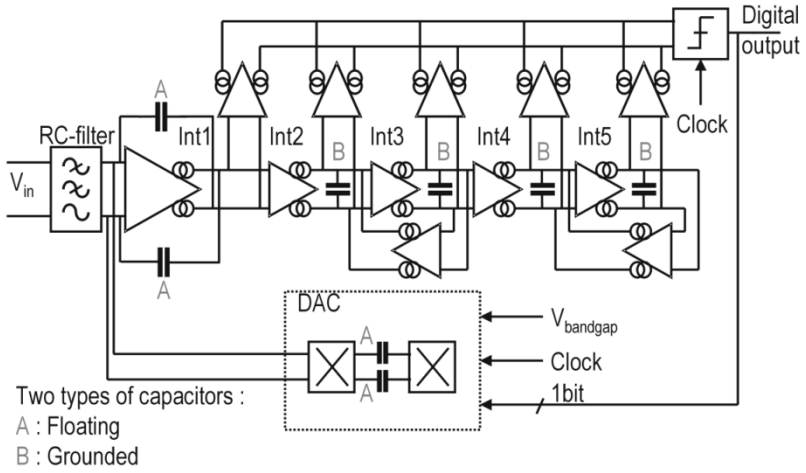


Fig. 7. Block diagram of the 1-bit fifth-order feedforward ΣΔ modulator.

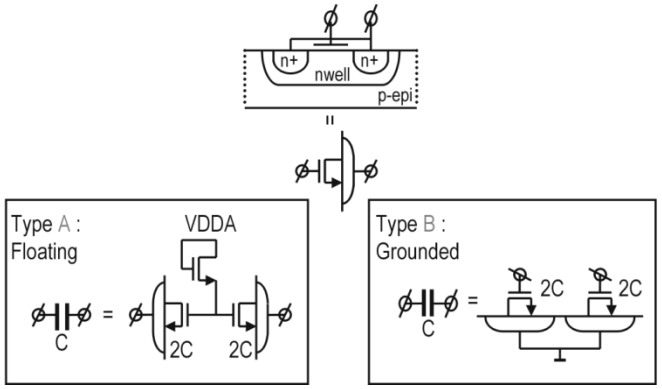


Fig. 8. Capacitors with NMOS in NWELL devices.

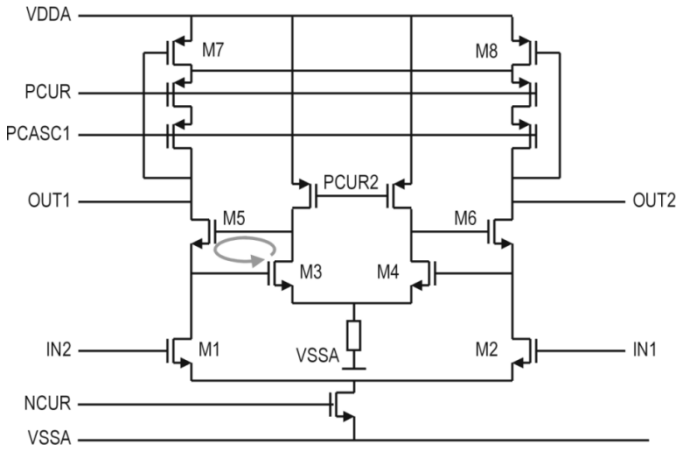
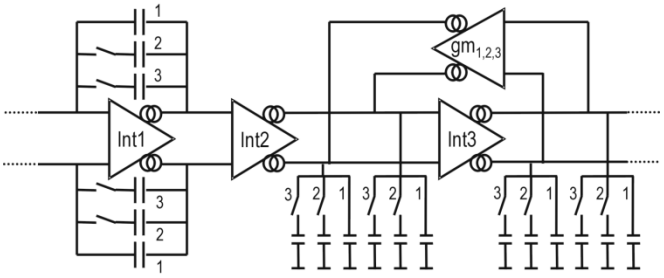


Fig. 9. Circuit diagram of the amplifier used in the first integrator.



Mode	Switch 3	Switch 2	Switch 3
UMTS	X	X	X
CDMA2000		X	X
GSM-EDGE			X

Fig. 10. Scaling of the loop.

conjugate poles to suppress the quantization noise at the edge of the signal band. The design and corresponding AC transfer function of the loopfilter is similar as described in [5].

A 1-bit quantizer is used together with a 1-bit inherently linear SC DAC. This way, the advantages of low-jitter sensitivity of SC ΣΔ modulators and high anti-alias suppression of continuous-time ΣΔ modulators are combined like in [6]. Table I shows the maximum achievable signal-to-quantization-noise ratio (SQNR) of the fifth-order modulator in all modes. The sample frequencies in the GSM/CDMA2000/UMTS modes are 26/76.8/153.6 MHz, respectively. Without clock jitter, the theoretical SQNR in GSM/CDMA2000/UMTS mode is 102/103/84 dB. Because the SQNR in all modes is at least 10 dB better than required, thermal noise is dominant which results in the lowest power consumption.

A. Capacitors With NMOS in NWELL Devices

All capacitors of the modulator are implemented as NMOS in NWELL devices, which have a well defined absolute value and show good matching. Because the NMOS in NWELL capacitors are normally on devices, these capacitors show good linearity at low bias voltages. A disadvantage of this type of capacitor is the large parasitic capacitance from NWELL to substrate. Capacitor type A (Fig. 8) uses two capacitors of which the gates are connected together and via a diode to the analog supply (VDDA), to create a floating feedback capacitor. At start-up the diode pulls up the capacitor gates to the VDDA, to bias the capacitors in their linear region. When the gates are charged to VDDA, the diode has a $V_{\rm GS}$ of zero volt and presents a high impedance. The NWELL terminals are the terminals of the capacitor. The parasitic capacitors of nonfloating capacitor type B are shorted by substrate contacts and (external) ground connections.

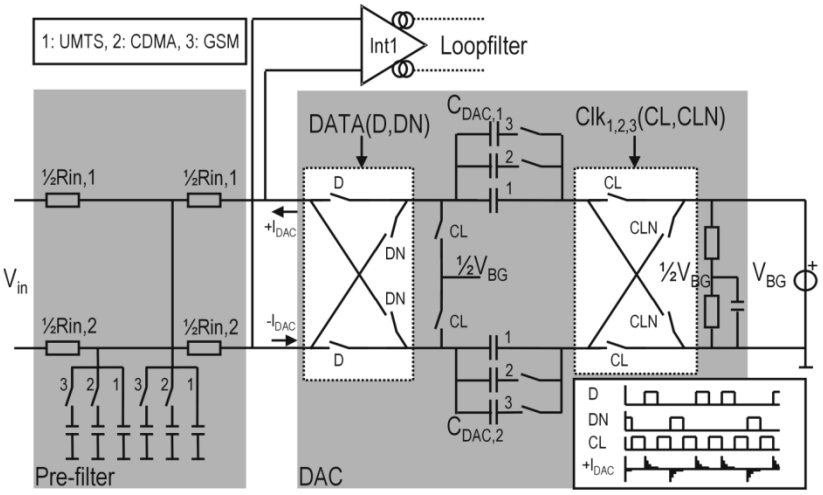


Fig. 11. Input filter and SC feedback DAC.

B. Loopfilter Design

The circuit of the amplifier used in the first integrator shown in Fig. 9, uses a regulated NMOS cascode which compensates for the low output impedance of the input transistors, which have minimum channel length to achieve high speed. The gain-boost amplifier is biased with a resistor to avoid the need for an additional common-mode circuit. The integrator stage achieves a DC gain of 80 dB.

The second–fifth integrator and feedforward coefficients are implemented with scaled transconductances, similar as described in [3]. The interface circuit to the comparator is different because only one instead of two comparators is used in this design.

The scaling of the loop filter is shown in Fig. 10. In the CDMA2000 mode, the switches numbered 2 are closed and additional capacitance is added to the output of the integrator. In the GSM-EDGE mode, the switches 2 and 3 are closed and, again, additional capacitance is switched to the integrator outputs to increase the integrator time-constants further to get the desired noise-shaping. The feedback transconductors are also scaled to move the complex-conjugate poles to the wanted frequencies.

To prevent the fifth-order slope of the quantization noise shifting into the signal band due to process variations, the notches created by the feedback transconductors are placed $\sim$10% higher than their optimum frequency. Since the maximum achievable SNR is not limited by the quantization noise in all three modes, additional margin is provided.

C. SC Feedback DAC

As concluded from Section III, to reduce the negative effect of pulse width jitter on the dynamic range of the converter, an SC feedback DAC is used.

In Fig. 11, the SC DAC circuit is shown in detail. The capacitors used in the DAC are of the semi-floating type A (see Fig. 8). In the first clock phase, the capacitors are charged to half the bandgap voltage $V_{\rm BG}$ by closing switches CL (switches CLN are open). In the second clock phase switches CLN are closed (switches CL are open) and the capacitors are discharged in a data-dependent way by closing switches D or DN depending on the output of the comparator. The DAC output current is subtracted from the input current and integrated on the capacitors of the first integrator. In GSM and CDMA2000 additional capacitors are switched on to keep a constant ratio between the input resistance and the effective DAC feedback resistance, which changes proportional to $1/(f_s \cdot C_{\rm DAC})$. This is to have the correct gain, as well as low enough $(k \cdot T)/C$ noise, in all modes.

In each mode, the cutoff frequency of the prefilters (see Fig. 11) is adapted to the lowest value possible to achieve the highest possible attenuation of out-of-band interferers.

Mode	f_{osc}[MHz]
UMTS	30.72 (X1)
CDMA2000	30.72 (X1)
GSM-EDGE	52 (X2)

Mode	f_{PLL}[MHz]
UMTS	307.2
CDMA2000	153.6
GSM-EDGE	n.a.

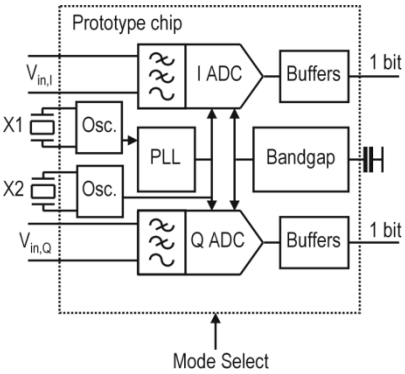


Fig. 12. Block diagram of the prototype chip.

V. Experimental Results

The block diagram of the prototype chip is shown in Fig. 12. The chip is fabricated in a single poly, five metal layer digital 0.18-μm CMOS process. The IC includes two oscillators, a PLL and a bandgap. The oscillator frequency is 52 MHz in GSM-EDGE mode while in CDMA2000 and UMTS mode an oscillator frequency of 30.72 MHz is used. The PLL generates the sample frequencies of 76.8 and 153.6 MHz for CDMA2000 and UMTS mode, respectively. In GSM-EDGE mode the PLL is not used and is powered down.

The die micrograph of a single triple-mode $\Sigma\Delta$ modulator is shown in Fig. 13. The modulator operates from 1.6 to 2.9 V with only $\pm$1-dB SNR variation. Power consumption of both the I and Q modulator is 3.8 mW in GSM-EDGE, 4.1 mW in CDMA2000 and 4.5 mW in UMTS mode at 1.8-V supply.

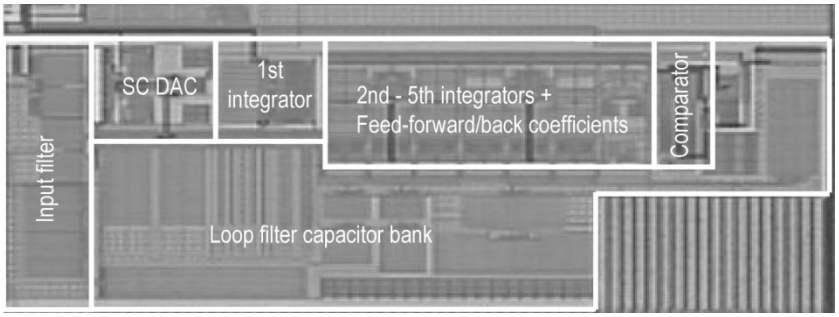


Fig. 13. Micrograph of a single modulator.

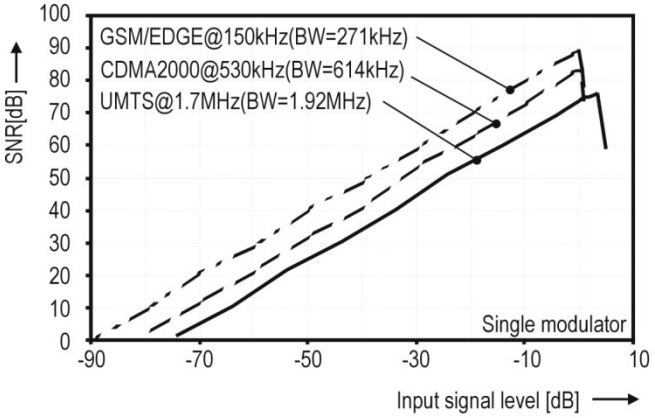


Fig. 14. SNR as a function of input level.

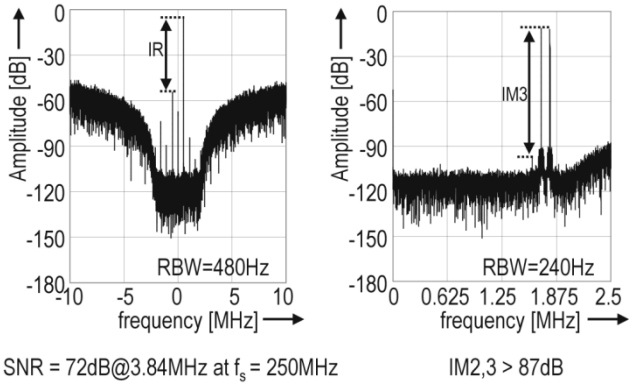


Fig. 15. Image rejection and intermodulation in the UMTS mode.

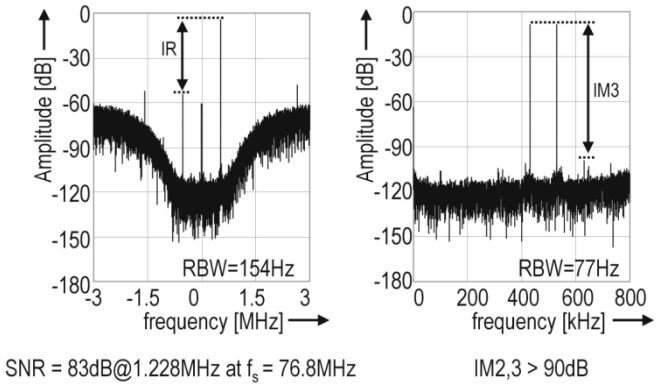


Fig. 16. Image rejection and intermodulation in the CDMA2000 mode.

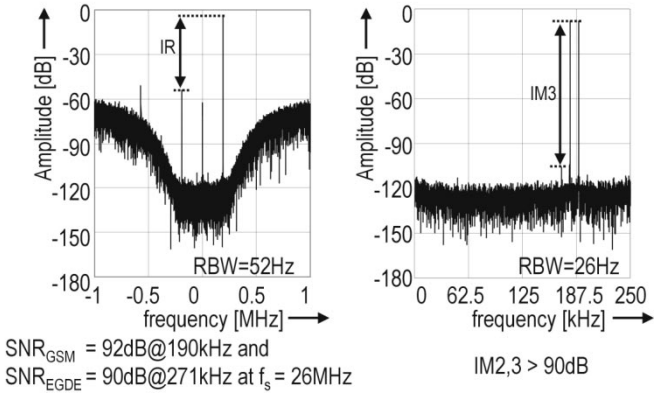


Fig. 17. Image rejection and intermodulation in the GSM–EDGE mode.

In Fig. 14, the SNR as a function of the input signal level is plotted. At full-scale input signals with frequencies of 150/530/1700 kHz for GSM-EDGE/CDMA2000/UMTS mode, the peak SNR is 92/83/72 dB in bandwidths of 200/1228/3840 kHz. The differential input swing is 1 $\mathrm{V_{rms}}$ in all measurements. In UMTS mode, a higher sample frequency of 250 MHz had to be used, instead of the intended 153.6 MHz. The reason for this is a design error of the different clocks in DAC. The data is clocked into the DAC flip-flops before it is stable. By using the higher clock, the clock edge can be shifted in time, to assure the data is clocked into the DAC flip-flops in the right way.

Due to the higher frequency the SC DAC has a lower effective resistance $1/(f_s \cdot C_{\mathrm{DAC}})$ than originally designed. Since the sample frequency is 1.6 times higher, the maximum input signal that can be applied to the $\Sigma\Delta$ modulator is 1.6 $\mathrm{V_{rms}}$ differential. At this input signal, the measured dynamic range of the I and Q combination is 76 dB in 3.84 MHz.

The measured I and Q output spectra are shown in the left spectra of Figs. 15–17. In all three modes the image rejection (IR) is 50 dB, which is limited by the amplitude and phase mismatch of the quadrature input signals generated by the arbitrary waveform generator (AWG). The harmonic distortion visible also originates from the AWG. This is shown by the intermodulation (IM) measurements displayed at the right of Figs. 15–17. Two differential tones are generated by two separate channels of the AWG, and are combined with a resistive 50 Ω network. This way, no IM components are produced by the AWG. The measured IM2 and IM3 distance is better than 87 dB in all modes, for two −6-dBFS input tones.

In Fig. 18 a measurement of the SNR in UMTS mode is displayed together with a number of calculated SNR curves

TABLE II
PERFORMANCE SUMMARY OF THE MODULATOR

Process	1P, 5M, standard 0.18 μm CMOS			
Supply voltage	1.6 – 2.9V (+/- 1dB DNR performance deviation)			
ΣΔ modulator	5th order CT, feedforward, 1 bit with SC DAC			
Input voltage range	1 V rms, differential			
Mode	**UMTS**	**CDMA2000**	**GSM (EDGE)**	
IF	Zero-IF	Zero-IF	Low-IF	
Sampling rate	153.6 MHz	76.8MHz	26MHz	
Signal bandwidth	3.84 MHz	1.228MHz	200kHz *(271kHz)*	
Oversampling ratio	40	64	65 (48)	
Dynamic range	74dB (f_s=250MHz)	83dB	92dB *(90dB)*	
Intermodulation distances	IM2>110dB*	IM2>98dB	IM2>110dB*	
	IM3>87dB	IM3>91dB	IM3>97dB	
Image Rejection	>50dB**	>50dB**	>50dB**	
	**** Not visible because of noise floor***			
	***** Measurement limited by test setup***			
Area and power	**Power@1.8V [mW]**			**Area [mm²]**
I&Q ΣΔ modulator	2*4.5	2*4.1	2*3.8	2*0.18
PLL	3.8	3.6	--	0.14
Oscillator	0.8	0.8	1	0.03
Bandgap	0.5	0.5	0.5	0.02
Total :	14.1	13.1	9.1	0.55

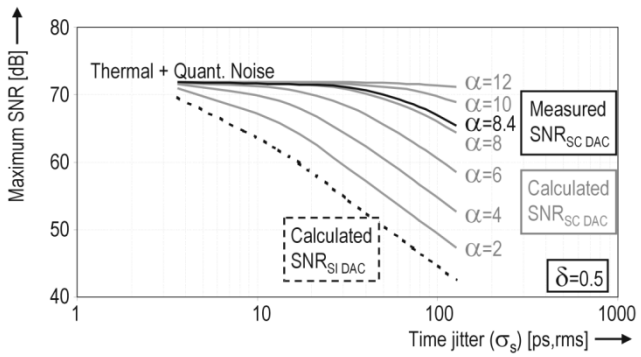


Fig. 18. Pulse width jitter measurement in the UMTS mode.

with different values for α. The measured curve is numerically mapped on the calculated curves, from which it is concluded that the α of the modulator is 8.4. This is in good agreement with the circuit simulation on the settling behavior of the SC DAC which predicted an α value of 8.

Fig. 18 also shows the maximum achievable SNR for a $\Sigma\Delta$ modulator with a switched current DAC. It can be concluded from the figure that the choice to use an SC feedback DAC is valid.

The performance of the modulator presented is summarized in Table II.

VI. CONCLUSION

A quadrature fifth-order 1-bit modulator has been presented that combines the advantages of low-jitter sensitivity of SC $\Sigma\Delta$ modulators and high anti-alias suppression of continuous-time $\Sigma\Delta$ modulators. The combination effectively reduces the influence of pulse width jitter on the dynamic range. The I and Q modulators together achieve a dynamic range of 92/83/72 dB in a bandwidth of 200/1228/3840 kHz. The measured IM2 and IM3 distances are better than 87 dB and the IR performance is limited to 50 dB by the measurement setup. This low-power high-resolution triple-mode modulator reduces the amount of prefiltering and AGC required in front of the ADC and thus enables a low-cost highly integrated receiver for telecom applications.

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Robert H. M. van Veldhoven was born in Eindhoven, The Netherlands, in 1972. He received the B.Sc. degree from the Eindhoven Polytechnical College, Eindhoven, in 1996, and the M.Sc. degree from the Eindhoven University of Technology, Eindhoven, in 2002, both in electrical engineering.

In 1996, he joined the Mixed-Signal Circuits and Systems group at Philips Research Laboratories, Eindhoven, where he worked on the design of high-resolution analog-to-digital and digital-to-anlaog converters and associated circuits for instrumentation, audio, and radio applications.