IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received January 15, 2019, accepted January 26, 2019, date of publication January 31, 2019, date of current version February 20, 2019.

Digital Object Identifier 10.1109/ACCESS.2019.2896756

A Triple-Mode Performance-Optimized Reconfigurable Incremental ADC for Smart Sensor Applications

BYUNGJOO OH, (Student Member, IEEE), KYEONGHWAN PARK, (Student Member, IEEE), AND JAE JOON KIM, (Senior Member, IEEE)

School of Electrical and Computer Engineering, Ulsan National Institute of Science and Technology, Ulsan 44919, South Korea

Corresponding author: Jae Joon Kim (jaejoon@unist.ac.kr)

This work was supported in part by the Ministry of Trade, Industry and Energy, Republic of Korea, through the Technology Innovation Program (Development of Suspended Heterogeneous Nanostructure-Based Hazardous Gas Microsensor System), under Grant 10054548, in part by the Ministry of Science and ICT, through the 2018 R&D support project based on science and technology according to the regional demand (Development of IoT Sensors and Plant-Safety Platform Against Hazardous Substances), under Grant REDE 2018 US 001, and in part by the National Research Foundation of Korea, Ministry of Education, through the Basic Science Research Program, under Grant 2016R1D1A1B03930404.

ABSTRACT This paper proposes a triple-mode discrete-time incremental analog-to-digital converter (IADC) employing successive approximation register (SAR)-based zooming and extended counting (EC) schemes to achieve programmable trade-off capability of resolution and power consumption in various smart sensor applications. It mainly consists of an incremental delta–sigma modulator and the proposed SAR-EC sub-ADC for alternate operation of the coarse SAR conversion and EC. They can be reconfigured to operate separately depending on the application requirements. The SAR-based zooming structure allows the IADC to have better linearity and resolution, and additional activation of the EC function gives the further resolution. During this reconfigurable conversion process, pipelined reusing operation of sub-blocks reduces the silicon area and the number of cycles for target resolutions. A prototype ADC is fabricated in a 180-nm CMOS process, and its triple-mode operation of high-resolution, medium-resolution, and low-power is experimentally verified to achieve 116.1-, 109.4-, and 73.3-dB dynamic ranges, consuming 1.60, 1.26, and 0.39 mW, respectively.

INDEX TERMS Analog-to-digital converter (ADC), incremental ADC, triple-mode, SAR-based zooming, extended counting, pipeline operation.

I. INTRODUCTION

Various of sensor interfaces [1], [2] and instrumentation systems [3] require energy-efficient high-resolution analog-to-digital conversion, and incremental Δ-Σ ADCs (IADC) have been widely utilized for such applications. For instance, displacement sensor applications require high-resolution ADCs with 16-bit or more resolution to provide high accuracy in measurements, and appropriate conversion speed is also needed to support fast moving objects [4], [5]. Recent sensor systems have been equipped with artificial intelligent algorithms to cope with various situations, which necessitates a kind of reconfigurable ADCs to provide some operational flexibility in their performance characteristics such as resolution, speed, and power consumption [6], [7]. When various types of sensors with different sensitivities are used, their system performance needs to be optimized by trimming the trade-off relationship between resolution and power consumption. On the other hand, achieving high accuracy from low-sensitivity sensors requires a high-resolution ADC with large power consumption and long conversion time while power-saving system requirement necessitates low-power operation with tolerable resolution. Additionally, intermediate-resolution ADCs are also needed to optimize various situations in a variety of sensor systems.

Incremental Δ-Σ ADCs (IADCs) have two conventional ways to improve their resolution: to increase the over-sampling ratio (OSR) or to use higher-order loop

The associate editor coordinating the review of this manuscript and approving it for publication was Kai Li.

filters [8], [9]. However, the higher OSR costs relatively long conversion time, which also requires high-performance amplifiers with a greater amount of silicon area and power consumption. In comparison, the higher-order loop-filter implementation for better noise shaping effect can reduce conversion times, but its feedback loop stability degrades. Thus, the coefficients of internal integrators in the loop filter should be lowered to improve stability, which causes an increase in the OSR to achieve similar resolution performance [10]. Another way to increase the IADC resolution can be provided by adopting a multi-bit quantizer, which does not require higher-order loop filters or more OSR [11]. However, the effective ADC resolution is affected by the linearity of its accompanied multi-bit DAC, and the resulting practical implementation consumes more power consumption than that of the single-bit quantizer. To overcome these fundamental limitations, additional enhancement methods such as two-step zooming [12], [13], two-step conversion [14] and extended counting (EC) [15] have been recently reported. These methods may provide additional resolution by obtaining high-order effects from lower-order loop-filter implementations. However, a large number of conversion cycles are still required to obtain high resolution of 16 bits or more. For example, 537 cycles are required for 16-bit resolution in a second-order IADC as in [8], which leads to longer conversion time. Alternatively, this long conversion time could be effectively reduced by utilizing the pipeline operation at the cost of area and power [16], [17]. In addition, oversampling SAR ADCs [18] and noise-shaping SAR ADCs [19] have been reported to give shorter conversion times and higher resolution, but their achieved resolutions are still limited.

Many conventional sensor systems adopt excessive high-performance incremental ADCs to meet worst-case requirements [20], [21] even though their requirements on resolution and speed vary with applications or operational states. Therefore, this paper presents a triple-mode reconfigurable IADC structure to provide optimal resolution with minimal power consumption. The reconfigurable capability is achieved through a proposed triple-mode structure which selectively combines two-step zooming and extended counting, also providing a pipeline operation capability for higher conversion speed. In order to support high resolution of 16 bits or more, as required in sensor interfaces or instrumentation applications, the target resolution in this work is set to minimum 18 bits within 1 mA current.

This paper is organized as follows. Section II describes the proposed reconfigurable architecture of the IADC including its theoretical analysis and simulation results. Section III shows circuit implementation details, and then measurement results are given in Section IV. Finally, conclusions are drawn in Section V.

II. TRIPLE-MODE ADC ARCHITECTURE

A. OPERATIONAL PRINCIPLE

Fig. 1 presents a conceptual diagram of the proposed triple-mode incremental ADC. It incorporates a SAR-EC ADC

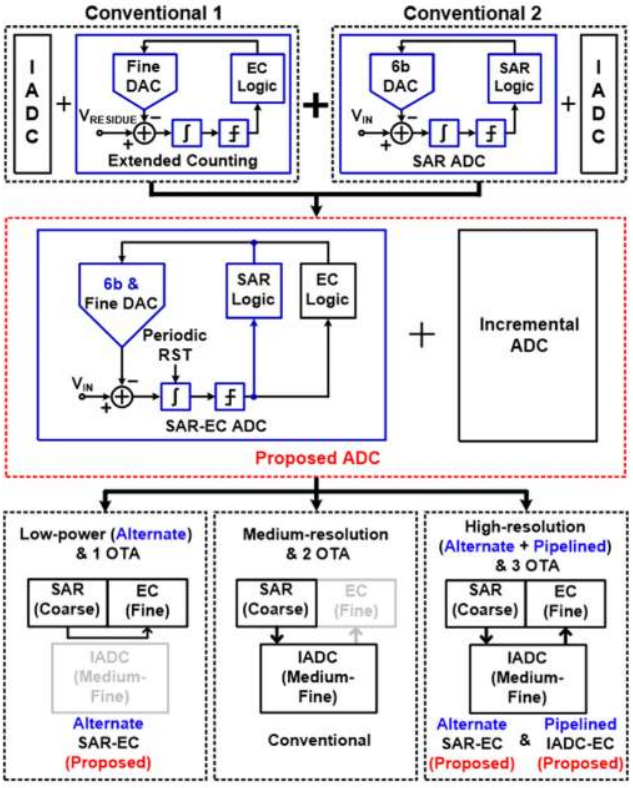


FIGURE 1. Conceptual block diagram of proposed reconfigurable IADC.

that can be used either as a coarse converter during two-step zooming, or as a fine converter during extended counting, and an incremental Δ-Σ ADC (IADC) that is used for medium-fine resolution conversions. A conventional two-step ADC achieves high resolution by using the extended counting conversion to resolve the residue remaining after an IADC conversion [15]. A two-step zooming ADC [12] uses information from a SAR ADC to limit the reference range of an IADC, thus reducing the swing of its internal integrators, and relaxing their linearity requirement. Considering that these two-step ADCs commonly consist of an IADC and an additional conversion stage, a reconfigurable architecture is proposed to include single SAR-EC ADC which can work for either two-step zooming or extended counting. Then, the proposed architecture can be configured to have three operation modes of low-power, medium-resolution and high-resolution. That is, reconfigured combination of the SAR-EC ADC and the IADC can provide the triple-mode operation. Firstly, the low-power mode is provided through alternate operation of the SAR and the extended counting by using the SAR-EC only, where the remaining residue after the SAR conversion is stored in an internal integrator and then it is reconfigured to begin the following extended counting operation. This shared integrator operation enables the alternate operation of the SAR and the extended counting. Secondly, the medium- and high-resolution modes are provided by activating the IADC with selective usage of the alternate operation of

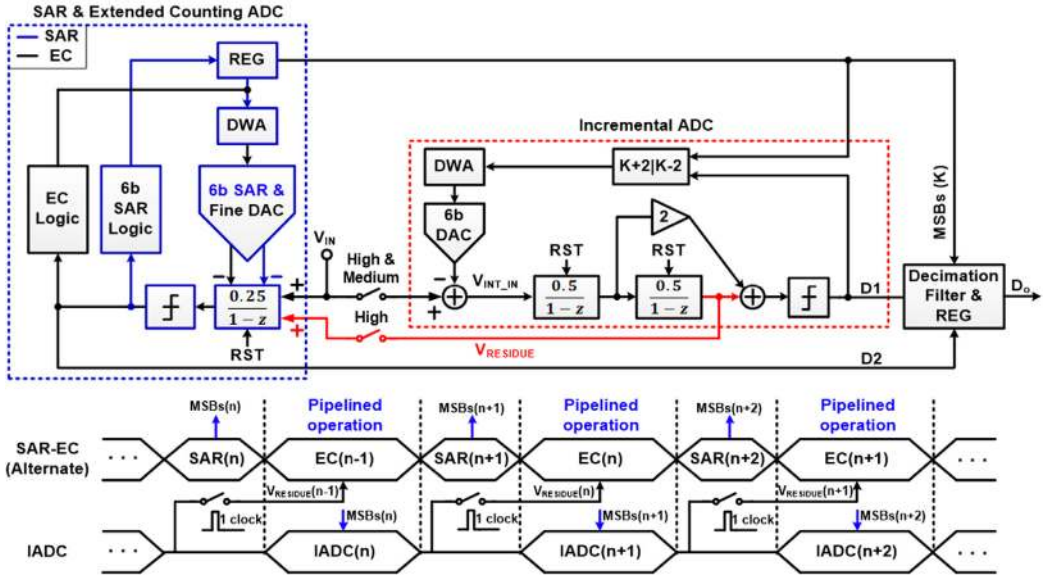


FIGURE 2. Block diagram of triple-mode reconfigurable IADC with pipelined high-resolution operation.

the SAR-EC. The medium-resolution mode is provided by two-step conversion of the SAR ADC and the IADC, and the high-resolution mode is provided by addition of the extended counting operation after the medium-mode operation. While the final residue is resolved through the extended counting operation, the IADC is designed to work on the next-cycle input's residue. It means the pipelined operation of the extended counting and the IADC, resulting in significant improvement of the overall conversion speed.

Detailed implementation of the proposed triple-mode reconfigurable IADC is shown in Fig. 2. The overall operation for the maximum resolution is as follows. First, the input V_{IN} goes through the 6-bit SAR-EC ADC, and residue V_{INT_IN} after its coarse SAR conversion is generated by subtraction with a 6-bit DAC. It passes through the following second-order IADC for medium-fine conversion, and its resulting residue $V_{RESIDUE}$, which is stored in a second integrator of IADC, enters the extended counting block for additional resolution. Then these three-step conversion outputs are assembled properly and decimated to give the final output (D_O). During this three-step conversion, the first-stage SAR operation gives 6-bit coarse conversion ($V_{SAR\_LSB} = 2V_{REF}/2^6$), and its digital output is converted into the corresponding analog voltage through the data weighted averaging (DWA) for ensuring linearity of SAR and EC operation and the 6-bit capacitive DAC ($V_{DAC} = K \cdot V_{SAR\_LSB}, 0\,K\,63$). The difference between the input signal and the DAC output, the first residue, is inserted to the following second-order IADC whose feedback DAC gives $(K - 2) \cdot V_{SAR\_LSB}$ or $(K + 2) \cdot V_{SAR\_LSB}$ depending on the single-bit quantizer output. This range setting of $\pm$ 2 is to prevent the overload in internal integrators and also to provide the redundancy for correction of possible instant errors in the previous coarse conversion.

In this proposed three-step ADC structure, the second-stage input corresponds to the remaining residue after the first-stage SAR conversion. Thus, the input range of the IADC is scaled down by 64 after the 6-bit SAR conversion, but adjusted to be scaled up by 1 bit for the redundancy utilization. For this reason, the reference voltage of the IADC is reduced by 1/16 compared to that of conventional IADCs, and the signal swing of internal integrators in the second-order IADC becomes much smaller. It can suppress nonlinearities from amplifiers significantly and relax settling requirements considerably [22]. It also allows the IADC to achieve high-resolution performance easily, resulting in power-efficient circuit design [12], [13]. The proposed IADC structure utilizes two identical 6-bit DACs, and their mismatch might affect the overall ADC performance. However, this mismatch effects can be minimized through symmetric layout, DWA, and redundancy conversion structure.

After the second-stage incremental Δ-Σ conversion, its second integrator output is utilized as the residue input for the third-stage extended counting operation. For the extended counting operation, the SAR-EC circuit is reconfigured by activating the extended counting control logic instead of the SAR control logic, and the 6-bit SAR DAC is also reconfigured as the 6-bit fine DAC. The comparator output (D2) from the extended counting operation is appropriately decimated through a decimation filter. In a conventional second-order two-step ADC [14], the second integrator remains in the hold mode to continuously provide its stored residue as the input to the next stage. However, the extended counting does not require the input holding inherently because the residue input value is estimated through the fine DAC [15]. Thanks to this advantage, as shown in the bottom of Fig. 2, the IADC can proceed to the next input $V_{IN}(n+1)$ while the extended counting works in response to $V_{RESIDUE}(n)$.

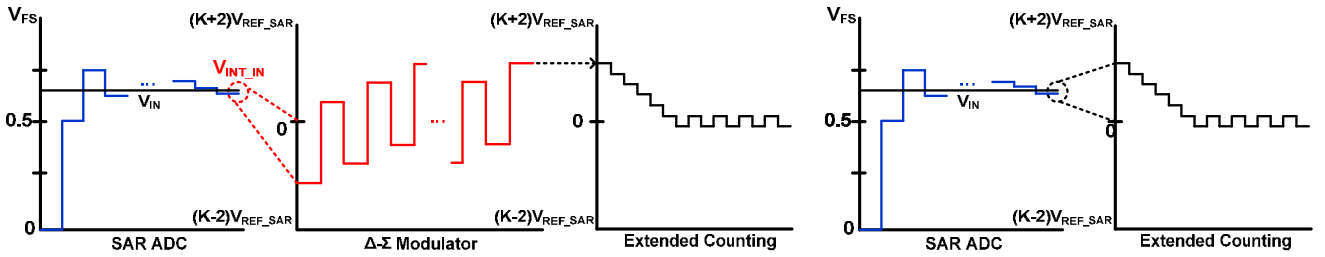


FIGURE 3. Detail operations of proposed reconfigurable IADC: (a) high-resolution mode and (b) low-power mode.

This pipelined operation of the IADC and the extended counting can improve the overall conversion speed significantly. Additionally, every sub-block for the extended counting including capacitive DACs, a comparator and an integrator is reused from the coarse SAR conversion, making additional components unnecessary. Detail operations of the proposed configuration are shown in Fig. 3, which illustrates two operational modes of the high-resolution and the low-power. The proposed reconfigurable IADC can provide the highest resolution through the full three-step conversion, where the SAR-EC ADC uses only one amplifier for lower power and relatively small integrating capacitors for higher speed.

B. BEHAVIOR ANALYSIS

In case of conventional IADCs, higher resolution requires higher OSR and higher-order loop filters, which leads to longer conversion time and lower ADC stability. To improve this fundamental trade-off limit, the proposed IADC employs the two-step zooming structure and the pipelined operation with extended counting to obtain high linearity and short conversion time. However, in order to optimize the OSR and the integrator's coefficient, theoretical modeling and analysis need to be performed together with iterative simulations [8], [23].

Therefore, a theoretical analysis has been done for the high-resolution mode configuration since the proposed IADC needs to be optimized for the maximum resolution performance. After the first-stage 6-bit SAR conversion, the remaining residue for the following IADC input is given by

$$V_{IADC\_IN}[m] = V_{IN}[m] - \left(\frac{SAR_{LSB}}{2^6}\right) 2V_{REF}, \quad (1)$$

where SAR_{LSB} is an instant digital output of the SAR conversion, V_{REF} is the reference voltage. After the SAR conversion, the following IADC is operated with 1-bit redundancy, and its internal integrators are bounded from $-V_{REF} / 2^4$ to $+ V_{REF} / 2^4$. Then, the second-stage residue which is stored in the second integrator after M1 cycles is

$$|V_{RES}[M_1]| = \left| ab \sum_{n=1}^{M_1-1} \sum_{m=1}^{n-1} \left\{ V_{IADC\_IN}[m] - \frac{D_1[m]}{2^4} V_{REF} \right\} \right| \leq \frac{V_{REF}}{2^4}, \quad (2)$$

where a and b are the coefficients of two internal integrators, D_1 is the comparator output, and M_1 is the number of cycles in the IADC. Subsequently, the extended counting process begins from the V_{RESDUE} which is stored in the second integrator. That is, V_{RESDUE} is quantized by a counting process with a fine DAC. The final residue after the extended counting, $V_{RES,EC}$ is as follows:

$$\left|V_{RES,EC}[M_2]\right| = \left| V_{RES}[M_1] - \frac{V_{REF}}{M_2 2^4} \sum_{l=1}^{M_2-1} D_2[l] \right| \leq \frac{V_{REF}}{2^4 M_2}, \quad (3)$$

where D_2 is the comparator output of the extended counting and M_2 is its number of cycles. Assuming V_{IN} is constant during one conversion cycle, the final residue is normalized as the effective quantization error (Q_e).

$$Q_e = \left| V_{IN} - \frac{SAR_{LSB}}{2^5} V_{REF} - \frac{2V_{REF}}{M_1(M_1-1)} \times \left\{ \sum_{n=1}^{M_1-1} \sum_{m=1}^{n-1} \frac{D_1[m]}{2^4} - \frac{1}{M_2 2^4} \sum_{l=1}^{M_2-1} D_2[l] \right\} \right| \leq \frac{V_{REF}}{8M_1(M_1-1)M_2 ab} \quad (4)$$

From the bounded quantization error in (4), the signal to quantization noise ratio (SQNR) is obtained, and then the effective number of bits (ENOB) is calculated from it [8]. As seen in (4), Q_e is strongly affected by M_1 and M_2, the OSR of the IADC and the extended counting. Fig. 4 depicts the performance comparison of the theoretical SQNR and the MATLAB simulation results SNR_{NOISE} for the proposed triple-mode reconfigurable ADC with respect to the ADC cycle (N), where N is set to $N = M_1 = M_2$. The MATLAB simulation environment includes non-ideal models on sampling

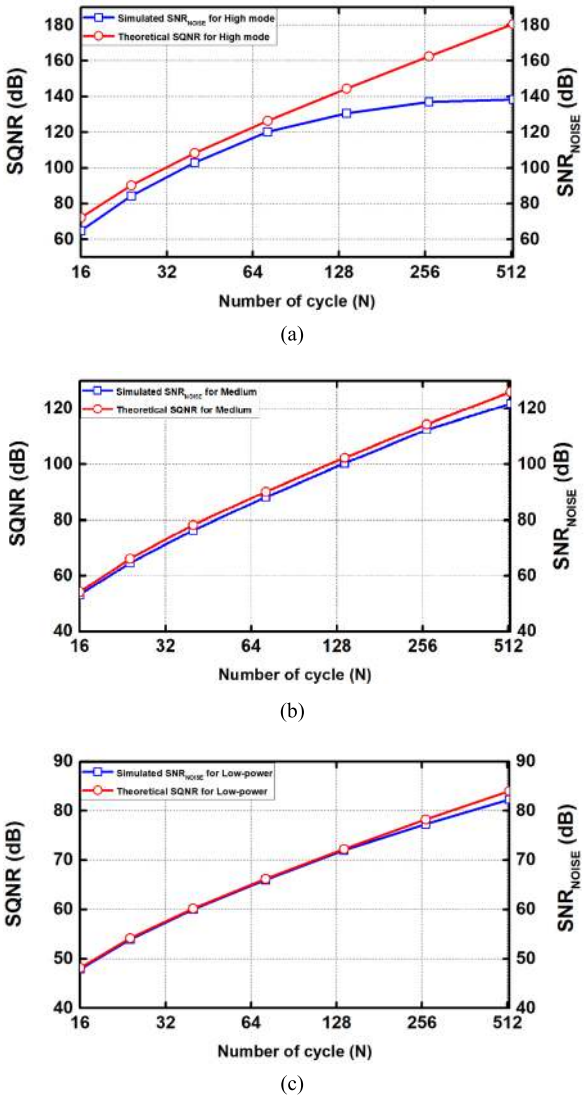


FIGURE 4. MATLAB simulation results (SNR_{NOISE}) and theoretical SQNR versus OSR of triple-mode IADC: (a) high-resolution mode, (b) medium-resolution mode, and (c) low-power mode.

jitters, circuit thermal noises, and finite amplifier gain [24], whose results show reasonable agreements with the theoretical SQNR in the low-power and the medium-resolution mode because kT/C thermal noises did not noticeably affect SNR_{NOISE} less than 120 dB. However, in the high-resolution mode, distinguished SNR_{NOISE} degradation appeared in high OSR region, which is mainly due to kT/C thermal noises in the IADC integrators. Considering this SNR_{NOISE} saturation phenomenon versus OSR and the target resolution of 18 bits, $N = 264$ is chosen in this work. The optimal coefficients of the integrators are chosen to guarantee the stability in the IADC feedback loop through iterative simulations, and it is set to 0.5. Its behavioral simulation for redundancy is also performed to depict the integrator output swings as shown in Fig. 5. In the proposed IADC where the integrator input signal is downscaled through the 6-bit SAR conversion, the integrator's theoretical full-swing voltage is 56.25 mV, but the

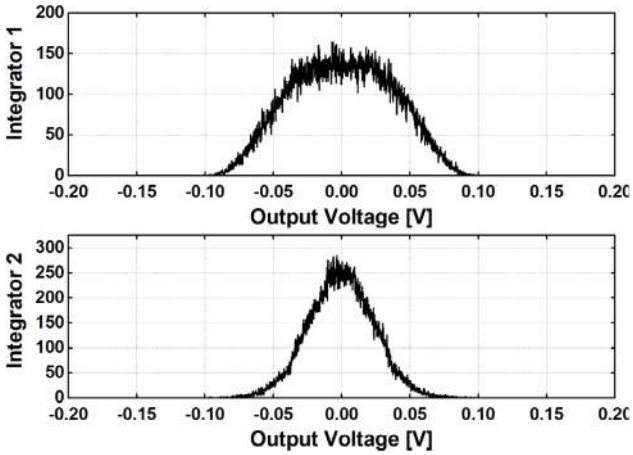


FIGURE 5. Histogram of integrator output swings in second-order IADC.

simulation has been done by using a 70-mV sinusoidal input signal for design margins. Simulated output swing range of the integrator is 103 mV and it corresponds to 5.72% of the reference voltage, which is smaller than the theoretical value of 6.25% from (2).

III. CIRCUIT IMPLEMENTAION

A. RECONFIGURABLE SAR-EC ADC

In the proposed triple-mode IADC, the reconfigurable SAR-EC ADC plays the most critical role which implements both the SAR conversion and the extended counting by replacing the control logic only. Fig. 6(a) presents a simplified single-ended circuit diagram of the proposed reconfigurable SAR-EC ADC that is implemented to be fully differential. In the coarse SAR ADC operation, an original input signal V_{in} is sampled as V_{IN} by the sample and holder (S/H) during first cycle. First, the switch S_{SAR} is turned on to activate the SAR conversion and V_{IN} is sampled by the 6-bit SAR DAC while the switch S_{RST} is turned on to reset the SAR-EC integrator. Then, the 6-bit capacitive SAR conversion is performed for the next six cycles, where the unit capacitance of the capacitive DAC is designed as 30 fF to consider target resolution and area. In case of the high-resolution mode, its conversion output is stored to a register bank and delivered to the 6-bit DAC in the IADC to generate its resulting residue input (V_{INT_IN}) for the following incremental operation. After the second-step IADC operation, the switch S_{RES} in the SAR-EC ADC was turned on to activate the third-step extended counting, receiving $V_{RESIDUE}$ from the second integrator of the IADC to the SAR DAC.

Timing diagrams for the triple-mode operation of the reconfigurable SAR-EC ADC are shown in Fig. 7. While every control signal is utilized for the high-resolution mode, the timing diagram of the medium-resolution mode shows that S_{RES}, S_{VCM1j}, S_{VCM2j}, S_{1j}, and S_{2j} are not utilized because it does not use the extended counting. In the low-power mode, $S_{SAR\_\Phi1}$ is utilized instead of S_{RES} because the residue after the coarse SAR conversion becomes the

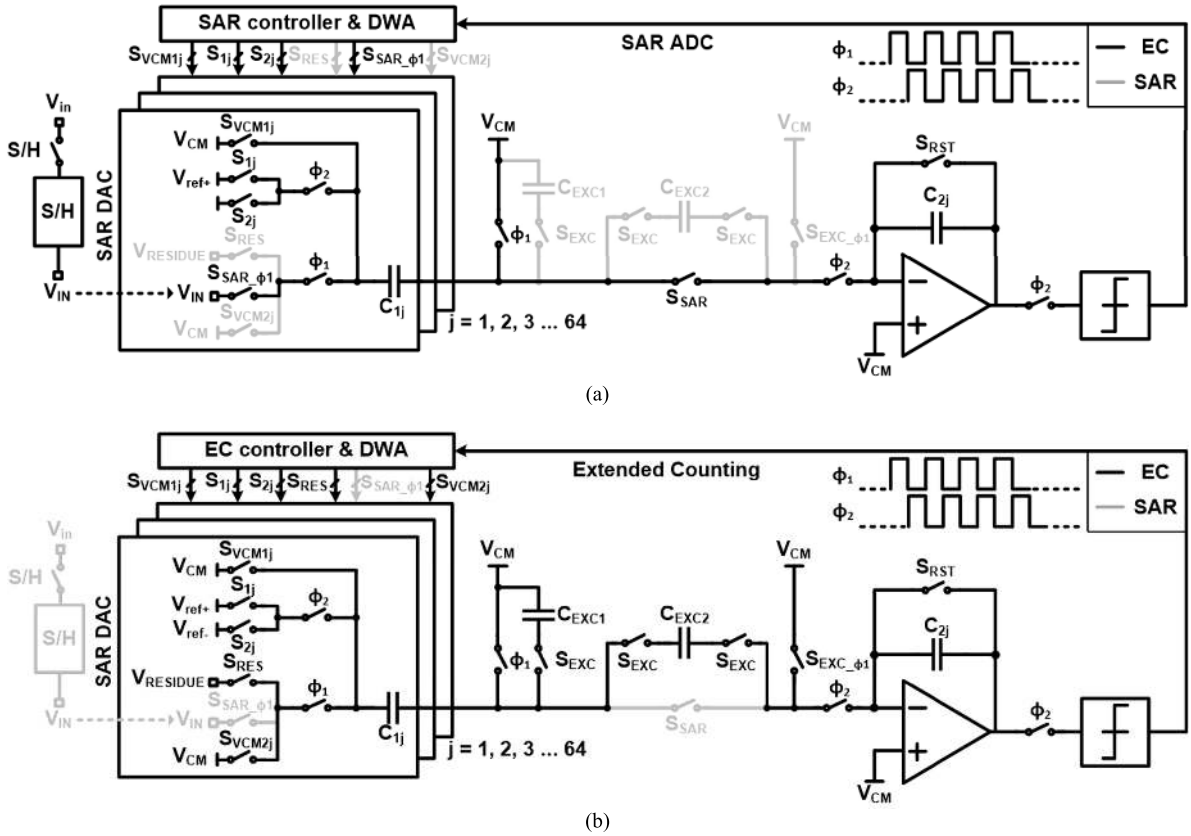


FIGURE 6. Simplified single-ended circuit diagram of fully-differential reconfigurable SAR-EC ADC. (a) coarse SAR ADC mode. (b) extended counting mode.

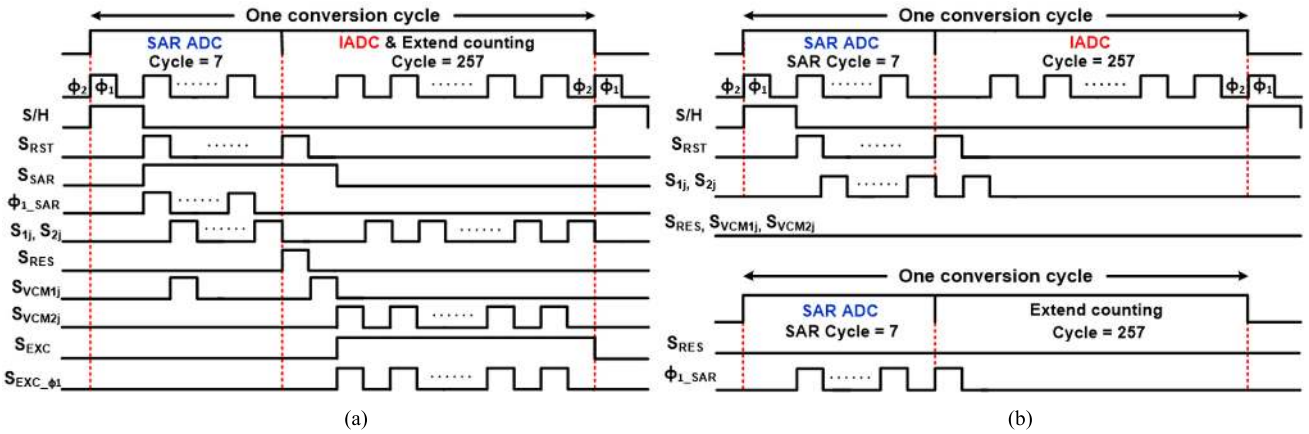


FIGURE 7. Clock timing diagram of reconfigurable coarse SAR-EC ADC: (a) high-resolution mode, (b) medium-resolution and low-power mode.

input of the extended counting, instead of the IADC's residue $V_{RESIDUE}$.

This integrator-based implementation of the reconfigurable SAR-EC ADC causes limited input swing range during the SAR conversion because the integrator amplifier's linearity degrades as the input swing becomes close to rail-to-rail voltage range, especially at its MSB conversion. To overcome this problem, the integrator output is designed to be periodically reset every sampling phase Φ_1. Even though the integrator swing becomes close to rail-to-rail, the following comparator work correctly and the next- cycle residue is designed to be regenerated from the updated SAR DAC and the S/H output V_{IN}. As a result, the effect of distortion and nonlinearity due to the swing range limitation is eliminated by utilizing this periodic reset structure, which makes the ADC output closer to the ideal.

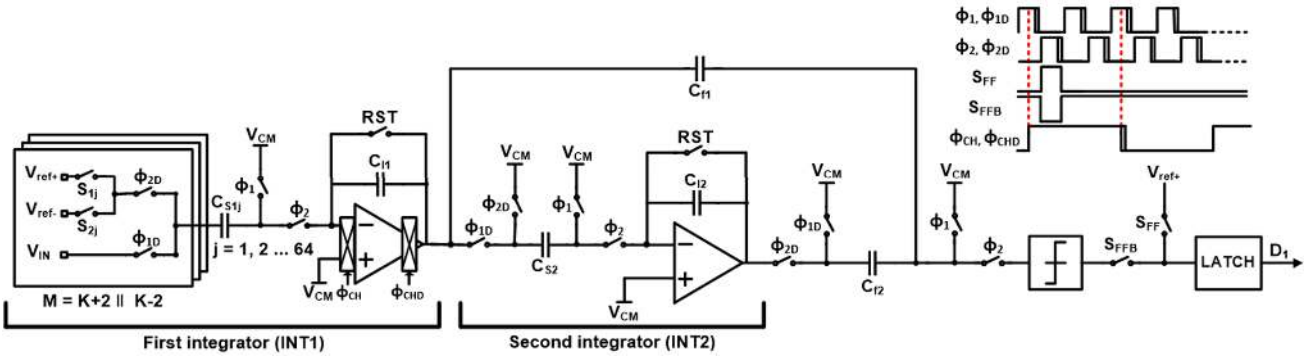


FIGURE 8. Simplified single-ended circuit diagram of fully-differential second-stage IADC.

For the extended counting operation of the SAR-EC ADC, every sub-block for the coarse SAR ADC mode are reused to constitute a kind of counting operation for further resolution. In case of the high-resolution mode, the extended counting is performed based on the residue information stored in the second integrator in the second-stage IADC. As shown in Fig. 6(b), the switches S_{EXC} and $S_{EXC\_\Phi1}$ are turned on to form a capacitive T-network [25] to generate the unit counting step of $V_{REF}/\ 2^4M_2$ in (3). The capacitive T-network allows the charge stored in the capacitors C_{1j} to be distributed by capacitor C_{EXC1} and C_{EXC2}, and less charge is transferred to the capacitors C_{2j}, which generates a smaller integrator coefficient. Since the residue input needs to be integrated one time in the extended counting, the switch S_{RES} is turned on only for one cycle, and for the remaining counting cycles the switch S_{VCM2} is turned on instead. During each cycle, S_{1j}, S_{2j} are selectively turned on according to the comparator output, and thereby the integrator output is reduced or increased by $V_{REF}/\ 2^4M_2$. As this counting process continues, the integrator output will be settled around the common-mode voltage.

The capacitive T-network in the extended counting requires very small capacitance, and it is implemented by connecting C_{EXC1} (1.86 pF) and C_{EXC2} (30 fF) in series with the 6-bit capacitive DAC. In a conventional extended counting works [15], the size of the sampling capacitor was reduced to obtain a small integrator coefficient, and this may cause a reduction of SNR due to kT/C noise. However, the proposed extended counting samples the input by utilizing the capacitive DAC, and the required counting resolution is achieved by activating the T-network to implement small capacitance. Therefore, this proposed structure can reduce the kT/C noise effect because it utilizes much bigger sampling capacitance from the DAC.

B. INCREMENTAL Σ-Δ MODULATOR

A simplified single-ended circuit diagram of the second-stage IADC is shown in Fig. 8, where it is implemented to have a second-order structure for sufficient resolution with relatively fast conversion time. To obtain high linearity, a feedforward structure is employed to reduce the signal swing of the integrator. Initially, the second-stage IADC is idle during the 6-bit coarse SAR conversion of the first-stage SAR-EC ADC. After this coarse conversion, the IADC performs second-step conversion based on the SAR residue. In the meanwhile, the SAR-EC performs the extended counting process for the previous input based on the previous IADC residue. For this pipelined operation, the IADC should be designed to deliver current residue in the second integrator to the extended counting before starting the reset function for the next conversion procedure. Subsequently, the next input is charged to sampling capacitors C_{S1j} ($j = 1, 2, 3 \ldots 64$) during sampling phase Φ_1, and the feedback DAC output is reflected as K+2 or K−2, depending on the comparator output during integration phase Φ_2.

The sum of the sampling capacitors C_{S1j} in the first integrator INT1 is designed as 8.32 pF to meet the target resolution. Since the coefficient of the integrator is set to 0.5 as in the section II, the first integrator capacitor C_{I1} is designed as 16.64 pF, two times of C_{S1}. To further improve the SNR, flicker noises are reduced by adopting the chopper stabilization technique [26] inside the first integrator. The chopper operates at midpoint of the Φ_1 period to prevent additional sampling noises [27]. The chopping frequency is set at 1/4 times the sampling frequency, whose timing diagram is shown at the top right of Fig. 8. Since the contribution of the second integrator to the overall noise performance is relatively small, its sampling capacitor (C_{S2}) and integrator capacitor (C_{I2}) are greatly reduced and designed as 0.5 pF and 1 pF, respectively.

The first-step SAR conversion reduces the input range of the following IADC, and the IADC integrators' output swing is also much reduced. Therefore, the integrator amplifier utilized the folded cascode structure which is easy to obtain low noise, sufficient phase margin, and high DC gain. Fig. 9 shows its circuit implementation, where rail-to-rail input range is supported for stable ADC operation to easily recover instant fluctuations in the integrator. The dynamic bias used in the PMOS cascade stage of the amplifier can easily create the bias voltage because the voltage head room is relatively small, and it has immunity to PVT variation through the negative feedback. The amplifier DC gain has significant impact on IADC performances. Therefore, a simulation

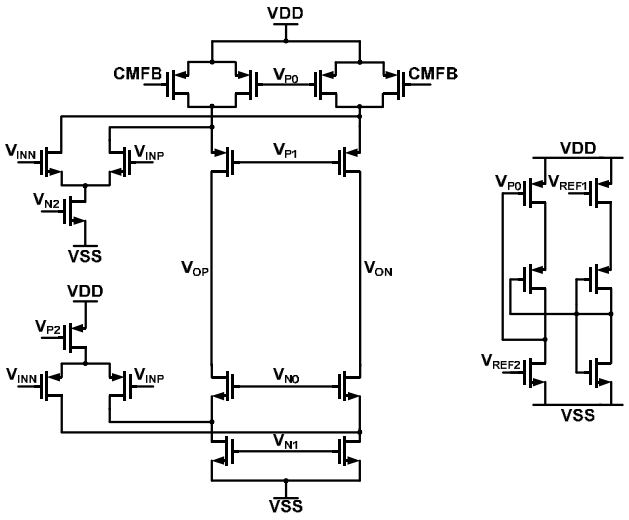


FIGURE 9. Circuit diagram of amplifier and bias in the integrator.

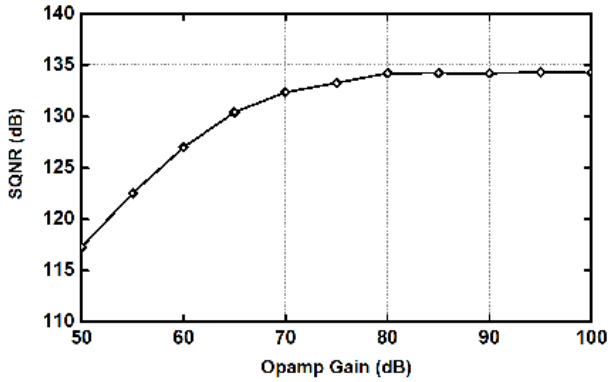


FIGURE 10. Simulated SQNR versus op-amp DC gain.

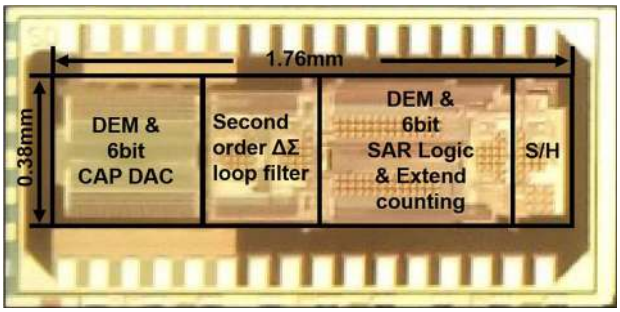


FIGURE 11. Chip micrograph.

analysis with respect to the DC gain is performed as shown in Fig. 10. The simulated SQNR of the proposed reconfigurable IADC in the high-resolution mode is almost constant beyond 80 dB DC gain, and the amplifier DC gain is designed to be 89 dB for some margin.

IV. MEASUREMENT RESULTS

The proposed triple-mode IADC prototype was fabricated in a 0.180 nm CMOS process with core area of 1.67 mm × 0.38 mm as shown in Fig. 11, where all the core components for the coarse SAR ADC, the IADC, and the extended counting are integrated together, excluding the decimation filter. The supply voltage was 1.8 V and a clock frequency of 3.33 MHz was used for this ADC prototype. A common-mode voltage of 0.9 V was used, and the full-scale range of the differential input is 3.44 V_{PP}. The low-power mode consumes 0.39 mW for 10 kHz bandwidth, and the high-resolution mode consumes 1.60 mW for 6.3 kHz bandwidth.

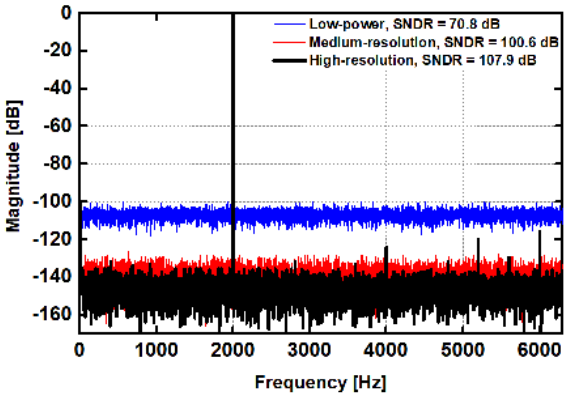


FIGURE 12. Measured output spectrums for the triple-mode.

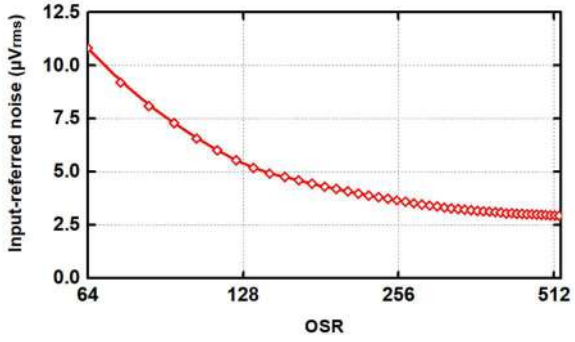


FIGURE 13. Measured input-referred noise versus OSR.

Fig. 12 shows the measured single-sided output power spectral densities (PSDs) for the triple-mode operation with a −1.1 dBFS, and 2-kHz sinusoidal differential input. The measured SNDRs of a high-resolution, medium-resolution, and low-power mode for the bandwidth of 6.3 kHz are 107.9 dB, 100.6 dB, and 70.8 dB, respectively. The output spectrum indicates that the spurious-free dynamic range of the high-resolution mode is 116.1 dB, which is limited by the third-order harmonic. The measured input-referred noise of the high-resolution mode with respect to the OSR is shown in Fig. 13. The input-referred noise is greatly reduced with increments of the OSR at the beginning. However, around OSR = 300, the reduction rate of the input-referred noise is gradually saturated, which is mainly limited by circuit thermal noises. At OSR = 264, the input-referred noise is approximately 3.6 μV, which is reasonable in comparison with the measured SNDR.

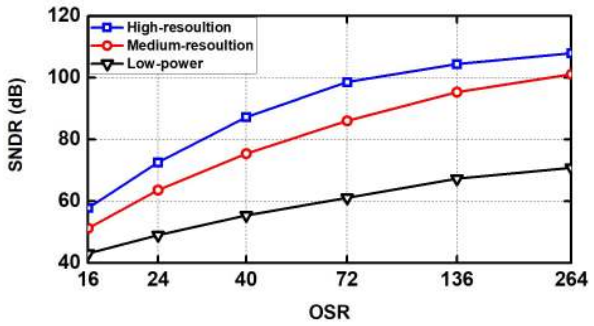


FIGURE 14. Measured SNDR for the triple-mode versus OSR.

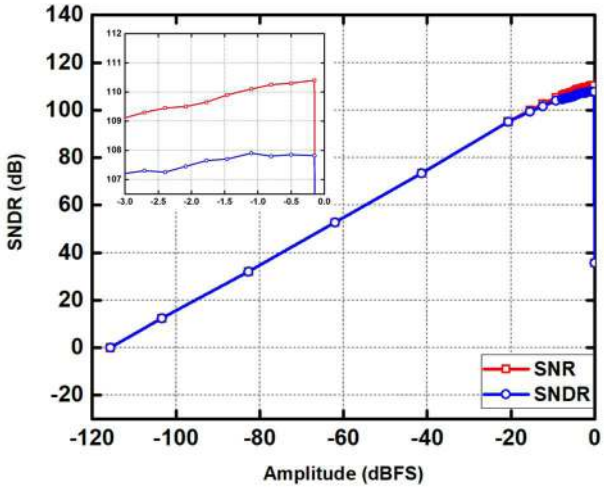


FIGURE 15. Measured SNR and SNDR versus the input amplitude for high-resolution mode.

The measured SNDR for the proposed triple mode with respect to the OSR is shown in Fig. 14. This means that the proposed reconfigurable IADC provide the dynamic performance required in high-bandwidth smart sensor applications by changing the OSR in each mode. The SNDR increasing rate of the low-power mode is similar to the ideal case. Meanwhile, in the high-resolution and medium-resolution modes, the enhancing rate of the SNDR decreases as the OSR increases. This degradation is supposed to be caused by increment of noise floor mainly due to non-ideal measurement environments including limited quality of signal source and non-ideal sample/hold circuit. The proposed reconfigurable IADC also provide the dynamic performance required in high-bandwidth smart sensor applications by modifying the OSR of each mode. The measured plots of SNR, SNDR, and DR versus the input amplitude for the high-resolution mode are shown in Fig. 15. Thanks to the first-stage SAR ADC mode that can receive an input signal close to the reference voltage, a triple-mode IADC has an input range close to twice the reference voltage, resulting in a relatively large DR. When the input signal amplitude approaches the reference voltage, the feedback in the IADC does not provide a value corresponding to K + 2, and the IADC operation becomes unstable, resulting in a drastic corruption of the SNR and SNDR. The measured SNDR, SNR, and DR were 107.9 dB, 110.4 dB, and 116.1 dB, respectively.

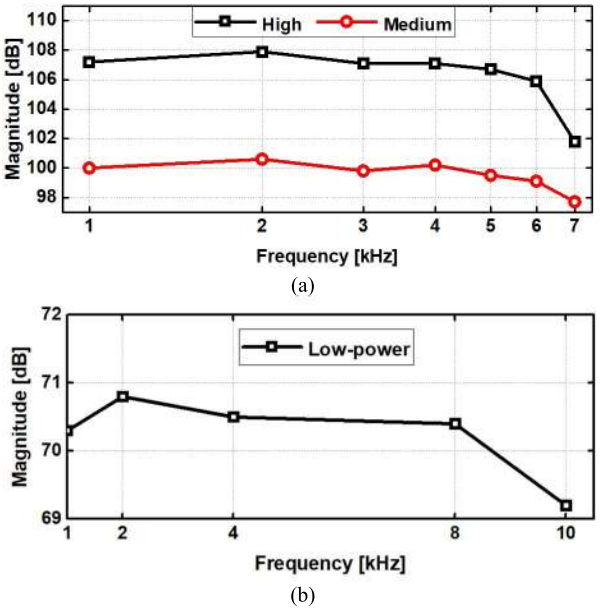


FIGURE 16. Measured SNDR over input signal frequency for triple-mode.

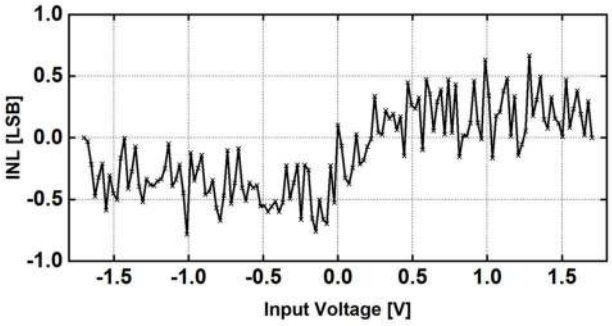


FIGURE 17. Measured INL with DWA turned on for 264 cycles in 18b accuracy LSBs.

Fig. 16 shows the SNDR over the input signal in-band frequency for the triple-mode. Due to the increase of the noise floor in the out-of-band mentioned by other reported zoom ADCs [28] and the insufficient settling time of the IADC, the SNDR of a high and medium-resolution mode are decreased at frequencies above about 6 kHz. However, the low-power mode has a much wider bandwidth than the other modes because it is operated by the SAR-EC structure with a relatively small integrator capacitor and T-network, which reduces the settling time required for stable operation. Fig. 17 presents the measured Integral Non-Linearity (INL) with DWA turned on for 264 cycles in 18b accuracy LSBs. A DAC with a 20-bit effective number of bits (ENOB) was used to measure the high resolution corresponding to the

TABLE 1. Performance summary and comparison with other recent work.

Parameter	This work			[13]	[14]	[15]	[29]	[30]	[31]	[32]	[33]	[34]
Architecture	Zoom ADC+ EC	Zoom ADC	SAR +EC	Zoom ADC	IADC2 +IADC1	IADC1 +Multi Slope	SAR+ IADC1	IADC1 +SAR	IADC2 +SAR	IADC2	Zoom ADC	Flexible SAR
Process [nm]	180			180	65	160	600	180	180	160	160	90
Area [㎟]	0.64			0.3	0.20	0.5	1.64	0.27	3.5	0.45	0.25	0.047
Supply Voltage [V]	1.8			1.4	1.2	1.5	3.3	1.5	1.38	1.0	1.8	0.7
MODE	High	Medium	Low	-	-	-	-	-	-	-	-	7~10 bit
Power [W] (digital)	1.60 m (0.15)	1.26 m (0.09)	0.39 m (0.13)	33.7 μ	10.7 μ	34.6 μ	64 μ	33.2 μ	38 m	20 μ	280 μ	1.6~3.6 μ
Sampling Freq. [Hz]	3.33 M			137 k	96 k	642 k	5 M	642 k	45.2 M	750 k	2 M	22 M
Input range [$V_{PP,diff}$]	3.44			-	2.2	2	2	2	2	0.7	-	0.9
BW [Hz]	6.30 k		10k	2.17k	250	1 k	9.75 k	1.2 k	1 M	666	1 k	1 M
Peak SNDR [dB]	107.9	100.6	70.8	-	90.8	96.8	70.7	96.6	86.3	81.9	118.1	57.8
SNR_{max} [dB]	110.4	102.9	71.6	94.7	97.0	98.4	-	97.1	89.1	-	119.1	-
DR [dB]	116.1	109.4	73.3	-	99.8	99.7	84.6	100.2	90.1	81.9	120.3	-
FoM_S †[dB]	182.1	176.4	147.4	172.8††	173.5	174.6	166.4	175.8	164.3	157.1	185.8	172.3†††

† $FoM_S = DR + 10\times\log_{10}$(Signal bandwidth/Power)
†† $FoM_S = SNR_{max} + 10\times\log_{10}$(Signal bandwidth/Power)
††† $FoM_S = SNDR_{max} + 10\times\log_{10}$(Signal bandwidth/Power)

18-bit ENOB and the measured INL was found to be between 0.67 LSB and −0.79 LSB.

The measurement results are summarized in Table 1, which also includes a comparison with other recent work. The IADC prototype achieved 182.1 dB figure of merit (FoM) in the high-resolution mode, which is comparable to recent records. Through the proposed triple-mode reconfigurable structure, the effective resolution of the IADC can be adjusted from 11 bits to 18 bits depending on application requirements while its power consumption is optimally minimized.

V. CONCLUSION

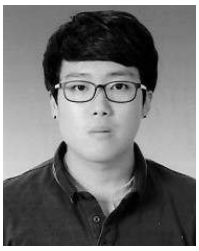
This paper presented a reconfigurable IADC with triple-mode operation of low-power, medium-resolution, and high-resolution. It was enabled by selective combination of the SAR-assisted two-step zooming and the extended counting Its chip prototype experimentally verified the effectiveness of the proposed reconfigurable operation, providing the peak SDNR of 107.9 dB with competitive FoM of 182.1 dB. During monitoring or idle operation of sensory systems, power consumption can be minimized through the low-power mode. After target detection, it may switch to the high- or medium-resolution modes for quantitative analysis. In this way, the proposed reconfigurable ADC could provide optimally programmable tradeoffs between resolution and power consumption.

REFERENCES

[1] S. Choi *et al.*, "A multisensor mobile interface for industrial environment and healthcare monitoring," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2344–2352, Mar. 2017.
[2] S.-W. Kim *et al.*, "A triple-mode flexible E-skin sensor interface for multi-purpose wearable applications," *Sensors*, vol. 18, no. 1, p. 78, Jan. 2018. doi: 10.3390/s18010078.
[3] D. Placko, *Fundamentals of Instrumentation and Measurement*. New York, NY, USA: Wiley, 2007.
[4] A. Fekri, M. Nabavi, N. C. Radeljić-Jakić, Z.-Y. Chang, M. Pertijs, and S. Nihtianov, "An eddy-current displacement-to-digital converter based on a ratio-metric delta-sigma ADC," in *Proc. Eur. Solid State Circuits Conf.*, Venice, Italy, Sep. 2014, pp. 403–406.
[5] S. Rana, B. George, and V. J. Kumar, "Sigma–delta digital converter suitable for a resistive displacement sensor with a floating slide," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 3, pp. 502–509, Mar. 2016.
[6] M. Yip and A. P. Chandrakasan, "A resolution-reconfigurable 5-to-10-bit 0.4-to-1 V power scalable SAR ADC for sensor applications," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1453–1464, Jun. 2013.
[7] K. Park, S. M. Kim, W.-J. Eom, and J. J. Kim, "A reconfigurable readout integrated circuit for heterogeneous display-based multi-sensor systems," *Sensors*, vol. 17, no. 4, p. 759, Apr. 2017. doi: 10.3390/s17040759.
[8] J. Markus, J. Silva, and G. C. Temes, "Theory and applications of incremental ΔΣ converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 4, pp. 678–690, Apr. 2004.
[9] M. Steiner and N. Greer, "A 22.3 b 1 kHz 12.7 mW switched-capacitor ΔΣ modulator with stacked split-steering amplifiers," in *IEEE ISSCC Dig. Tech. Papers*, Jan./Feb. 2016, pp. 284–285.
[10] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho, and A. Matsuzawa, "A fifth-order continuous-time delta-sigma modulator with single-opamp resonator," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 697–706, Apr. 2010.
[11] J.-Y. Wu, Z. Zhang, R. Subramoniam, and F. Maloberti, "A 107.4 dB SNR multi-bit sigma delta ADC with 1-PPM THD at-0.12 dB from full scale input," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3060–3066, Nov. 2009.
[12] Y. Chae, K. Souri, and K. A. A. Makinwa, "A 6.3 μW 20 bit incremental zoom-ADC with 6 ppm INL and 1 μV offset," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3019–3027, Dec. 2013.
[13] S. Oh, W. Jung, K. Yang, D. Blaauw, and D. Sylvester, "15.4 b incremental sigma-delta capacitance-to-digital converter with zoom-in 9 b asynchronous SAR," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2014, pp. 1–2.
[14] C.-H. Chen, Y. Zhang, T. He, P. Y. Chiang, and G. C. Temes, "A micropower two-step incremental analog-to-digital converter," *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1796–1808, Aug. 2015.
[15] Y. Zhang, C.-H. Chen, T. He, and G. C. Temes, "A 16 b multi-step incremental analog-to-digital converter with single-opamp multi-slope extended counting," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1066–1076, Apr. 2017.

[16] Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/S 13 b fully differential ring-amplifier-based SAR-assisted pipeline ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2015, pp. 1–3.
[17] S. Tao and A. Rusu, "A power-efficient continuous-time incremental sigma-delta ADC for neural recording systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 6, pp. 1489–1498, Jun. 2015.
[18] Y.-S. Shu, L.-T. Kuo, and T.-Y. Lo, "An oversampling SAR ADC with DAC mismatch error shaping achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Paper*, Jan./Feb. 2016, pp. 458–459.
[19] C.-C. Liu and M.-C. Huang, "A 0.46 mW 5MHz-BW 79.7 dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 466–467.
[20] R. Wu, J. H. Huijsing, and K. A. A. Makinwa, "A 21 b ±40 mV range read-out IC for bridge transducers," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 110–111.
[21] D. Strle *et al.*, "Integrated high resolution digital color light sensor in 130 nm CMOS technology," *Sensors*, vol. 15, no. 7, pp. 17786–17807, Jul. 2015.
[22] H. Park, K. Nam, D. K. Su, K. Vleugels, and B. A. Wooley, "A 0.7-V 870-μW digital-audio CMOS sigma-delta modulator," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1078–1088, Apr. 2009.
[23] J. Roh, S. Byun, Y. Choi, H. Roh, Y.-G. Kim, and J.-K. Kwon, "A 0.9-V 60-mW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 361–370, Feb. 2008.
[24] P. Malcovati, S. Brigati, F. Francesconi, F. Maloberti, and A. Baschirotto, "Behavioral modeling of switched-capacitor sigma-delta modulators," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 50, no. 3, pp. 352–364, Mar. 2003.
[25] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ, USA: IEEE Press, 2005.
[26] K. Lee *et al.*, "A wireless ExG interface for patch-type ECG holter and EMG-controlled robot hand," *Sensors*, vol. 17, no. 8, p. 1888, Aug. 2017. doi: 10.3390/s17081888.
[27] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-db 68-mw chopper-stabilized stereo multibit audio ADC in 5.62 mm^2," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2061–2068, Dec. 2003.
[28] B. Gönen, F. Sebastiano, R. van Veldhoven, and K. A. A. Makinwa, "A 1.65 mW 0.16 mm^2 dynamic zoom-ADC with 107.5 dB DR in 20 kHz BW," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 282–283.
[29] S. Ha, J. Park, Y. M. Chi, J. Viventi, J. Rogers, and G. Cauwenberghs, "85 dB dynamic range 1.2 mW 156 kS/s biopotential recording IC for high-density ECoG flexible active electrode array," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2013, pp. 141–144.
[30] Y. Zhang, C.-H. Chen, T. He, K. Sobue, K. Hamashita, and G. C. Temes, "A two-capacitor SAR-assisted multi-step incremental ADC with a single amplifier achieving 96.6 dB SNDR over 1.2 kHz BW," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Austin, TX, USA, Apr. 2017, pp. 1–4.
[31] A. Agah, K. Vleugels, P. B. Griffin, M. Ronaghi, J. D. Plummer, and B. A. Wooley, "A high-resolution low-power incremental $\Sigma\Delta$ ADC with extended range for biosensor arrays," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1099–1110, Jun. 2010.
[32] C. Chen, Z. C. Tan, and M. A. P. Pertijs, "A 1V 14b self-timed zero-crossing-based incremental $\Delta\Sigma$ ADC," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 274–275.
[33] S. Karmakar, B. Gönen, F. Sebastiano, R. V. Veldhoven, and K. A. A. Makinwa, "A 280 μW dynamic-zoom ADC with 120 dB DR and 118 dB SNDR in 1 kHz BW," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 238–239.
[34] P. Harpe, Y. Zhang, G. Dolmans, K. Philips, and H. De Groot, "A 7-to-10 b 0-to-4 MS/s flexible SAR ADC with 6.5-to-16 fJ/conversion-step," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 472–474.

BYUNGJOO OH (S'13) received the B.S. and M.S. degrees in electrical and computer engineering from Kyungpook National University, South Korea, in 2013 and 2015, respectively. He is currently pursuing the Ph.D. degree with the Ulsan National Institute of Science and Technology, South Korea, where he is investigating the CMOS analog/mixed IC design and data converters.



KYEONGHWAN PARK (S'15) was born in Yangsan, South Korea, in 1991. He received the B.S. degree in electrical and computer engineering from the Ulsan National Institute of Science and Technology, Ulsan, South Korea, in 2013, where he is currently pursuing the Ph.D. degree in electrical engineering. His research interests include data converters, in particular successive approximation register analog-to-digital converters.

JAE JOON KIM (S'96–M'03–SM'18) received the B.S. degree in electronic engineering from Hanyang University, Seoul, South Korea, in 1996, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 1998 and 2003, respectively. From 2000 to 2001, he was with Berkana Wireless, Inc., San Jose, CA, USA (now merged into Qualcomm, Inc.), where he was involved in designing wireless transceivers. From 2003 to 2005, he was with Hynix Semiconductor, Seoul, where he was involved in wireless transceivers and smart-card controllers. From 2005 to 2011, he was the Deputy Director with Ministry of Information and Communications, Korean Government, and the Ministry of Trade, Industry and Energy. From 2009 to 2011, he was a Research Engineer II with the Georgia Institute of Technology, Atlanta, GA, USA. Since 2011, he has been an Associate Professor with the Ulsan National Institute of Science and Technology, Ulsan, South Korea. His research interests include integrated circuits for various sensor systems, wireless transceivers, consumer electronics, biomedical appliances, and automotive electronics.