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# A Tutorial and Review Discussion of Modulation, Control and Tuning of High-Performance DC-DC Converters Based on Small-Signal and Large-Signal Approaches

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**ABSTRACT** Many commercial controller implementations for dc-dc converters are based on pulse-width modulation (PWM) and small-signal analysis. Increasing switching frequencies, linked in part to wide bandgap devices, provide the opportunity to increase operating bandwidth and enhance performance. Fast processors and digital signal processing offer new computational techniques for power converter control. Conventional control techniques rarely make full use of operating capability. The objectives of this paper are to present an overview and link to literature on conventional modulation and control techniques for hard-switched dc-dc converters, identify performance limits associated with conventional small-signal-based design, discuss geometric control approaches, and compare strategies for control tuning. The discussion shows how current mode controls have alternative state feedback implementations, and describes unusual opportunities for large-signal control tuning. Considerations for minimum response time are described. Comparisons among tuning methods illustrate how geometric controls can achieve order of magnitude dynamic performance increases. The paper is intended as a baseline tutorial reference for future work on power converter control.

**INDEX TERMS** Current mode control, dc-dc converters, feedback control, feedback tuning, fixed frequency pulse-width modulation, sliding mode control, switching boundary control, time optimal control, variable frequency modulation.

## I. INTRODUCTION

This paper seeks to review control and modulation methods for dc-dc switching power converters, as well as approaches for controller tuning. Most controllers use sawtooth-based pulse-width modulation (PWM) and small-signal-based feedback controls, but this paper explores a wider range and extends into large-signal approaches. The emergence of fast wide bandgap switches, combined with continuing advances in digital signal processing and sensors, motivates faster, more sophisticated controls. The emphasis here is on high-performance converters — a growing market segment.

In this review, converter topology acts as a control constraint. In concept, the right constraints allow a given control method to work with many circuits. One example is the converter output objective. Digital electronics usually seek tight load voltage regulation. LED lighting motivates current-regulated loads. Battery chargers usually employ both voltage and current regulation modes. Digital loads, and dc sources and loads in microgrids, benefit from droop relationships. The review addresses non-isolated buck and boost converters, but there is no loss of generality, and methods can be applied across dc-dc converter families. The coverage emphasizes

**TABLE 1. Converter Objectives With Control Implications**

| *Type of objective* | *Typical examples* | *Related examples* | *Additional examples* |
|---|---|---|---|
| **Static operation** | Output voltage value<br>Output voltage tolerance band<br>Output impedance | Voltage regulation<br>Load/line regulation<br>Ripple limits, percentage error | Power range<br>Temperature effects<br>Dynamic voltage scaling |
| **Dynamic operation** | Response to step changes<br>Load current slew rate<br>Audio susceptibility | Rise time, settling time<br>Peak overshoot/undershoot<br>Disturbance rejection | Start-up time<br>Phase margin, gain margin<br>Control bandwidth |
| **Operating requirements** | FCC radiated EMI rules<br>Input current THD, efficiency | Power-up sequencing,<br>Interactive redundancy | Hot plugging<br>Light load efficiency |
| **Fault management and protection** | Current limit or foldback<br>Thermal protection | Inrush/start-up current limit<br>Packaging and cooling methods | Mean time to failure<br>Recovery time |

hard-switched converters. New results linked to state feedback control and large-signal tuning are included.

Controls for dc-dc converters must address at least four types of objectives, summarized in Table 1. These include static and dynamic operating requirements. Other operating requirements such as electromagnetic interference (EMI), efficiency, and reliability are not always associated with control. Fault management and protection requirements are usually addressed separately. Many requirements in Table 1 seem independent, but some large-signal controllers can manage them directly. The full set of requirements represented by Table 1 is linked to converter design. Slew rate limits and ripple bands are determined by inductor and capacitor choices. EMI is linked to parasitics and influenced by layout. Even so, it is possible in principle to define a cost function $J(x)$ linked to all operating variables and parameters in a converter, such that

$$J(x) = \sum_{i=1}^{N} \alpha_i f_i(x), \tag{1}$$

where functions $f_i(x)$ are various functions of the variables $x$ and parameters, and $\alpha_i$ are weights. Examples include RMS currents and fluxes (linked to losses), output voltage error and ripple, load current rise time, peak device voltage stresses, peak junction temperature, switching frequency variation, and so on. In [1], multi-objective optimization of power converters is formulated as a geometric program, a type of convex optimization problem, in which multiple operating points, converter topologies, and components can be considered. Thermal management and electromagnetic effects also can be embedded in the electrical design for optimizing power density of dc-dc converters [2]. A performance index, the opposite of a cost function, could have been defined similarly. The cost function is to be minimized, and a design or control problem can be formulated into an optimization problem.

Consider the basic converters shown in Fig. 1, which could include synchronous operation. The dc-dc converter control problem can be conceptualized at a high level. In the broadest sense, the question is: Given a cost function (1) that reflects specifications of a converter, and given suitable design choices and layout, find a set of turn-on times and turn-off times for switches $S_1$ and $S_2$ that minimizes the cost function. This

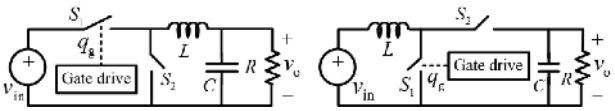


**FIGURE 1. Dc-dc buck converter (left) and boost converter (right).**

control optimization problem is distinct from the circuit design optimization problem [3], because here we seek to get the best performance from a given converter.

The timing problem, although easy to pose, is not tractable in general. It might be possible to solve for simple converters given simplified specifications. However, as specification details and uncertainty are added, the problem grows in complexity. It does motivate certain approaches. Trajectory-based controls [4], [5], seek to change the timing problem into a state-variable formulation. In constrained time optimal control [6], [7], [8], the question of when to switch for fastest rejection of a step load change, given constraints on a converter and its operation, is posed and solved. Prior work on fast response used separate circuits such as clamps [9]. In [10], [11], even faster disturbance rejection is obtained by altering a converter with additional switches and devices. An alternative based on steering inductor energy was presented in [12]. Other efforts are discussed in Section VI.

Since the generic switch timing problem is intractable, a designer must settle for accessible approaches. Typically, this imposes at least two constraints beyond those in Table 1:

1) The converter operating regimes are constrained. A classic example is to enforce a fixed switching frequency.
2) A simplified model of the converter is used as the basis for control design and operation. A classic example is to use a small-signal linearization of an averaged model.

The first of these limits timing flexibility, turning the problem into a cycle-by-cycle duty ratio. The second gives rise to *model limited control*, in which the full dynamic capabilities of the converter might not be attainable.

Fig. 2 shows the block diagram of a basic feedback and feedforward buck converter control system. The feedback sensing block is band limited to avoid ripple effects. For digital control, additional signal conditioning and

**TABLE 2. Parameter Set for dc-dc Buck and Boost Converters**

| Converter | Input Voltage | Output Voltage | Inductor | Capacitor | Switching Frequency | Load current |
|---|---|---|---|---|---|---|
| Buck converter | 12 V | 3.3 V | 10 $\mu$H | 470 $\mu$F | 200 kHz | 1 to 20 A |
| Boost converter | 8 V | 12 V | 4 $\mu$H | 150 $\mu$F | 500 kHz | 0.5 to 5 A |

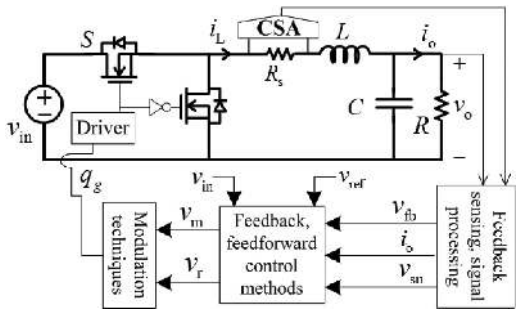


**FIGURE 2. Feedback control of a buck converter: $v_{in}$ and $v_o$ are the input and output voltages; $v_{fb}$, $v_{ref}$, and $v_{sn}$ are the feedback voltage, reference voltage, and voltage associated with the sensed inductor current, respectively; $v_m$ and $v_r$ are the modulating and ramp signals; $q_g$ is the gate signal for the controllable MOSFET $S$; "CSA" represents a current sense amplifier.**

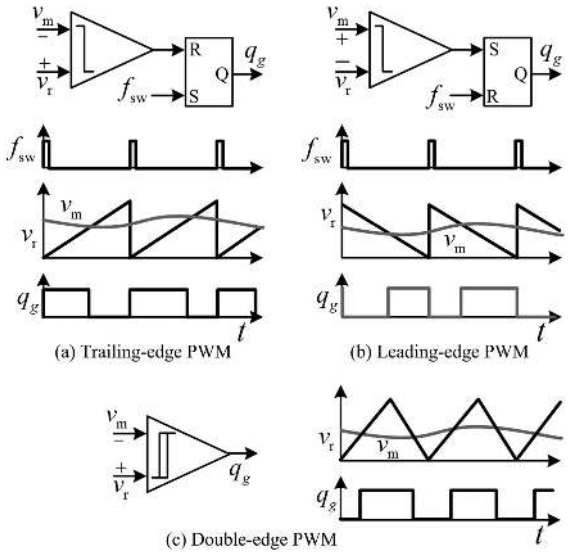


**FIGURE 3. Three PWM carriers for dc-dc converters.**

analog-to-digital converters (ADCs) are needed. Output feedback is required for precise output regulation or tracking. Inductor current feedback can be used for control or for current-regulated loads. A converter can be controlled using output feedback or state feedback. Feedforward action, using input voltage, load current, or other information, can reduce audio susceptibility or output impedance, or provide better disturbance rejection. The controller drives a modulator to generate gate signal $q_g$ for the controllable switch. In a boost converter, the modulator requires a limiter function.

Table 2 provides a set of converter design parameters that will be used here for simulation and comparison. These converters have been built and are used here for experimental testing as well.

The discussion is organized as follows. Section II presents an overview of various modulation techniques and shows how they differ in operation. Control methods based on feedback interconnections such as in Fig. 2 are discussed in Section III. Various large-signal and small-signal modeling techniques along with the associated dynamics of PWM dc-dc converters are presented in Section IV. Small-signal control and tuning methods are summarized in Section V. Section VI presents large-signal control and tuning methods. Section VII presents a comparative performance analysis using small-signal and large-signal approaches along with some design case studies. This includes experimental validation of the work. Section VIII concludes the paper.

## II. CONTROL TECHNIQUES BASED ON FUNDAMENTAL MODULATION PRINCIPLES

### A. FIXED FREQUENCY PWM

In a typical converter, the combination of a carrier signal at fixed frequency $f_{sw}$, comparator, and latch implement gate signal $q_g$ of the controllable switch. For synchronous operation or bidirectional current, the other switch would be in complement to $q_g$ except for a dead time. As shown in Fig. 3, a rising sawtooth, falling sawtooth, or triangle $v_r(t)$ can be used as the carrier, and the comparator can set or reset the latch based on modulation signal $v_m(t)$. Fixed $f_{sw}$ can be enforced with a clock signal. The latch should be reset dominant in Fig. 3(a) (otherwise 0% duty cycle is avoided) and set dominant for Fig. 3(b) (otherwise 100% duty cycle is avoided). The latch prevents "double-pulsing," as the switch can act only once per cycle. Without it, the control can produce chaotic operation [13], [14], [15]. The rising sawtooth produces *trailing-edge* modulation. The falling sawtooth produces *leading-edge* modulation. The triangle produces *double-edge* modulation. Double-edge modulation corresponds to naturally sampled PWM. It has technical advantages in time-domain performance that are helpful in precision applications such as class-D audio amplifiers [16]. Trailing-edge modulation can impose a time delay $t_d$ up to $(1-D)T$, where $D$ is the active switch duty ratio and $T = 1/f_{sw}$, to respond to a step-up transient. For leading-edge modulation, $t_d$ can be up to $DT$ during a step-down transient.

The delay distinctions of leading-edge and trailing-edge modulation have been employed to alter phase behavior of closed-loop controllers. In [17], leading-edge modulation phase characteristics tend to compensate for non-minimum phase dynamics. The effect is not really general, and more detail is provided in [18]. As shown there, combinations of

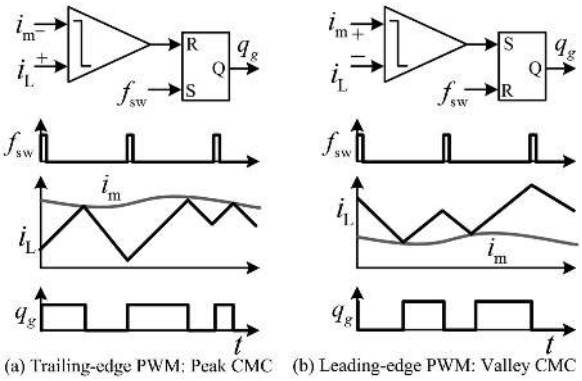


**FIGURE 4.** Two PWM current mode control techniques.

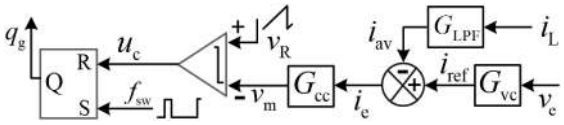

**FIGURE 5.** Block diagram of average CMC under trailing edge PWM.

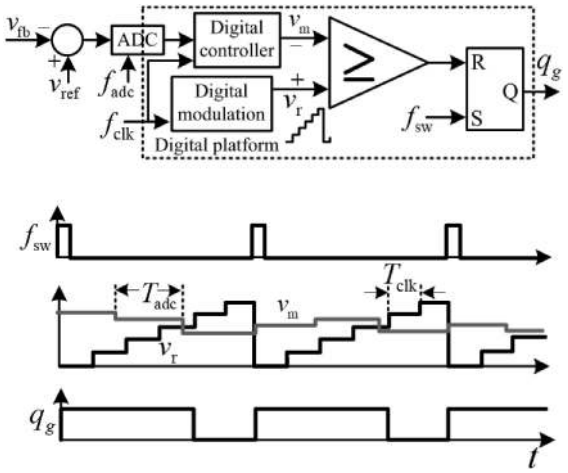


**FIGURE 6.** Fixed-frequency (trailing-edge) digital pulse width modulation.

sampling times and modulation ramp types can alter control-to-output responses. Non-minimum phase behavior is a physical property of boost and other indirect converters. Controller changes might avoid immediate impacts of a disturbance, but do not eliminate the physical behavior.

In general, *voltage mode control* (VMC) refers to dc-dc converter controls that employ output voltage feedback. In *current mode control* (CMC) [19], the sensed inductor current replaces the sawtooth waveform. Trailing-edge modulation becomes analogous to peak CMC and leading-edge modulation becomes analogous to valley CMC. The CMC arrangements are shown in Fig. 4, in which an equivalent current modulating signal $i_m$ and the inductor current $i_L$ are used instead of $v_m$ and the sawtooth signal $v_r$ in Fig. 3. In *flux mode control* (also termed *sensorless current mode control*) [20], a voltage integral that tracks inductor flux replaces the sawtooth instead. Current or flux used in place of a ramp produces instability for half of the duty ratio range, but this can be avoided by retaining a sawtooth and subtracting it as a stabilizing ramp [21], [22]. Stabilizing ramps are less suitable for precise average current control applications because of varying ripple current for varying duty ratio. Average CMC or flux mode controls are preferred in those cases.

Fig. 5 shows a block diagram of average CMC, consisting of a voltage compensator $G_{vc}$ with the (output) error voltage $v_e$ as the input and a current compensator $G_{cc}$ with the error current $i_e$ (relative to the average value) as the input. For current regulated loads, $i_{ref}$ is set to the desired current; otherwise, it is generated by the voltage controller $G_{vc}$. Low pass filter $G_{LPF}$ attenuates ripple and extracts the average inductor current value $i_{av}$. A proportional-integral (PI) controller is typical for $G_{cc}$ to drive $i_e$ to zero for average current tracking. Average CMC [23] does not suffer from current loop instability for wide duty ratio operation. Although average CMC offers superior average current regulation, it is relatively slow. It remains difficult to deliver both fast performance and accurate current regulation using available CMC methods. Both are important for phase current balancing in multi-phase converters, as in many low-voltage high-current applications [24], [25], [26]. High conversion ratios impose current sensing and stability constraints on fixed-frequency CMC methods. A more comprehensive version was presented in [27].

### *B. FIXED-FREQUENCY DIGITAL PWM*

Based on trailing-edge PWM in Fig. 3(a), digital versions can be implemented using an ADC and a digital controller, as shown in Fig. 6. The resolution of digital PWM must be finer than that of the ADC to avoid quantization effects which may lead to limit cycle oscillations [28], [29]. Typical approaches use a counter to create a ramp, which is then compared to a digital signal. With a counter, the digital clock governs the internal time resolution of the pulse width. For example, if 1,000 distinct pulse widths are desired in a converter switching at 100 kHz, a 100 MHz clock must drive the counter. An extreme example is a class-D amplifier switching at 352.8 kHz, with a desired pulse width resolution of 24 bits [30]. The time resolution should be 0.17 ps. This corresponds to a counter clock rate of 5.92 THz. Such an extreme clock rate is implausible. Other techniques use tapped delay-line PWM [31], [32], ring oscillator implementations [33], hybrid digital PWM [34] or noise shaping [16] to allow the same effective output resolution with coarser time resolution. Even so, counter-based PWM implementations are ubiquitous, and are the basis of output ports in many processor families.

The sampling frequency $f_{adc}$ of the ADC is usually an integer multiple of $f_{sw}$, i.e., $f_{adc} = Nf_{sw}$ (most often $N = 1$). This practice seeks to allow nearly a full switching cycle for computation. For example, if a dc-dc converter switching and sampling at 500 kHz is implemented with a microcontroller

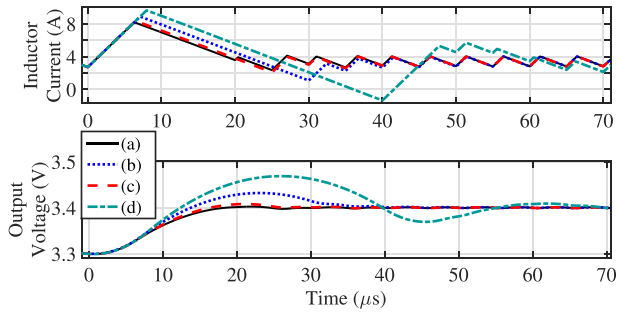


**FIGURE 7.** Effect of $\tau_d$ in peak CMC on the reference transient performance of a buck converter using a PI voltage controller and an analog current loop with 12 V input and $R = 1\ \Omega$. Traces (a) and (d) correspond to analog PWM with $\tau_d = 0$ and $\tau_d = T$, respectively. Traces (b) and (c) correspond to digital PWM with $f_{adc} = f_{sw}$ and $f_{adc} = 20 f_{sw}$, respectively.

clocked at 200 MHz, there are about 400 clock pulses per switching cycle available for computation. The controller can alter tuning parameters or other attributes on a cycle-by-cycle basis. Limits or fault conditions can be enforced as soon as they are detected.

Compared to analog PWM, sampling introduces a delay $\tau_d$ which increases with decreasing $f_{adc}$. A larger $\tau_d$ can degrade large-signal recovery as shown in Fig. 7. Sampling with $N > 1$ has benefits in linear controllers with digital PWM, where an increase in sampling rate decreases the phase lag, $1/(2Nf_{sw})$, associated with digital PWM [35]. Fig. 7 shows that a higher $f_{adc}$ can achieve nearly the same performance as analog CMC without a delay. However, the performance of analog CMC degrades if there is a full cycle delay, even compared to $f_{adc} = f_{sw}$. A delay of a full cycle is the worst-case (transient) detection delay for extreme duty ratio operation using either trailing-edge or leading-edge modulation techniques, as discussed in Section II-A. Ever-decreasing costs of digital processors support increasing control complexity.

### C. PHASE MODULATION

Fixed-frequency phase shift modulation is common in full-bridge isolated topologies for bidirectional power flow [36]. This often leads to high RMS current in the transformer in a dual active bridge converter under light load conditions. Dual phase shift modulation introduces the duty ratio as an additional degree of freedom [37]. A triple phase shift modulation technique can offer three degrees of freedom for further optimization [38]. A comprehensive review of various fixed-frequency control methods for dual active bridge converters is presented in [39], [40].

### D. VARIABLE FREQUENCY MODULATION TECHNIQUES

Variable frequency modulation most often takes one of three basic forms [3], [41]. These are (a) constant off-time, (b) constant on-time, and (c) hysteresis control. Hysteresis control is not usually considered a modulation approach, but the operational structure is about the same, so it is discussed here.

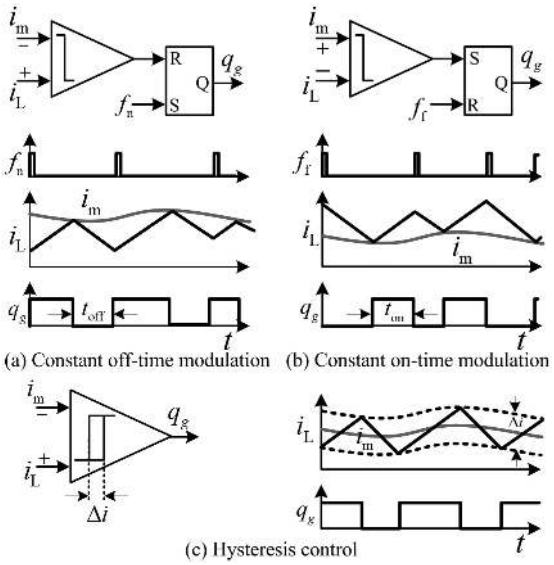


**FIGURE 8.** Current controlled variable frequency modulation techniques.

Typical current-controlled methods are shown in Fig. 8. For constant off-time and on-time modulators, timing parameters are loaded using monostable multivibrators to activate respective flag signals $f_n$ and $f_f$ after triggering. The latch set or reset terminals determine which is being controlled.

#### 1) CONSTANT OFF-TIME MODULATION

For constant off-time modulation [42], the active switch off interval is fixed, and the on time is modulated. In the example here, an equivalent modulation signal $i_m$ varies. The current is compared to $i_m$ as shown in Fig. 8(a), and the switch turns off when the current reaches the modulation signal. This is analogous to peak CMC in Fig. 4(a), but now with varying switching period. The perturbed current dynamics during the $n$th switching cycle can be written as

$$i_{n+1} = i_m - m_2 T_{off} \quad \Rightarrow \tilde{i}_{n+1} = \tilde{i}_m, \tag{2}$$

where $m_2$ is the magnitude of the falling slope of $i_L$, and $i_m$ is the modulating signal in Fig. 8. Unlike current-loop instability in peak CMC for $D > 0.5$, (2) shows that the control is inherently stable irrespective of the duty ratio.

In voltage controlled constant off-time modulation, $i_L$ in Fig. 8(a) is replaced by a sawtooth waveform. This becomes analogous to trailing-edge PWM in Fig. 3(a). The steady-state switching frequency $f_{sw}$ can be derived as

$$f_{sw} = \begin{cases} (v_{in} - v_o)/(v_{in} T_{off}) & \text{buck converter} \\ v_{in}/(v_o T_{off}) & \text{boost converter} \end{cases} \tag{3}$$

A constant switching frequency can be accomplished by adjusting the off time slowly and using an additional phase locked loop (PLL) to regulate $f_{sw}$. This adds a slow (frequency) control loop around a fast one. The slow loop will limit performance, although it can be argued that if the outer

loop merely makes a slow adjustment to the off time until the frequency locks in, the practical impact on dynamic performance is minimal. An early review of methods to enforce a fixed switched frequency under variable modulation approaches can be found in [43]. More recent results can be found in [44].

### 2) CONSTANT ON-TIME MODULATION

Constant on-time operation was motivated initially by resonant pulses fixed in duration [45]. It has become more widely applicable to light load management [46]. The active switch on interval is fixed, and the off time is modulated by the control. A current-based method invoking a modulating signal $i_{\mathrm{m}}$ is shown in Fig. 8(b). This example is analogous to valley CMC in Fig. 4(b). The perturbed current dynamics during the $n^{\mathrm{th}}$ switching cycle can be written as

$$i_{\mathrm{n+1}} = i_{\mathrm{m}} + m_1 T_{\mathrm{on}} \quad \Rightarrow \tilde{i}_{\mathrm{n+1}} = \tilde{i}_{\mathrm{m}}. \tag{4}$$

In contrast to valley CMC, which is unstable for $D < 0.5$, (4) implies that current-based constant on-time modulation avoids this problem.

In VMC constant on-time modulation, $i_{\mathrm{L}}$ in Fig. 8(b) is replaced by a sawtooth waveform, analogous to leading-edge PWM. The steady-state $f_{\mathrm{sw}}$ is

$$f_{\mathrm{sw}} = \begin{cases} (v_{\mathrm{o}} - v_{\mathrm{in}}) / (v_{\mathrm{o}} T_{\mathrm{on}}) & \text{boost converter} \\ v_{\mathrm{o}} / (v_{\mathrm{in}} T_{\mathrm{on}}) & \text{buck converter} \end{cases} \tag{5}$$

As with constant off-time modulation, a slow PLL-based outer loop can adjust the target on time until a desired switching frequency is achieved.

### 3) CONSTANT ON-TIME CONTROL IN DISCONTINUOUS CONDUCTION MODE

The dynamic behavior of constant on-time modulation alters if the converter inductance is below the critical value [47]. Switching converters are said to enter *discontinuous conduction mode* (DCM) when the inductor current drops to zero and switch action is no longer constrained to maintain a current path. A more comprehensive analysis can be found in [48]. DCM is typical under light load conditions. It is sometimes designed deliberately. For example, a flyback converter operating in DCM with a fixed duty ratio will track its input voltage [49], [50].

Fig. 9 shows conventional buck and boost converters in DCM given limited output voltage ripple and high inductor current ripple. For constant on time, in DCM, the steady-state switching frequency can be derived by enforcing charge balance in the output capacitor. The results are

$$f_{\mathrm{sw}} = \begin{cases} \dfrac{2 L v_{\mathrm{o}}}{(v_{\mathrm{in}} - v_{\mathrm{o}})\, v_{\mathrm{in}}} \times \left( \dfrac{i_{\mathrm{o}}}{t_{\mathrm{on}}^2} \right) & \text{buck converter} \\ \dfrac{2L\,(v_{\mathrm{o}} - v_{\mathrm{in}})}{v_{\mathrm{in}}^2} \times \left( \dfrac{i_{\mathrm{o}}}{t_{\mathrm{on}}^2} \right) & \text{boost converter} \end{cases} \tag{6}$$

For a given set of power circuit parameters and operating input and output voltages, the switching frequency $f_{\mathrm{sw}}$ varies linearly with the load current $i_{\mathrm{o}}$ if the on time is fixed. The switching frequency drops as the load current decreases, as shown for a DCM buck converter in Fig. 10. This tends to improve light load efficiency, so the approach is applied in many commercial products. Many products shift from fixed-frequency modulation to constant on-time modulation when the load current falls below a threshold [51].

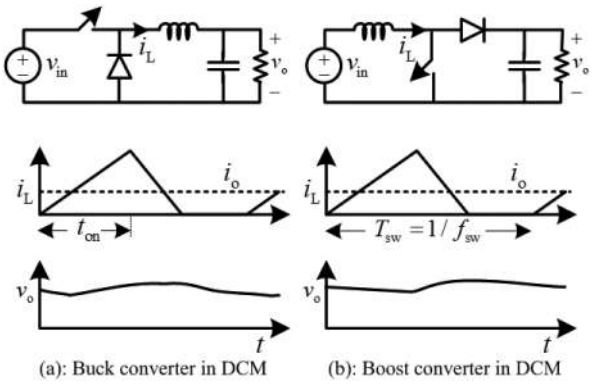


**FIGURE 9.** Current and voltage waveforms of dc-dc converters in DCM.

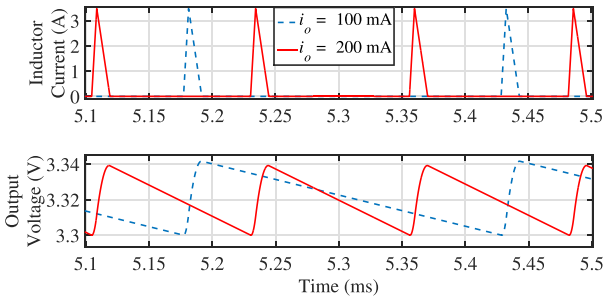


**FIGURE 10.** Output voltage-based constant on-time modulation in a DCM buck converter using the parameter set in Table 2 with 12 V input and 3.3 V output.

Under light load conditions deep in DCM, the inductor current ripple is much larger than the load current, and the output voltage ripple can be approximated as [52]

$$\Delta v_{\mathrm{o}} \approx \begin{cases} \dfrac{(v_{\mathrm{in}} - v_{\mathrm{o}})\, v_{\mathrm{in}}}{v_{\mathrm{o}}} \times \dfrac{t_{\mathrm{on}}^2}{2LC} & \text{buck converter} \\ \dfrac{v_{\mathrm{in}}^2}{(v_{\mathrm{o}} - v_{\mathrm{in}})} \times \dfrac{t_{\mathrm{on}}^2}{2LC} & \text{boost converter} \end{cases} \tag{7}$$

For a given set of power circuit parameters and operating input and output voltages, the ripple $\Delta v_{\mathrm{o}}$ under constant on-time modulation remains more or less constant as the load decreases, which is consistent with Fig. 10. However, $\Delta v_{\mathrm{o}}$ increases with $v_{\mathrm{in}}^2$ and may violate ripple design constraints under high line conditions. This can be corrected by reducing $t_{\mathrm{on}}$ as $v_{\mathrm{in}}$ increases. An adaptive constant on-time modulator adjusts $t_{\mathrm{on}}$ as a function of $v_{\mathrm{in}}$ to keep $\Delta v_{\mathrm{o}}$ within a specified limit and to help regulate $f_{\mathrm{sw}}$ [51].

#### 4) HYSTERESIS CONTROL

Hysteresis determines switching times directly rather than adjusting a duty ratio or time interval, so it is not normally considered among modulation methods. However, the implementation can be similar, as shown in [53], so it is discussed here. Fig. 8(c) removes the latch to implement current hysteresis control. The inductor current $i_L$ is constrained within a hysteresis band $\Delta i$. The band can be left to the specific implementation of the comparator, or can be treated as a separate control parameter. The steady-state switching frequency $f_{sw}$ can be derived as

$$f_{sw} = \begin{cases} \dfrac{(v_{in} - v_o)\, v_o}{L v_{in}} \times \dfrac{1}{\Delta i} & \text{buck converter} \\ \dfrac{(v_o - v_{in})\, v_{in}}{L v_o} \times \dfrac{1}{\Delta i} & \text{boost converter} \end{cases} \tag{8}$$

For a given set of power circuit parameters and operating input and output voltages, $f_{sw}$ is inversely proportional to $\Delta i$ and $L$. Nonlinear magnetic inductor cores and saturation can lead to undesired frequency deviations. If frequency regulation is desired, one approach is to adjust $\Delta i$ slowly and use a PLL to lock in a target frequency [54].

Voltage hysteresis can be realized by replacing $i_L$ in Fig. 8(c) by the feedback voltage $v_{fb}$ in Fig. 2 and $\Delta i$ by $\Delta v$. However, voltage hysteresis control cannot be used directly in boost, buck-boost, and other cascaded converters because of non-minimum phase dynamics. In a boost converter, for example, a command to turn on the active switch (seeking to increase the output voltage) decouples the input and output energy flows and further decreases the output voltage. It is not difficult to overcome the problem — enforcement of a duty ratio or on-time limit is sufficient — but current hysteresis control is often preferred in commercial products.

A challenge in any hysteresis control is signal-to-noise ratio. Hysteresis controllers that seek tight ripple bands are affected by measurement noise. Lack of a latch can lead to chaotic dynamics [55]. Hysteresis control is a simple example of a geometric control, discussed in more depth below.

#### 5) OTHER MODULATION TECHNIQUES

Variable frequency modulation techniques for light load conditions include pulse skipping modulation (PSM) and burst mode control. A PSM technique [56], [57], skips switch action for entire cycles when the load is light enough. In effect, it makes discrete adjustments to reduce the switching frequency as the load decreases. The method can be derived from trailing-edge PWM in Fig. 3(a), in which the control output $q_g$ is ANDed with a PSM logic signal $q_{PSM}$ to generate the final gate signal $q_f$. The status is updated at every rising edge of the switching clock, and $q_{PSM}$ is set high if the output voltage $v_o$ is smaller than a reference value $v_{ref}$, i.e., $v_o < v_{ref}$. A pulse is skipped if the output voltage is acceptable.

Burst mode control, in general, combines PWM and hysteresis control [58], [59]. The concept is to turn off the converter for a time when the load is light, turning it back on when the output voltage falls to a lower ripple limit. This seeks to maintain the output voltage within a hysteresis band $\Delta v$. The control logic enables the modulator if $v_o \le (v_{ref} - \Delta v/2)$. If $v_o \ge (v_{ref} + \Delta v/2)$, modulation is disabled. When timing of the enable or disable decisions coincide with fixed switching period intervals, the approach is the same as PSM. Burst mode improves light load efficiency while holding ripple within a predefined limit. The general case has variable switching frequency and can impose EMI challenges [59]. It is easy to implement at the level of an integrated circuit (IC), and is relatively common in commercial power supplies.

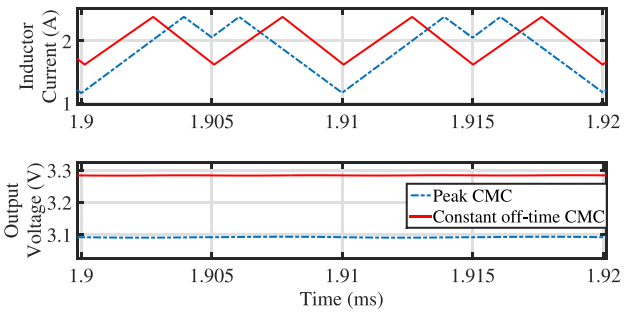


**FIGURE 11.** Current-based trailing-edge modulation in a buck converter with $v_{in} = 6$ V and $i_o = 2$ A. Here only the inner current loop is closed.

Nonlinear carrier modulation, a variation on conventional PWM, has merit for applications with a wide duty ratio range. One example is active power factor correction (PFC), in which a converter such as a boost circuit is expected to operate with a duty ratio over nearly the full 0 to 1 range. Judicious adjustment of the carrier shape can facilitate operation of these converters [60], [61], [62], [63].

A pulse-train control method was described in [64]. This approach allows pulses with either a long on-time or a short on-time, using short pulses when voltage error is low and long pulses when it is high. This method for adapting to light loads has been implemented in a commercial IC.

### *E. PERFORMANCE UNDER VARIOUS MODULATION TECHNIQUES*

#### 1) CURRENT LOOP STABILITY

For CMC trailing-edge modulation, constant off-time control in Fig. 8 (a) offers inherent stability compared to its fixed-frequency counterpart in Fig. 4 (a). The latter is shown to exhibit fast-scale instability in Fig. 11 for duty ratio $D > 0.5$ in the synchronous buck converter from Table 2. The peak current $i_{peak}$ is set to achieve 3.3 V output. The unstable counterpart results in higher voltage error and larger current ripple compared to constant off-time control.

#### 2) CONSTANT ON-TIME MODULATION IN A PFC BOOST CONVERTER

A boost converter is often used as a PFC circuit in ac-dc power conversion to achieve unity power factor and low line-frequency distortion. The primary control objective is to force the average inductor current to track a sinusoidal current

**TABLE 3. Summary of Various Modulation Techniques and Their Applications**

| *Modulation* | *Advantages and shortcomings* | *Primary applications* |
|---|---|---|
| **Trailing edge (TE) PWM** [in Fig. 3 (a)] | *VMC* - single loop control<br>*Peak CMC* - two-loop control, high bandwidth, but unstable for $D > 0.5$ | *VMC* - voltage regulators<br>*CMC* - voltage/current regulated loads (VRM, LED, chargers, etc.) |
| **Leading edge (LE) PWM** [in Fig. 3 (b)] | *VMC* - single loop control<br>*Valley CMC* - two-loop control, high bandwidth, but unstable for $D < 0.5$ | *VMC* - boost converters [17]<br>*CMC* - high duty ratio voltage and current regulators |
| **Constant off-time modulation** [in Fig. 8 (a)] | *VMC* - as in TE case<br>*Peak CMC* - analogous to TE CMC, no stability issue, but varying $f_{sw}$ | Not common<br>*CMC* - wide duty ratio VR applications, LED drivers, etc. |
| **Constant on-time modulation** [in Fig. 8 (b)] | *VMC - as in LE case*<br>*Valley CMC* - similar to LE CMC, no stability issue, but varying $f_{sw}$ | *VMC* - Light-load in DCM, PFC<br>*CMC* - low duty ratio multi-phase buck VRM, battery chargers, etc. |

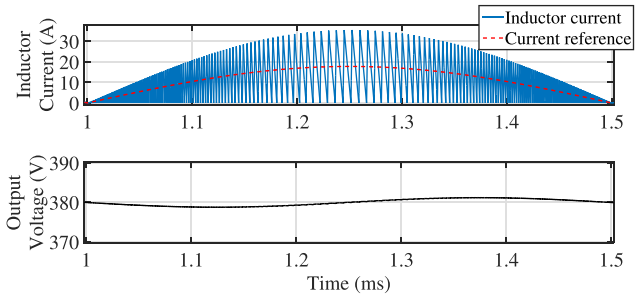


**FIGURE 12. Constant on-time modulation in a PFC boost converter in critical conduction mode with $V_{ac} = 230$ V, $V_{dc} = 380$ V, load resistance $R = 50\ \Omega$, inductance $L = 10\ \mu$H, capacitance $C = 500\ \mu$F, and ac line frequency of 1 kHz.**

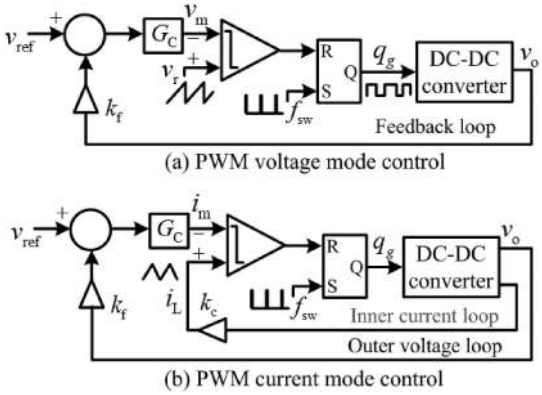


**FIGURE 13. Linear PWM (a) VMC and (b) CMC.**

reference $i_{ref}(t) = (V_{dc}/V_{ac})^2 \times |v_{in}(t)|/R$. Here $V_{dc}$ and $V_{ac}$ are the output dc link voltage and input RMS voltage, $R$ is the output load resistance, and $v_{in}(t)$ is the instantaneous input ac voltage. Average CMC, as in Fig. 5, is suitable for this purpose, but constant on-time modulation can achieve near-perfect current tracking, especially in critical conduction mode as shown in Fig. 12. Critical conduction mode adjusts frequency to keep the inductor exactly at the critical value throughout converter operation. Here, the on time is set to $T_{on} = 2L(P_{out}/V_{ac}^2)$, where $L$ and $P_{out}$ are the inductance and output power of the boost converter. This technique is used in many commercial products [65], in which $T_{on}$ needs to adapt to varying $P_{out}$ or $V_{ac}$.

A comprehensive summary of modulation techniques along with their applications is presented in Table 3, and their impacts on stability and non-minimum phase characteristics of a digitally controlled CMC boost converter are discussed in [66].

## III. CONTROL METHODS BASED ON FEEDBACK AND FEEDFORWARD INTERCONNECTION

Overall feedback control can be classified into several categories. Most typical are (a) output feedback control, (b) state feedback control, (c) observer-based feedback control, and (d) predictive control. Feedforward control can supplement feedback control to further improve disturbance rejection and transient recovery to meet certain performance objectives, as discussed below. There are other designs that use energy sensing [67]. Output feedback control can be implemented with modulation. As in CMC, sometimes converter waveforms can be used directly, a method more broadly termed *ripple-based control* [68], [69]. It is also established that ripple can be demodulated to provide feedback information [70].

### A. OUTPUT FEEDBACK CONTROL LINKED TO MODULATION

#### 1) LINEAR OUTPUT FEEDBACK MODULATION CONTROL

Fig. 13(a) shows conventional VMC, in which the output voltage is sensed and filtered to limit the effects of ripple, and a function of the output voltage error signal $v_{ref} - v_o$ serves as the modulation signal $v_m$. Conventional approaches use variants of PI control; these designs invoke linear system tools even though the implementations in Fig. 13 are nonlinear circuits. Terminology of linear control sometimes generates confusion. For example, an integral control is sometimes called a Type I compensator. A Type II compensator cascades an integrator with a phase-lead network. A Type III compensator cascades an integrator with two phase-lead networks. Any of

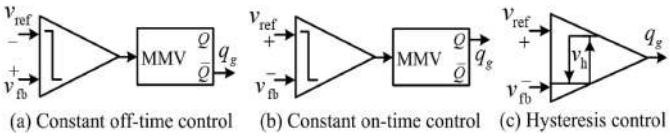


**FIGURE 14.** Voltage-ripple-based variable frequency control methods [69].

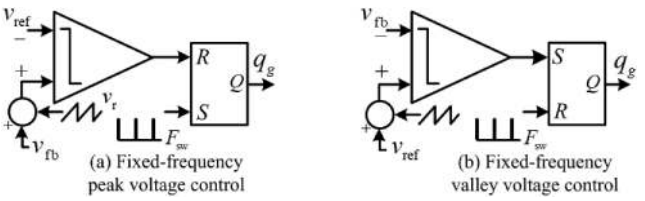


**FIGURE 15.** Voltage-ripple-based fixed-frequency control methods [69].

these four types (PI, Types I, II, III) can be implemented with a single operational amplifier or a single transconductance amplifier [71].

VMC operation in some sense is indirect, since voltage error must first drive a change in inductor current. The advantages of current sensing based on [19] have been considered compelling enough that CMC dominates dc-dc control implementations, but it is important to recognize that similar performance can be achieved using VMC if the loop transfer function can be matched to that with CMC. This requires perfect cancellation of complex poles and time scale separation. In practice, CMC treats the inductor as a controlled current source, which inherently achieves time scale separation and makes the design relatively robust. For example, charge-based controls [72], [73], and flux-based controls [20], use structures similar to VMC and achieve performance similar to CMC methods. It is also known that CMC has less favorable noise properties than VMC [74]. CMC alternatives employ output voltage error to generate a current reference signal, which in turn serves as the input for a current regulator.

#### 2) NONLINEAR PWM OUTPUT FEEDBACK CONTROL

In linear PWM control, analysis and design are carried out based on linearization around an operating point. The underlying assumption is that duty ratio perturbations (and others) must be small compared to steady-state values. Such methods may not be sufficient for wide operating ranges or nonlinear loads. An example is a dc-dc converter driving a constant power load — often another power converter [75], [76]. The negative incremental effect of a constant power load leads to a nonlinear output feedback loop. One alternative is input-output feedback linearization, in which the modulation voltage $v_m$ is a suitable nonlinear function of $v_o$ and the system parameters. Another is geometric control [77]. Constant power loads remain challenging [78], [79], [80].

### B. RIPPLE-BASED OUTPUT FEEDBACK CONTROL

Ripple-based methods can be developed based on constant on-time, constant off-time, and hysteresis controls [68], [69]. Fig. 14 shows voltage-mode ripple-based control methods, in which the feedback voltage is compared directly to a reference voltage $v_{ref}$ and the gate pulse $q_g$ of the controllable switch is generated based on a modulation strategy. In constant on-time and off-time methods, a monostable multivibrator is added. The comparator output acts as the external trigger input. The monostable enters its astable state when the trigger input is activated, and returns to its stable state at the end of the constant timing interval. Hysteresis control is the same as before, switching based on a target ripple value $\Delta v_o$.

Voltage ripple-based constant on- or off-time control methods will have variable switching frequency, but can become unstable because of step ripple on the capacitor equivalent series resistance (ESR) [81]. For application of voltage-based constant off-time and hysteresis control methods to boost and buck-boost converters, an on-time or duty limiter is essential because of non-minimum phase behavior. Inductor current can be used instead as in CMC. Frequency variation for the methods in Fig. 14 can be addressed by synchronizing to an external clock as shown in Fig. 15.

Other ripple-based control methods include $V^2$ control [62], [82], which attempts to extract capacitor current information using ESR-dominated voltage ripple. This method requires a larger ESR, which makes it susceptible to subharmonic instability and produces larger voltage ripple. Capacitor current feedback may be added to improve transient performance [83], although this method does not apply directly to non-minimum phase converters. Alternatively, direct capacitor current control can be used to achieve near-time-optimal performance [84], and this can be extended to boost converters [85].

### C. STATE FEEDBACK CONTROL

State feedback in general implies sensing and control of capacitor voltages and inductor currents. In basic dc-dc converters with only two state variables, such controls share much in common with CMC. For example, if an external reference $i_{ref}$ and current feedback are used explicitly in Fig. 13(a) and $G_c$ is replaced with a proportional gain, the switching control law becomes

$$v_m = k_i\,(i_{ref} - i_L) + k_v\,(v_{ref} - v_o)\,. \tag{9}$$

This is a state feedback control with gains on current and voltage. It becomes a PI control if the parameter $i_{ref}$ is replaced with the function

$$i_{ref} = k_p\,(v_{ref} - v_o) + k_{int}\int (v_{ref} - v_o)\;dt\,. \tag{10}$$

It is possible to use $k_p = 0$, given the proportional term in (9). The time domain performance details of peak CMC and of state feedback control are essentially the same. Fig. 16 shows the response of a buck converter from Table 2 to a step in the reference voltage. The converter switches at 200 kHz. For

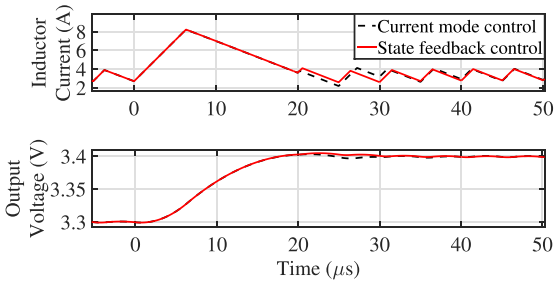


**FIGURE 16.** Reference transient response of a buck converter using peak CMC and state feedback control. The parameter set is in Table 2.

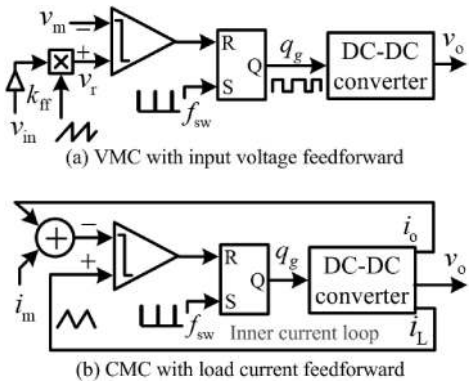


**FIGURE 17.** Linear PWM (a) VMC and (b) CMC.

peak CMC, as in Fig. 13(b), the converter uses a PI controller with $k_v = 80$ and $k_{int} = 100000$ to set the comparison signal for the current waveform. This converter reaches steady state in about eight switching cycles. The same transient performance can be achieved using trailing edge modulation with the state feedback laws in (9) and (10), as in Fig. 13(a), with $k_p = 0$, $k_i = 1$, $k_v = 80$ and $k_{int} = 100000$. It is of interest that state feedback control imposes no limitations on duty ratio since action is governed by a fixed ramp.

Full state feedback is conventional and well known, and analysis and design of converters on the basis of state feedback was established relatively early [86], [87]. The equivalence between CMC and current feedback control is rarely discussed, and the near-exact equivalence demonstrated here seems to be a new result. State feedback control avoids the duty ratio instabilities and signal-to-noise ratio problems associated with current ripple. A state feedback law can be implemented as a single loop in a process structured like a VMC.

### *D. OBSERVER-BASED CONTROL*

As in any control system, the state variables can be sensed, or can be replaced or augmented with various observers. A basic example is *one-cycle control*, in which an integrator tracks an inductor voltage to allow the switching controller to force the inductor voltage average to zero [88]. A more complete example is to use inductor voltage integration as an observer for inductor current [20]. An example for an inverter is given in [89]. The methods are related to *model reference adaptive* control [90].

The connection between model reference adaptive controls and observer-based controls links to a larger family of model-based controls and predictive controls. Low-cost digital processors are fueling application of predictive and adaptive control techniques in dc-dc converters. Model predictive control techniques are gaining attention in high power dc-dc converters switching up to a few hundred kHz, particularly for dc microgrid applications [91], [92].

### *E. COMBINED FEEDFORWARD AND FEEDBACK CONTROL*

An ideal converter has zero output impedance and infinite bandwidth so that the output voltage remains unaffected by transients in input voltage $v_{in}$, load current $i_o$, or parameters. Feedforward methods can supplement feedback control to approach ideal operation.

#### 1) INPUT VOLTAGE FEEDFORWARD IN VMC

The output voltage will exhibit overshoot or undershoot for transients since bandwidth is limited. Feedforward action can reduce these effects. For example, the output of a buck or boost converter is proportional to $v_{in}$. If the input voltage is applied as a feedforward parameter, the converter control can be made insensitive to changes in $v_{in}$ [93]. A similar approach can correct for the load current $i_o$ [94]. Fig. 17(a) shows a feedforward process in a VMC with constant $v_m$. The feedback loop has been broken, and the ramp slope is $m_c = k_{ff} v_{in}$ with feedforward gain $k_{ff}$. The duty ratio can be obtained as $d = v_m/(m_c T)$, and the average output voltage in the case of a buck converter becomes

$$\bar{v}_o = d\bar{v}_{in} = \frac{\bar{v}_m \bar{v}_{in}}{m_c T} = \frac{\bar{v}_m \bar{v}_{in}}{k_{ff} \bar{v}_{in} T} = \frac{\bar{v}_m}{k_{ff} T}. \tag{11}$$

The average output voltage now is independent of the input voltage, and therefore insensitive to supply variation.

#### 2) LOAD CURRENT FEEDFORWARD IN CMC

Fig. 17(b) shows feedforward action in CMC with constant $v_m$. The outer voltage feedback loop has been broken, and the sensed load current $i_o$ is added to $v_m$ to provide a load-tracking reference current for the inner current feedback loop. Any change in the load current automatically changes the reference current in such a way that the effective duty ratio remains constant. This reduces output voltage sensitivity to load variation. However, the finite slew rate of the inductor will limit the impact, since the inductor current must track any change in the load current.

The capacitor current can also be used for feedforward [84], [95], providing the effect of an output derivative, since the capacitor current reflects time rate of change of output voltage. Thus output capacitor current feedforward is nearly the same as output derivative feedback.

## IV. LARGE- AND SMALL-SIGNAL DYNAMICS OF PWM DC-DC CONVERTERS

Dc-dc converters are large signal nonlinear circuits by virtue of switch action. A general modeling framework can be created with piecewise-linear systems [96]. Given $N$ possible circuit configurations determined by switching, the model becomes

$$\dot{\mathbf{x}} = \sum_{i=1}^{N} (\mathbf{A}_i \mathbf{x} + \mathbf{B}_i \mathbf{u})\, q_i(\mathbf{x}, \mathbf{u}, t) \tag{12}$$

where $\mathbf{x}$ is a vector of state variables, $\mathbf{u}$ is a vector of inputs, $\mathbf{A}_i$ and $\mathbf{B}_i$ are matrices with various parameters, and the sequence of time and state-dependent switching functions $q_i \in \{0, 1\}$ represents switch action. Formally, this is a *hybrid* system in which discrete events interact with continuous state variables [97]. Nonlinear elements, such as real inductors, can be brought into this framework by means of component-level piecewise models [98]. One difference between general hybrid systems and power converters is that state variables in power converters (inductor currents and capacitor voltages) are continuous and do not show jumps. The state variables are continuous, but as (12) shows, their derivatives are not. There is a growing literature on piecewise-linear systems and switched linear systems, although only a few authors have linked the work to dc-dc converters [99]. However, piecewise-linear system models are widely used for simulation of power converters [100], [101], [102].

The representation in (12) drives at least three large-signal approaches to dc-dc converter analysis and control:

1) Discrete-time formulations and control, based on $z$ transforms and related concepts.
2) Switching boundary control, in which the Heaviside step function $H(x)$ governs switch action as in

$$q_i(\mathbf{x}, \mathbf{u}, t) = H(f_i(\mathbf{x}, \mathbf{u}, t)) \tag{13}$$

   where $f_i$ are sets of control laws.
3) Averaging, in which a new set of variables represents smoothed action with switching integrated out.

### A. LARGE-SIGNAL PIECEWISE MODELING

As an example of direct piecewise models, consider a buck converter in Fig. 2 and its control waveforms in Fig. 3 while operating in continuous conduction mode (CCM). The overall piecewise-linear state-space model of a CCM buck converter can be written as

$$\dot{\mathbf{x}} = \mathbf{A}_i \mathbf{x} + \mathbf{B}_i v_{\text{in}}, \quad i \in \{\text{on, off}\}, \tag{14}$$

where $\mathbf{x} = [i_{\text{L}}, v_{\text{cap}}]^T$; $i_{\text{L}}$ and $v_{\text{cap}}$ are the inductor current and capacitor voltage, and the matrices are

$$A_{\text{on}} = A_{\text{off}} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}, \; B_{\text{on}} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}, \; B_{\text{off}} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

The individual configurations for a given index $i$ in (14), linked to gate signal $q_{\text{g}}$, have separate (stable) equilibrium points. Neither of them alone can achieve the desired step-down operation and switch action is required. Suitable logic for $q_{\text{g}}$ implies a switched linear system,

$$\dot{\mathbf{x}} = \left[q_{\text{g}} A_{\text{on}} + \left(1 - q_{\text{g}}\right) A_{\text{off}}\right] \mathbf{x} + \left[q_{\text{g}} B_{\text{on}} + \left(1 - q_{\text{g}}\right) B_{\text{off}}\right] v_{\text{in}}. \tag{15}$$

Large-signal behavior of a dc-dc converter can be analyzed by considering the model in (15) along with a switching control law. Using the model in (14), the large-signal behavior can be characterized using state-plane geometry.

### B. DISCRETE-TIME DETAILED MODELING

Piecewise-linear systems lend themselves well to discrete-time models, in which the system behavior is tracked at discrete intervals. From (12), at a set of discrete times $t_k$, a simplified version becomes the transition function

$$\mathbf{x}_{k+1} = \mathbf{A}_k \mathbf{x}_k + \mathbf{B}_k \mathbf{u}_k \tag{16}$$

where $k$ indicates the particular switch configuration during the time interval and the derivatives are constant in each interval. Even if the behavior is more complicated, it is straightforward to generalize by solving (12) interval by interval and then piecing results together. The final condition of one interval becomes the initial condition for the next one. If time intervals are uniform, the model of (16) (or its generalization) can be written immediately in terms of $z$ transforms. However, the *modified* $z$ transform [103] does not require uniform intervals and applies to the broader problem.

A caveat when using $z$ transforms is that the control is through the actual switch timing, so the time intervals linked to duty ratios are, in turn, linked to control action. This is distinct from a conventional discrete-time system, in which the time intervals are determined externally. Even with this limitation, several authors have applied sampled data and discrete time methods to power converter control successfully [104]–[108]. In [106], relationships among state-space averaging, Laplace-domain analysis, and $z$-domain analysis are discussed in depth. In [107], an extensive review of sampled data methods up to that time is included. More recent authors have applied these methods to high-performance dc-dc converters. In [109], response times below 5 $\mu$s are achieved with a sampled data control. In [110], the authors show how to design a discrete-time dc-dc controller that delivers high-performance tracking with uncertain parameters. In [95], it is shown that a converter can respond to a disturbance with an effective bandwidth higher than the switching frequency.

The model in (12) can be considered for a closed-loop system. Such models have been used to predict various nonlinear phenomena in dc-dc converters [111]. A model set up with uniform time intervals $T$, as in Fig. 18, will track the values $i_k$ at the moment of switch turn on. The natural behavior of such a model is *envelope tracking* of the minimum current values. A discrete-time model set up to coincide with the moment of switch turn off will instead track the maximum current values.

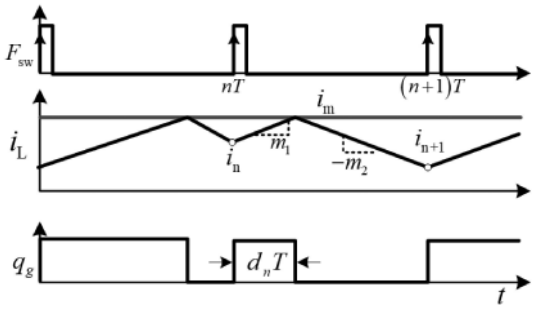


**FIGURE 18.** Control waveforms of a dc-dc converter under peak CMC.

### C. NONLINEAR AVERAGE MODELING

The discontinuous derivatives in (12) limit the applicability of many control methodologies. Many methods for nonlinear control require a system to satisfy a Lipschitz condition, but the piecewise-linear switch-based models for power converters in (12) do not meet this. This negates methods of nonlinear control found in classic work, such as [112]. Averaging is an approach that seeks to identify a time-invariant system that tracks the full piecewise system. The time-invariant model has continuous derivatives, and therefore lends itself to a broad range of control possibilities. Such a model can also be linearized, linking to conventional methods for linear time-invariant systems. Averaging can be applied either top down from the circuit [113], [114] or bottom up from the equations [115]. It has also been developed from an Euler-Lagrange perspective in [116].

From a mathematical point of view, averaging seeks to consider a general time-varying nonlinear system with an identifiable small parameter $\epsilon$ [117], given by

$$\dot{\mathbf{x}} = \epsilon F(\mathbf{x}, \mathbf{u}, t). \tag{17}$$

This is mapped to a set of new variables $\mathbf{y}$, new inputs $\mathbf{v}$, and a function $G$, such that

$$\dot{\mathbf{y}} = \epsilon G(\mathbf{y}, \mathbf{v}), \tag{18}$$

in which $G$ is defined in an averaged sense and $\mathbf{y}$ tracks the behavior of $\mathbf{x}$ in a well-defined manner. That is, we seek

$$G(\cdot) = \frac{1}{T}\int_{t-T}^{t} F(s, \cdot)\, ds \tag{19}$$

In a power converter, a typical choice for the small parameter is the switching period $T$. It is known that variables $\mathbf{y}$ track variables $\mathbf{x}$ in the limit of small $\epsilon$, provided inputs $\mathbf{v}$ are chosen to track the average behavior of actual inputs $\mathbf{u}$. The agreement is not exact in general, and a procedure can be obtained to create refinements to the model [117]. The details were proved in [118]. Alternative extensions of averaging based on harmonic analysis have also been presented [119].

Variables $\mathbf{y}$ can be represented as the averages $\bar{\mathbf{x}}$, and new system matrices $\bar{\mathbf{A}}$ and $\bar{\mathbf{B}}$ are computed as weighted averages of the sum in (12). In state space averaging [113], [115], duty ratios substitute for switching functions and provide the weights. For the CCM buck converter in (15), the average dynamics can be represented as

$$\begin{aligned}
&\dot{\bar{\boldsymbol{x}}} = A_{\rm av}\bar{\boldsymbol{x}} + B_{\rm av}\bar{v}_{\rm in} \triangleq F_{\rm av}\left(\bar{\boldsymbol{x}},\ \bar{v}_{\rm in},\ d\right), \quad \text{where} \\
&\bar{\boldsymbol{x}} = \frac{1}{T}\int_{t-T}^{t} \boldsymbol{x}(s)ds; \quad \bar{v}_{\rm in} = \frac{1}{T}\int_{t-T}^{t} v_{\rm in}(s)ds, \\
&A_{\rm av} = dA_{\rm on} + (1-d)A_{\rm off}, \quad B_{\rm av} = dB_{\rm on} + (1-d)B_{\rm off},
\end{aligned} \tag{20}$$

and $d$ is the duty ratio. The switching nonlinearity in (15) has been transformed into a smooth model in (20).

In general, models obtained with averaging are nonlinear, although without switching discontinuities. Methods of nonlinear control, including feedback linearization [120], synergetic control [121], sliding mode control [122], and many others [112] can be applied. In the case of sliding mode control, it is possible to use switching directly to form a sliding mode. Sliding mode controls can be designed directly from (12) [123]. Since averaged models do not include switching behavior — it is assumed to be fast — the controls become *model limited* and are valid for design only up to some fraction of $f_{\rm sw}$. Fast slew rates associated with ripple are not in the model, so an averaging-based controller will have limits on fast dynamic performance.

### D. MODEL LIMITS ON CONTROL

What about this issue of model-limited control? What ratio of switching frequency to control bandwidth is necessary for a workable result? This issue has been debated extensively in many forums. The details of averaging in [117] for dc-dc converters do not really limit the frequency, although too extreme a control bandwidth will interact with switching ripple and undermine the performance. It is self-evident that the phase of a sufficiently fast disturbance can interact with the switching function phase, leading to aliasing effects. Consider a unity-gain crossover frequency $f_{\rm c}$. Sampling theory considerations [16] suggest that the ratio $f_{\rm sw}/f_c$ should be greater than $\pi$ (not the Nyquist ratio of 2 since these systems do not involve ideal sampling). Theory of distortion for naturally-sampled PWM [16] suggests that aliasing will be down more than 100 dB for ratios above about six. Most designers cite a rule of thumb for a ratio of about 10. It is important to remember that this ratio is for convenience in establishing a smooth averaged model and associated controls and does not represent a fundamental performance limit on the converter itself.

### E. LINEARIZATION AND SMALL-SIGNAL MODELING

#### 1) SMALL-SIGNAL MODELING FROM AVERAGING

Consider small perturbations around a target steady-state operating point, written in terms of the averages as $\bar{\boldsymbol{x}} = \tilde{\boldsymbol{x}} + \boldsymbol{X}_{\rm ss}$, $d = \tilde{d} + D$, $\bar{v}_{\rm in} = \tilde{v}_{\rm in} + V_{\rm in}$, where $D$ is the steady-state duty

**TABLE 4.** Parameters for Buck and Boost Converters [$D' = (1 - D)$, $r'_e = r_e/D'$, $\alpha = (R + r_e)/R$ (Buck), $\alpha = (R + r'_e)/R$ (Boost), $Z_c = \sqrt{L/C}$, $Z'_c = Z_c/D'$]

| Parameters | $\omega_o$ | $Q$ | $\omega_z$ | $\omega_{rhp}$ | $\omega_{z1}$ | $\omega_{z2}$ | $V_e$ |
|---|---|---|---|---|---|---|---|
| Ideal Buck | $\frac{1}{\sqrt{LC}}$ | $\frac{R}{Z_C}$ | N.A. | N.A. | $\frac{1}{RC}$ | 0 | $V_{in}$ |
| Ideal Boost | $\frac{D'}{\sqrt{LC}}$ | $\frac{RD'}{Z_C}$ | N.A. | $\frac{R(D')^2}{L}$ | $\frac{1}{RC}$ | 0 | $\frac{V_o}{D'}$ |
| Practical Buck | $\sqrt{\frac{(R+r_e)}{(R+r_C)}}\cdot\frac{1}{\sqrt{LC}}$ | $\alpha\left[\frac{(r_C+r_e)}{Z_c}+\frac{Z_c}{R}\right]^{-1}$ | $\frac{1}{r_C C}$ | N.A. | $\frac{1}{(R+r_C)C}$ | $\frac{r_e}{L}$ | $\frac{V_{in}}{\alpha}$ |
| Practical Boost | $\sqrt{\frac{(R+r'_e)}{(R+r_C)}}\times\frac{D'}{\sqrt{LC}}$ | $\alpha\left[\frac{(r_C+r'_e)}{Z'_c}+\frac{Z'_c}{R}\right]^{-1}$ | $\frac{1}{r_C C}$ | $\frac{\left[(D')^2(R-r'_e)\right]}{L}$ | $\frac{1}{(R+r_C)C}$ | $\frac{r'_e}{L}$ | $\frac{V_o(R-r'_e)}{D'(R+r'_e)}$ |

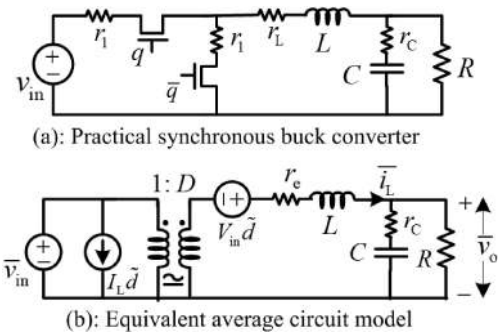


**FIGURE 19.** A synchronous buck converter and its average equivalent circuit. The equivalent resistance is $r_e = r_1 + r_L$ and $D$ is the steady-state duty ratio.

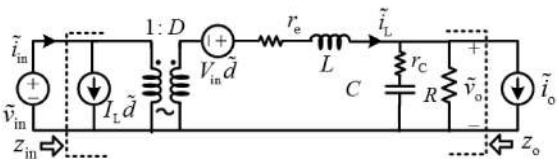

**FIGURE 20.** Small signal equivalent circuit of the buck converter in Fig. 19 (a).

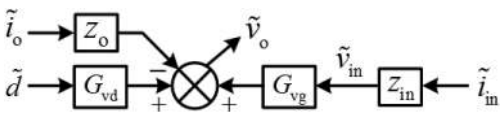

**FIGURE 21.** Small-signal block diagram of a PWM dc-dc converter.

ratio and $V_{in}$ is the dc input voltage. A Taylor series representation of the averaged model in (20) yields the form

$$\dot{\tilde{x}} = \bar{A}\tilde{x} + \bar{B}\tilde{v}_{in} + \left.\frac{\partial F_{av}}{\partial d}\right|_{ss}\tilde{d} + \text{higher order terms.} \qquad (21)$$

This requires well-defined derivatives, which is why it is useful with the averaged model but not the piecewise model. In steady state $\dot{\tilde{x}} = 0$. For a simplified buck converter, this can be solved to obtain

$$V_o = DV_{in}, \quad I_L = V_o/R = I_o. \qquad (22)$$

Eq. (21) without higher order terms is a linear model, valid near the steady-state operating point. Its Laplace transform is

$$\tilde{x}(s) = \left(sI - \bar{A}\right)^{-1}\bar{B}\left[\tilde{d}(s),\ \tilde{v}_{in}(s)\right]^T, \qquad (23)$$

where $\bar{B}$ has been augmented to include derivatives $[\frac{\partial F_{av}}{\partial \tilde{d}}|_{ss},\ \frac{\partial F_{av}}{\partial \tilde{v}_{in}}|_{ss}]$.

Of particular interest are the control-to-output transfer function $G_{vd} = \tilde{v}_o/\tilde{d}$, the input-to-output transfer function (audio susceptibility) $G_{vg} = \tilde{v}_o/\tilde{v}_{in}$, the input impedance $z_{in} = \tilde{v}_{in}/\tilde{i}_{in}$, and the output impedance $z_o = \tilde{v}_o/\tilde{i}_o$. For an ideal buck converter in CCM, some of these are

$$G_{vd} = \frac{V_{in}}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}, \quad G_{vg} = \frac{D}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}}. \qquad (24)$$

Here the radian frequency is $\omega_o = 1/\sqrt{LC}$, the characteristic impedance is $Z_c = \sqrt{L/C}$, and the quality factor is $Q = R/Z_c$. State space averaging and linearization, or equivalently circuit averaging, remain valid as parasitics and linear elements are added to the circuits, as in Fig. 19.

### F. DYNAMICS OF OPEN-LOOP PWM BUCK CONVERTERS UNDER CCM

Fig. 20 shows the small signal equivalent circuit of a CCM buck converter in Fig. 19, with the addition of "probing" current sources at the input and output to test the respective impedances. This gives rise to more complete transfer function expressions. The parameter values for buck and boost converters are listed in Table 4, but notice that many do not apply in the ideal case. Transfer functions for the converters are listed in Table 5. The output impedance $z_o$ at the probing point in Fig. 20 requires careful attention to voltage and current polarities.

The ESR value $r_C$ plays an important role in a practical converter. At low frequency, the output impedance $z_o$ is the load in parallel with the equivalent resistance $r_e$ in Fig. 19. At high frequency, the output impedance is the load in parallel with ESR. Fig. 21 shows the small-signal block diagram of a dc-dc converter. The poles in $G_{vd}$ will be complex conjugate

**TABLE 5. Transfer Functions for Buck and Boost Converters**

| Transfer functions | $G_{\mathrm{vd}}(s)$ | $G_{\mathrm{vg}}(s)$ | $z_{\mathrm{in}}(s)$ | $z_{\mathrm{o}}(s)$ |
|---|---|---|---|---|
| Ideal Buck | $\frac{V_{\mathrm{in}}}{\left(1+\frac{sL}{R}+s^2LC\right)}$ | $\frac{D}{\left(1+\frac{sL}{R}+s^2LC\right)}$ | $\frac{R\left(1+\frac{sL}{R}+s^2LC\right)}{D^2(1+sRC)}$ | $\frac{sL}{\left(1+\frac{sL}{R}+s^2LC\right)}$ |
| Ideal Boost | $\frac{V_{\mathrm{in}}\left(1-\frac{sL}{RD'^2}\right)}{\left(D'^2+\frac{sL}{R}+s^2LC\right)}$ | $\frac{D'}{\left(D'^2+\frac{sL}{R}+s^2LC\right)}$ | $\frac{R\left(D'^2+\frac{sL}{R}+s^2LC\right)}{(1+sRC)}$ | $\frac{sL}{\left(D'^2+\frac{sL}{R}+s^2LC\right)}$ |
| Practical Buck | $\frac{V_{\mathrm{e}}\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)}{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ | $\frac{D\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)}{\alpha\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ | $\frac{\alpha R}{D^2}\frac{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}{\left(1+\frac{s}{\omega_{\mathrm{z1}}}\right)}$ | $\frac{r_{\mathrm{e}}}{\alpha}\frac{\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)\left(1+\frac{s}{\omega_{\mathrm{z2}}}\right)}{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ |
| Practical Boost | $V_{\mathrm{e}}\frac{\left(1-\frac{s}{\omega_{\mathrm{rhp}}}\right)\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)}{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ | $\frac{1}{\alpha D'}\frac{\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)}{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ | $\frac{\alpha R\left(D'\right)^2\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}{\left(1+\frac{s}{\omega_{\mathrm{z1}}}\right)}$ | $\frac{r'_{\mathrm{e}}}{\alpha}\frac{\left(1+\frac{s}{\omega_{\mathrm{z}}}\right)\left(1+\frac{s}{\omega_{\mathrm{z2}}}\right)}{\left(1+\frac{s}{Q\omega_{\mathrm{o}}}+\frac{s^2}{\omega_{\mathrm{o}}^2}\right)}$ |

given a resistive load $R$ if

$$Q>1 \quad \Rightarrow \quad R>\left[\frac{(r_{\mathrm{e}}+r_{\mathrm{c}})R}{Z_{\mathrm{c}}}+Z_{\mathrm{c}}\right]-r_{\mathrm{e}}. \tag{25}$$

Ideally, the condition in (25) becomes $R > Z_{\mathrm{c}}$, which will lead to underdamped behavior with low phase margin as the load power decreases. The dc gain of $G_{\mathrm{vd}}$ depends on input voltage, reflecting the fact that the open-loop output is proportional to input. A higher input voltage tends to increase the crossover frequency and control bandwidth, but at the cost of reduced phase margin. The ESR zero $\omega_{\mathrm{z}}$ might be near the double-frequency pole $\omega_{\mathrm{o}}$ if ESR is high, which would provide phase boost and may lead to overdamped behavior. However, high ESR imposes larger output voltage ripple.

At low frequency, $G_{\mathrm{vg}}$ in Table 5 shows that the duty ratio directly relates the input and output voltages. Any input disturbance impacts the output in proportion to $D$. It will be important to compensate for the input in a closed-loop control.

For practical converters, it is obvious enough that low output impedance is advantageous, but the values of $r_e$ and ESR impose limiting cases. The form of $z_{\mathrm{o}}$ in Table 5 confirms that small $r_e$ and ESR are beneficial, but also suggests that there could be a condition in which terms in $s$ cancel and $z_{\mathrm{o}}$ becomes frequency independent. It is well known that frequency-independent output impedance is optimal, in some sense, for power converter transient response [124], [125]. Even though the converter will not regulate perfectly through a transient, if the output impedance is frequency independent and resistive, the converter will show simple droop response to transients at any speed.

### G. DYNAMICS OF BOOST PWM CONVERTERS UNDER CCM

Fig. 22 shows the small-signal equivalent circuit of a CCM boost converter, which can be used to derive the control-to-output transfer function $G_{\mathrm{vd}}$, audio susceptibility $G_{\mathrm{vg}}$, input impedance $z_{\mathrm{in}}$, and output impedance $z_{\mathrm{o}}$. The poles in $G_{\mathrm{vd}}$ in

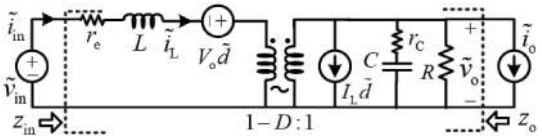


**FIGURE 22. Small signal equivalent circuit of a synchronous boost converter.**

Table 5 will be complex conjugate for a resistive load if

$$Q>1 \quad \Rightarrow \quad R>\left[\frac{\left(r'_{\mathrm{e}}+r_{\mathrm{c}}\right)R(1-D)}{Z_{\mathrm{c}}}+\frac{Z_{\mathrm{c}}}{(1-D)}\right]-r'_{\mathrm{e}}. \tag{26}$$

This requires $R > Z_{\mathrm{c}}/(1-D)$, and leads to underdamped behavior and decreasing phase margin as the load power decreases, as in the buck case. The biggest difference is the right-half-plane (RHP) zero in $G_{\mathrm{vd}}$. This reflects the nonminimum phase physics of the converter, in which energy can be delivered from input to output only with a two-step process in which energy is first stored in the inductor (as the output decays) and then transferred to the capacitor.

The RHP zero frequency, $f_{\mathrm{rhp}}$, effectively limits the achievable (model-limited) closed-loop small-signal bandwidth. The value is

$$f_{\mathrm{rhp}}=\frac{\omega_{\mathrm{rhp}}}{2\pi}=\frac{(1-D)^2R}{2\pi L}. \tag{27}$$

This shows that $f_{\mathrm{rhp}}$ varies with the load current and the duty ratio, with the slowest performance corresponding to the highest output power and highest duty ratio. The effective bandwidth can be raised by reducing $L$, but this trades off against higher ripple. Lighter loads reduce damping and phase margin, whereas heavier loads reduce achievable bandwidth as the RHP zero decreases. The combination makes it difficult for small-signal controls to cover a wide operating range. Active PFC converters are an application example, mitigated because the control dynamics are linked to mains frequency and switching frequency is much higher.

**TABLE 6.** Parameters of (28); $K = 2L/(RT)$, $k_1 = (1-M)/(2-M)$ and $k_2 = (M-1)/(2M-1)$

| *Converter* | $K_{\rm d}$ | $\omega_{\rm d}$ | $M$ |
|---|---|---|---|
| **Buck** | $2V_o k_1/D$ | $\dfrac{1}{k_1 RC}$ | $\frac{1}{2}\left(1+\sqrt{1+4D^2/K}\right)$ |
| **Boost** | $2V_o k_2/D$ | $\dfrac{1}{k_2 RC}$ | $2/\left(1+\sqrt{1+4K/D^2}\right)$ |

The audio susceptibility of a boost converter has $D' = 1 - D$ in the denominator. Any disturbance at the open-loop converter input impacts the output immediately. As with a buck converter, $z_{\rm o}$ in Table 5 implies that low $r_e$ and ESR will be beneficial. It is also possible to attempt cancellation of the $s$-dependent terms in $z_{\rm o}$, potentially yielding a frequency-independent resistive output impedance. As in the buck case, this has advantages in transient response, since the output will show a simple resistive droop to a load transient.

### H. DYNAMICS OF PWM DC-DC CONVERTERS IN DCM

During each switching cycle under DCM, the inductor current starts from zero and returns to zero, as shown in Fig. 9. The dual condition in boost-buck and other converters with capacitive transfer sources starts and returns the capacitor voltage to zero during a switching period. In DCM, an additional *duty ratio constraint* is needed to set up dynamic analysis. An extensive analysis can be found in [48]. Simplified control-to-output transfer functions of buck and boost converters under DCM can be written as

$$G_{\rm vd} = \left.\frac{\tilde{v}_{\rm o}}{\tilde{d}}\right|_{\tilde{v}_{\rm in}=0} = K_{\rm d}/\left(1+\frac{s}{\omega_{\rm d}}\right), \tag{28}$$

where expressions for $K_{\rm d}$ and $\omega_{\rm d}$ are given in Table 6.

The small-signal model in (28) does not include the (fast) dynamics of the inductor current $i_L$. While accurately capturing low frequency behavior, this model is not sufficient for predicting high frequency dynamics. State-space averaging as in [126], and circuit averaging as in [127], can be used to improve accuracy. It is reported in [127] that the RHP zero in a non-minimum phase boost converter is not completely removed from the control-to-output transfer function $G_{\rm vd}$ under DCM. However, its effect is reduced substantially compared to CCM as the RHP zero is pushed to the right in the $s$ plane with decreasing load current. A discrete-time model can be used to improve accuracy and to predict bifurcation phenomena in a DCM boost converter [128]. Although high frequency dynamics are important, for a small-signal-based controller design, the simplified model in (28) suffices up to $f_{\rm sw}/10$.

## V. SMALL-SIGNAL BASED TUNING

Frequency domain design tools are helpful for small-signal-based PWM control and are used in the majority of commercial power supply products. Primary design objectives are to meet a desired control bandwidth with acceptable phase margin. The unity-gain crossover frequency $f_{\rm c}$ is often used as the control bandwidth, and the concepts are used interchangeably in the following design case studies.

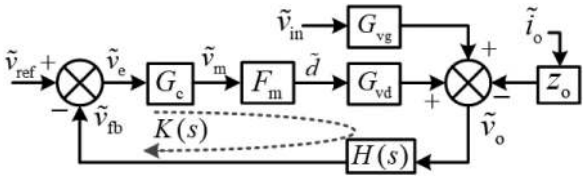


**FIGURE 23.** Block diagram of a closed-loop dc-dc converter, VMC.

### A. DESIGN OF PWM VMC

Fig. 23 shows the block diagram of a closed-loop dc-dc converter set up for PWM VMC. The modulator is assigned a gain $F_{\rm m} = f_{\rm sw}/m_{\rm c}$ where $m_{\rm c}$ is the slope of the ramp signal. The feedback block $H(s)$ comprises a voltage divider and a low pass filter. The objective is to design a suitable compensator $G_{\rm c}(s)$ for shaping the closed loop gain $K(s)$ at a target operating point to meet transient and steady-state specifications. High loop gain at low frequency ensures that the output voltage will be near the reference value. The closed-loop transfer function in Fig. 23 is

$$\frac{\tilde{v}_{\rm o}}{\tilde{v}_{\rm ref}} = \frac{1}{H(s)} \times \frac{K(s)}{1+K(s)} \approx \frac{1}{H(s)} \tag{29}$$

where $K(s) = G_{\rm c}(s)F_{\rm m}G_{\rm vd}(s)H(s)$. With high gain, this is nearly independent of parameter variations in the open-loop plant $G_{\rm vd}$. Since the gain is not unlimited, analysis must establish (1) robustness again parameter variations and unmodeled dynamics, (2) acceptable stability margins, (3) adequate transient performance, and (4) useful design guidelines.

The control-to-output transfer function $G_{\rm vd}$ in Table 5 of an open-loop nonideal buck converter consists of one ESR zero and a double pole or complex conjugate poles at $\omega_o$. Typical worst-case design requirements seek low-frequency gain above 40 dB to achieve better than 1% steady state error, crossover frequency $f_c$ above $f_{\rm sw}/10$, phase margin of 45° or more, and gain margin of 10 dB or more. An integral term can force the steady state output voltage to match the reference.

#### 1) AN ANALYTICAL APPROACH TO DESIGN A TYPE III COMPENSATOR FOR A VMC BUCK CONVERTER

Typically, the compensator should include two zeros near $\omega_{\rm o}$ to compensate phase lag due to the integrator and the double pole, one pole either to cancel the ESR zero or at $f_{\rm sw}/2$ to attenuate switching noise, whichever is smaller, and another pole at the desired crossover frequency $f_{\rm c}$. This leads to a Type III compensator,

$$G_{\rm c}(s) = \frac{k_{\rm c}\left(1+\dfrac{s}{\omega_{\rm cz1}}\right)\left(1+\dfrac{s}{\omega_{\rm cz2}}\right)}{s\left(1+\dfrac{s}{\omega_{\rm cp1}}\right)\left(1+\dfrac{s}{\omega_{\rm cp2}}\right)}. \tag{30}$$

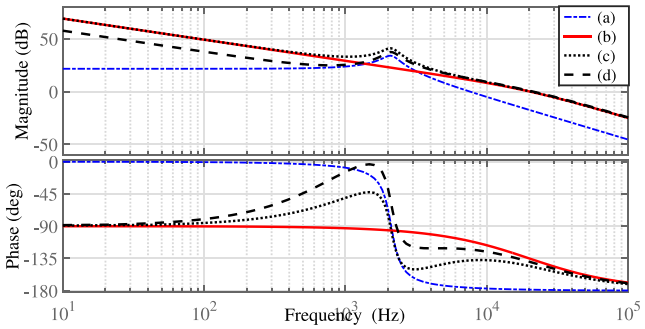


**FIGURE 24.** Loop gain analysis of an ideal CCM buck converter: (a) uncompensated loop gain and compensated loop gain using (b) exact complex pole-zero cancellation, (c) $\omega_{cz1} = \omega_{cz2} = \omega_o$, and (d) $\omega_{cz1} = \omega_{cz2} = \omega_o/2$.

Here $k_c$ sets the low-frequency loop gain. For an ideal buck converter with $r_C = r_e = 0$, one of the compensator poles is effectively $\omega_{cp2} = \infty$ and therefore is not needed.

The primary loop-shaping objective is to design the compensator $G_c(s)$ in (30) for transfer functions of the form

$$K(s) = \frac{k_{des}}{s\left(1 + \dfrac{s}{\omega_{des}}\right)}; \quad \frac{\tilde{v}_o}{\tilde{v}_{ref}} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \qquad (31)$$

where $H(s) = 1$, $\omega_n = \sqrt{k_{des}\omega_{des}}$, and $\xi = \frac{1}{2}\sqrt{\omega_{des}/k_{des}}$. If $\omega_{des}$ is $2\pi f_c$, $k_{des}$ can be computed as $k_{des} = \sqrt{2}\omega_{des}$. This can achieve 45° phase margin with $\xi = 0.42$ for the closed-loop system in (31) with 20% peak overshoot.

The compensator zeros are computed from

$$\omega_{cz1} + \omega_{cz2} = \frac{1}{RC}, \quad \omega_{cz1}\omega_{cz2} = \frac{1}{LC}. \qquad (32)$$

Here $L$ and $C$ are fixed in the power stage design, but the load resistance $R$ changes. Exact pole-zero cancellation is not feasible in general. Alternatively, two real zeros may be placed near the double pole, with $\omega_{cz1} = \omega_{cz2} = \omega_o = 1/\sqrt{LC}$. Fig. 24 compares the cases. If the zeros are placed at $\omega_{cz1} = \omega_{cz2} = \omega_o/2$, the same phase margin and crossover frequency can be retained as in case of exact pole-zero cancellation, but low frequency gain decreases slightly. Although the tuning depends on load and parameters, a digital version can be designed to adapt and adjust tuning. See [129] for a comprehensive discussion and review.

After zero placement, pole placement is carried out using $\omega_{des} = 2\pi f_{sw}/10$. The value $k_{des}$ can be set to $k_{des} = \sqrt{2}\omega_{des}$ through a suitable choice of the compensator gain in (30), given $k_c = k_{des}/[F_m v_{in} H(s)]$. The worst-case result for a CCM buck converter corresponds to the smallest duty ratio and lightest load. For a wide load range, performance may be reduced at nominal operation if parameters are fixed. Digital controls can alter parameters if output current feedforward is available. Table 5 shows that the loop gain varies with $V_{in}$. The control will benefit from input voltage feedforward to adapt to a wide input voltage range.

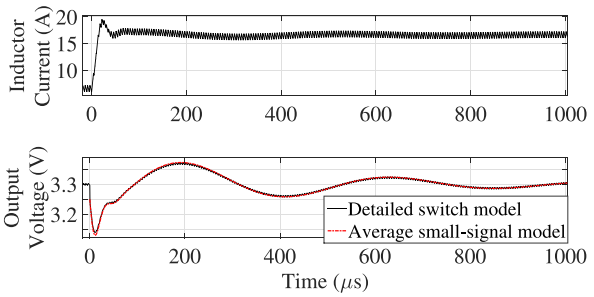


**FIGURE 25.** Load transient response in a buck converter for a load step size of 10 A with 12 V input using VMC set for $f_c = f_{sw}/10$ and 45° phase margin.

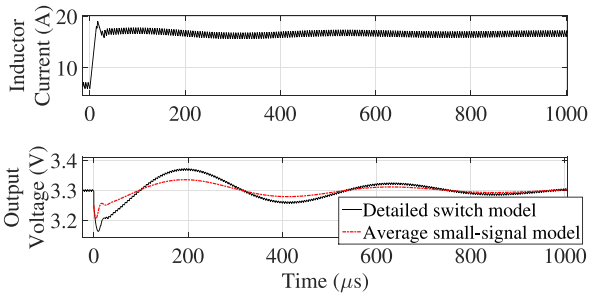


**FIGURE 26.** Similar operating condition as in Fig. 25, except with $f_c = f_{sw}/5$.

### 2) VALIDITY OF SMALL-SIGNAL-BASED VMC DESIGN

Fig. 25 shows load transient performance of a VMC buck converter with a Type III compensator in (30) using the design steps in Section V-A1 to achieve $f_c = f_{sw}/10$ and 45° phase margin. The same compensator is used in a detailed switching model and a small-signal model in Table 5, and the responses match for the desired closed-loop bandwidth of $f_{sw}/10$.

Seeking to design the compensator in (30) for a higher bandwidth, $f_c = f_{sw}/5$, Fig. 26 shows that the response using the small-signal model-based design deviates from that using a detailed switching model. The time-domain performance is almost unchanged compared to $f_{sw}/10$. The mismatch is caused by large duty ratio perturbations as well as by duty ratio saturation, for which small-signal models no longer apply, but the actual bandwidth has not improved. Thus, typically the bandwidth is set no higher than $f_c = f_{sw}/10$ as discussed at the end of Section IV-C.

### 3) PID CONTROLLER TUNING IN A VMC BUCK CONVERTER

A proportional-integral-derivative (PID) controller is sometimes used in dc-dc converters based on familiarity and functionality [130], even though the derivative term can add noise sensitivity. It takes the form

$$v_m(t) = k_p v_e(t) + k_{int}\int_0^t v_e(\tau)d\tau + k_d\frac{dv_e(t)}{dt}, \qquad (33)$$

where $v_e(t)$ is a voltage error signal, $v_m(t)$ is the resulting modulating signal, and $k_p$, $k_{int}$, and $k_d$ indicate proportional, integral, and derivative gains.

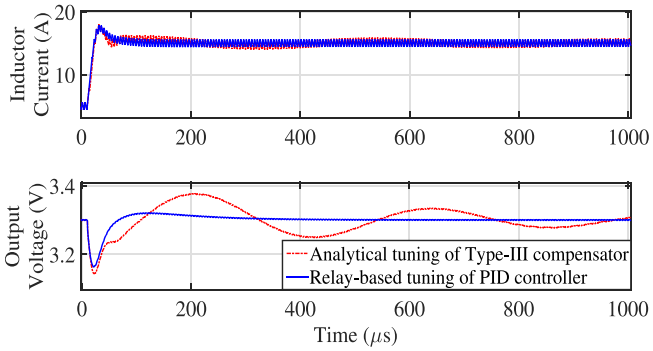


**FIGURE 27.** Load transient response of a VMC buck converter with the operating condition of Fig. 25 for two different controller tuning methods. The objectives are to achieve $f_c = f_{sw}/10$ and 45° phase margin.

Real-time PID controller tuning can be implemented on a digital platform, motivated by a wide operating range [131]. PID controller tuning based on model reference adaptive control was applied successfully to a CCM buck converter in [132], [133]. Relay-feedback-based auto-tuning was applied in a digitally controlled dc-dc converter [134], and the method is discussed below. Tuning methods based on online identification of the control-to-output frequency response were applied to CCM buck converters in [135]. A nonlinear PID controller can improve performance [136].

A relay-based tuning approach [137] can be used to design and operate a PID controller for a VMC buck converter using the block diagram in Fig. 23. In a relay-based tuning set-up, the controller transfer function $G_c$ consists of a parallel combination of a PID controller in (33) and a relay block. A switch enables only one block at a time. During the tuning process, the relay block is activated. This produces a controlled oscillation in the closed-loop system; thereafter, the amplitude and frequency of oscillation can be measured in real time. Using a frequency domain approach, PID controller parameters can be obtained online by setting a desired phase margin of 45° at the desired crossover frequency $f_c = f_{sw}/10$ [134], based on parameters at that moment. Once parameters are obtained, the relay block is deactivated and the PID controller is activated.

Fig. 27 shows load transient performance of a VMC buck converter operating with relay-based tuning configured to achieve $f_c = f_{sw}/10$ and 45° phase margin. It is compared to a Type III compensator. The initial transient and the inductor current response are about the same for both controllers, but the conventional Type III compensator results in additional overshoot and a long settling time in the output voltage.

#### 4) DESIGN OF A VMC BOOST CONVERTER

The presence of a RHP zero and a double pole in a boost converter complicates controller design. A limit on duty ratio (or switch on time) is necessary to prevent locking up at $D = 1$. A Type III compensator as in (30) is typical for the controller. The two zeros are placed near $\omega_o$ to compensate phase lag due to the integrator and the double pole. The pole $\omega_{p1}$ is placed to cancel the ESR zero $\omega_z$. The pole $\omega_{p2}$ is placed coincident with the RHP zero. If either the RHP zero or the ESR zero is higher than $f_{sw}/2$, the corresponding compensation pole is placed at $f_{sw}/2$ instead. The crossover frequency $f_c$ should not exceed the least of $f_{sw}/10$, $f_{rhp}/5$, or $\omega_o/(4\pi)$. To maintain stability, it is necessary to have $\omega_{rhp} > \omega_o$.

Unfortunately, both $\omega_{rhp}$ and $\omega_o$ vary with the duty ratio and the former with load. For a VMC boost converter, the crossover frequency $f_c$ is limited by the location of the RHP zero for high load current and duty ratio, whereas poor phase margin for lighter loads and lower duty ratios constrains $f_c$. Thus, VMC is not common in high-performance boost converters with a wide operating range.

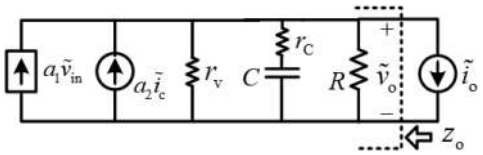


**FIGURE 28.** Equivalent circuit of a dc-dc converter under CMC. Here $a_1 = 0$, $a_2 = 1$ and $r_v = \infty$ for a buck converter, whereas $a_1 = 1/[(1-D)R)]$, $a_2 = (1-D)(1 - s/\omega_{rhp})$ and $r_v = R$ for a boost converter.

**TABLE 7.** Parameters of CMC Converters in (34)

| *Converter* | $k_g$ | $\omega_z$ | $\omega_{rhp}$ | $\omega_p$ |
|---|---|---|---|---|
| **Buck** | $R/R_s$ | $\dfrac{1}{r_C C}$ | none | $\dfrac{1}{(R+r_C)\,C}$ |
| **Boost** | $\dfrac{RD'}{2R_s}$ | $\dfrac{1}{r_C C}$ | $D'^2R/L$ | $\dfrac{2}{(R+2r_C)\,C}$ |

### B. SMALL-SIGNAL PWM CMC

#### 1) APPROXIMATE LOW FREQUENCY MODEL, CMC

Fig. 28 shows a simplified equivalent circuit of a dc-dc converter under CMC given low ripple on $i_L$ relative to the average value [138]. The perturbed control current is $\tilde{i}_c \approx \tilde{i}_L$. If $R_s$ is an equivalent sense resistance (shown in Fig. 2), the control voltage becomes $\tilde{v}_c = R_s\tilde{i}_c$, and the control-to-output transfer function can be derived as

$$G_{vc} = \left.\frac{\tilde{v}_o}{\tilde{v}_c}\right|_{\tilde{v}_{in}=\tilde{i}_o=0} = \frac{k_g\left(1+\dfrac{s}{\omega_z}\right)\left(1-\dfrac{s}{\omega_{rhp}}\right)}{\left(1+\dfrac{s}{\omega_p}\right)}, \qquad (34)$$

where the parameters are given in Table 7. Eq. (34) suggests that the transfer function can be approximated by a first-order system. A Type II compensator should be sufficient, although the closed-loop bandwidth is limited by $\omega_{rhp}$ in the boost case.

#### 2) MORE ACCURATE MODELING OF CMC

The equivalent model in Fig. 28 provides insight into the low frequency behavior but does not account for inductor current

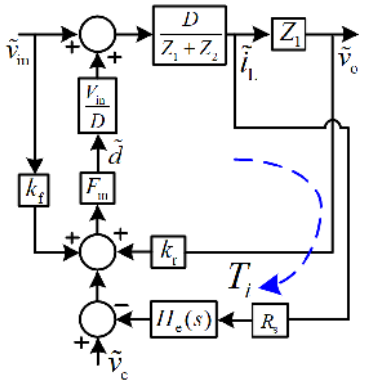


**FIGURE 29.** Small-signal block diagram of a CMC buck converter [141].

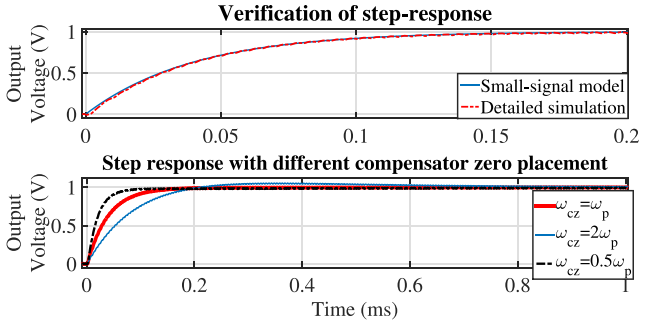


**FIGURE 30.** Unit step response of a closed-loop CMC buck converter with $v_{in} = 12$ V, $v_o = 3.3$ V, and $f_{sw} = 200$ kHz using different $\omega_{cz}$ values in (38). The top trace zooms in on the pole-zero cancellation case.

ripple and current-loop sampling effects. Accuracy can be improved using the analytical approach in [139] by considering current ripple along with the sampled data model of [140]. Ridley demonstrated a natural sampling effect in CMC [141] and sought to incorporate this into an equivalent circuit model.

Combining Fig. 19 with a sampled-data model, Fig. 29 shows the block diagram of a peak CMC buck converter, with impedances $Z_1 = [r_C + 1/(sC)]||R$ and $Z_2 = r_e + sL$. The modulator gain $F_m$ and other gains $k_r$ and $k_f$, as well as the (current-loop) sampling transfer function $H_e(s)$, can be found in [141]. The control-to-output transfer function can be approximated as

$$G_{vc} = \frac{\tilde{v}_o}{\tilde{v}_c} = \frac{R}{R_s} \times \frac{1}{1 + \frac{RT}{L}\left(\alpha_c D' - 0.5\right)} F_p(s) F_h(s), \quad (35)$$

where $\alpha_c = 1 + m_c/m_1$ and $R_s$ is the current sense resistance; $m_c$ and $m_1$ are the slope of the compensating ramp and rising slope of the inductor current. The functions are

$$\begin{aligned} &F_p(s) = \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)}, \quad F_h(s) = \left(1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2}\right), \\ &\omega_z = \frac{1}{r_C C}, \quad \omega_p = \frac{1}{RC} + \frac{T}{LC}\left(\alpha_c D' - 0.5\right), \\ &\omega_n = \pi/T, \quad Q_p = \frac{1}{\pi\left(\alpha_c D' - 0.5\right)}. \end{aligned} \quad (36)$$

If the current-loop sampling effect is neglected, i.e., $F_h(s) \approx 1$ and $RT/L < 1$, a low-frequency approximation of the control-to-output transfer function in (35) can be shown to take the simpler form in (34). This means that the inner current loop in CMC transforms a second order $G_{vd}$ in Table 5 under VMC into an approximate first-order $G_{vc}$ in (34) by treating the inductor as a controlled current source. However, since current state feedback is equivalent to CMC, the effect is more related to time scale separation, and control design is limited by the slow outer voltage loop.

### C. DESIGN OF PWM CMC: AN OUTPUT FEEDBACK APPROACH

#### 1) DESIGN OF A CMC BUCK CONVERTER

Based on (34), a Type II compensator is sufficient for CMC, with

$$G_c(s) = k_c \frac{\left(1 + \frac{s}{\omega_{cz}}\right)}{s\left(1 + \frac{s}{\omega_{cp}}\right)}. \quad (37)$$

Using (34) and (37), the loop transfer function becomes

$$K(s) = \frac{k_g k_c \left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{s}{\omega_{cz}}\right)}{s\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{\omega_{cp}}\right)} \quad (38)$$

The design procedure is:

1) Set $\omega_{cz}$ to cancel the pole $\omega_p$.
2) Set $\omega_{cp}$ to cancel the ESR zero $\omega_z$. Under perfect pole-zero cancellation, the closed-loop transfer function takes the form of a first-order system with time constant $\tau = 1/(k_g k_c)$.
3) Set the compensator gain $k_c$ to meet the desired closed-loop bandwidth. For an ideal buck converter with $r_C = 0$, $\omega_z = \infty$, and $\omega_{cp} = \infty$, $G_c$ in (37) takes the form of a PI controller,

$$G_c(s) = k_p + \frac{k_{int}}{s}, \quad (39)$$

with $k_{int} = k_c$ and $k_p = k_c/\omega_{cz}$.

Pole $\omega_p$ varies with load, so perfect pole-zero cancellation in (38) is not possible using a fixed compensator. Load feedforward can be employed to help adapt the parameters.

The top traces in Fig. 30 show that under perfect pole-zero cancellation, step response predicted using the simplified model in (34) matches that of a detailed switch-based model. However, if the control bandwidth is pushed closer to $f_{sw}/2$, the former model fails to capture high-frequency behavior accurately. The higher-order model in (35) will help. The bottom traces in Fig. 30 demonstrate step responses for

various values of compensator zero $\omega_{cz}$. The choice $\omega_{cz} < \omega_p$ results in faster transient performance but higher peak current (not shown). For a load range, $\omega_{cz}$ can be selected close to $\omega_{p,max}$, corresponding to the lightest load. One challenge of pole-zero cancellation is that it implies loss of controllability. A current limit can be imposed separately to avoid problems with inductor saturation.

In contrast to pole-zero cancellation, a state-feedback design can take all internal states into account. This supports methods for optimizing a dynamic-performance cost function from the perspective of a linear quadratic regulator (LQR) through suitable placement of the closed-loop poles. Constraints on overshoot or undershoot of voltages and currents can be brought into the cost function. Although model uncertainties and parameter variations require a robust design, observers can be employed to reduce the impact of noise and measurement error. An approach that combines converter design with LQR control was presented in [142]. Procedures to make an LQR approach robust were discussed in [143]. Feedforward can help in this context, particularly for the RHP zero effects in a boost converter [144].

### 2) DESIGN OF A CMC BOOST CONVERTER

Consider the approximate low frequency model of $G_{vc}$ in (34) for a boost converter. A Type II compensator in (37) should be sufficient. The ESR of the output capacitor should be kept low to minimize output ripple. Therefore the frequency associated with the ESR zero should be far beyond the RHP zero frequency, i.e., $\omega_z \gg \omega_{rhp}$, and the loop transfer of a CMC boost converter can be written approximately, using (34) and (37), as

$$K(s) \approx \frac{k_g k_c \left(1 - \frac{s}{\omega_{rhp}}\right)\left(1 + \frac{s}{\omega_{cz}}\right)}{s\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{\omega_{cp}}\right)}. \tag{40}$$

The design steps for a CMC boost converter are as follows:

1) Set $\omega_{cz}$ to cancel the pole at $\omega_p$.
2) Set $\omega_{cp}$ coincident with the RHP zero $\omega_{rhp}$.
3) Set the dc gain $k_c$ of the compensator as $k_c = \omega_c/k_g$, where $\omega_c$ is the crossover radian frequency.

Here $k_c$ can be computed using the frequency response of the loop transfer function in (40) at $\omega = \omega_c$ under perfect pole-zero compensation. The frequency response can be written as

$$K(j\omega_n) = \left(\frac{k_g k_c}{\omega_n \omega_{rhp}}\right) \angle -90^\circ - \tan^{-1}\left(\frac{2\omega_n}{1-\omega_n^2}\right), \tag{41}$$

where $\omega_n = \omega/\omega_{rhp}$. If the desired phase margin is set to 45°, the crossover radian frequency $\omega_c$ becomes $\omega_c = (\sqrt{2} - 1)\omega_{rhp}$; consequently, $k_c = (\sqrt{2} - 1)\omega_{rhp}/k_g$. If the current sense resistance $R_s$ is normalized to unity, $k_c$ in (37) becomes $k_c = (0.828\, v_{in})/(L\, v_{ref})$. Fig 31 shows the corresponding (step-up) reference transient performance of a closed-loop boost converter under CMC using the parameter set in Table 2.

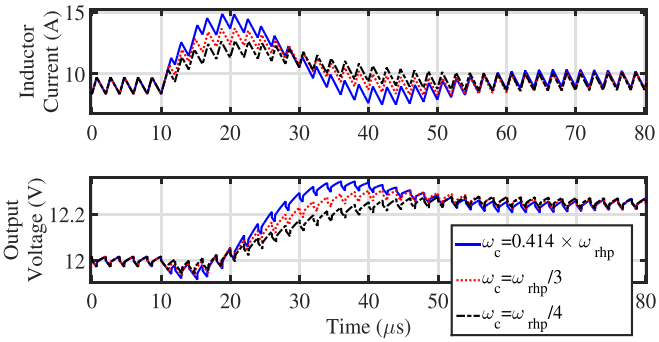


**FIGURE 31.** Transient response of a CMC boost converter for a step change in $v_{ref}$ from 12 to 12.25 V with $v_{in} = 8$ V and $R = 2\ \Omega$ using different $\omega_c$ values.

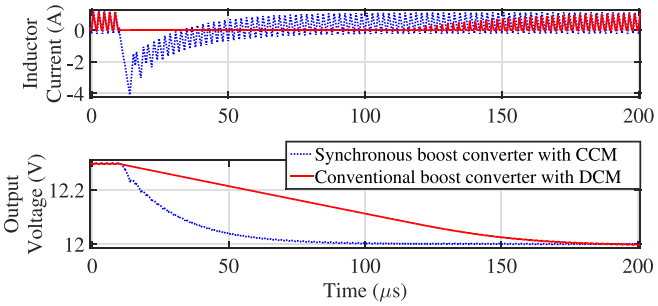


**FIGURE 32.** Comparative reference step transient response of a CMC boost converter for the same operating condition as in Fig. 31. CCM and DCM with $R = 40\ \Omega$ use a crossover frequency $f_c = \min(f_{rhp}/3, f_{sw}/10)$.

The design achieves higher bandwidth, but 45° phase margin leads to nearly 20% (output) voltage overshoot and 5 A current overshoot. If $\omega_c$ is reduced, the voltage and current overshoots can be reduced, but the transient performance is degraded for $\omega_c < \omega_{rhp}/4$. A practical trade-off could use $\omega_c = \omega_{rhp}/3$ [145] to target 65° phase margin.

### 3) EXTENSION OF CMC DESIGN TO A DCM BOOST CONVERTER

A Type II compensator as designed just above for a CCM boost converter can be applied for a DCM configuration as well, and closed-loop stability can be ensured analytically using the small-signal model in (28). Fig. 32 shows the transient performance of a CMC boost converter for a downward step in the reference voltage under light load conditions using both synchronous and conventional boost configurations. At light load, the RHP zero is pushed far beyond the control bandwidth. Therefore the crossover frequency is taken as the minimum of $f_{rhp}/3$ and $f_{sw}/10$. Fig. 32 shows that both configurations have stable, well-damped, transient performance. However, the DCM configuration results in long recovery time because the excess (output) capacitor charge is removed only through the high load resistance. Faster energy removal is possible through the input inductor using a synchronous configuration, although this leads to higher conduction losses.

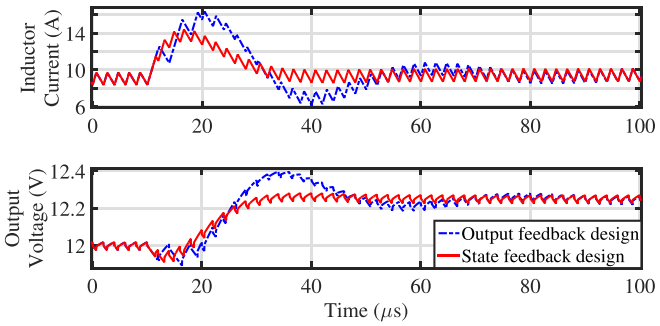


**FIGURE 33.** Transient response of a CMC boost converter for a step change in $v_{\text{ref}}$ from 12 to 12.25 V with $v_{\text{in}} = 8$ V, $R = 2\ \Omega$, and $\omega_{\text{c}} = \omega_{\text{rhp}}/2$.

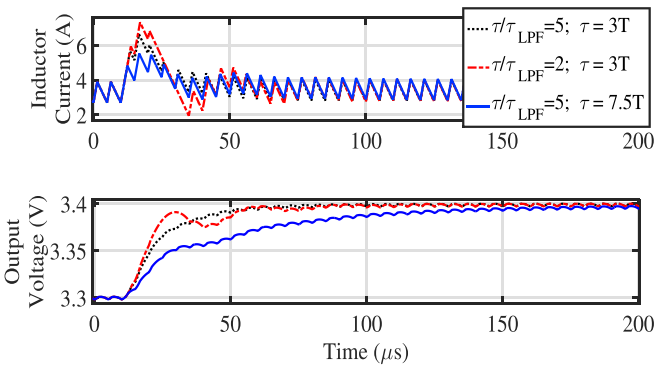


**FIGURE 34.** A loop interaction case study in a CMC buck converter for a step change in $v_{\text{ref}}$ from 3.3 to 3.4 V with $v_{\text{in}} = 12$ V and $R = 1\ \Omega$.

Combined CCM and DCM operation can retain fast transient response and high efficiency by operating the synchronous MOSFET until the excess charge is removed. Thereafter, it is deactivated as the diode remains in place.

### *D. DESIGN OF PWM CMC: A STATE FEEDBACK APPROACH*

The trade-off between phase margin and $\omega_{\text{c}}$ makes is hard to provide fast transient response with low overshoot in a CMC boost converter. A state feedback approach is an effective alternative to provide more design flexibility to meet both requirements.

Instead of a Type II compensator, a PI controller as in (39) is considered with state feedback. The overall closed-loop system constitutes a third-order state-space model. The desired closed-loop eigenvalues are selected by considering (i) the PI controller, (ii) crossover radian frequency $\omega_{\text{c}}$, and (iii) deliberate time scale separation. The closed-loop characteristic polynomial can be written as

$$\Delta_{\text{CL}}(s) = (s + a_1)(s + \omega_{\text{c}})(s + 10\omega_{\text{c}}), \qquad (42)$$

where $a_1$ is set as the ratio of the integral to the proportional gain of the PI controller in (39). The desired poles in (42) are taken as three real poles corresponding to (i) the zero of the PI controller, (ii) the pole due to the output capacitor, which is set to the desired crossover radian frequency $\omega_{\text{c}}$, and (iii) the pole due to the input inductor, set ten times faster for time scale separation. The feedback controller gains are computed using Ackermann's formula [146].

A boost converter design case study is shown in Fig. 33 using the same power circuit parameter set as in Fig. 31. With the objective to achieve high closed-loop bandwidth, $\omega_{\text{c}}$ is set to $\omega_{\text{rhp}}/2$. A design based on conventional output feedback with a Type II compensator leads to phase margin of only 37°. This yields high overshoot in the output voltage and inductor current. For the same closed-loop bandwidth, the state feedback design leads to fast transient performance with no output voltage overshoot and reduced current overshoot. The state feedback approach uses the controllability property to control both the output voltage and inductor current dynamics. This flexibility supports placement of closed-loop poles for a better trade-off between phase margin and bandwidth. Such flexibility is lost in conventional output feedback control because of pole-zero cancellation that makes the corresponding state uncontrollable.

### *E. DESIGN ASPECTS OF MULTI-LOOP CMC*

Conventional multi-loop CMC is a cascaded control architecture with inner current and outer voltage loops. A primary requirement is to ensure a fast inner loop with sufficient time-scale separation from the slower outer loop. A case study is discussed below.

The current-loop bandwidth will be limited if the controller uses low-bandwidth current sensors, current sense amplifiers, or signal conditioning circuits. For such a case, consider a first-order low pass filter with time constant $\tau_{\text{LPF}}$ to model the effects. The design steps in Section V-C1 can be applied to achieve a closed-loop bandwidth $\omega_{\text{c}}$ if the constraint $\omega_{\text{c}} < 1/(5\tau_{\text{LPF}})$ is enforced to maintain the validity of the model in (34). The model implicitly takes the inductor current to be a controlled source with fast dynamics.

Fig. 34 shows a loop-interaction case study in a CMC buck converter using a PI controller designed following the steps in Section V-C1 to achieve a closed-loop bandwidth equal to $f_{\text{sw}}/10$. If the inner current loop is kept much faster than the outer voltage loop, the response is found to be consistent with the analytical prediction using an approximate single-pole model as in (34). If the design attempts to increase the bandwidth relative to $1/\tau_{\text{LPF}}$, both loops start interacting, and the result is higher overshoot or undershoot. This loop interaction can be avoided by reducing the bandwidth, in which case the closed-loop response in Fig. 34 can be predicted using the analysis in Section V-C1.

### *F. FEEDFORWARD ACTIONS AND THEIR IMPACTS*

Load current and input voltage feedforward can achieve near-ideal load regulation under CMC. This is particularly useful for non-minimum phase converters [94].

Fig. 35 shows the effect of load current feedforward on the load transient response of a buck converter using CMC. An adaptive voltage positioning (AVP) strategy is used to

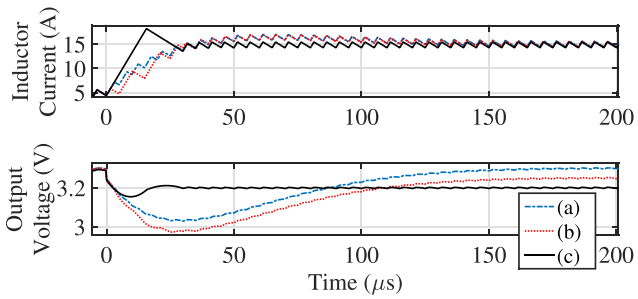


**FIGURE 35.** Improving output impedance in CMC: Load transient response of a buck converter with 12 V input using a PI controller (a) without and (b) with droop [147] and (c) a proportional controller with droop.

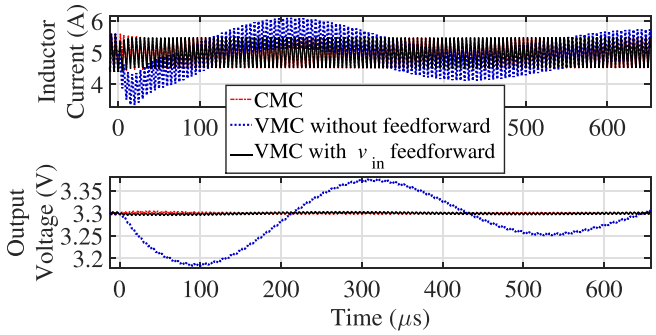


**FIGURE 36.** Transient performance of a buck converter for a step change in input voltage from 12 V to 8 V using CMC and VMC techniques with $i_o = 5$ A.

adjust the set point for varying load current, equivalent to droop action. This can enhance the bandwidth; however, the capacitor ESR and converter characteristic impedance will set an upper limit [147]. For a suitable choice of proportional gain, the closed-loop output impedance can be made nearly independent of frequency — a resistive impedance which must be larger than the ESR.

Although VMC offers superior output impedance at low frequency compared to CMC, it is still limited by the effective resistance $r_e$ in a practical dc-dc converter. Near-ideal output impedance can be obtained by considering load current feedforward to anticipate the effect due to $r_e$ at low frequency.

Fig. 36 shows the response to a supply step transient in a buck converter using two different control methods. Inductor current feedback in CMC provides inherent input voltage compensation, thereby achieving excellent supply disturbance rejection. Similar performance can be achieved in VMC by incorporating input voltage feedforward. Input voltage feedforward action is also inherent in flux-mode control [20] and in one-cycle control [88].

## VI. LARGE-SIGNAL-BASED CONTROL AND DESIGN

### A. GEOMETRIC CONTROL METHODS IN DC-DC CONVERTERS

Geometric control is a broad class of methods based on differential geometry, system trajectories, and manifolds [148]. Sliding mode control is a relatively familiar subset of geometric control [149], in which a system is controlled by imposing specific state action through switching. Sliding mode control is an updated version of relay-based systems, in which on-off or bang-bang control action selects among configurations of a system or among inputs.

The term *boundary control* usually refers to the idea of using different control strategies or gain settings near a particular operating trajectory, or boundary. In switching power converters, geometric control considers the ways in which switch action interacts with state trajectories. Therefore, *switching boundary control* is used here to describe system control by means of *switching boundaries* [5], [150]. These are geometric structures that govern switch action. A basic example is a line in a two-dimensional state space, given by

$$\sigma(x_1, x_2) = k_1(x_{1,0} - x_1) + k_2(x_{2,0} - x_2), \tag{43}$$

where $\{x_{1,0}, x_{2,0}\}$ is the target operating point. In multiple dimensions, a boundary is generalized to a manifold (which might be nonlinear) with the form

$$\sigma(\mathbf{x}) = F(\mathbf{x}). \tag{44}$$

The concept is direct: given an operating state at a specific time $t_0$, compute $F(\mathbf{x}(t_0))$ and $\sigma(\mathbf{x}(t_0))$. If $F(\mathbf{x}) > \sigma(\mathbf{x})$ then switch to one configuration. If instead $F(\mathbf{x}) < \sigma(\mathbf{x})$, switch to a different configuration. This is a simple conditional control law, equivalent to a signum function $\text{sgn}(F - \sigma)$. In a system with a single active boundary, a necessary condition is that $\sigma(\mathbf{x})$ must divide the equilibrium points such that switch action always forces trajectories toward the boundary. More details about conditions for stability are presented in [151], with extensive analysis and discussion of nonlinear boundaries in [152]. It is clear how a conditional control law might apply to a system with a single active switch, but more complicated structures or multiple structures can be employed to govern the action of multiple switches. In a dc-dc converter, the active switch governs energy feed from the input source, so a switching boundary control becomes a bang-bang control.

Switching boundary control can be used to push performance up to the physical limits of dc-dc converters, as shown in [150]. As a direct large-signal control approach, it can be used to address start up, steady state operation, and fault protection in a combined framework. For example, a segmented switching boundary can enforce a current limit.

Fig. 37 illustrates a switching boundary controller for a dc-dc converter with a first-order switching surface $\sigma$,

$$\sigma = k_v\,(v_{ref} - v_c) + k_i\,(i_{ref} - i_L)\,, \tag{45}$$

where $k_v$ and $k_i$ are voltage and current gains. The slope of the surface (a line in this case) can be represented by a normalized gain $k_p = k_v/k_i$. It is the only free parameter, and is varied to obtain the desired dynamic performance. Fig. 38 shows the state-plane performance of a buck converter for a step load change from 1 A to 20 A using parameters from Table 2 with a hysteresis band around $\sigma$ to enforce $\Delta i = 1$ A. A choice $k_p = 50$ yields fast recovery. A larger $k_p = 70$ leads to voltage overshoot. A small value slows the response, but drives the

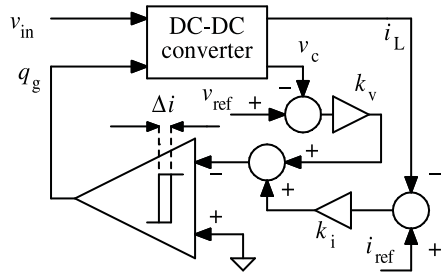


**FIGURE 37.** Boundary control of a dc-dc converter using a first order switching surface with hysteresis.

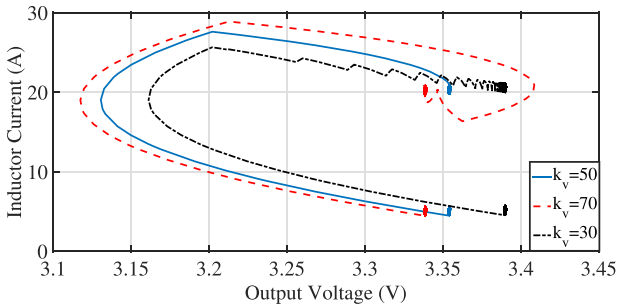


**FIGURE 38.** Phase plane plot of load transient response using the boundary control in Fig. 37 with $k_i = 1$ for various values of $k_v$.

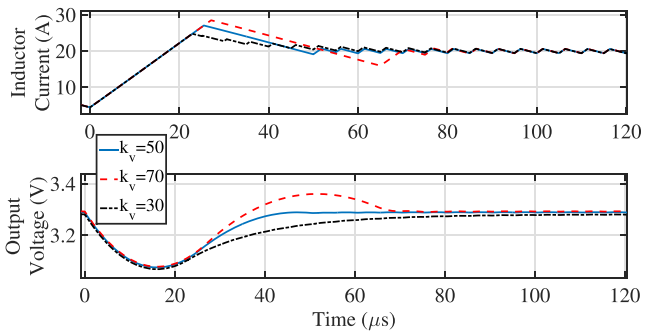


**FIGURE 39.** Time domain waveforms corresponding to Fig. 38.

system to a sliding mode that tracks the intended current. The behavior in time domain is shown in Fig. 39.

Results in Fig. 38 suggest that there is a choice of $k_p$ that will minimize the response time. This does indeed follow from the literature. It is well known that minimum time response in a bang-bang control requires using all available power until just the right moment. Theorem 5 in LaSalle [153] shows that if there is a solution for a system (which can be time varying), based on a signum function of the variables, that drives the output to a target state, that solution is optimum in time. In a power converter, this means that if the target output can be reached with a single on-off switch sequence, that sequence is guaranteed to be the fastest possible control. Burns provides examples in [150]. For Fig. 38, a minimum-time solution can be found by analysis forward in time from the initial operating point, combined with analysis in reverse from the target final operating point. The intersection of the two results gives the switching time for fastest response. The method follows from [153], which states that the optimum-time solution can be found in many cases by running the system in reverse from the final point. For power converters, the approach is discussed in [151].

The minimum-time solution depends on the starting point and parameters. Burns shows how a suitable nonlinear switching boundary can produce minimum response time over an operating range [150]. More recent work shows how to adapt the boundary with an active computation [154] to cover wide operation and uncertain parameters.

As in state feedback control, the value of $i_{ref}$ in (45) depends on load and is not necessarily known. There are at least three ways to address this limitation:

1) Use an integral voltage error term $i_{ref} = k_{int} \int (v_{ref} - v_o)\, dt$.
2) Set the slope $k_p$ to be steep enough to limit the change in current. The slope becomes a droop characteristic, the same as AVP.
3) Use load current feedforward as the basis for computing the expected inductor current, with $i_{ref}$ taken from the result.

An integral complicates the control and must be tested for stability. Droop works well for small variations, but a single choice of slope is not likely to be the right choice for a wide load range. The adaptive method described in [154] extends the range of fast response and provides a steep local slope that provides acceptable droop. The load feedforward method is a possible alternative for future work.

Linear switching boundaries are rarely the best choice to produce fast large-signal transient response and acceptable small-signal performance. Higher-order switching boundaries [155], [156], [157] can be set up to support better tradeoffs. A second-order surface takes the form [155]

$$\sigma_2 = c_2 \left[ i_L - (v_o/R) \right]^2 + (v_o - v_{ref}), \tag{46}$$

where the coefficient $c_2$ is a nonlinear function of states and power circuit parameters. An interesting alternative is to link the shape of switching boundaries to trajectory shapes, yielding a *natural* switching boundary [158], [159]. The approaches are parameter sensitive, and methods have been explored for addressing the challenges [160], [161]. Any of these methods can, in principle, support disturbance recovery up to the slew rate limits in a converter.

### B. TIME OPTIMAL CONTROL IN DC-DC CONVERTERS

Minimum-time large-signal recovery involves one switching action, as discussed above. Fig. 40 shows the details of time-optimal (in the sense of minimum time) transient response to a load step increase in a buck converter, generalized from Fig. 39. The inductor energy slews as quickly as possible to return to the reference voltage in the shortest time. This is a *deadbeat control* [162], meaning that there is complete transient recovery in finite time. Timing constraints can be added

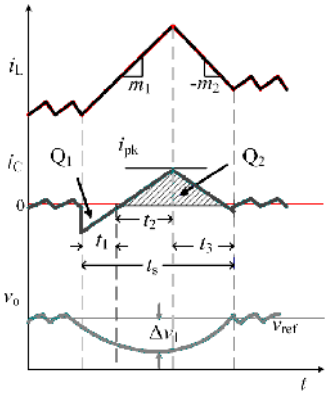


**FIGURE 40.** Capacitor charge-balance waveforms related to transient response for a step change in load current in a synchronous buck converter.

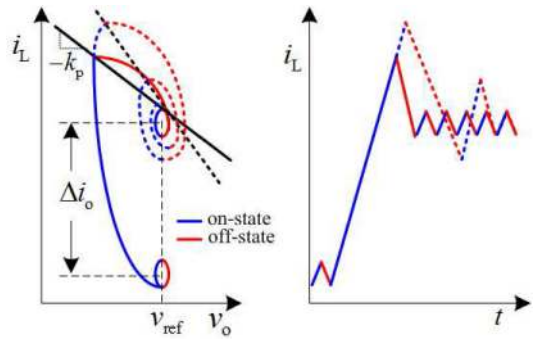


**FIGURE 41.** Time optimal load step-up recovery in a buck converter.

to enforce fixed frequency even through a transient [163]. For a load increase $\Delta i_o$, recovery time $t_s$, peak current $i_{pk}$, and voltage undershoot $\Delta v_1$ can be obtained as [164]

$$\begin{aligned} t_s &= \frac{L\Delta i_o}{(v_{in}-v_o)}\left(1+\frac{1}{\sqrt{D}}\right), i_{pk} = \sqrt{D}\Delta i_o, \\ \Delta v_1 &= \frac{1}{2}\frac{Z_c^2\Delta i_o^2}{(v_{in}-v_o)}, Z_c = \sqrt{L/C}, \end{aligned} \tag{47}$$

where $D$ is the nominal duty ratio prior to the change. The recovery time and voltage undershoot in (47) are linked to slew rate and to characteristic impedance. A smaller inductor can reduce $t_s$ by increasing the slew rate, but this will increase the ripple current and losses. A larger capacitor tends to decrease $\Delta v_1$, but this will decrease converter power density. In dynamic voltage scaling applications, load current and reference voltage change together, following a droop slope. The corresponding parameters for minimum-time recovery can be found in [164]. The perspective is not unique. In [165], several geometric approaches listed lead to minimum-time recovery.

To meet ever-increasing load current slew rate demands from fast loads, the constraints in (47) and the associated undershoot may not be sufficient. Faster performance is possible by providing auxiliary paths to the source, load, or storage elements [10], [12]. If certain aspects of the load disturbances are known (e.g., step changes within a predefined range), auxiliary methods can reject disturbances in much less than a switching cycle [11]. The limitation is linked to disturbance detection time. Capacitor pre-charge can be used to achieve ultra-fast reference transient performance with minimal energy overhead [164].

### C. GEOMETRIC VIEWPOINT OF PID CONTROL FOR PWM DC-DC CONVERTERS

The derivative term in a conventional PID controller in (33) can be replaced with the capacitor current in a buck converter because $d(v_{ref} - v_o)/dt = i_c/C$. A PID controller can be set up as a switching boundary control

$$\sigma = k_c i_c + k_p (v_{ref} - v_o) + k_{int}\int_0^t (v_{ref} - v_o)\, d\tau, \tag{48}$$

where the current gain $k_c$ can be factored out. The alternative PID formulation in (48) represents a two degree-of-freedom tuning problem for a PID control, as the switching boundary realization shows.

This boundary formulation is representative of a capacitor current controlled buck converter (with a PI controller in the voltage feedback path), in which near-load-invariant regulation can be achieved even without integral action [166]. Although an integral term eliminates steady-state error, it can degrade stability margin. Finite integrator range leads to windup problems, eventually resulting in limit cycle oscillations or even closed-loop instability. Integrators need resets or limiters. The objectives of PID tuning are to achieve (i) closed-loop stability over the target operating range, (ii) robustness against parameter variations and model uncertainty, (iii) fast transient recovery, (iv) good line and load regulation, (v) low computational burden, and (vii) acceptable noise attenuation.

### D. GEOMETRIC TUNING METHODS FOR DC-DC CONVERTERS

Early discussions of switching boundary tuning and gain selection for dc-dc converters were presented in [47] and in [150]. An alternative approach, summarized in Fig. 41, is divided into two steps [167], [168]. It follows from (48). After detecting a load transient, the integral action is deactivated, and the PD control (with gain $k_p$ to be derived from phase plane analysis) guides the converter trajectory toward the final operating point. Following this, small-gain integral action is reinitiated to eliminate steady-state error.

The piecewise-linear state-space model of an ideal CCM buck converter driving a constant current load $i_o$ is written as [167]

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \frac{q_g}{L} & 0 \\ 0 & \frac{-1}{C} \end{bmatrix}\begin{bmatrix} v_{in} \\ i_o \end{bmatrix}, \tag{49}$$

where $x_1$ and $x_2$ indicate inductor current $i_L$ and capacitor voltage $v_C$. The instantaneous load current is taken as an external input to the controller.

As the PD controller is expected to drive large-signal recovery, the gain $k_p$ in (48) needs to be determined for time-optimal recovery. Consider a load step from $i_{o1}$ with a step size $\Delta i_o$. With instantaneous load current dynamics, the change is

$$\frac{dx_2}{dx_1} = \frac{Z_c^2\,(x_1 - i_o)}{\left(q_g v_{in} - x_2\right)}; \quad Z_c = \sqrt{L/C}. \tag{50}$$

Using (50), trajectories can be obtained as

$$\int_{i_i}^{i_f} (x_1 - i_o)\,dx_1 + \int_{v_i}^{v_f} \left(x_2 - q_g v_{in}\right) dx_2 = 0, \tag{51}$$

where $i_i$ and $v_i$ are initial conditions of $x_1$ and $x_2$, and $i_f$ and $v_f$ are final conditions. A general solution is [167]

$$\begin{aligned} &F_i\,(i_i, v_i) = F_f\,(i_f, v_f)\,, \quad \text{where} \\ &F_k\,(i_k, v_k) = \tfrac{i_k^2}{2} + \tfrac{v_k^2}{2Z_c^2} - \left[i_k i_o + v_k q_g v_{in}/Z_c^2\right]. \end{aligned} \tag{52}$$

After detecting a load step-up transient, the trajectory moves along the on-time path from an initial point $(i_{o1},\ v_{ref})$, and then changes to the off-time trajectory after intersecting the switching surface $\sigma$ given by

$$\sigma = (i_o - i_L) + k_p\,(v_{ref} - v_o)\,. \tag{53}$$

It tracks the off-time path until reaching the final condition $(i_{o1} + \Delta i_o,\ v_{ref})$. By solving for the on-state and off-state trajectory intersection points with the switching surface, the gain for minimum-time response $k_p$ can be formulated as [168]

$$k_p = \lambda/\Delta i_o Z_c^2, \ \text{ where } \ \lambda = \sqrt{4 v_{in} v_{ref} - \Delta i_o^2 Z_c^2}. \tag{54}$$

This requires information about step size, input voltage, reference voltage, and characteristic impedance $Z_c$. Hence, $k_p$ can be computed online given quick assessment of the step size. In practice, the step size does not need to be known instantly, since the on-state trajectory continues until the intersection point with $\sigma$; there is a time interval between the disturbance and the intersection point that can be used for computation.

The gain for minimum-time response to a step-down load transient can be derived using similar methodology. The results are

$$k_p = \lambda/\Delta i_o Z_c^2, \ \text{ where } \lambda = \sqrt{4 v_{in}(v_{in} - v_{ref}) - \Delta i_o^2 Z_c^2}. \tag{55}$$

Notice that conventional tuning for small-signal models also requires parameter knowledge across the operating range. Adaptive online tuning [169] is complicated in conventional controls for dc-dc converters, but transition dynamics obtained with small-signal tuning are still model limited and cannot take advantage of converter slew rates. In contrast, the large-signal two-step approach computes the gain for minimum-time response $k_p$ from instantaneous values of the input voltage, reference voltage, load current, and characteristic impedance. If these are sampled and updated often, detection of the step size is the most computationally intensive action, and a large-signal geometric control would be expected to act much more quickly than an adaptive small-signal control. Fast performance extends beyond the local neighborhood of an operating point.

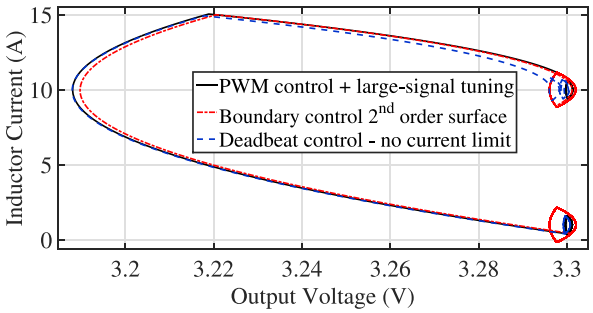


**FIGURE 42. Phase plane plots corresponding to load transient response using switching boundary control methods with second-order switching surface [155], deadbeat control [162], [163] and PWM control with large-signal tuning [168] using the parameter set in Table 2 and 12 V input.**

This large-signal tuning method can be applied to boost and buck-boost converters to achieve minimum-time performance. The details can be found in [170]. Thus, minimum response time can be achieved using existing PWM methods by selecting suitable controller gains and adding load-current feedforward. A load estimator (or observer) can be applied if load current sensing is problematic.

In all of these converters, geometric controls can add additional constraints such as current limits or deviation limits. These will slow the response but still achieve time optimality in the sense of minimum time subject to the constraints [171]. The results in [154] and [158] can also lead to minimum response time. Recent linkages back to modulation in [165] are helpful.

### *E. PERFORMANCE COMPARISON USING SWITCHING BOUNDARY CONTROLLERS*

Fig. 42 shows load transient performance of a buck converter for a 10 A load step using various switching boundary controllers. This shows that a time-optimal deadbeat controller is possible using a variety of geometric methods; the converter can recover from a large-signal transient with one switching action. If a peak current limit is enforced, more switching actions will be required and recovery time is longer, as shown in Fig. 43. The converter still recovers in finite time, but the current limit adds a second set of computations. A second-order switching surface is powerful and can provide minimum-time recovery. Fixed switching frequency can be enforced using large-signal PID tuning [168]. The approach provides near-time-optimal performance in which only the proportional gain needs to be tuned based on changes in input voltage and load current.

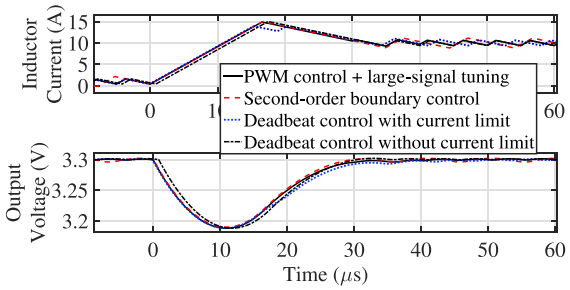


**FIGURE 43.** Time domain results corresponding to Fig. 42, adding a deadbeat controller [162] with a 15 A current limit.

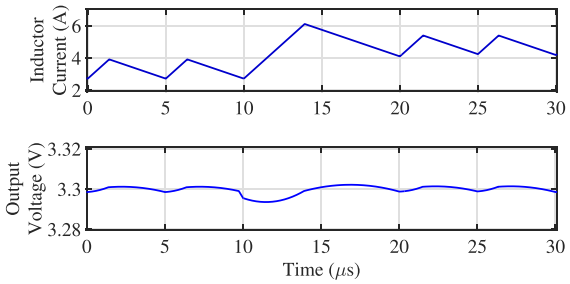


**FIGURE 44.** Transient performance of a CMC buck converter using large-signal tuning for a step change in $i_o$ from 3.3 A to 4.8 A with 12 V input.

## VII. SMALL-SIGNAL VS. LARGE-SIGNAL CONTROL

Small-signal controllers are suitable for a vast range of applications. The linkage to conventional frequency-domain design methods is helpful and supported by network analyzers and other test methods. The need to design for a specified operating point means that small-signal controllers have separate soft start and inrush management, protection management, and strategies to adapt to a wide load range. Extensive literature seeks to enhance dynamic performance.

In contrast, large-signal controllers support transitions between disparate operating points. Transitions can employ converter slew rate capabilities. Startup and fault management can be considered like operating points or enforced with switching boundaries. In applications with wide load ranges or fast dynamic requirements, large-signal controllers offer important alternatives.

For small-signal controllers and tuning methods, averaging and small perturbations are part of the process. Slew rates and dynamic trajectories are not considered, and the modeling steps limit the achievable performance. In large-signal geometric controls, fast switching dynamics are applied in the controllers and the tuning processes. "Control bandwidth" is a concept that implies a frequency-domain perspective and small-signal models. The time-domain framework of large-signal geometric controls is different, and response times are linked to slew rates rather than bandwidths. If a converter can slew quickly enough, recovery times from a disturbance can be faster than $T = 1/f_{sw}$. An example is shown in Fig. 44. For a load step from 3.3 A to 4.8 A (about 45%), large-signal

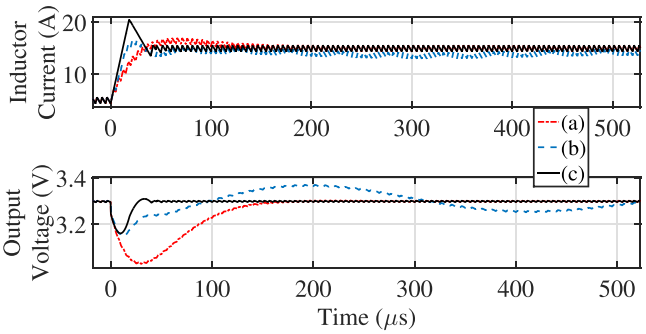


**FIGURE 45.** Load step-up transient response of a synchronous buck converter with $\Delta i_o = 10$ A. Trace (a) uses small-signal tuning for CMC, trace (b) uses small-signal tuning for VMC, and trace (c) uses large-signal tuning for VMC. The parameter set is in Table 2.

tuning as in Section VI-D results in 4.8 $\mu$s recovery time—less than one switching period. For this control, deadbeat recovery recovers synchronous switch action and holds the switching frequency effectively constant — notice the switch action at 10 $\mu$s and at 20 $\mu$s. It is also possible to constrain the timing and enforce constant switching frequency even through the transient. Details are given in [163]. A few case studies in this section explore broader performance capabilities.

### A. SUMMARY AND COMPARISON OF TUNING METHODS AND PARAMETERS FOR LOAD TRANSIENTS IN A BUCK CONVERTER

Table 8 summarizes small-signal and large-signal tuning for a buck converter given a step-up load transient, and corresponding simulation results are shown in Fig. 45. For small-signal methods, exact pole-zero cancellation is used as a best-case result, with $R$ corresponding to the post-step load. Fig. 45 shows that transient performance improves substantially with large-signal tuning.

Experimental converters were prepared as in Table 2. Load transient performance is explored in Fig. 46. The output voltage traces for the experimental tests are ac coupled to allow them to zoom in on transients and ripple. The controls have integral terms, so dc average values will return to the pre-disturbance values in these control studies.

For high-performance small-signal design, the relay based tuning approach in [131], [134], as discussed in Section V-A3, is used. For a load step-up transient in a buck converter, Fig. 46(a) shows that relay-based tuning results in 100 $\mu$s settling time (about 20 cycles in this case), 260 mV output voltage undershoot, and 1.5 A current overshoot.

Under the test conditions of Fig. 46(a), load transient performance based on (54) and (55) is shown in Fig. 46(b). Notice the faster time scale, which shows transient recovery within 20 $\mu$s (about four cycles), 160 mV voltage undershoot, and 2.5 A current overshoot for a step-up transient. The large-signal controller improves the settling time nearly five-fold compared to a more conventional approach. However, the current overshoot increases: faster recovery requires faster energy

**TABLE 8. Summary of Tuning Methods and Parameters for a $\Delta i_0$ Step-up Load Transient in a Buck Converter**

| Control method | Voltage controller $G_c$ | Tuning parameters | Tuning objectives and method |
|---|---|---|---|
| Small-signal CMC | $\frac{k_c\left(1+\frac{s}{\omega_{cz}}\right)}{s}=k_p+\frac{k_i}{s}$ | $\omega_{cz}=\frac{1}{RC},\ k_c=2\pi f_c\times\frac{1}{R},$ $k_p=\frac{k_c}{\omega_{cz}},\ k_i=k_c$ | Small-signal tuning in Section V-C1 with desired crossover frequency $f_c=\frac{f_{sw}}{10}$ |
| Small-signal VMC | $\frac{k_c\left(1+\frac{s}{\omega_{cz1}}\right)\left(1+\frac{s}{\omega_{cz2}}\right)}{s\left(1+\frac{s}{\omega_{cp1}}\right)\left(1+\frac{s}{\omega_{cp2}}\right)}$ | $\omega_{cp2}=\infty,\ \omega_{cp1}=2\pi f_c,$ $\omega_{cz1}+\omega_{cz2}=\frac{1}{RC},$ $\omega_{cz1}\omega_{cz2}=\frac{1}{LC},\ k_c=\frac{2\pi\sqrt{2}f_c}{v_{in}F_m}.$ | Small-signal tuning in Section V-A1 with desired phase margin of 45° and crossover frequency $f_c=\frac{f_{sw}}{10}$ |
| Large-signal CMC with load current feedforward | $k_p+\frac{k_i}{s}$ | $k_p\approx\frac{2C\sqrt{v_{in}v_{ref}}}{L\Delta i_o},\ k_i=\frac{\omega_o}{10}$ | Large-signal based tuning [168] method discussed in Section VI-D |
| Large-signal VMC | $k_p+\frac{k_i}{s}+\frac{k_d s}{s\tau_f+1}$ | $k_p\approx\frac{2C\sqrt{v_{in}v_{ref}}}{L\Delta i_o},\ k_i=\frac{\omega_o}{10},$ $k_d=C,\ \tau_f=T/200$ | Large-signal based tuning in [168] with $i_L-i_0$ replaced by $C\frac{dv_0}{dt}$ |

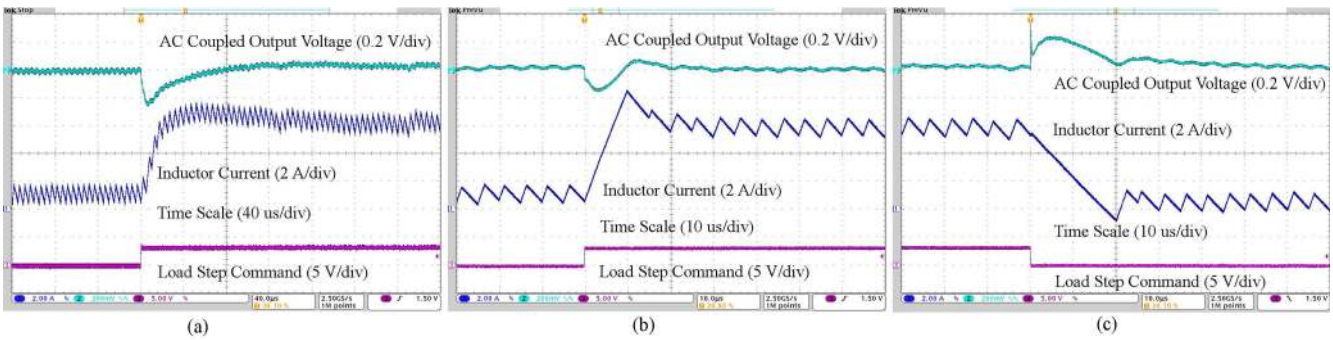


**FIGURE 46. Experimental load transient response of a buck converter from 1 A to 6 A, and vice-versa with 12 V input: (a) step-up response using small-signal relay-based tuning; (b) step-up response using large-signal tuning; (c) step-down response using large-signal tuning. The results are reproduced from [168].**

injection. For a load step-down transient, Fig. 46(c) shows that large-signal tuning results in 20 $\mu$s settling time, 220 mV voltage overshoot, and 1.6 A current undershoot. These results are essentially the same as for time optimal recovery for these transients.

The efficiency of a dc-dc converter is usually considered in steady state. However, frequent transients affect the overall efficiency. This is particularly important as transient step size increases. It is advantageous to minimize the switching event count during large-signal recovery. Time optimal recovery involves one switching action. Multiple switching actions following a conventional small-signal tuning method can reduce the overall efficiency. The same converter was exposed to load steps from 0.5 to 5 A and back every millisecond with $v_{in}=12$ V. The measured efficiency using large-signal tuning is found to be 90.6%, compared to 86.7% using relay-based tuning.

### *B. SUMMARY AND COMPARISON OF TUNING METHODS AND PARAMETERS FOR A REFERENCE TRANSIENT IN A BOOST CONVERTER*

Table 9 summarizes small-signal and large-signal tuning methods in a boost converter for a step-up reference transient, and corresponding simulation results are shown in Fig. 47 using the parameter set in Table 2. For small-signal methods, one of the controller poles is placed at the RHP zero frequency, with $R$ corresponding to the post-step load. Fig. 47 shows that the transient performance improves substantially using large-signal tuning — close to time-optimal performance. This trades against higher current overshoot and voltage undershoot. Minimum time recovery in a non-minimum phase converter will result in a larger output deviation [172], since the extra inductor energy to drive rapid output recovery is injected during the on-time when the output is decaying. The current overshoot and voltage undershoot can be reduced in

**TABLE 9. Summary of Tuning Methods and Parameters for a Step-Up Reference Transient With a Step-Size $\Delta v_{\text{ref}}$ in a Boost Converter**

| Control method | Voltage controller $G_c$ | Tuning parameters | Tuning objectives and method |
|---|---|---|---|
| Small-signal CMC | $\dfrac{k_c\left(1+\dfrac{s}{\omega_{cz}}\right)}{s\left(1+\dfrac{s}{\omega_{cp}}\right)}$ | $\omega_{\text{cz}}=\dfrac{2}{RC},\ \omega_{\text{cp}}=\omega_{\text{rhp}},$ $k_{\text{c}}=2\pi f_{\text{c}}\times\dfrac{2}{R(1-D)}.$ | Small-signal tuning in Section V-C2 with desired crossover frequency $f_{\text{c}}=\dfrac{f_{\text{rhp}}}{3}$ |
| Small-signal VMC | $\dfrac{k_{\text{c}}\left(1+\dfrac{s}{\omega_{\text{cz1}}}\right)\left(1+\dfrac{s}{\omega_{\text{cz2}}}\right)}{s\left(1+\dfrac{s}{\omega_{\text{cp1}}}\right)\left(1+\dfrac{s}{\omega_{\text{cp2}}}\right)}$ | $\omega_{\text{cp2}}=\infty,\ \omega_{\text{cp1}}=\omega_{\text{rhp}},$ $\omega_{\text{cz1}}+\omega_{\text{cz2}}=\dfrac{1}{RC},$ $\omega_{\text{cz1}}\omega_{\text{cz2}}=\dfrac{(1-D)^2}{LC},$ $k_{\text{c}}=2\pi f_{\text{c}}\times\dfrac{(1-D)}{F_{\text{m}}V_{\text{ref}}}$ | Small-signal tuning in Section V-A4 with desired phase margin of around 60 degree and crossover frequency $f_{\text{c}}=\dfrac{f_{\text{rhp}}}{5}$ |
| Large-signal CMC with load current feedforward | $k_{\text{p}}+\dfrac{k_i}{s}$ | $k_{\text{p}}\approx\sqrt{\dfrac{C}{L}}\left[\sqrt{\dfrac{2(v_{\text{ref}}-v_{\text{in}})}{\Delta v_{\text{ref}}}-1}\right]$ $-\dfrac{3Dv_{\text{ref}}i_o}{2v_{\text{in}}\Delta v_{\text{ref}}};\quad k_i=\dfrac{\omega_o}{20}.$ | Large-signal based tuning [170] method with normalized load current feedforward discussed in Section VI-D |

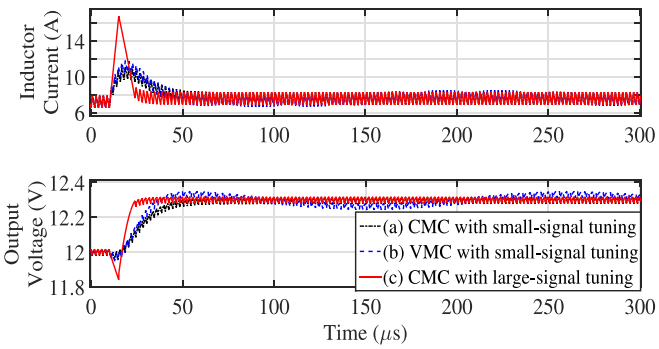


**FIGURE 47. Step-up reference transient response of a boost converter with 8 V input.**

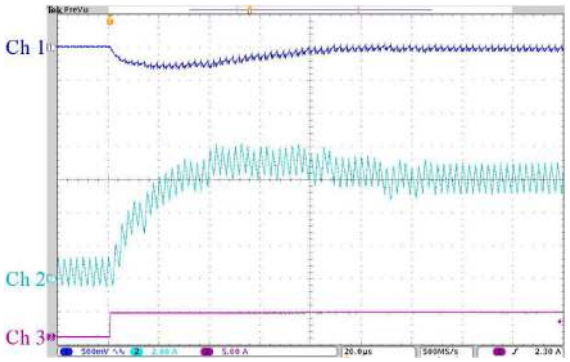


**FIGURE 48. Experimental load transient response of a CMC boost converter with small-signal tuning for a step change in $i_o$ from 0.4 A to 4.8 A. Ch 1, Ch 2, and Ch 3 indicate the ac coupled output voltage (500 mV/div), the inductor current (2 A/div), and the load current (5 A/div), on a time scale of 20 $\mu$s/div. The results are reproduced from [170].**

large-signal tuning by setting current and voltage limits, as discussed in [170].

### C. SUMMARY AND COMPARISON OF LOAD TRANSIENT RESPONSE IN A BOOST CONVERTER

An experimental boost converter with the parameters in Table 2 was prepared to compare load transient performance. Fig. 48 shows transient response of a CMC boost converter, in which the PI voltage controller is designed following the small-signal design steps in Section V-C1. Keeping in mind $f_{\text{rhp}}$, the desired phase margin and crossover frequency are set to 48° and 10 kHz; consequently, the controller gains are found to be $k_p = 11.5$ and $k_{\text{int}} = 0.98$. Small-signal tuning results in 72 $\mu$s recovery time (about 28 switching cycles).

Fig. 49 shows experimental transient response of this synchronous boost converter to a step change in load current from 0.4 to 4.8 A with large-signal tuning. Without a current limit, the step change results in near-time-optimal recovery with 8 $\mu$s settling time (about four switching cycles), 11.5 A peak current, and 300 mV voltage undershoot as shown in Fig. 49(a). This achieves almost nine times faster response than that using small-signal tuning. The result shows that geometric controllers can manage non-minimum phase converters. This comparative study is summarized in Table 10. Using the same gain, if an inductor current limit of 8 A is imposed, the voltage undershoot decreases to 250 mV, but the response time increases to 16.8 $\mu$s as shown in Fig. 49(b). The response time and voltage undershoot are reduced to 11.2 $\mu$s and 220 mV as compared to the current-limiting case when a 200 mV voltage-deviation constraint is imposed, as shown in Fig. 49(c). The actual deviation is more than the constraint because of sampling delay. Fig. 50 shows phase plane plots corresponding to time responses in Fig. 49. These results were

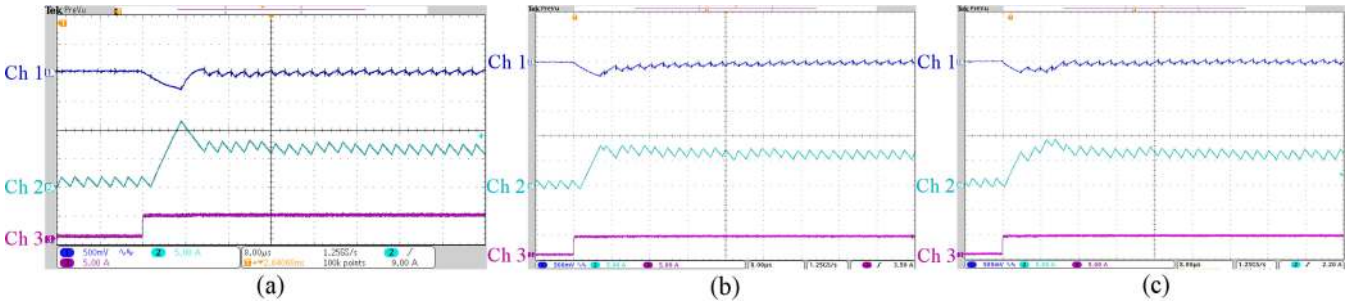


**FIGURE 49.** Transient response of a boost converter with large-signal tuning for a step change in load current from 0.4 A to 4.8 A for gains $k_p = 16$ and $k_i = 0.015$ with 8 V input and 12 V output (a) without current and voltage limits, (b) with 8 A current limit, and (c) with 200 mV voltage deviation limit. Ch 1, Ch 2, and Ch 3 indicate the ac coupled output voltage (500 mV/div), the inductor current (5 A/div), and the load current (5 A/div), respectively, with a time scale of 8 $\mu$s/div. The results are reproduced from [170].

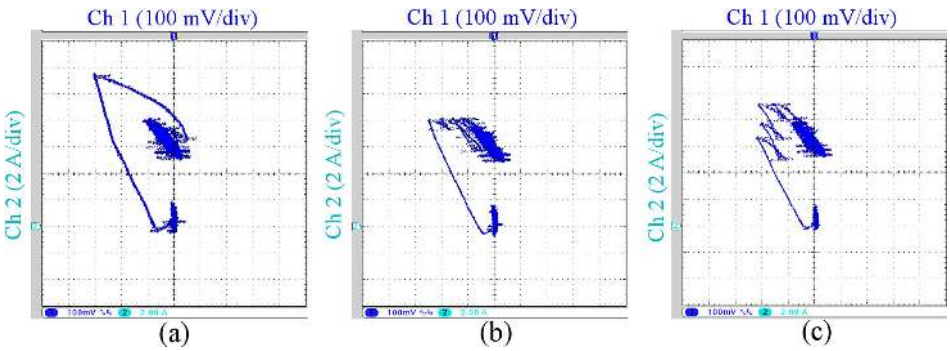


**FIGURE 50.** Experimental results, with (a), (b), and (c) showing phase-plane plots corresponding to load transient responses in Fig. 49. Ch 1 and Ch 2 indicate the ac coupled output voltage and inductor current, respectively. The results are reproduced from [170].

**TABLE 10.** Transient Response for a Boost Converter Load-step Change From 0.4 to 4.8 A. The Table is from [170]

| Control Methods | | Settling time | Voltage undershoot |
|---|---|---|---|
| Small-signal tuning | | 72 $\mu$s | 320 mV |
| Large-signal based tuning | Unconstrained $i_L$ and $v_o$ limit | 8 $\mu$s | 300 mV |
| | Constained $i_L$ with 8 A limit | 16.8 $\mu$s | 250 mV |
| | Constrained 200 mV $v_o$ limit | 11.2 $\mu$s | 220 mV |

reported earlier in [172]. A designer can trade off voltage deviation and current limits based on the performance index guide in [173].

To test efficiency, the same boost converter was tested with a load step from 0.5 to 5 A and back, imposed once per millisecond. Small-signal tuning achieved 81% energy efficiency, whereas large-signal tuning achieved 85%. This effect is linked to the reduced switch action during recovery with a large-signal geometric control.

## VIII. CONCLUSION

This paper considers various conventional and geometric control techniques along with their design methods. Both small-signal and large-signal based design approaches are discussed for well-known PWM control methods for hard-switched dc-dc converters. A summary of outcomes is as follows:

- Small-signal models and tuning have the advantage of linking to long-established frequency-domain design tools. By following known rules and conventional procedures, a designer can achieve performance limited to bandwidths governed by the lesser of $f_{sw}/10$ or $f_{rhp}/3$. The performance can be robust (if this is designed in), although oscillatory, and can be mapped into digital formats.
- Small-signal models and methods do not provide systematic ways to run dynamic response up to slew rate limits and do not account for nonlinear considerations such as current limits or duty ratio saturation.
- By definition, small-signal controls need separate blocks for large-signal startup and fault protection.
- Large-signal controls tuned based on geometric perspectives can drive dynamic response up to converter slew-rate limits.

- In geometric controls, aspects such as startup and fault protection can be visualized as involving multi-segment boundaries.
- The robustness and sensitivity issues are actually fairly consistent between small-signal and large-signal methods: Both benefit from parameter information, both benefit from feedforward, both work best when the model is complete and accurate, and both benefit from adaptation to changing conditions.
- In geometric controls, simple linear boundaries are rarely the best solutions, and this observation tends to be an important consideration in using large-signal vs. small-signal control approaches. The results presented in the paper show how feedforward information can allow boundaries to adapt.
- State-feedback-based design is an important alternative to conventional output feedback for CMC design.

Control of dc-dc converters typically is implemented with PWM ramps and comparators. Small-signal models derived from averaging are convenient for application of conventional control system design tools. However, these models imply dynamics slower than the switching frequency. Geometric controls based on piecewise-linear large-signal analysis can implement the fastest possible dynamic response. Low-cost digital controls are facilitating fast sampling and switching boundary controls. Online adaptive geometric controls have promise for high-performance dc-dc converters. The review and tutorial framework provided here is intended to serve as a base for access to a wide range of prior work on dc-dc converter control and tuning. It also motivates future work on state-feedback alternatives and adaptive large-signal tuning for high-performance dc-dc converters.

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## REFERENCES

[1] A. Stupar, T. McRae, N. Vukadinovic, A. Prodic, and J. A. Taylor, "Multi-objective optimization of multi-level DC-DC converters using geometric programming," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 11 912–11 939, Dec. 2019.

[2] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of DC-DC converter systems," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 288–300, Jan. 2009.

[3] Y. Yuan, F. C. Y. Lee, and J. E. Triner, "Power converter design optimization," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-15, no. 3, pp. 344–355, May 1979.

[4] W. W. Burns and T. G. Wilson, "State trajectories used to observe and control DC-to-DC converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-12, no. 6, pp. 706–717, Nov. 1976.

[5] W. W. Burns and T. G. Wilson, "Analytic derivation and evaluation of a state-trajectory control law for DC-to-DC converters," in *Rec. IEEE Power Electron. Spec. Conf.*, 1977, pp. 70–85.

[6] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Parameter-independent time-optimal digital control for point-of-load converters," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2235–2248, Oct. 2009.

[7] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimovic, "Proximate time-optimal digital control for synchronous buck DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008.

[8] L. Corradini, A. Babazadeh, A. Bjeletic, and D. Maksimovic, "Current-limited time-optimal response in digitally controlled DC-DC converters," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2869–2880, Nov. 2010.

[9] A. M. Wu and S. R. Sanders, "An active clamp circuit for voltage regulation module (VRM) applications," *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 623–634, Sep. 2001.

[10] P. T. Krein, "Feasibility of geometric digital controls and augmentation for ultrafast DC-DC converter response," in *Proc. IEEE Workshop Comput. Power Electron.*, Jul. 2006, pp. 48–56.

[11] S. Kapat, P. S. Shenoy, and P. T. Krein, "Near-null response to large-signal transients in an augmented buck converter: A geometric approach," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3319–3329, Jul. 2012.

[12] A. Stupar, Z. Lukic, and A. Prodic, "Digitally-controlled steered-inductor buck converter for improving heavy-to-light load transient response," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 3950–3954.

[13] D. C. Hamill and D. J. Jeffries, "Subharmonics and chaos in a controlled switched-mode power converter," *IEEE Trans. Circuits Syst.*, vol. 35, no. 8, pp. 1059–1061, Aug. 1988.

[14] J. R. Wood, "Chaos: A real phenomenon in power electronics," in *Proc. IEEE Appl. Power Electron. Conf.*, 1989, pp. 115–124.

[15] J. H. B. Deane and D. C. Hamill, "Instability, subharmonics, and chaos in power electronic systems," *IEEE Trans. Power Electron.*, vol. 5, no. 3, pp. 260–268, Jul. 1990.

[16] C. Pascual, Z. Song, P. T. Krein, D. V. Sarwate, P. Midya, and W. J. Roeckner, "High-fidelity PWM inverter for digital audio amplification: Spectral analysis, real-time DSP implementation, and results," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 473–485, Jan. 2003.

[17] D. M. Sable, B. H. Cho, and R. B. Ridley, "Use of leading-edge modulation to transform boost and flyback converters into minimum-phase-zero systems," *IEEE Trans. Power Electron.*, vol. 6, no. 4, pp. 704–711, Oct. 1991.

[18] V. Yousefzadeh, M. Shirazi, and D. Maksimovic, "Minimum phase response in digitally controlled boost and flyback converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2007, pp. 865–870.

[19] C. W. Deisch, "Simple switching control method changes power converter into a current source," in *Rec. IEEE Power Electron. Spec. Conf.*, 1978, pp. 300–306.

[20] P. Midya, P. T. Krein, and M. F. Greuel, "Sensorless current mode control-an observer-based technique for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 522–526, Jul. 2001.

[21] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109–124, Apr. 1987.

[22] J.-H. Cheng and A. F. Witulski, "Steady-state and large-signal design of current-programmed DC-DC converters," *IEEE Trans. Power Electron.*, vol. 12, no. 4, pp. 743–751, Jul. 1997.

[23] L. Dixon, "Average current mode control of switching power supplies," Unitrode Application Note U-140, Texas Instruments, 1999.

[24] G. Eirea and S. R. Sanders, "Phase current unbalance estimation in multiphase buck converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 137–143, Jan. 2008.

[25] V. Svikovic, J. J. Cortes, P. Alou, J. A. Oliver, O. Garcia, and J. A. Cobos, "Multiphase current-controlled buck converter with energy recycling output impedance correction circuit (OICC)," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5207–5222, Sep. 2015.

[26] B. Halivni and M. M. Peretz, "Digital controller for high-performance multiphase VRM with current balancing and near-ideal transient response," in *Proc. IEEE Appl. Power Electron. Conf.*, 2020, pp. 2206–2213.

[27] G. Garcera, E. Figueres, and A. Mocholi, "Novel three-controller average current mode control of DC-DC PWM converters with improved robustness and dynamic response," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 516–528, May 2000.

[28] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 301–308, Jan. 2003.

[29] H. Peng, A. Prodic, E. Alarcon, and D. Maksimovic, "Modeling of quantization effects in digitally controlled DC-DC converters," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 208–215, Jan. 2007.

[30] "Dxd audio format, Merging Technologies." [Online]. Available: http://www.merging.com/highlights/high-resolution.

[31] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Rec. IEEE Power Electron. Spec. Conf.*, 1997, pp. 21–27.

[32] C. Huang and P. K. T. Mok, "A delay-line-based voltage-to-duty-cycle controller for high-frequency PWM switching converters," *IEEE Trans. Circuits Syst. II*, vol. 62, no. 8, pp. 751–755, Aug. 2015.

[33] A. V. Peterchev, J. Xiao, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 356–364, Jan. 2003.

[34] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital pwm controller ic for dc-dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 438–446, Jan. 2003.

[35] L. Corradini, W. Stefanutti, and P. Mattavelli, "Analysis of multisampled current control for active filters," *IEEE Trans. Ind. Appl.*, vol. 44, no. 6, pp. 1785–1794, Nov./Dec. 2008.

[36] R. W. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three phase soft-switched high-power-density DC/DC converter for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.

[37] T. Hirose and H. Matsuo, "A consideration of bidirectional superposed dual active bridge DC-DC converter," in *Proc. IEEE Int'l. Symp. Power Electron. Distrib. Gener. Syst.*, 2010, pp. 39–46.

[38] F. Krismer and J. W. Kolar, "Accurate small-signal model for the digital control of an automotive bidirectional dual active bridge," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2756–2768, Dec. 2009.

[39] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Overview of dual-active-bridge isolated bidirectional DC-DC converter for high-frequency-link power-conversion system," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4091–4106, Aug. 2014.

[40] N. Hou and Y. W. Li, "Overview and comparison of modulation and control strategies for a nonresonant single-phase dual-active-bridge dc-dc converter," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 3148–3172, Mar. 2020.

[41] A. S. Kislovski, R. Redl, and N. O. Sokal, *Dynamic Analysis of Switching-Mode DC/DC Converters*. Lexington, MA: Design Automation, 1991.

[42] W. McMurray, "A constant turn-off time control for variable frequency thyristor inverters," *IEEE Trans. Ind. Appl.*, vol. IA-13, no. 5, pp. 418–422, Sep. 1977.

[43] T. Szepesi, "Stabilizing the frequency of hysteretic current-mode DC/DC converters," *IEEE Trans. Power Electron.*, vol. PE-2, no. 4, pp. 302–312, Oct. 1987.

[44] V. Repecho, D. Biel, J. M. Olm, and E. F. Colet, "Switching frequency regulation in sliding mode control by a hysteresis band controller," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1557–1569, Feb. 2017.

[45] W. McMurray, "Silicon-controlled rectifier DC-to-DC power converters," *IEEE Trans. Comm. Electron.*, vol. 83, no. 71, pp. 198–203, Mar. 1964.

[46] D. Y. Chen, H. A. Owen, T. G. Wilson, and T. G. Wilson Jr, "Design of reasctors for single-winding constant on-time and constant off-time DC-to-DC converters operating in the discontinuous mode," *IEEE Trans. Magn.*, vol. MAG-17, no. 6, pp. 3290–3292, Nov. 1981.

[47] P. T. Krein, *Elements of Power Electronics*, 2nd ed. New York: Oxford University Press, 2015.

[48] D. Maksimovic and S. Cuk, "A unified analysis of PWM converters in discontinuous modes," *IEEE Trans. Power Electron.*, vol. 6, no. 3, pp. 476–490, Jul. 1991.

[49] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 1990, pp. 792–801.

[50] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York: Kluwer, 2004.

[51] B. Sahu and G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time pulse-frequency modulation (PFM) control," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 2, pp. 312–321, Feb. 2007.

[52] B. C. Mandi, S. Kapat, and A. Patra, "Unified digital modulation techniques for DC-DC converters over a wide operating range: Implementation, modeling, and design guidelines," *IEEE Trans. Circuits Syst. I*, vol. 65, no. 4, pp. 1442–1453, Apr. 2018.

[53] L. Corradini, A. Bjeletic, R. Zane, and D. Maksimovic, "Fully digital hysteretic modulator for DC-DC switching converters," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2969–2979, Oct. 2011.

[54] S. Kapat, "Parameter-insensitive mixed-signal hysteresis-band current control for point-of-load converters with fixed frequency and robust stability," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5760–5770, Jul. 2017.

[55] D. C. Hamill, J. H. B. Deane, and D. J. Jefferies, "Modeling of chaotic DC-DC converters by iterated nonlinear mappings," *IEEE Trans. Power Electron.*, vol. 7, no. 1, pp. 25–36, Jan. 1992.

[56] P. Luo, L. Luo, Z. Li, J. Yang, and G. Chen, "Skip cycle modulation in switching DC-DC converter," in *Proc. IEEE Int'l. Conf. Comm. Circuits Syst.*, 2002, pp. 1716–1719.

[57] A. V. Peterchev and S. R. Sanders, "Digital loss-minimizing multimode synchronous buck converter control," in *Proc. IEEE Power Electron. Spec. Conf.*, 2004, pp. 3694–3699.

[58] "8-pin high performance resonant mode controller," Texas Instruments, Dallas. UCC25700, Sep. 2008. [Online]. Available: http://focus.ti.com/lit/ds/symlink/ucc25600.pdf

[59] L. Huber and M. M. Jovanovic, "Analysis and comparison of audible noise caused by magnetic components in switch-mode power supplies operating in burst mode and frequency-foldback mode," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5299–5308, Sep. 2015.

[60] D. Maksimovic, Y. Jang, and R. W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 578–584, Jul. 1996.

[61] R. Zane and D. Maksimovic, "Nonlinear-carrier control for high-power-factor rectifiers based on up-down switching converters," *IEEE Trans. Power Electron.*, vol. 13, no. 2, pp. 213–221, Mar. 1998.

[62] J. Li and F. C. Lee, "Modeling of $V^2$ current-mode control," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 9, pp. 2552–2563, Sep. 2010.

[63] V. Michal, "Modulated-ramp PWM generator for linear control of the boost converter's power stage," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2958–2965, Jun. 2012.

[64] M. Telefus, A. Shteynberg, M. Ferdowsi, and A. Emadi, "Pulse train control technique for flyback converter," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 757–764, May 2004.

[65] "Critical conduction mode pfc controller utilizing a transconductance error amplifier," ON Semiconductor, Jul. 2015. [Online]. Available: https://www.onsemi.com/pub/Collateral/NCP1608-D.PDF

[66] K. Hariharan, S. Kapat, and S. Mukhopadhyay, "Constant off-time digital current-mode controlled boost converters with enhanced stability boundary," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 10 270–10 281, Oct. 2019.

[67] A. M. Stankovic, G. Escobar, R. Ortega, and S. R. Sanders, "Energy-based control in power electronics," in *Nonlinear Phenomena in Power Electronics*, S. Banerjee and G. C. Verghese, Eds. New York: IEEE Press, 2001.

[68] J. Sun, "Characterization and performance comparison of ripple-based control for voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 346–353, Mar. 2006.

[69] R. Redl and J. Sun, "Ripple-based control of switching regulators – an overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.

[70] P. Midya, P. T. Krein, R. J. Turnbull, R. Reppa, and J. Kimball, "Dynamic maximum power point tracker for photovoltaic applications," in *Rec. IEEE Power Electron. Spec. Conf.*, 1996, pp. 1710–1716.

[71] S. Lee, "Demystifying type II and type III compensators using op-amp and OTA for DC-DC converters," Texas Instruments Application Report SLVA662, Jul. 2014. [Online]. Available: http://www.ti.com/lit/an/slva662/slva662.pdf

[72] D. Mitchell, *DC-DC Switching Regulator Analysis*. NewYork: McGraw-Hill, 1988.

[73] W. Tang, F. C. Lee, R. B. Ridley, and I. Cohen, "Charge control: Modeling, analysis, and design," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 396–403, Oct. 1993.

[74] P. T. Krein and P. Midya, "Nonlinear noise effects in power converters," in *Nonlinear Phenomena in Power Electronics*, S. Banerjee and G. C. Verghese, Eds. New York: IEEE Press, 2001.

[75] N. O. Sokal, "System oscillations from negative input resistance at power input port of switching-mode regulator, amplifier, DC-DC converter, or DC-AC inverter," in *Rec. IEEE Power Electron. Spec. Conf.*, 1973, pp. 138–140.

[76] B. Choi, B. H. Cho, and S.-S. Hong, "Dynamics and control of DC-to-DC converters driving other converters downstream," *IEEE Trans. Circuits Syst. I*, vol. 46, no. 10, pp. 1240–1248, Oct. 1999.

[77] M. Anun, M. Ordonez, I. G. Zurbriggen, and G. C. Oggier, "Circular switching surface technique: High-performance constant power load stabilization for electric vehicle systems," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4560–4572, Aug. 2015.

[78] Y. Azadeh, E. Babaei, H. Tarzamni, and M. Sabahi, "Single-inductor dual-output DC-DC converter with capability of feeding a constant power load in open-loop manner," *IEEE Trans. Ind. Electron.*, vol. 66, no. 9, pp. 6906–6915, Sep. 2019.

[79] A. Kwasinski, W. Weaver, and R. Balog, *Microgrids and Other Local Area Power and Energy Systems*. Cambridge, UK: Cambridge University Press, 2016.

[80] B. A. Martinez-Trevino, A. El Aroudi, A. Cid-Pastor, and L. Martinez-Salamero, "Nonlinear control for output voltage regulation of a boost converter with a constant power load," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10 381–10 385, Nov. 2019.

[81] T. Qian, "Subharmonic analysis for buck converters with constant on-time control and ramp compensation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1780–1786, May 2013.

[82] G. Zhou, S. Mao, S. Zhou, Y. Wang, and T. Yan, "Discrete-time modeling and symmetrical dynamics of $V^2$ controlled buck converters with trailing-edge and leading-edge modulations," *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 8, to appear 2020.

[83] J. Cortes, V. Svikovic, P. Alou, J. A. Oliver, J. A. Cobos, and R. Wisniewski, "Accurate analysis of subharmonic oscillations of $V^2$ and $V^2I_c$ controls applied to buck converter," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 1005–1018, Feb. 2015.

[84] S. Kapat and P. T. Krein, "Improved time optimal control of a buck converter based on capacitor current," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1444–1454, Mar. 2012.

[85] S. Kapat and P. T. Krein, "Formulation of PID control for DC-DC converters based on capacitor current: A geometric context," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1424–1432, Mar. 2012.

[86] M. Clique and A. J. Fossard, "Design of feedback laws for DC-DC converters using modern control theory," in *Rec. IEEE Power Electron. Spec. Conf.*, 1978, pp. 2–11.

[87] F. E. Thau, "A feedback compensator design procedure for switching regulators," *IEEE Trans. Ind. Electron. Cont. Instrum.*, vol. IECI-26, no. 2, pp. 104–110, May 1979.

[88] K. M. Smedley and S. Cuk, "One-cycle control of switching converters," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 625–633, Nov. 1995.

[89] P. Peltoniemi, P. Nuutinen, and J. Pyrhonen, "Observer-based output voltage control for DC power distribution purposes," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1914–1926, Apr. 2013.

[90] G. Joos, P. D. Ziogas, and D. Vincenti, "A model reference adaptive PWM technique," in *Rec. IEEE Power Electron. Spec. Conf.*, 1989, pp. 695–703.

[91] T. Geyer, G. Papafotiou, and M. Morari, "Hybrid model predictive control of the step-down DC-DC converter," *IEEE Trans. Control System Tech.*, vol. 16, no. 6, pp. 2552–2563, Nov. 2008.

[92] P. Karamanakos, T. Geyer, and S. Manias, "Direct voltage control of DC-DC boost converters using enumeration-based model predictive control," *IEEE Trans. Power Electron.*, vol. 29, no. 2, pp. 968–978, Feb. 2014.

[93] B. Arbetter and D. Maksimovic, "Feedforward pulse width modulators for switching power converters," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 361–368, Mar. 1997.

[94] R. Redl and N. O. Sokal, "Near-optimum dynamic regulation of DC-DC converters using feed-forward of output current and input voltage with current-mode control," *IEEE Trans. Power Electron.*, vol. PE-1, no. 3, pp. 181–189, Jul. 1986.

[95] A. Soto, P. Alou, and J. Cobos, "Nonlinear digital control breaks bandwidth limitations," in *Proc. IEEE Appl. Power Electron. Conf.*, 2006, pp. 724–730.

[96] N. B. O. L. Pettit, *The Analysis of Piecewise Linear Dynamical Systems*. Tauntin, UK: Research Studies Press, 1995.

[97] D. Liberzon, *Switching in Systems and Control*. Boston: Birkhauser, 2003.

[98] P. Pejovic and D. Maksimovic, "An algorithm for solving piecewise-linear networks that include elements with discontinuous characteristics," *IEEE Trans. Circuits Syst. I*, vol. 43, no. 6, pp. 453–460, Jun. 1996.

[99] T. Saito, T. Kabe, Y. Ishikawa, Y. Matsuoka, and H. Torikai, "Piecewise constant switched dynamical systems in power electronics," *Int'l. J. Bifurcation Chaos*, vol. 17, no. 10, pp. 3373–3386, 2007.

[100] R. C. Wong, H. A. Owen, and T. G. Wilson, "An efficient algorithm for the time-domain simulation of regulated energy-storage DC-to-DC converters," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 154–168, Apr. 1987.

[101] P. Pejovic and D. Maksimovic, "A method for fast time-domain simulation of networks with switches," *IEEE Trans. Power Electron.*, vol. 9, no. 4, pp. 449–456, Jul. 1994.

[102] J. H. Alimeling and W. P. Hammer, "PLECS-piece-wise linear electrical circuit simulation for simulink," in *Proc. IEEE Int'l. Conf. Power Electron. Drive Syst.*, 1999, pp. 355–360.

[103] J. A. Cadzow and H. R. Martens, *Discrete-time and Computer Control Systems*. Englewood Cliffs, NJ: Prentice-Hall, 1970.

[104] A. Capel, J. G. Ferrante, and R. Prajoux, "Dynamic behaviour and Z-transform stability analysis of DC/DC regulators with a non linear PWM control loop," in *Rec. IEEE Power Electron. Spec. Conf.*, 1973, pp. 149–157.

[105] F. C. Y. Lee, R. P. Iwens, Y. Yu, and J. E. Triner, "Generalized computer-aided discrete time-domain modeling and analysis of DC-DC converters," *IEEE Trans. Ind. Electron. Cont. Instrum.*, vol. IECI-26, no. 2, pp. 58–69, May 1979.

[106] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," in *Rec. IEEE Power Electron. Spec. Conf.*, 1981, pp. 349–369.

[107] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A general approach to sampled-data modeling for power electronic circuits," *IEEE Trans. Power Electron.*, vol. PE-1, no. 2, pp. 76–89, Apr. 1986.

[108] F. Huliehel and S. Ben-Yaakov, "Low-frequency sampled-data models of switched mode DC-DC converters," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 55–61, Jan. 1991.

[109] X. Cui, C. Keller, and A. Avestruz, "A 5 MHz high-speed saturating inductor DC-DC converter using cycle-by-cycle digital control," in *Proc. IEEE Workshop Control Model. Power Electron.*, 2019, pp. 1–8.

[110] C. Zhang, J. Wang, S. Li, B. Wu, and C. Qian, "Robust control for PWM-based DC-DC buck power converters with uncertainty via sampled-data output feedback," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 504–515, Jan. 2015.

[111] S. Banerjee and P. Ranjan, "Border collision bifurcations in the current-mode-controlled boost converter," in *Nonlinear Phenomena in Power Electronics*, S. Banerjee and G. C. Verghese, Eds. New York: IEEE Press, 2001.

[112] H. K. Khalil, *Nonlinear Systems*. New York: Macmillan, 1992.

[113] G. W. Wester and R. D. Middlebrook, "Low-frequency characterization of switched DC-DC converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-9, no. 3, pp. 376–385, May 1973.

[114] S. R. Sanders and G. C. Verghese, "Synthesis of averaged circuit models for switched power converters," *IEEE Trans. Circuits Syst.*, vol. 38, no. 8, pp. 905–915, Aug. 1991.

[115] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *Rec. IEEE Power Electron. Spec. Conf.*, 1976, pp. 18–34.

[116] H. Sira-Ramirez and M. D. deNieto, "A Lagrangian approach to average modeling of pulsewidth-modulation controlled dc-to-dc power converters," *IEEE Trans. Circuits Syst. I*, vol. 43, no. 5, pp. 427–430, May 1996.

[117] P. T. Krein, J. Bentsman, R. M. Bass, and B. L. Lesieutre, "On the use of averaging for the analysis of power electronic systems," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 182–190, Apr. 1990.

[118] B. Lehman and R. M. Bass, "Extensions of averaging theory for power electronic systems," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 542–553, Jul. 1996.

[119] S. R. Sanders, J. M. Noworolski, X. Z. Liu, and G. C. Verghese, "Generalized averaging method for power conversion circuits," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 251–259, Apr. 1991.

[120] S. Arora, P. Balsara, and D. Bhatia, "Input-output linearization of a boost converter with mixed load (constant voltage load and constant power load)," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 815–825, Jan. 2019.

[121] M. Cupelli, M. Moghimi, A. Riccobono and A. Monti, "A comparison between synergetic control and feedback linearization for stabilizing MVDC microgrids with constant power load," in *Proc. IEEE PES Innovative Smart Grid Tech.*, Istanbul, Turkey, 2014.

[122] H. Sira-Ramirez and M. Rios-Bolivar, "Sliding mode control of DC-to-DC power converters via extended linearization," *IEEE Trans. Circuits Syst. I*, vol. 41, no. 10, pp. 652–661, Oct. 1994.

[123] H. Sira-Ramirez, "Sliding motions in bilinear switched networks," *IEEE Trans. Circuits Syst.*, vol. 34, no. 8, pp. 919–933, Aug. 1987.

[124] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 1998, pp. 170–176.

[125] K. Yao, K. Lee, M. Xu, and F. C. Lee, "Optimal design of the active droop control method for the transient response," in *Proc. IEEE Appl. Power Electron. Conf.*, 2003, pp. 718–723.

[126] J. Sun, D. M. Mitchell, M. F. Greuel, P. T. Krein, and R. M. Bass, "Averaged modeling of PWM converters operating in discontinuous conduction mode," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 482–492, Jul. 2001.

[127] V. Vorperian, "Simplified analysis of PWM converters using model of PWM switch. II. Discontinuous conduction mode," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 26, no. 3, pp. 497–505, May 1990.

[128] C. K. Tse, "Flip bifurcation and chaos in three-state boost switching regulators," *IEEE Trans. Circuits Syst. I*, vol. 41, no. 1, pp. 16–23, Jan. 1994.

[129] C. Olalla, R. Leyva, I. Queinnec, and D. Maksimovic, "Robust gain-scheduled control of switched-mode dc-dc converters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3006–3019, Jun. 2012.

[130] K. H. Ang, G. Chong, and Y. Li, "PID control system analysis, design, and technology," *IEEE Trans. Cont. Syst. Tech.*, vol. 13, no. 4, pp. 559–576, Jul. 2005.

[131] K. J. Astrom and T. Hagglund, *Automatic Tuning of PID Controllers*. Research Triangle Park, NC: Instrum. Soc. Amer., 1988.

[132] L. Corradini, P. Mattavelli, W. Stefanutti, and S. Saggini, "Simplified model reference-based autotuningfor digitally controlled SMPS," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1956–1963, Jul. 2008.

[133] J. Morroni, R. Zane, and D. Maksimovic, "Design and implementation of an adaptive tuning system based on desired phase margin for digitally controlled DC-DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 559–564, Feb. 2009.

[134] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of digitally controlled DC-DC converters based on relay feedback," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 199–207, Jan. 2007.

[135] M. Shirazi, R. Zane, and D. Maksimovic, "An autotuning digital controller for DC-DC power converters based on online frequency-response measurement," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2578–2588, Nov. 2009.

[136] V. Yousefzadeh and S. Choudhury, "Nonlinear digital PID controller for DC-DC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 1704–1709.

[137] K. J. Astrom and T. Hagglund, *Advanced PID Control*. NC Research Tech. Park: ISA, 2005.

[138] R. D. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 36–52, Jan. 1989.

[139] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109–124, Apr. 1987.

[140] G. C. Verghese, C. A. Bruzos, and K. N. Mahabir, "Averaged and sampled-data models for current mode control: A re-examination," in *Rec. IEEE Power Electron. Spec. Conf.*, 1989, pp. 484–491.

[141] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[142] C. Gezgin, B. S. Heck, and R. M. Bass, "Simultaneous design of power stage and controller for switching power supplies," *IEEE Trans. Power Electron.*, vol. 12, no. 3, pp. 558–566, May 1997.

[143] C. Olalla, R. Leyva, A. El Aroudi, and I. Queinnec, "Robust LQR control for PWM converters: An LMI approach," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2548–2558, Jul. 2009.

[144] M. Zhang, X. Li, J. Liu, and H. Su, "Dual-mode LQR-feedforward optimal control for non-minimum phase boost converter," *IET Power Electron.*, vol. 10, no. 1, pp. 92–102, Jan. 2017.

[145] J. Falin, T. Allag, and B. Hopf, "Compensating the current-mode controlled boost converter," Texas Instruments, Dallas, Jul. 2012. [Online]. Available: http://www.ti.com/lit/an/slva452/slva452.pdf.

[146] K. Ogata, *Modern Control Engineering*. Upper Saddle River NJ USA: Prentice-Hall, 2002.

[147] K. Yao, Y. Ren, and F. C. Lee, "Critical bandwidth for the load transient response of voltage regulator modules," *IEEE Trans. Power Electron.*, vol. 19, no. 6, pp. 1454–1461, Nov. 2004.

[148] R. Brockett, "The early days of geometric nonlinear control," *Automatica*, vol. 50, no. 9, pp. 2203–2224, 2014.

[149] V. Utkin, J. Guldner, and J. Shi, *Sliding Mode Control in Electromechanical Systems*, 2nd ed. Boca Raton, FL: CRC Press, 2009.

[150] W. W. Burns and T. G. Wilson, "A state-trajectory control law for DC-DC converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-14, no. 1, pp. 2–20, Jan. 1978.

[151] M. Greuel, R. Muyshondt, and P. T. Krein, "Design approaches to boundary controllers," in *Rec. IEEE Power Electron. Spec. Conf.*, 1997, pp. 672–678.

[152] O. Kirshenboim and M. M. Peretz, "Stability analysis of boundary and hybrid controllers for indirect energy transfer converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3360–3371, Apr. 2016.

[153] J. P. LaSalle, "Time optimal control systems," *Proc. Nat. Acad. Sci.*, vol. 45, pp. 573–577, 1959.

[154] G. E. Pitel and P. T. Krein, "Minimum-time transient recovery for DC-DC converters using Raster control surfaces," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2692–2703, Dec. 2009.

[155] K. K. S. Leung and H. S.-H. Chung, "Derivation of a second-order switching surface in the boundary control of buck converters," *IEEE Power Electron. Lett.*, vol. 2, no. 2, pp. 63–67, Jun. 2004.

[156] J. Y. C. Chiu, K. K. S. Leung, and H. S. Chung, "High-order switching surface in boundary control of inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1753–1765, Sep. 2007.

[157] W.-T. Yan, C. N.-M. Ho, H. S.-H. Chung, and K. T. K. Au, "Fixed-frequency boundary control of buck converter with second-order switching surface," *IEEE Trans. Power Electron.*, vol. 24, no. 9, pp. 2193–2201, Sep. 2009.

[158] M. Ordonez, M. T. Iqbal, and J. E. Quaicoe, "Selection of a curved switching surface for buck converters," *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1148–1153, Jul. 2006.

[159] J. M. Galvez, M. Ordonez, and M. Anun, "Normalized geometrical analysis: Unified theory and derivation of natural trajectories for basic dc-dc topologies," in *Proc. IEEE Workshop Comput. Power Electron.*, 2013, pp. 1–5.

[160] J. M. Galvez, M. Ordonez, F. Luchino, and J. E. Quaicoe, "Improvements in boundary control of boost converters using the natural switching surface," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3367–3376, Nov. 2011.

[161] J. Li and A. Wu, "Influence of nonideal factors on the boundary control of buck converters with curved switching surfaces," *IEEE Access*, vol. 7, pp. 52 790–52 803, 2019.

[162] J. T. Mossoba and P. T. Krein, "Exploration of deadbeat control for dc-dc converters as hybrid systems," in *Proc. IEEE Power Electron. Specialists Conf.*, 2005, pp. 1004–1010.

[163] J. T. Mossoba and P. T. Krein, "Null audio susceptibility of current-mode buck converters: Small signal and large signal perspectives," in *Proc. IEEE Power Electron. Specialists Conf.*, 2003, pp. 1605–1611.

[164] S. Kapat and V. I. Kumar, "Single-inductor multioutput-level buck converter for reducing voltage-transition time and energy overheads in low power DVS-enabled systems," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2254–2266, Mar. 2018.

[165] I. G. Zurbriggen, F. Degioanni, and M. Ordonez, "Near time optimal dynamics in PWM DC-DC converters: Dual-loop geometric control," *IEEE J. Emerging Sel. Topics Power Electron.*, to appear 2020.

[166] G. K. Schoneman and D. M. Mitchell, "Output impedance considerations for switching regulators with current-injected control," *IEEE Trans. Power Electronics*, vol. 4, no. 1, pp. 25–35, Jan. 1989.

[167] S. Kapat, "Near time optimal PID tuning in a digitally controlled synchronous buck converter," in *Proc. IEEE Workshop Control Model. Power Electron.* , Jun. 2014, pp. 1–8.
[168] V. I. Kumar and S. Kapat, "Unified digital current mode control tuning with near optimal recovery in a CCM buck converter," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8461–8470, Dec. 2016.
[169] M. Al-Greer, M. Armstrong, M. Ahmeid, and D. Giaouris, "Advances on system identification techniques for DC-DC switch mode power converter applications," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6973–6990, Jul. 2019.
[170] K. Hariharan and S. Kapat, "Near optimal controller tuning in a current-mode DPWM boost converter in CCM and application to a dimmable LED array driving," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 2, pp. 1031–1043, Jun. 2019.
[171] O. Kirshenboim and M. M. Peretz, "Fast response of deviation-constrained hybrid controllers for indirect energy transfer converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2615–2629, Mar. 2018.
[172] M. M. Peretz, B. Mahdavikhah, and A. Prodic, "Hardware-efficient programmable-deviation controller for indirect energy transfer DC-DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3376–3388, Jun. 2015.
[173] I. G. Zurbriggen and M. Ordonez, "Benchmarking the performance of boost-derived converters under start-up and load transients," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 3125–3136, May 2016.

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