A Universal Core Model for Multiple-Gate Field-Effect Transistors. Part II: Drain Current Model

Juan Pablo Duarte, Sung-Jin Choi, Dong-Il Moon, Jae-Hyuk Ahn, Jee-Yeon Kim, Sungho Kim, and Yang-Kyu Choi

***Abstract*—A universal drain current model for multiple-gate field-effect transistors (FETs) (Mug-FETs) is proposed. In Part I, a universal charge model was derived using the arbitrary potential method. Using this charge model, Pao–Sah's integral is analytically carried out by approximating its integrand. The model describes both the subthreshold inversion for undoped FETs and the effects of finite doping density in the channel. With an explicit and continuous expression, the proposed drain current model covers all regions of device operation: subthreshold, linear, and saturation. The accuracy from the proposed model is comparable with that from well-known previous models for double-gate (DG) and cylindrical gate-all-around (Cy-GAA) FETs with an undoped channel. In addition, the model shows good agreement with 2-D and 3-D numerical simulations for doped-channel multiple-gate structures such as single-gate, DG, triple-gate, rectangular gate-all-around, and Cy-GAA FETs. The proposed model is well suited to be a core model for Mug-FETs due to its good computational efficiency and high accuracy; hence, it is useful for compact modeling.**

***Index Terms*—Compact modeling, cylindrical gate-all-around (Cy-GAA) field-effect transistor (FET), double-gate (DG) FET, FinFET, multiple-gate FET (Mug-FET), Pao–Sah's integral, Poisson's equation, rectangular gate-all-around (Re-GAA) FET, semiconductor device modeling, single-gate (SG) FET, triple-gate (TG) FET.**

I. Introduction

FULLY DEPLETED multiple-gate field-effect transistors (FETs) (Mug-FETs) [1] have been proposed as an alternative to planar devices in the nanoscale transistor era. Leading microelectronics for the past four decades, conventional planar CMOS transistors on bulk silicon substrates are approaching the fundamental physical limits related to device downscaling. Thus, gate oxide tunneling and short-channel effects (SCEs) [2], [3] are of crucial concern. However, Mug-FETs effectively suppress SCEs by virtue of their overwhelming electrostatic control of the channel potential, which alleviates the stringent demand of aggressive gate oxide downscaling.

Compact models are essential for the comprehensive understanding of device properties and performance dependence on device parameters. They are also indispensable in fast circuit simulators due to their good accuracy and good computational efficiency. Several compact models have been proposed for a large variety of Mug-FET structures such as double-gate (DG) [4]–[12], triple-gate (TG) [13]–[15], rectangular gate-all-around (Re-GAA) [15]–[17], or cylindrical gate-all-around (Cy-GAA) FETs [18]–[21]. Most of those core models are obtained using the gradual channel approximation [22] and solving Poisson's equation in the channel. However, this approach becomes impractical for nonsymmetrical structures (see Fig. 1) or FETs with finite channel doping concentration. Indeed, a direct analytical solution of Poisson's equation is only available for the cases of undoped DG [4] and Cy-GAA FETs [18] because those 3-D Poisson equations can be reduced to a 1-D form. Even though other structures such as TG or Pi-gate FETs offer simpler fabrication processes than other symmetric structures [23], compact models are rarely found in the literature. Hence, physically based core models for structures to have nonsymmetric geometry need to be developed.

In Part I, a universal charge model for Mug-FETs was proposed. The charge model showed good agreement with numerical simulations [24] for several Mug-FET structures and with the direct analytical results of Poisson's equation which were available for the cases of undoped DG [4] and Cy-GAA FETs [18]. In this paper, utilizing Pao–Sah's integral and the universal charge model from Part I, a universal drain current model for Mug-FETs is developed. The proposed drain current model is validated for various multiple-gate structures: single-gate (SG), DG, TG, Re-GAA, and Cy-GAA FETs. The proposed model shows good agreement with 2-D and 3-D numerical simulations [24] and with the drain current models for undoped DG [5] and Cy-GAA FETs [19].

II. Charge Model

In Part I, accurate charge models for DG and Cy-GAA FETs were derived utilizing the arbitrary potential method. Thereafter, using an equivalence found between the charge models of DG and Cy-GAA FETs, a universal charge model was derived for other Mug-FET structures by directly mapping the device parameters (gate capacitance, channel capacitance,

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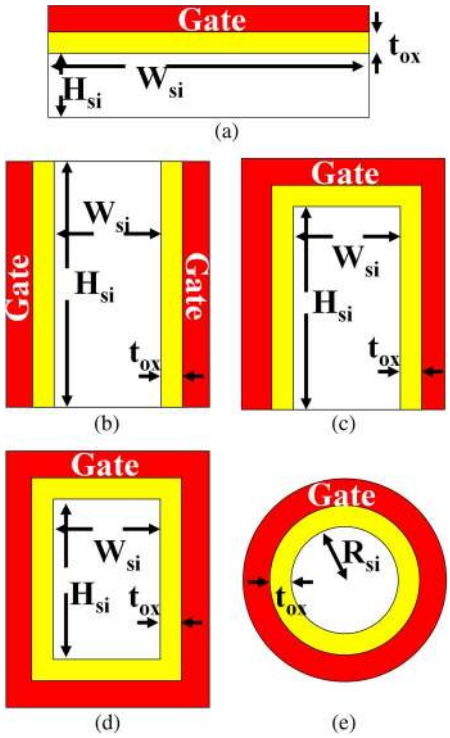

Fig. 1. Schematic diagrams of Mug-FET cross sections. (a) SG FET. (b) DG FET. (c) TG FET. (d) Re-GAA FET. (e) Cy-GAA FET.

channel doping, and cross-sectional area) from the Mug-FET structures. The implicit charge model is given by

$$V_G - V_{\rm FB} + \frac{Q_{D,n}}{C_{g,n}} - V = -\frac{Q_{e,n}}{C_{g,n}} + v_T \ln \frac{-Q_{e,n}}{q\frac{n_i^2}{N_{\rm si}}A_{{\rm ch},n}} + v_T \ln \frac{-(Q_{e,n}/\alpha_n + Q_{d,n})/v_T C_{{\rm ch},n}}{1-\exp\frac{Q_{e,n}/\alpha_n+Q_{d,n}}{v_T C_{{\rm ch},n}}} \quad (1)$$

where V_G is the gate voltage, $V_{\rm FB}$ is the flatband voltage, V is the electron quasi-Fermi potential, $N_{\rm si}$ is the doping concentration in the channel, n_i is the intrinsic carrier concentration, v_T is the thermal voltage equal to kT/q, $Q_{d,n}$ is the depletion charge per unit length, $Q_{e,n}$ is the mobile electron charge per unit length, $C_{g,n}$ is the gate oxide capacitance per unit length, $C_{{\rm ch},n}$ is the channel capacitance per unit length, $A_{{\rm ch},n}$ is the area of the channel, and α_n is a fixed parameter added in Part I.[1] The "n" term denotes the device structure being used, e.g., $n =$ DG refers to a DG FET. Each structural term was provided in Part I. High accuracy of (1) was confirmed. For example, it precisely matches the simulation data not only for the electron concentration in the channel but also for high-order derivatives of the electron concentration (see Fig. 2). It also captures the subthreshold inversion of undoped Mug-FETs. Moreover, (1) describes the charge behavior of nonsymmetric Mug-FETs, which cannot be described by the use of symmetric DG and Cy-GAA models (see Fig. 3).

[1]For simplicity, (32) from Part I is used in the drain current model derivation; however, (3) from this paper can be used for the same purpose.

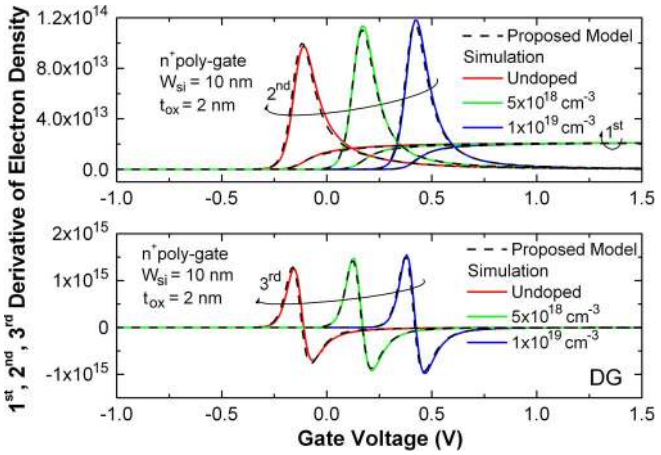

Fig. 2. First, second, and third derivatives of the electron density with respect to the gate voltage for a DG FET with different doping concentrations, which are obtained from the proposed model (1) with $\alpha_{\rm DG} = 1.8$ and numerical simulations.

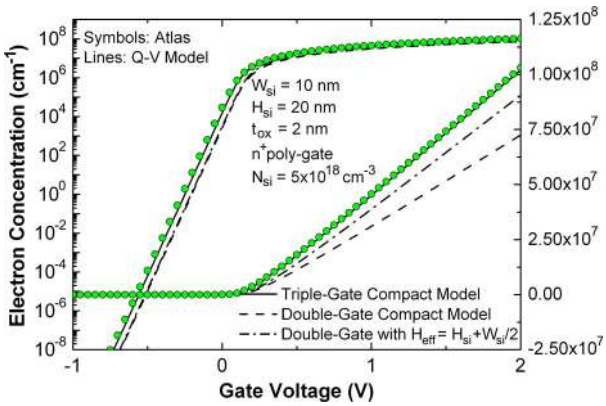

Fig. 3. Mobile electron concentration per unit length in a doped TG FET obtained from numerical simulations and the proposed model (1) for three miscellaneous cases: TG structure, a DG structure neglecting the top surface, and a DG structure with an effective $H_{\rm si}$. Note that the use of DG models gives inaccurate results for a TG structure in all regions of device operation.

Using (1), a threshold voltage ($V_{\rm TH}$) expression can also be obtained

$$V_{{\rm TH},n} = V_{\rm FB} - \frac{Q_{d,n}}{C_{g,n}} + 2v_T \ln\frac{N_{\rm si}}{n_i} - v_T \ln\left[\frac{C_{{\rm ch},n}}{C_{g,n}}\left(1 - e^{\frac{Q_{d,n}}{v_T C_{{\rm ch},n}}}\right)\right]. \quad (2)$$

The threshold voltage expressed by (2) serves as a universal $V_{\rm TH}$ for Mug-FETs. In Part I, it was also noted that (1) can be expressed with a continuous and explicit form by the use of the method proposed in [25]. Therefore, due to the good accuracy and computational efficiency of the proposed universal charge model, it will be used to obtain a universal drain current model, which can be used as a core model in fast circuit simulators.

III. Drain Current Model

Drain current models for long-channel FETs are commonly obtained with the assumption that drift and diffusion are the main transport mechanisms which govern the total current in the FETs. Another assumption is that the carrier mobility

is constant along the channel. Following these assumptions, the drain current in a FET is obtained by solving Pao–Sah's double integral [22], which can be expressed in the following form [20]:

$$I_{\rm DS} = -\frac{\mu}{L}\int_{Q_{e,S}}^{Q_{e,D}} Q_{e,n}\frac{dV}{dQ_{e,n}}dQ_{e,n}. \tag{3}$$

In (3), μ is the electron mobility, L is the channel length, $Q_{e,D}$ is the mobile electron charge density at the drain region, and $Q_{e,S}$ is the mobile electron charge density at the source region. Here, $Q_{e,D}$ and $Q_{e,S}$ are obtained from (1) by replacing V with V_D and V_S, respectively. From (1), $dV/dQ_{e,n}$ is given by

$$\frac{dV}{dQ_{e,n}} = \frac{1}{C_{g,n}} - \frac{v_T}{Q_{e,n}} - \frac{v_T}{Q_{e,n}+\alpha_n Q_{d,n}} - \frac{1/\alpha_n C_{{\rm ch},n}}{\exp -\frac{Q_{e,n}/\alpha_n + Q_{d,n}}{v_T C_{{\rm ch},n}} - 1}. \tag{4}$$

If (4) is directly plugged into (3), analytical integration is not possible because the last term in the RHS of (4) leads to an integral which is similar in form to the well-known Fermi–Dirac integral, which is not available for analytical integration. However, with consideration of the asymptotic behavior of (4), (3) can be analytically integrated. In strong inversion, the last term in the RHS of (4) tends to be zero. However, in the subthreshold region, the last term in the RHS of (4) has two different behaviors depending on the doping concentration. If the doping concentration is high, it is much smaller than the rest of the terms; thus, it can be neglected. On the other hand, if the doping concentration is low, the last term in the RHS of (4) tends to be $v_T/(Q_{e,n}+Q_{d,n})$; thereby, it cancels out the penultimate term in the RHS of (4) under a weak-inversion condition. Following these asymptotic behaviors, an approximation for (4) can be made as follows:

$$\frac{dV}{dQ_{e,n}} \approx \frac{1}{C_{g,n}} - \frac{v_T}{Q_{e,n}} - \frac{v_T}{Q_{e,n}+\gamma_n Q_{d,n}} - \frac{\frac{1}{\gamma_n C_{{\rm ch},n}}}{\left(1-\frac{Q_{e,n}/\gamma_n + Q_{d,n}}{v_T C_{{\rm ch},n}}\right)} \cdot \frac{1}{\left(-\frac{Q_{e,n}/\gamma_n + Q_{d,n}}{v_T C_{{\rm ch},n}}\right)} \tag{5}$$

where γ_n is approximately equal to α_n. It is used to fit (5) with (4). For simplicity, in this section, γ_n is taken to be equal to α_n. This assumption still produces very accurate results. Hence, in the next section, γ_n is further optimized to obtain better accuracy for the proposed model. Expression (5) shows the same behavior as (4). In the strong inversion, the last term in the RHS of (5) is canceled out. For highly doped FETs, it is much smaller than the other terms; thus, it can be neglected. Finally, for a lightly doped FET in the subthreshold region, it cancels out the penultimate term in the RHS of (5). Fig. 4 compares the values of $-Q_{e,n}\times dV/dQ_{e,n}$ obtained using (4) and (5) for a DG FET as an example. As expected, good agreement is found between both expressions. This accuracy can further be optimized by fitting γ_n or by the use of a higher order approximation for (4) as shown in Section V.

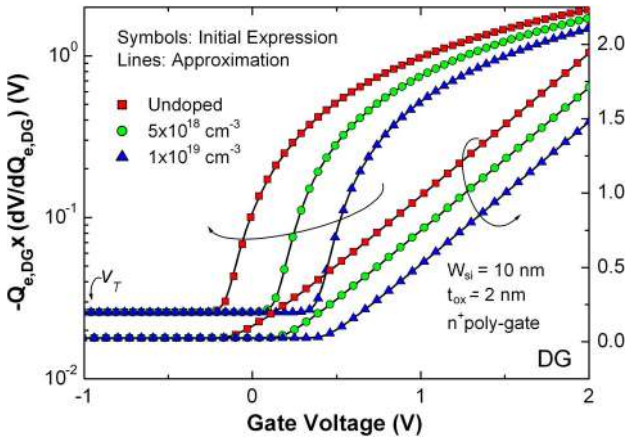

Fig. 4. $-Q_{e,n}\times dV/dQ_{e,n}$ obtained using the initial expression of $dV/dQ_{e,n}$ given by (4) and the approximation given by (5). Using $\gamma_n = \alpha_n$, the peak error of (5) is approximately 5% in the moderate-inversion region of undoped devices and less than 0.1% for doped devices. A better approximation for $dV/dQ_{e,n}$ is presented in Section V.

Using (5), (3) can be analytically integrated, which gives

$$I_{\rm DS} = -\frac{\mu}{L}\left[\frac{Q_{e,n}^2}{2C_{g,n}} - 2v_T Q_{e,n} - v_T(\gamma_n v_T C_{{\rm ch},n} - \gamma_n Q_{d,n}) \times \ln(\gamma_n v_T C_{{\rm ch},n} - \gamma_n Q_{d,n} - Q_{e,n})\right]\Bigg|_{Q_{e,S}}^{Q_{e,D}}. \tag{6}$$

The form of the drain current model expressed by (6) is commonly seen in compact modeling applications [6], [9], [11]. For example, in the case of a lightly doped FET, (6) approximately reduces to the expression in [6]. On the other hand, for a heavily doped FET, (6) approximately reduces to the representation in [9]. In addition, (6) has the same form as the previous drain current model in [11], which was known to have a source/drain (S/D) exchanging feature. This is an important requirement for compact modeling applications because FETs are physically symmetric across S/D.

IV. Results and Discussion

To validate the proposed universal drain current model, several approaches will be used. First, the proposed model will be compared with the well-known analytical models for undoped DG [5] and Cy-GAA FETs [19]. Thereafter, for doped devices, 2-D simulations [24] for SG and DG FETs and 3-D simulations [24] for Cy-GAA, TG, and Re-GAA FETs will be used to validate the proposed model for each Mug-FET structure. In Section V, an extensive study of the drain current model error is analyzed and improved. The same value of the electron mobility ($\mu = 100$ cm^2/V $\cdot$ s) is used for the proposed model and the simulations, with a gate length (L) of 1 μm. In addition, the source and drain charges are calculated using the explicit form of (1) obtained with the method proposed in [25]. A floating body is assumed in all the simulations.

Figs. 5 and 6 show the drain current versus the drain voltage and gate voltage, respectively, for undoped DG and Cy-GAA FETs, obtained from (6). Also, they are compared with the

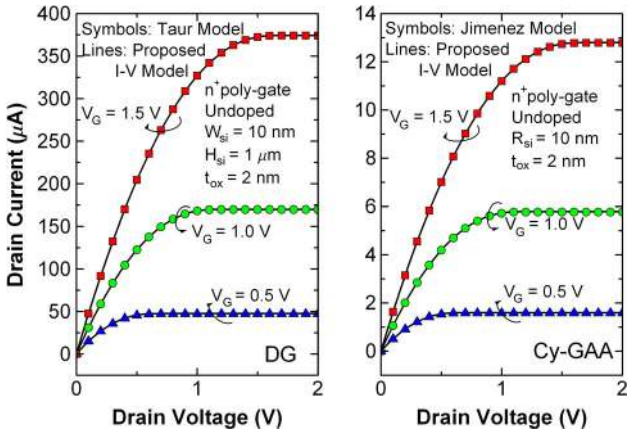

Fig. 5. Drain current versus drain voltage of undoped DG and Cy-GAA FETs, obtained from the proposed drain current model and the models for undoped DG [5] and Cy-GAA FETs [19].

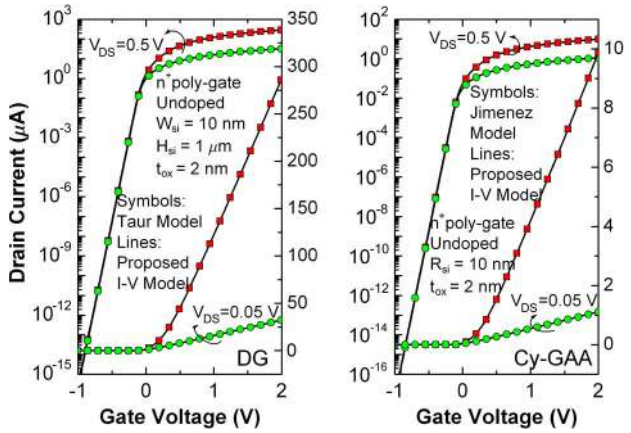

Fig. 6. Drain current versus gate voltage of undoped DG and Cy-GAA FETs, obtained from the proposed drain current model and the models for undoped DG [5] and Cy-GAA FETs [19].

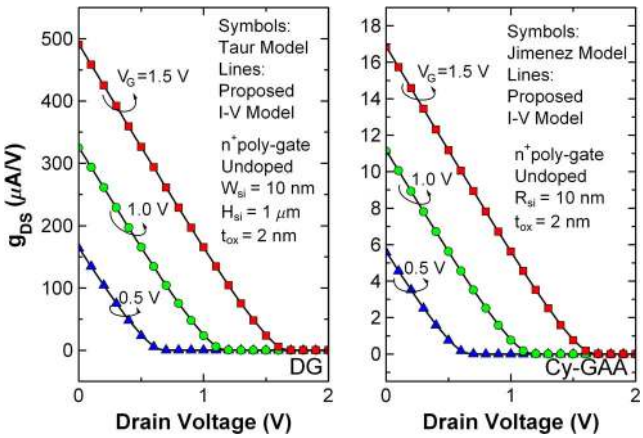

Fig. 7. Output conductance (g_{DS}) versus drain voltage of undoped DG and Cy-GAA FETs, obtained from the proposed drain current model and the models for undoped DG [5] and Cy-GAA FETs [19].

models proposed in [5] and [19]. Good agreement is shown between the proposed model and the models for undoped FETs [5], [19]. In addition to the drain current, the output conductance (g_{DS}) and the transconductance (g_m) obtained from the proposed model also show good agreement with respect to those in [5] and [19], as shown in Figs. 7 and 8.

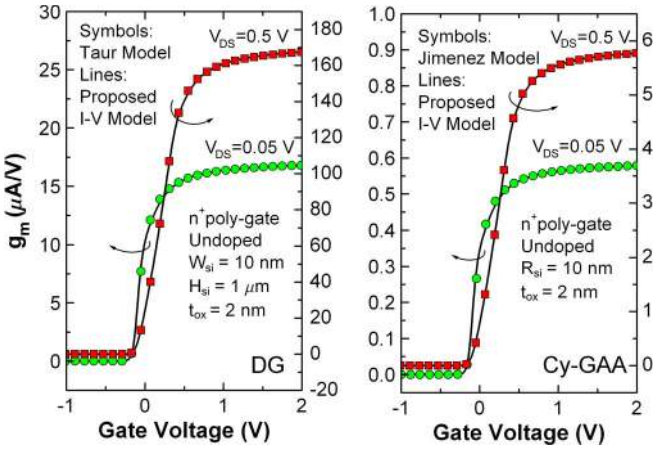

Fig. 8. Transconductance (g_m) versus gate voltage of undoped DG and Cy-GAA FETs, obtained from the proposed drain current model and the models for undoped DG [5] and Cy-GAA FETs [19].

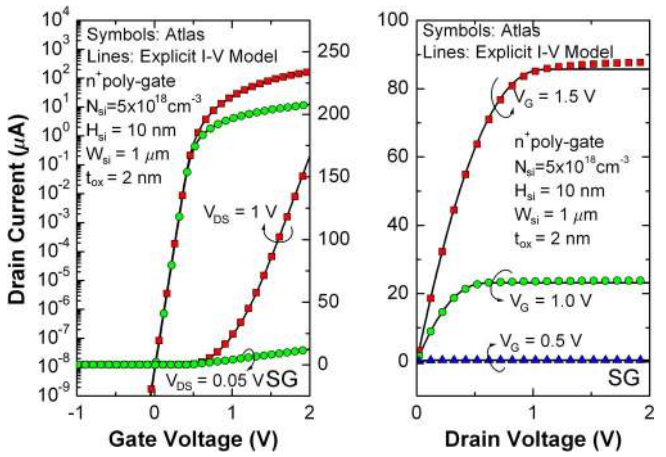

Fig. 9. Drain current versus gate voltage and drain current versus drain voltage of a doped SG FET obtained from the proposed drain current model and the numerical simulations.

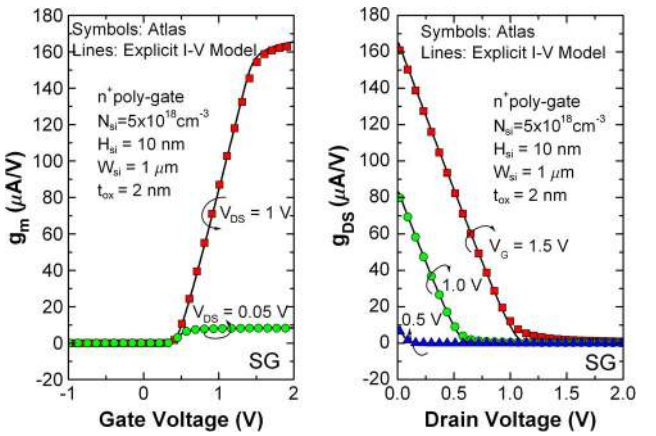

Fig. 10. Transconductance (g_m) versus gate voltage and output conductance (g_{DS}) versus drain voltage of a doped SG FET obtained from the proposed drain current model and the numerical simulations.

Figs. 9–18 show the drain current versus the gate voltage and drain voltage for doped SG, DG, TG, Re-GAA, and Cy-GAA FETs, obtained from the proposed model and the numerical simulations [24]. The output conductance (g_{DS}) and the transconductance (g_m) obtained from the proposed model

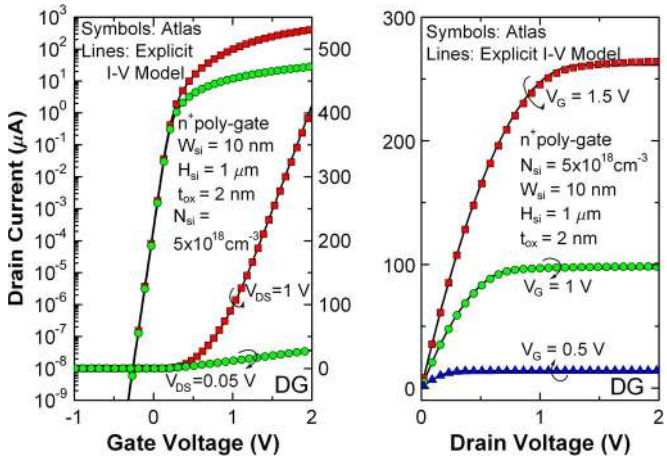

Fig. 11. Drain current versus gate voltage and drain current versus drain voltage of a doped DG FET obtained from the proposed drain current model and the numerical simulations.

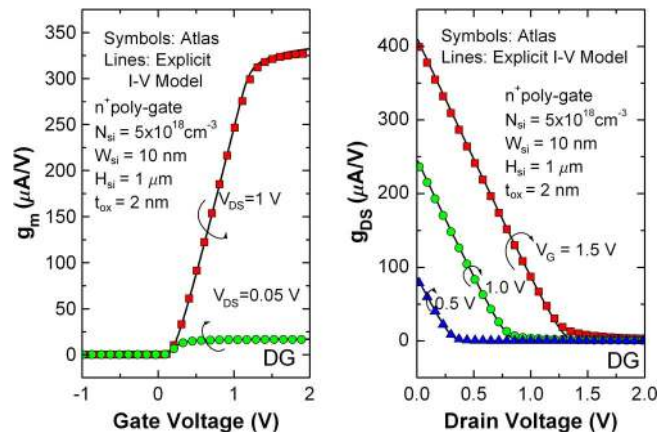

Fig. 12. Transconductance (g_m) versus gate voltage and output conductance $(g_{\rm DS})$ versus drain voltage of a doped DG FET obtained from the proposed drain current model and the numerical simulations.

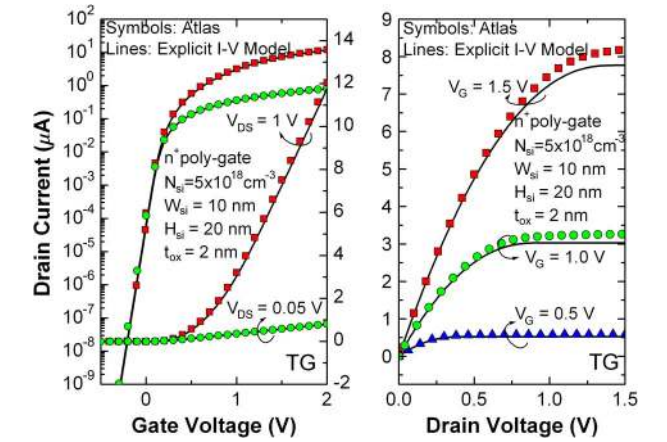

Fig. 13. Drain current versus gate voltage and drain current versus drain voltage of a doped TG FET obtained from the proposed drain current model and the numerical simulations.

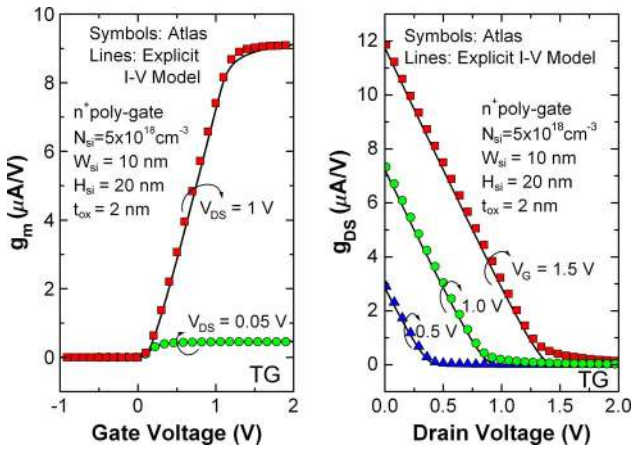

Fig. 14. Transconductance (g_m) versus gate voltage and output conductance $(g_{\rm DS})$ versus drain voltage of a doped TG FET obtained from the proposed drain current model and the numerical simulations.

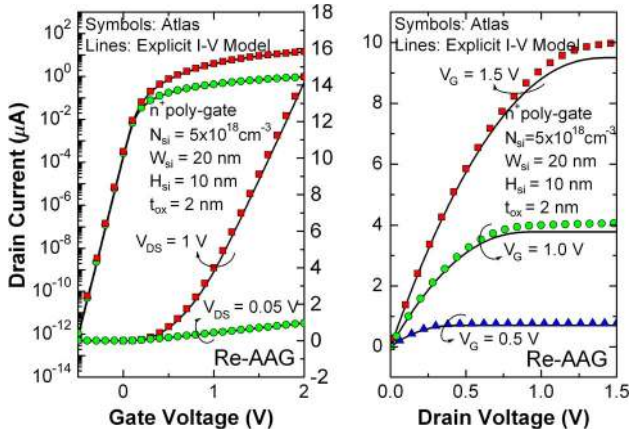

Fig. 15. Drain current versus gate voltage and drain current versus drain voltage of a doped Re-GAA FET obtained from the proposed drain current model and the numerical simulations.

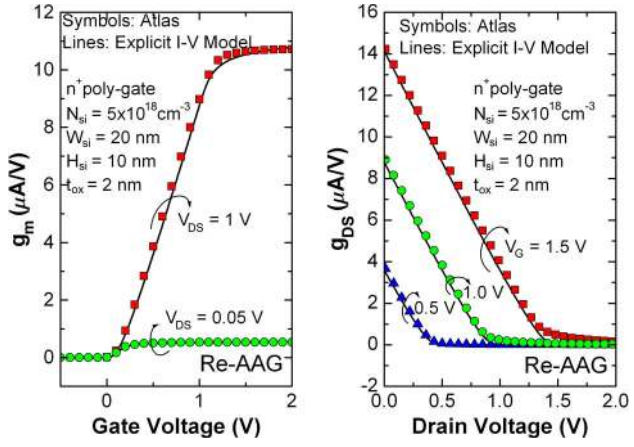

Fig. 16. Transconductance (g_m) versus gate voltage and output conductance $(g_{\rm DS})$ versus drain voltage of a doped Re-GAA FET obtained from the proposed drain current model and the numerical simulations.

are also compared with those from numerical simulations [24]. Good agreement is also found between the proposed model and the numerical simulations. This good agreement is further improved in Section V. A small difference in the ON-current level is observed between the proposed model and the 3-D simulations of TG, Re-GAA, and Cy-GAA FETs. These differences come principally from finite mesh density [19] (note the good agreement for Cy-GAA FETs shown in Figs. 5–8).

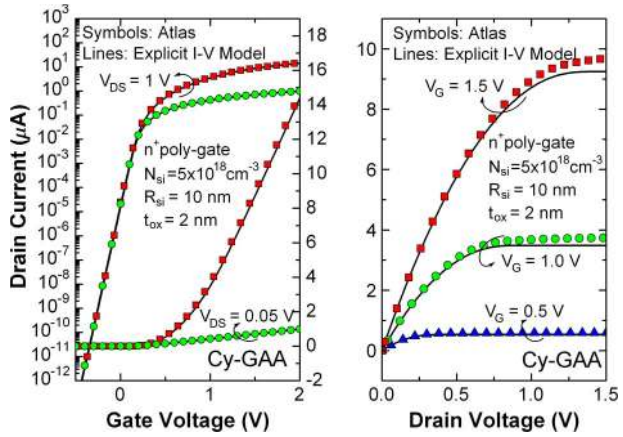

Fig. 17. Drain current versus gate voltage and drain current versus drain voltage of a doped Cy-GAA FET obtained from the proposed drain current model and the numerical simulations.

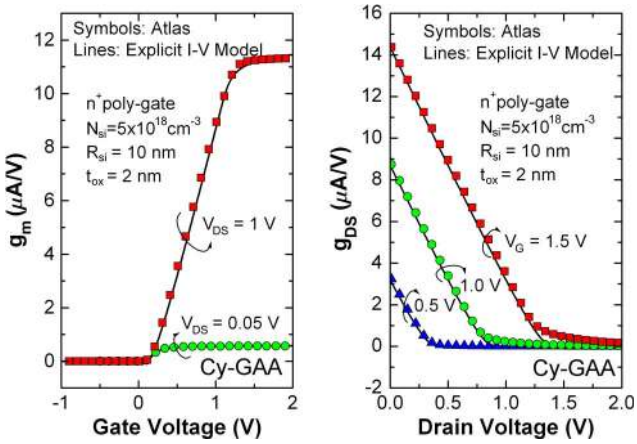

Fig. 18. Transconductance (g_m) versus gate voltage and output conductance ($g_{\rm DS}$) versus drain voltage of a doped Cy-GAA FET obtained from the proposed drain current model and the numerical simulations.

The drain current characteristics in all regions of device operation, i.e., subthreshold, linear, and saturation regions, are represented with a continuous and explicit expression in the proposed model arising from (6). In the subthreshold region, the second and third terms in the RHS of (6) are dominant; thus, the drain current is approximately given by

$$I_{\rm DS} \approx \frac{\mu}{L} v_T^2 C_{g,n} \exp\left(\frac{V_G - V_{{\rm TH},n}}{v_T}\right)\left(1 - \exp\frac{-V_{\rm DS}}{v_T}\right). \quad (7)$$

Note that (7) is independent of $C_{g,n}$ for undoped devices. In the linear and saturation regions, the first term in the RHS of (6) is dominant. Hence, the drain currents in the linear and saturation regions are approximately given by

$$I_{\rm DS} \approx \frac{\mu}{L} C_{g,n}(V_G - V_{{\rm TH},n} - V_{\rm DS}/2)V_{\rm DS} \quad (8)$$

$$I_{\rm DS} \approx \frac{\mu}{2L} C_{g,n}(V_G - V_{{\rm TH},n})^2. \quad (9)$$

V. Optimization of Drain Current Models

As shown in Section III, the accuracy from the proposed model is comparable with that from well-known previous models for DG [5] and Cy-GAA FETs [19] with an undoped channel. In addition, the model shows good agreement with 2-D and 3-D numerical simulations for doped-channel Mug-FETs. This section is devoted to further analyzing and optimizing the accuracy of the proposed drain current model expressed by (6). In addition, another approximation for $dV/dQ_{e,n}$ is proposed. This new approximation shows more accurate results than the one expressed by (6) but with a more complex formulation. It also provides a drain current model which is symmetric with respect to S/D exchange as needed for some analog applications [26], [27].

One of the main steps used in the derivation of the drain current expressed by (6) was the use of an approximation for $dV/dQ_{e,n}$, which is expressed by (5). However, for undoped devices, this approximation produces an error of $\sim$5% at the moderate-inversion mode if γ_n is assumed to be equal to α_n, as shown in Fig. 4. In order to improve this approximation, γ_n can be optimized using the reported models for undoped DG [5] and Cy-GAA FETs [19]. These models were based on the direct analytical solutions of Poisson's equation; however, they are only valid for undoped devices. Note that γ_n can be optimized directly using (4) as well. Indeed, both approaches give similar values of γ_n. It is preferred to use the models for undoped DG [5] and Cy-GAA FETs [19] for the optimization of γ_n because, from this procedure, the accuracy of the proposed model can also be evaluated.

The drain current obtained from (6) and the reported model for undoped DG FETs [5] using different device parameters and values for $\gamma_{\rm DG}$ were compared. The error of the data from the proposed model was obtained for different V_G's from -0.5 to 0.5 V, $V_{\rm DS}$'s from 0.1 to 1.0 V, $W_{\rm si}$'s from 1 to 50 nm, $t_{\rm ox}$'s from 1 to 10 nm, and $\gamma_{\rm DG}$'s from 1.8 to 2.6 and for fixed doping (undoped), $H_{\rm si}$ (1 μm), and gate work function (n$^+$ polygate). As expected from Part I, the peak errors are relatively serious in the moderate-inversion mode. A value of $\gamma_{\rm DG} = 2.3$ gives the best optimization with a worst peak error of 5.803%. This is an improved result compared with the case of $\gamma_{\rm DG} = 1.8$ as in Section III (9% error). In the case of Cy-GAA FETs, the same procedure used for DG FETs is employed but using R from 1 to 25 nm. The error from (6), using the charge model expressed by (8) in Part I (linear potential with $\alpha_{\rm Cy} = 1.6$), with respect to the model from [19] was calculated. In this case, an optimum value of $\gamma_{\rm Cy} = 1.8$ produces the lowest peak error of 4.49%.

Even though the drain current model can give good accuracy for DG ($< 5.803\%$) and Cy-GAA FETs ($< 4.49\%$) for a wide range of device parameters and biases, it is possible to further improve it by the use of a second-order approximation for $dV/dQ_{e,n}$. This second-order approximation is proposed as follows:

$$\frac{dV}{dQ_{e,n}} \approx \frac{1}{C_{g,n}} - \frac{v_T}{Q_{e,n}} - \frac{v_T}{Q_{e,n} + \gamma_n Q_{d,n}} - \frac{1/\gamma_n C_{{\rm ch},n}}{\left(1 - \frac{Q_{e,n}/\gamma_n + Q_{d,n}}{v_T C_{{\rm ch},n}} + \left(\frac{Q_{e,n}/\gamma_n + Q_{d,n}}{v_T C_{{\rm ch},n}}\right)^2\right)} \times \frac{1}{\left(-\frac{Q_{e,n}/\gamma_n + Q_{d,n}}{v_T C_{{\rm ch},n}}\right)}. \quad (10)$$

In this expression, γ_n is also utilized to optimize the proposed model. Using approximation (10), it is possible to analytically

solve Pao–Sah's double integral [22] in (3). This results in a new drain current expressed by

$$I_{\rm DS} = -\frac{\mu}{L}\left[\frac{Q_{e,n}^2}{2C_{g,n}} - 2v_T Q_{e,n} + f(Q_{e,n})\right]\Bigg|_{Q_{e,S}}^{Q_{e,D}} \quad (11)$$

where $f(Q_{e,n})$ is given by

$$\begin{aligned} f(Q_{e,n}) = &-\frac{v_T}{\sqrt{3}}\gamma_n(v_T C_{{\rm ch},n} - 2Q_{d,n}) \\ &\times \operatorname{arccot}\left[\frac{\sqrt{3}\gamma_n v_T C_{{\rm ch},n}}{2\gamma_n Q_{d,n} - \gamma_n v_T C_{{\rm ch},n} + 2Q_{e,n}}\right] \\ &+ \frac{v_T}{2}\gamma_n Q_{d,n}\ln \\ &\times \left[\gamma_n\left(Q_{d,n}^2 - v_T C_{{\rm ch},n}Q_{d,n} + C_{{\rm ch},n}^2 v_T^2\right)\right. \\ &\left. + \gamma_n(2Q_{d,n} - v_T C_{{\rm ch},n})Q_{e,n} + Q_{e,n}^2\right]. \quad (12) \end{aligned}$$

In the same manner as (6), (11) continuously represents the drain current in Mug-FETs under each operational region: subthreshold, linear, and saturation. The form of (11) is not commonly seen in compact modeling; thus, symmetry cannot be easily checked by its form. Symmetry with respect to S/D exchange, the so-called Gummel symmetry [26], is an important requirement for drain current models [26], [27]. It can be shown that (11) fulfills the requirements of the Gummel symmetry test [26]. Therefore, this expression can also be used as a universal drain model for Mug-FETs.

Equation (11) can be optimized using the proposed model for undoped DG FETs from [5] as it was done for (6). The error of the drain current model for DG FETs from (11) with respect to the proposed model for undoped DG FETs in [5] was calculated for different device parameters and gate and drain biases. In this case, an optimum value of $\gamma_{\rm DG}$ equal to 3.65 gives the lowest peak error of 3.06%. In the case of Cy-GAA FETs, (11) can also be optimized using the model reported in [19] for undoped Cy-GAA FETs. Using a $\gamma_{\rm Cy}$ of 2.6 gives a peak error equal to 2.18%. For SG FETs, the same parameters ($\alpha_{\rm DG}$ and $\gamma_{\rm DG}$) used for DG FETs are assumed. In addition, for TG and Re-GAA FETs, it is possible to use an average between the parameters obtained for DG ($\alpha_{\rm DG}$ and $\gamma_{\rm DG}$) and Cy-GAA FETs ($\alpha_{\rm Cy}$ and $\gamma_{\rm Cy}$) or simply use the parameters for DG FETs, which also give a low peak error for the Cy-GAA FET case. Both approaches give good accuracy ($<\sim$5% error). In addition, note that the proposed models have rms errors lower than $\sim$1%. In the case that a more specific optimization is needed, numerical simulations are required to obtain α_n and γ_n for TG and Re-GAA FETs.

VI. Conclusion

A universal core model has been proposed for fully depleted Mug-FETs. In Part I, a universal charge model was derived by the use of the arbitrary potential method, which was very convenient for Pao–Sah's integral. The electron charge density and its high-order derivatives obtained from the proposed charge model showed good accuracy for each Mug-FET structure. It was also shown that the proposed charge model can capture the behaviors of several nonsymmetric Mug-FET structures, which cannot be represented by the models for DG or Cy-GAA FETs. In this paper, a universal drain current model has been analytically obtained from Pao–Sah's integral and the charge model proposed in Part I. The proposed universal core model can be expressed with a continuous and explicit form, which is desired for fast simulator programs. It showed good agreement not only with well-known analytical models for undoped DG and Cy-GAA FETs but also with 2-D and 3-D numerical simulations (rms errors lower than $\sim$1%). Hence, the proposed model is well suited to be a core model for Mug-FETs due to its good computational efficiency and high accuracy. It can also be extended to other FET structures, such as Pi- or Omega-gate FETs, by deriving proper gate and channel capacitances for these structures. To complete the proposed universal core model, additional physical effects should be included, e.g., quantum mechanical effects, SCEs, field-dependent mobility, S/D resistances, partial depletion effects, corner effects, and noise.

References

[1] J. Colinge, "Multiple-gate SOI MOSFETs," *Solid State Electron.*, vol. 48, no. 6, pp. 897–905, Jun. 2004.

[2] M. Liu, M. Cai, B. Yu, and Y. Taur, "Effect of gate overlap and source/drain doping gradient on 10-nm CMOS performance," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 3146–3149, Dec. 2006.

[3] D. Frank, R. Dennard, E. Nowak, P. Solomon, Y. Taur, and H. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–288, Mar. 2001.

[4] Y. Taur, "An analytical solution to a double-gate MOSFET with undoped body," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 245–247, May 2000.

[5] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, Feb. 2004.

[6] J. Sallese, F. Krummenacher, F. Prégaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid State Electron.*, vol. 49, no. 3, pp. 485–489, Mar. 2005.

[7] A. Ortiz-Conde, F. García Sánchez, and J. Muci, "Rigorous analytic solution for the drain current of undoped symmetric dual-gate MOSFETs," *Solid State Electron.*, vol. 49, no. 4, pp. 640–647, Apr. 2005.

[8] M. Dunga, C. Lin, X. Xi, D. Lu, A. Niknejad, and C. Hu, "Modeling advanced FET technology in a compact model," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1971–1978, Sep. 2006.

[9] O. Moldovan, A. Cerdeira, D. Jimenez, J. Raskin, V. Kilchytska, D. Flandre, N. Collaert, and B. Iñiguez, "Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications," *Solid State Electron.*, vol. 51, no. 5, pp. 655–661, May 2007.

[10] G. Smit, A. Scholten, G. Curatola, R. van Langevelde, G. Gildenblat, and D. Klaassen, "PSP-based scalable compact FinFET model," in *Proc. Nanotechnol.*, 2007, pp. 520–525.

[11] M. Dunga, *Nanoscale CMOS Modeling*. Berkeley, CA: Univ. California, 2008.

[12] F. Liu, L. Zhang, J. Zhang, J. He, and M. Chan, "Effects of body doping on threshold voltage and channel potential of symmetric DG MOSFETs with continuous solution from accumulation to strong-inversion regions," *Semicond. Sci. Technol.*, vol. 24, no. 8, p. 085005, Aug. 2009.

[13] H. Abd El Hamid, J. Guitart, V. Kilchytska, D. Flandre, and B. Iniguez, "A 3-D analytical physically based model for the subthreshold swing in undoped trigate FinFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2487–2496, Sep. 2007.

[14] A. Tsormpatzoglou, C. Dimitriadis, R. Clerc, G. Pananakakis, and G. Ghibaudo, "Semianalytical modeling of short-channel effects in lightly doped silicon trigate MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 10, pp. 2623–2631, Oct. 2008.

[15] B. Yu, J. Song, Y. Yuan, W. Lu, and Y. Taur, "A unified analytic drain-current model for multiple-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2157–2163, Aug. 2008.

[16] E. Moreno, J. Roldán, F. Ruiz, D. Barrera, A. Godoy, and F. Gámiz, "An analytical model for square GAA MOSFETs including quantum effects," *Solid State Electron.*, vol. 54, no. 11, pp. 1463–1469, Nov. 2010.
[17] E. Moreno Perez, J. Roldan Aranda, F. Garcia Ruiz, D. Barrera Rosillo, M. Ibanez Perez, A. Godoy, and F. Gamiz, "An inversion-charge analytical model for square gate-all-around MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2854–2861, Sep. 2011.
[18] Y. Chen and J. Luo, "A comparative study of double-gate and surrounding-gate MOSFETs in strong inversion and accumulation using an analytical model," in *Proc. Int. Conf. Model. Simul. Microsyst.*, 2001, vol. 1, pp. 546–549.
[19] D. Jiménez, B. Iniguez, J. Sune, L. Marsal, J. Pallares, J. Roig, and D. Flores, "Continuous analytic IV model for surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 571–573, Aug. 2004.
[20] F. Liu, J. He, L. Zhang, J. Zhang, J. Hu, C. Ma, and M. Chan, "A charge-based model for long-channel cylindrical surrounding-gate MOSFETs from intrinsic channel to heavily doped body," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2187–2194, Aug. 2008.
[21] S. Venugopalan, D. Lu, Y. Kawakami, P. Lee, A. Niknejad, and C. Hu, "BSIM-CG: A compact model of cylindrical/surround gate MOSFET for circuit simulations," *Solid State Electron.*, vol. 67, no. 1, pp. 79–89, Jan. 2012.
[22] H. Pao and C. Sah, "Effects of diffusion current on characteristics of metal–oxide (insulator)–semiconductor transistors," *Solid State Electron.*, vol. 9, no. 10, pp. 927–937, Oct. 1966.
[23] J. Park, J. Colinge, and C. Diaz, "Pi-gate SOI MOSFET," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 405–406, Aug. 2001.
[24] *Atlas User's Manual, Device Simulation Software*, Silvaco, Santa Clara, CA, 2008, software ver, vol. 5, no. 0.
[25] B. Yu, H. Lu, M. Liu, and Y. Taur, "Explicit continuous models for double-gate and surrounding-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2715–2722, Oct. 2007.
[26] C. McAndrew, "Validation of MOSFET model source–drain symmetry," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2202–2206, Sep. 2006.
[27] D. Lu, "Compact models for future generation CMOS," Ph.D. dissertation, EECS Dept., Univ. California, Berkeley, CA, 2011.

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