A very fast control based on hysteresis of the C_{out} current with a frequency loop to operate at constant frequency

Santa C. Huerta[1], P. Alou[1], J.A. Oliver[1], O. Garcia[1], J.A. Cobos[1], A. Abou-Alfotouh[2]

[1] Universidad Politécnica de Madrid
Centro de Electrónica Industrial
Madrid, SPAIN
e-mail: conihuerta@etsii.upm.es

[2] Enpirion Inc.
685 Route 202/206
Bridgewater, NJ 08807 USA
e-mail: aalfotouh@enpirion.com

***Abstract*- The combination of non-linear control and linear control proposed in [1] provides very fast transient response (voltage step from 1 V to 1.5 V in 2 µs). This non-linear control is based on hysteretic control of the C_{out} current. This system is very sensitive to effects like aging, temperature, input and output voltage variation, etc., that modify the switching frequency. This paper proposes a frequency loop to avoid the frequency variation and to adjust the switching frequency to the nominal value by changing the hysteretic band. The design and analysis of the non-linear loop, the voltage loop and frequency loop are presented in detail with a design example. A 5 MHz buck converter is developed and experimental results validate the loops design, obtaining the same fast transient response (from 1.5 V to 2.5 V in 2 µs) but keeping constant the switching frequency in steady state.**

I. INTRODUCTION

Many applications demand fast dynamic response. Besides the dynamic requirements, size can also be a main constrain. A fast dynamic control technique can provide reduction in the size of the components (output capacitor) making easier the integration of the power converter. Different techniques have been presented in order to obtain fast transient response like the combination of non-linear and linear control. The non-linear control and linear control is not new, many ideas have been presented in the literature [1-22]. Figure 1 shows the non linear and linear control scheme presented in [1], this technique presents fast transient response given for the non linear loop and accurate regulation (linear voltage loop). A very fast transient response (voltage step from 1 V to 1.5 V in 2 µs) is obtained in [1]. In order to achieve fast transient response, the non-linear scheme is based on measuring the current of the output capacitor.

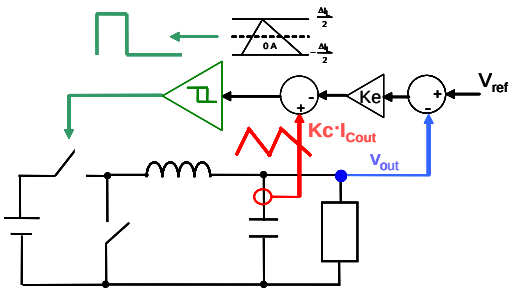


Figure 1. Linear and non-linear loop control scheme.

Nevertheless this non-linear and linear control scheme is sensitive to different effects (aging, temperature, etc.) that modify the switching frequency. In this paper a frequency loop to adjust the switching frequency to the nominal value is proposed, this frequency loop makes feasible the use of this non-linear control technique operating at constant f_{sw}.

II. MEASUREMENT OF OUTPUT CAPACITOR CURRENT

In order to achieve fast transient response the non-linear scheme is based on measuring the current of the output capacitor [1]. The sensing circuit is a RLC network in parallel with the output capacitor (Figure 2). It is designed to mirror the actual capacitor current with a trans-impedance amplifier (Figure 3) by matching time constants (equations 1 and 2) and scaling the impedance (n) of the parallel RLC network (equation 3). The gain of the non-linear loop (Kc) is given by equation (4).

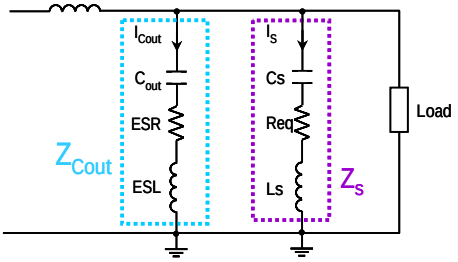


Figure 2. Capacitor current sensing method (RLC network).

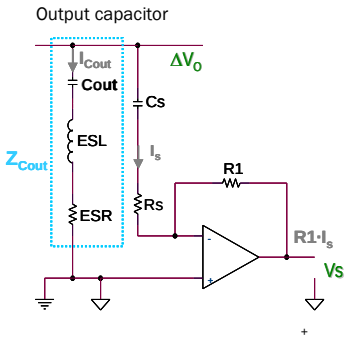
$$ESR \cdot C_{out} = Req \cdot Cs \quad (1)$$

$$ESL \cdot C_{out} = Ls \cdot Cs \quad (2)$$

$$n \cdot |Z_{Cout}| = |Z_S| \quad (3)$$

III. TOLERANCE ANALYSIS

In this section the variables that modify the switching frequency are explained. The RLC network is adjusted to the nominal output capacitor impedance, any mismatching between these two impedances causes an error measurement that produces a frequency deviation.



$$Kc = \frac{Vs}{I_{Cout}} = -\frac{R1}{n} \quad (4)$$

Figure 3. Physical implementation of the capacitor current sensing method (RLC network).

A. Output capacitor (C_{out})

The deviation of the capacitance value depends on tolerance of the dielectric and the aging. The proper operation of this sensor strongly depends on the relative position of the converter switching frequency (f_{sw}) and the C_{out} resonant frequency (f_{res}). If $f_{sw} > f_{res}$, the C_{out} impedance presents inductive behavior (Figure 4). When $f_{sw} < f_{res}$, the impedance is capacitive. If the sensor is designed for the inductive side, f_{res} must be always lower than f_{sw} to guarantee the appropriate operation. Therefore, the impedance behavior at the f_{sw} should be the same for all the output capacitor tolerances.

Although the previous constrain is met, the capacitor tolerances can produce switching frequency deviation. When the sensor is designed for the capacitive side, a 20% decrement in the capacitance value results on approximately 20% frequency increment and vice versa. If the system is designed for the inductive side, the capacitance variation does not affect the f_{sw} but, a 2% increment of ESL results on approximately 2% frequency increment and vice versa.

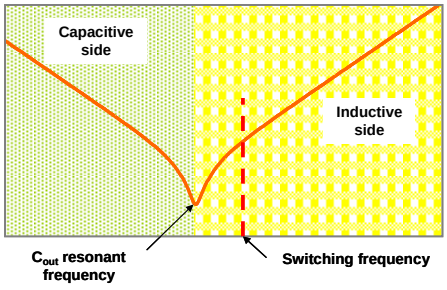


Figure 4. Impedance of the output capacitor.

B. Tolerance of the Op-Amp bandwidth (ΔB) and open loop gain (A_{DC})

The RLC network is adjusted with the bandwidth and the open loop gain of the Op-Amp used in the trans-impedance amplifier (see equations 5, 6 and 7). Therefore, the design of this current sensor is sensitive to parameters such as bandwidth (ΔB) and dc gain of the Op-Amp (A_{DC}). The deviation of the ΔB or A_{DC} value affects switching frequency, for example ΔB tolerance (-15%) of the Op-Amp generate f_{sw} variation (-15%). Figure 5 shows the range of ΔB and A_{DC} variation for a specific Op-Amp (AD8061) and Figure 6 shows how the temperature affects the value of the ΔB.

$$Ls = \frac{R1}{\Delta B} \quad (5)$$

$$Ri = \frac{R1}{A_{DC}} \quad (6)$$

$$Rs = Req - Ri \quad (7)$$

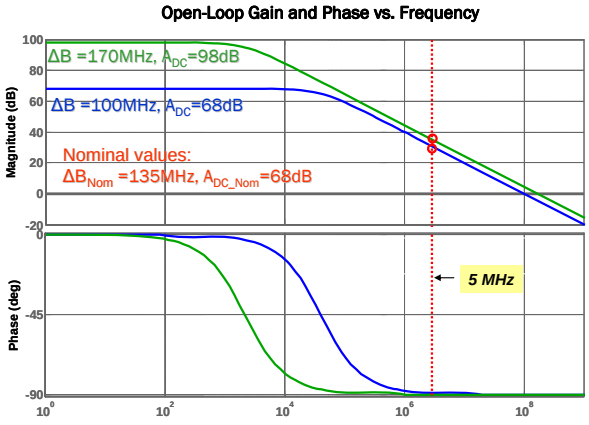
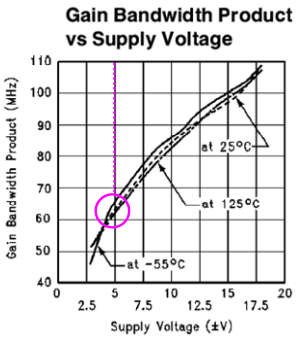


Figure 5. Frequency response of Op-Amp: AD8061. Maximum and minimum bandwidth and A_{DC} according to data sheet.



ΔB variation (Temperature)= +6.4% ΔB (decrement from 25ºC to -55ºC) and -1.6% ΔB (increment from 25ºC to 125ºC).

Figure 6. Tolerance of the Op-Amp bandwidth. LM6171.

C. Input voltage (V_{in}) and output voltage (V_{out})

Variation range of V_{in} and V_{out} produces also frequency deviation due to the change of the inductor current ripple. In the considered example, the input voltage ranges between 2.7 V to 5 V and the output voltage ranges between 1 V to 2 V. Considering as nominal case 5 V at the input and 1 V at the output, the frequency deviation is +59 % and -35% of the nominal value (5 MHz).

D. Adding external output capacitor

In some applications, the load already has a decoupling capacitor. The sensor is designed and adjusted for the converter output capacitor and this additional capacitor can not be accounted in the sensor design, producing an error in the sensor measurement that also generates a frequency deviation.

D.1 External capacitor is equal to converter C_{out}

Adding parallel C_{out} causes measurement deviation but, the C_{out} sensed current and the actual current are in phase (Figure 7) if the external capacitors are just the same than the converter one. Table 1 shows how the f_{sw} changes when external capacitors are added in parallel (external ceramic capacitors are equal than the internal one).

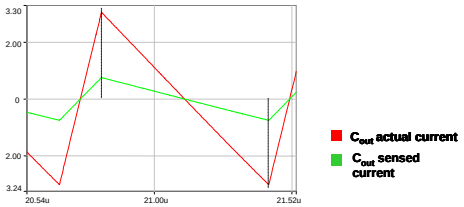


Figure 7. Adding parallel C equal to internal C_{out}. The C_{out} sensed current and the actual current are in phase.

Paralleled C_{out}	Frequency
1	5MHz
2	2.6MHz
4	1.3MHz
6	.8MHz

Table 1. Adding parallel C_{out} causes frequency deviation. External C is equal to internal C_{out}.

D.2 External capacitor is different than converter C_{out}

The decoupling capacitors can present different frequency impedance than the converter C_{out} that can affect the sensed current and hence the system performance. For example tantalum capacitors, OSCON capacitors, different ceramic capacitors, etc.

Figure 8 shows a comparison between impedances of tantalum capacitors. At 5 MHz (switching frequency) high impedances tantalum capacitor (Case 1: C= 220 µF, ESR= 0.17 Ω and ESL= 1.4 nH) does not affect steady state system performance. However, low impedance tantalum capacitor (Case 2: C= 330 µF, ESR= 10 mΩ and ESL= 0.7 nH) causes measurement deviation (see Figure 8).

For example, adding a 4mF external OSCON capacitor (being 10µF the converter capacitor) increases the equivalent capacitance +39,900 %, however the equivalent impedance at f_{sw} is reduced only -82% since we are working in the inductive side. This variation in the equivalent impedance (-82%) generate f_{sw} variation (- 99%).

Therefore, the effect of adding additional output capacitors depends on the change of the equivalent capacitor impedance at f_{sw} but not on the change of the equivalent capacitance.

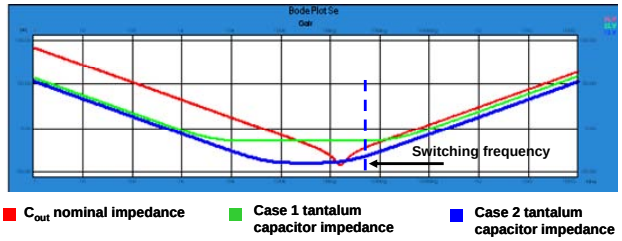


Figure 8. Impedances of tantalum capacitors. Low impedance tantalum capacitor (Case 2) produces deviation between C_{out} sensed and actual current.

IV. Scheme of the Proposed Control

Figure 9 shows the proposed control to achieve fast transient response with no frequency variation. The scheme of this converter is composed basically of three control loops: the non-linear loop, the linear voltage loop and the frequency loop. The design criteria of each loop are presented in the following section.

The function of the non-linear loop (hysteretic current loop) is to provide fast transient response and to lead the converter close to the steady state. The functionality of the voltage linear loop is to provide accurate regulation of the output voltage in steady state. Finally, the contribution of the frequency loop is to regulate the f_{sw} to the nominal value avoiding the frequency deviation caused by the effects presented in section II. This regulation is done by adjusting the hysteretic band (H).

V. Control Loop Design and Design Example

The design of the control loops is presented in this section, being applied to a design example. The input specifications for the example are: V_{in}= 3 V, V_{out}= 1 V, C_{out}= 4 µF, ESR= 4.5 mΩ, ESL= 450 pH and f_{sw}= 5 MHz.

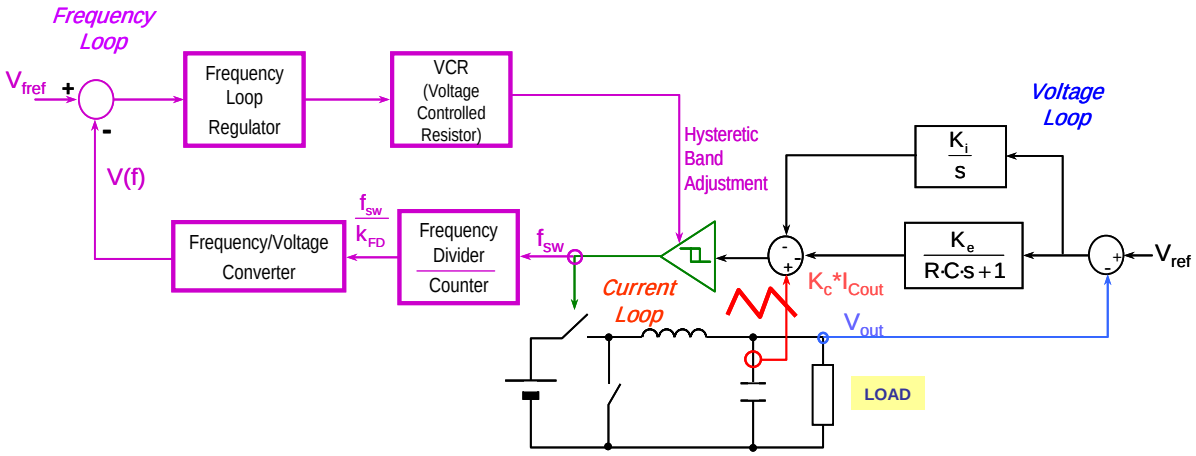


Figure 9. Proposed control scheme to achieve fast transient response with no frequency variation.

The design of the control loops are based on the following steps:

1.- Design of the current sensor:
In this design example the selected gain for the current sensor (Kc) is 1 V/A. Details about the sensor design are presented in [22].

2.- Design of the linear voltage loop: The design of the linear voltage loop needs to guarantee:

A. Maximum bandwidth of the linear voltage loop. If the f_{sw} is below the resonant frequency (f_{res}) the bandwidth of the voltage loop should be limited to one tenth of the f_{sw}, but if the f_{sw} is above the f_{res} the bandwidth of the voltage loop should be limited to one tenth of the f_{res} [1]. For the design example the $f_{res} < f_{sw}$, therefore the bandwidth of the voltage loop should be limited to one tenth of the f_{res}, in this case the $\Delta B \leq 150$ kHz. The selected bandwidth is 150 kHz.

$$\Delta B \leq \min\left(\frac{f_{sw}}{10}, \frac{f_{res}}{10}\right) \qquad (8)$$

B. Design criterion to meet voltage steps. This design procedure is focused on Dynamic Voltage Scaling (DVS) application where the output voltage needs to be dynamically regulated. DVS is a recent technique that reduces energy consumption in high performance digital systems. The tracking time is defined as the time required to step the voltage from one value to another.

B.1.- Determine the tracking time. The relationship between the required tracking time and the control bandwidth is given by equation (9). Equation (9) shows the minimum system bandwidth required to achieve the specified tracking time [18]. In this example the minimum tracking time for the selected bandwidth (ΔB = 150 kHz) is 2.12 µs.

$$\Delta B(Hz) = \frac{1}{\pi \cdot t_{track}} \qquad (9)$$

B.2.- Determine the gain of the linear voltage loop (Ke). The voltage loop commands a current source (Buck converter + hysteretic control) that supplies the C_{out} and the load. This voltage loop only requires [1] a constant gain (Ke) to follow the voltage reference. Equation (10) provides the required Ke to achieve the needed tracking time for whatever reference step. For the design example the Ke gain that guarantee the tracking time (2.12 µs) is equal to 3.77.

$$\frac{Ke}{Kc} = \frac{2 \cdot C}{t_{track}} \qquad (10)$$

C. Non interaction criterion with the non-linear loop. According to [1], the gain of the voltage loop (Ke) must be limited to avoid the amplification of the output voltage ripple and its interaction with the current loop. For that reason equation (11) should be accomplish to guarantee the non interaction criterion between the loops.

$$\frac{Ke \cdot \Delta V_{pp}}{Kc \cdot \Delta I_L} << 1 \Rightarrow Z_{Cout}(f_{sw}) \cdot \frac{Ke}{Kc} << 1 \qquad (11)$$

D.- Stability analysis. The non linear part (Buck converter + hysteretic control) is modeled as current source (Figure 10). This model is valid for frequencies smaller than $f_{sw}/5$. The value of the current source is given by $I_{Cout}=I_{ref}/Kc$. The external voltage loop commands a current source of the output capacitor.

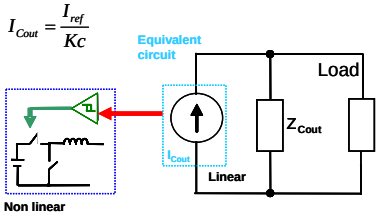


Figure 10. Equivalent circuit of the non linear loop.

In order to guarantee the no interaction criteria and the stability of the system a pole at the resonant frequency of the output capacitor is necessary to be added.

Figure 11 shows the average model of the external loop with a pole at resonant frequency of the C_{out} in the voltage regulator ($Ke/(RC \cdot s+1)$). Figure 12 shows the open loop gain of the external loop with a pole at f_{res}.

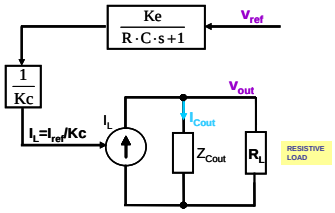


Figure 11. Average model of the external voltage loop with no integrator.

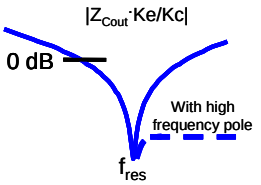


Figure 12. Open loop gain of the external voltage loop: Z_{Cout}*Ke/Kc.

Figure 13 shows the simulation of the open loop transfer function (V_{out}/V_{ref}) of the design example. The simulation results validate the design, the system is stable and the phase margin is 102º and the bandwidth is 140.9 kHz. This proposed scheme has dc error since the voltage loop regulator has not integrator.

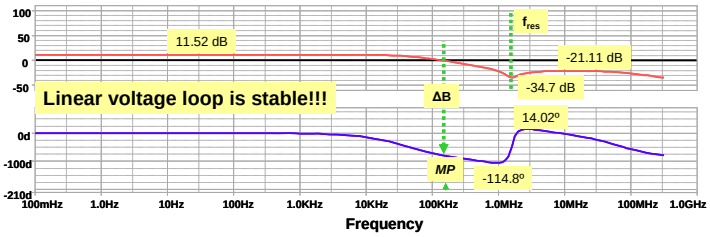


Figure 13. Open loop transfer function (V_{out}/V_{ref}) with a resistive load. The margin phase= 102º and ΔB= 140.9 kHz.

E. Designing for zero dc error. Figure 14 shows the integrator which is added to eliminate the dc error. Figure 15 shows the open loop transfer function with integrator to reduce the dc error. This integrator provides high gain at low frequencies but it is not affecting the stability and bandwidth of the linear voltage loop. For this example the Ki gain (integrator gain) is equal to 94.24e3 and the selected bandwidth for the integrator is 15 kHz.

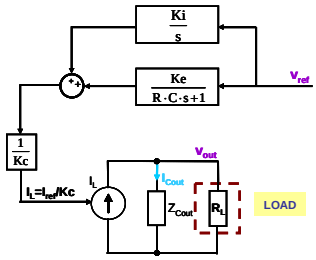


Figure 14. Average model of the external voltage loop with integrator (Ki/s) to reduce dc error.

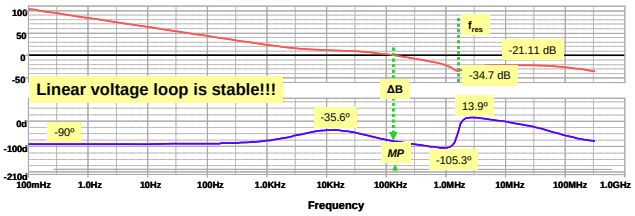


Figure 15. Open loop transfer function (V_{out}/V_{ref}) with a resistive load and an integrator (Ki/s). The margin phase= 102° and ΔB= 140.9 kHz.

F.- Response under load steps: The response of this control to load step is really fast thanks to the hysteretic control. However, this response also depends on the linear voltage loop. Therefore, once the voltage loop is designed, the response under load steps must be validated by simulation. Figure 16 shows the system performance under load step, this validation is done by simulation, the simulation shows a load step from 0.5 to 1.5 A (100A/µs). Also, the recovery of the voltage loop is very fast.

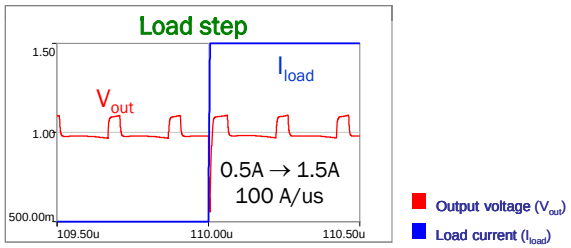


Figure 16. Simulation results. Response of the converter to a load step from 0.5 to 1.5 A (400 A/µs).

3.- Design of the frequency loop: The function of the frequency loop is to avoid the frequency variation (aging, temperature, etc.) and to adjust the switching frequency to the nominal value by changing the hysteretic band.

Figure 17 shows the blocks of the frequency loop scheme. It has five blocks: frequency divider (counter), frequency to voltage converter (VCO), frequency loop regulator, the voltage controlled resistor (VCR) and the hysteretic circuit.

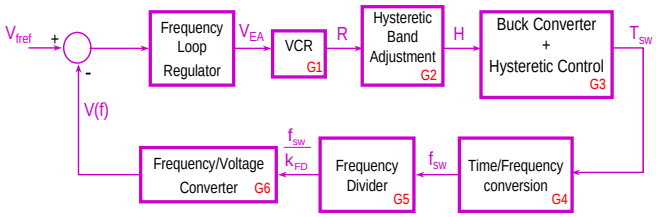


Figure 17. Frequency loop block diagram.

A. Frequency divider (counter). The frequency divider is based on binary asynchronous counters (Figure 18) and the principal functionality of this block is to scale the switching frequency down (divide the f_{sw} by K_{FD} factor). This is done because of the commercial frequency to voltage converter works in a range of tens of kHz. For the example the f_{sw} is divided by 1125.

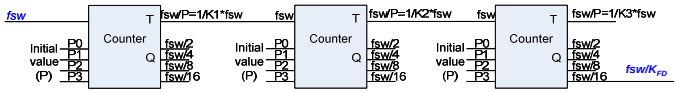


Figure 18. Binary asynchronous counters array used to divide the switching frequency by K_{FD} factor.

B. Frequency to voltage converter (VCO). This block converts the input frequency (switching frequency) into a linear proportional voltage (equation 12). The proportional voltage is defined approximately by the following equation:

$$V(f) = Vcc \cdot R \cdot C \cdot \frac{f_{SW}}{K_{FD}} \qquad (12)$$

C. Voltage controlled resistor (VCR). The VCR has a drain to source resistance that is controlled by the applied voltage in V_{GS}. Therefore, the VCR is considered as a variable resistance and the value depends on the V_{EA} (frequency loop command) applied in V_{GS}. The predictable resistance value (Rds_{ON}) is given by equation (13).

$$Rds_{ON} = \frac{Rds_{Vg}}{1 - \frac{V_{GS}}{Vgs_{Off}}} \qquad (13)$$

For the example the selected VCR is VCR7N (JFET voltage controlled resistor). These n-channel devices feature Rds_{Vg} ranging from 20 Ω to 60 Ω and the V_{GS} ranging from -3.5 V to -7 V.

D. Hysteretic circuit

The hysteretic circuit used to adjust the hysteretic band is shown in Figure 19. According to equation 14, variation in R4 (VCR) produces variation in the hysteretic band. The hysteretic band value (H) depends on the voltage applied to the variable resistor (VCR), the frequency loop and the hysteretic circuit. Therefore, adjusting these parameters is possible to adjust the hysteretic band and to maintain constant the switching

frequency. Figure 20 shows simulation results of the regulation capability, variation in R4 (VCR) produce band variation of +70% (2.94 MHz) and -35 % (7.7 MHz) around the nominal case (5 MHz).

$$H = \frac{\frac{R4\cdot(R1+R2)}{R4+R1+R2}\cdot R1\cdot Vcc}{\left(R3+\frac{R4\cdot(R1+R2)}{R4+R1+R2}\right)\cdot(R1+R2)} \qquad (14)$$

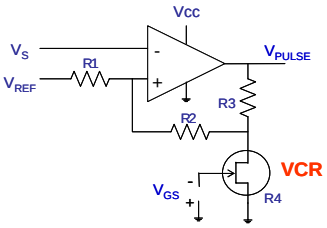


Figure 19. Hysteretic circuit to adjust the frequency variation using a voltage controlled resistor (VCR).

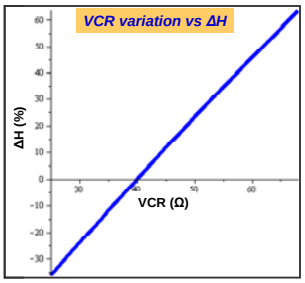


Figure 20. Example of regulation capability for a specific design.

E. Frequency loop regulator

Once the voltage linear loop and the non-linear loop is designed and validated by simulation. In order to design the regulator, it is necessary to linearize the system around the operating point. The small signal model is designed accounting the gain variations (produced for the VCR, V_{in} and V_{out}) and linearizing the gains of the frequency loop around working point (5 MHz). For this example the bandwidth for the frequency loop is 240 Hz and the dc gain of 60 dB.

The frequency loop must be a slow loop (bandwidth lower than 1.5 kHz) to avoid interactions with the voltage and current loops. Besides, the goal of this loop is to keep constant the switching frequency under steady state operation, thus dynamics requirements for this loop are very soft. Figure 21 shows the open loop gain of this frequency loop considering gain variations (maximum, nominal and minimum variation in GH, considering: maximum variations in VCR and maximum variations in V_{in} and V_{out}).

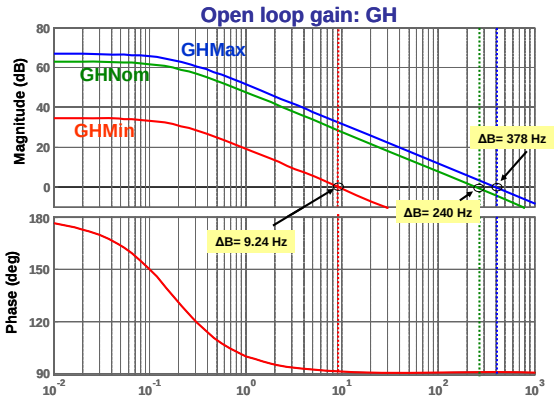


Figure 21. Maximum, nominal and minimum variation in GH ($error_f/V(f)$), considering: maximum VCR variations and maximum input and output voltage variations.

VI. Experimental Results

A discrete buck converter at 5 MHz of switching frequency is designed for specifications used along the design example. The trans-impedance amplifier used for the current sensor design is AD8061 (ΔB= 300 MHz). Experimental results show a proper operation of the proposed scheme during voltage step. Figure 22 shows a fast transition time from 1.5 V to 2.5 V and 2.5 V to 1.5 V in 2 µs. Also the no interaction of the control loops is validated.

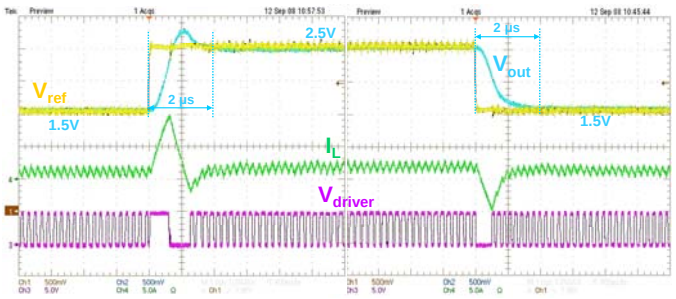


Figure 22. Voltage step (V_{ref}) from 1.5 V to 2.5 V within 2 µs (1 µs/div), V_{out} (500 mV/div), I_L (5 A/div).

Variations in V_{out} produce frequency deviation. Figure 23 shows how the frequency loop command adjusts the hysteretic band in order to keep constant the switching frequency. The dynamic response of the frequency loop is slow and takes 4 seconds to adjust the hysteretic band to the new steady state.

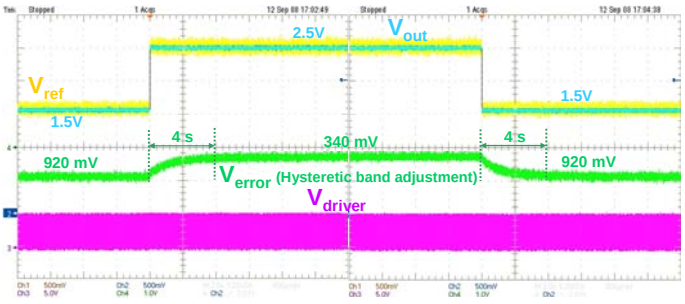


Figure 23. Frequency loop adjusts the hysteretic band to keep f_{sw} at 5 MHz. Voltage step (V_{ref}) from 1.5 V to 2.5 V V_{out} (500 mV/div), V_{error} (1 V/div).

The regulation under 45 A/µs load step is shown in Figure 24. Under a 1A load steps the output voltage deviation is approximately 50 mV being the output capacitance only 4 µF (4·1µF). Figure 25 shows the no interaction of the frequency loop during load steps, it also shows no dc error since there is an integration action in the voltage loop. This figure also shows that under load step the output voltage recovers the steady state in 40 µs.

VII. Conclusions

The control technique presented in [1] has very fast dynamic response. However, this method suffers of variable frequency.

In this paper the influence of parameters that modify the switching frequency is analyzed. An additional frequency loop is proposed in order to avoid the frequency deviation. Therefore, the frequency loop makes feasible the use of this non-linear control technique operating at constant f_{sw}.

The design methodology of the voltage loop (based-on stability and dynamic response issues) and the frequency loop is presented in detail and validated by simulation and experimentally. The loops are designed to guarantee no interaction among them. Experimental results show a very fast dynamic response in Buck converter (step voltage of 1.5 V to 2.5 V and from 2.5 V to 1.5 V in 1 µs).

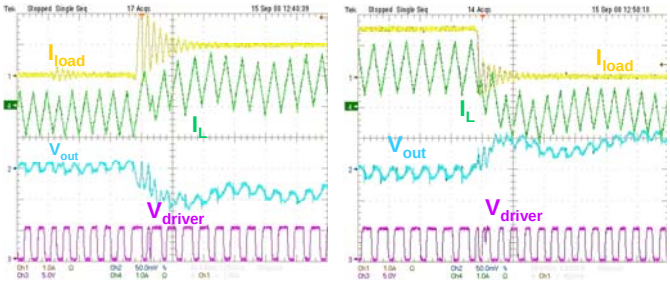


Figure 24. Output voltage regulation under a 45 A/µs load step (400 ns/div), V_{out} (50 mV/div), I_{load} (1 A/div), I_L (1 A/div).

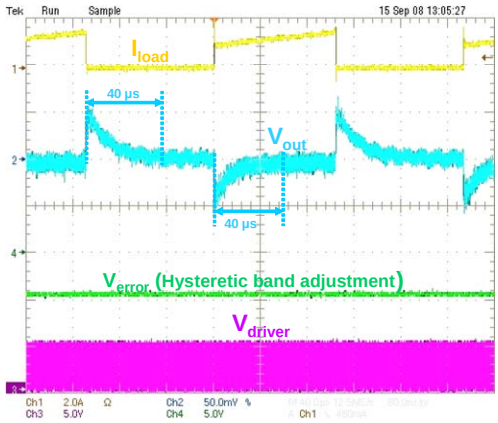


Figure 25. Frequency loop does not interact with linear loop under a 45A/µs load step. (400 ns/div), V_{out} (50 mV/div), I_{load} (1 A/div).

REFERENCES

[1] A. Soto, P. Alou and J.A. Cobos, "Non-Linear Digital control Breaks Bandwidth Limitations", in Proceedings of 2006 Applied Power Electronics Conference APEC '06.

[2] A. Abou-Alfotouh, A. Lotfi and M. Orabi, "Compensation Circuit Design Considerations for high Frequency DC/DC Buck Converters with Ceramic Output Capacitors", in Proceedings of the IEEE 2006 Applied Power Electronics Conference APEC '07.

[3] D. Goder, and W. R. Pelletier, "V2 architecture provides ultra-fast transient response in switch mode power supplies", in Proceedings of HFPC Power Conversion 1996.

[4] K. Leung and H. S. Chung, "Dynamic hysteresis band control of the buck converter with fast transient response," IEEE Trans. Circuits Syst., vol. 52, no. 7, Jul. 2005.

[5] G. Schuellein, "Current sharing of redundant synchronous buck regulators powering high performance microprocessors using the V2 control method", in Proceedings of the IEEE Applied Power Electronics Conference APEC'98.

[6] S. Qu, "Modeling and Design Considerations of V2 Controlled Buck Regulator", in Proceedings of the IEEE Applied Power Electronics Conference APEC'01.

[7] W. Huang, "A New Control for Multi-phase Buck Converter with Fast Transient Response", in Proceedings of the IEEE Applied Power Electronics Conference APEC'01.

[8] G. Feng, E. Meyer, and Y.F. Liu, "Novel digital controller improves dynamic response and simplifies design process of voltage regulator module," in Proceedings of the IEEE Applied Power Electronics Conference APEC'07.

[9] E. Meyer, Z. Zhang and Y.-F. Liu, "An Optimal Control Method for Buck Converters Using a Practical Capacitor Charge Balance Technique", in IEEE Trans. Power Electron., vol. 23, July 2008.

[10] Z. Zhao and A. Prodic, "Continuous-Time Digital Controller for High-Frequency DC-DC Converters", in IEEE Transactions on Power Electronics, vol. 23, pp. 564-573, March 2008.

[11] A. Costabeber, L. Corradini, P. Mattavelli and S. Saggini, "Time optimal, parameters-insensitive digital controller for DC-DC buck converters", in Proc. Conf. PESC'08.

[12] D. Biel, L. Martinez, J. Tenor, B. Jammes and J.C. Marpinard, "Optimum dynamic performance of a buck converter", in Proc. IEEE ISCAS'96.

[13] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao and D. Maksimovic, "Proximate Time-Optimal Digital Control for Synchronous Buck DC–DC Converters", in IEEE Transactions on Power Electronics, vol. 23, pp. 2018 - 2026, July 2008.

[14] V. Yousefzadeh and S. Choudhury, "Nonlinear digital PID controller for DC-DC converters", in Proceedings of the IEEE Applied Power Electronics Conference APEC'08.

[15] H. Haitao, V. Yousefzadeh and D. Maksimovic, "Nonlinear Control for Improved Dynamic Response of Digitally Controlled DC-DC Converters", in Proc. Conf. PESC'06, June 2006.

[16] A. Barrado et al.,"New DC-DC Converter With Low Output Voltage and Fast Transient Response", in Proceedings of the IEEE Applied Power Electronics Conference APEC'03

[17] A. Barrado, R. Vázquez, E. Olías, A. Lázaro and J. Pleite. "Fast Transient Response In Hybrid Sources with Combined Linear-Non-Linear Control", pp. 1599-1604, PESC'02, 2002.

[18] A. Soto, P.Alou, and J.A. Cobos, "Design Methodology for Dynamic Voltage Scaling in the Buck Converter", in Proceedings of the IEEE Applied Power Electronics Conference APEC'05

[19] A. Soto, A. de Castro, P. Alou, J.A. Cobos, J. Uceda and A. Lotfi, "Analysis of the Buck Converter for Scaling the Supply Voltage of Digital Circuits", in Proceedings of the IEEE 2003 Applied Power Electronics Conference APEC'03.

[20] S. K. Changchien, T.J. Liang, J.F. Chen, L.S. Yang, "Fast Response DC/DC Converter with Transient Suppression Circuit" in Proc. Conf. PESC06, June 2006.

[21] R. Redl, B. P. Erisman, and Z. Zansky, "Optimizing the load transient response of the buck converter," in Proc. IEEE APEC Conf. 1998, Volume 1, 15-19 Feb. 1998, pp. 170 – 176.

[22] S.C. Huerta, P. Alou, J.A. Oliver, O. Garcia, J. A. Cobos, A. Abou-Alfotouh, "Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast non-linear control", IEEE Applied Power Electronics Conference APEC'09.