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A VLSI Architecture for a High-Speed All-Digital Quadrature Modulator and Demodulator for Digital Radio Applications

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Abstract—**An all-digital architecture is presented for implementing the front-end signal processing functions in a quadrature modulator and demodulator for high bit-rate digital radio applications. A pair of CMOS chips has been designed and submitted for fabrication in a 1.25 μm process and is expected to accommodate symbol rates up to 35 MBd. The modulator chip accepts a pair of 8 b in-phase and quadrature data streams and generates a bandlimited IF output with an excess bandwidth factor of 35%. The demodulator chip accepts a digitized IF input signal and generates a pair of filtered in-phase and quadrature baseband signals. Clock and carrier recovery must be performed external to the demodulator chip. The modulator and demodulator chips each incorporate 40-tap multiplierless FIR square-root Nyquist matched filters and the cascade of the two chips achieves a peak intersymbol interference distortion of −54 dB (assuming ideal D/A and A/D conversion). The modulator chip can generate any arbitrary signal constellation within a rectangular grid of 256 × 256 points, thus, the all-digital implementation results in a generic chip set suitable for a wide variety of high bit-rate digital modem designs using various modulation formats such as M-ary PSK and QAM.**

I. Introduction

To accommodate demands for increasing data rates, many digital communication systems are switching over to more complex modulation formats which allow data transmission at higher rates without requiring larger bandwidths. As a consequence of these high data rates, most of the baseband signal processing is currently implemented with analog hardware. For example, in [1], a 400 Mb/s 256-QAM modem is described which primarily uses analog hardware for most of the signal processing functions.

Unfortunately, it becomes difficult and expensive to implement modems with complex modulation formats using analog hardware because the overall performance becomes very sensitive to various nonidealities, such as dc offset voltages, dc voltage drifts, analog filter phase distortions, and amplifier and mixer nonlinearities. However, with digital hardware implementations, virtually all of these distortions are eliminated and very precise and controllable performance can be achieved without sophisticated compensation techniques. Of course, even with a digital implementation of the baseband signal processing, amplifiers, mixers, and filters are still required at the IF and RF stages of the system implementation and careful design of these components is necessary in order to achieve satisfactory system performance. Other advantages of digital implementations include the ability to easily program the hardware to accommodate different data rates, modulation formats, and filter specifications. However, previous all-digital modem architectures, such as those described in [2] and [3], have been designed for relatively low-speed applications, i.e., less than 2 Mb/s.

In this paper, an all-digital architecture is presented for implementing the front-end signal processing functions in a high-speed quadrature modulator and demodulator. The architecture is partitioned into a modulator chip and demodulator chip each of which incorporate 40-tap FIR square-root Nyquist matched filters with an excess bandwidth factor of 35%. The excess bandwidth factor was chosen so that the transmit signal spectrum would satisfy FCC mask requirements for the commonly used microwave digital radio systems [4] (15 MBd in a 20 MHz channel at 4 GHz, 22.5 MBd in a 30 MHz channel at 6 GHz, and 35 MBd in a 40 MHz channel at 11 GHz). Fully parallel and pipelined architectures were adopted to accommodate modem designs with data rates up to 35 MBd.

The modulator chip accepts a pair of in-phase (I) and quadrature (Q) data streams and generates a bandlimited IF output signal at a rate of 4 samples per symbol (e.g., 140 MHz for a 35 MBd system). This signal must then be D/A converted and translated to the appropriate RF carrier frequency for transmission. The I and Q input symbols to the modulator chip can each have up to 8 b of precision, thus, any signal constellation in a space of 256 × 256 points can be generated. The receiver must translate the RF input signal to an IF frequency equal to the symbol rate where it is to be digitized at a rate of 4 samples per symbol. The demodulator chip accepts the digitized IF signal and generates a pair of I and Q filtered baseband signals at a rate of 2 samples per symbol. Clock and carrier recovery functions must be implemented external to the demodulator chip. When the modulator and

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demodulator chips are cascaded, a peak intersymbol interference (ISI) distortion of -54 dB is achieved (assuming ideal D/A and A/D conversion). The effects of limited precision D/A and A/D converters on ISI performance are discussed in Section III.

By choosing the modulator and demodulator IF frequencies to be equal to the transmitted symbol rate and by implementing multiplierless transmit and receive matched filters, significant hardware reductions were achieved which allowed single chip VLSI implementations at clock rates in excess of 100 MHz. Prototype modulator and demodulator chips have been designed and submitted for fabrication in a 1.25 μm CMOS process. The all-digital architectures result in a very flexible chip set which can be used in a wide variety of high-performance digital modem designs using various advanced multilevel modulation formats. The details of the chip architectures are presented in Section II and the finite wordlength tradeoffs are presented in Section III.

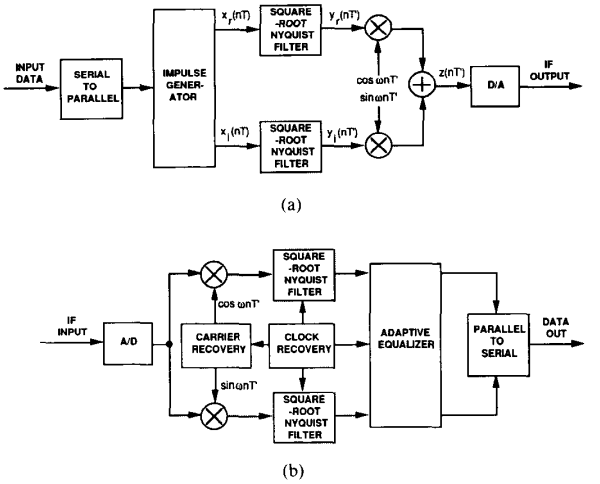


Fig. 1. Basic all-digital architectures. (a) Modulator. (b) Demodulator.

II. Architecture Description

Simplified block diagrams of an all-digital quadrature modulator and demodulator are shown in Fig. 1. Note that the D/A and A/D conversion is performed at IF rather than baseband. The primary function of the modulator shown in Fig. 1(a) is to accept a serial input data stream and generate a bandlimited IF analog output waveform. The serial input data stream is first converted into a lower rate symbol stream which can be interpreted as the real and imaginary parts of a complex stream of impulses $x(nT) = x_r(nT) + jx_i(nT)$. Different modulation formats are accommodated by specifying different signal constellations for $x(nT)$.

The impulses $x_r(nT)$ and $x_i(nT)$ are then filtered by a pair of identical interpolating low-pass filters which generate the real and imaginary parts of the complex bandlimited baseband signal $y(nT') = y_r(nT') + jy_i(nT')$, where $T' = T/K$, and K is the integer factor by which the sampling rate must be increased in order that Nyquist's Sampling Theorem is not violated by the modulation process. The resulting modulated signal $z(nT')$ is therefore given by

$$z(nT') = \mathrm{Re}\left[y(nT')e^{-j\omega nT'} \right]. \tag{1}$$

The demodulator shown in Fig. 1(b) performs the inverse function of the modulator. The digitized IF signal is quadrature downconverted to baseband and low-pass filtered by the receive square-root Nyquist matched filters. Ideally, the outputs of the receive matched filters, when sampled every T seconds, should correspond to the original transmitted symbols $x_r(nT)$ and $x_i(nT)$.

The transmit and receive filters are critical elements in the modulator and demodulator. They must meet very strict frequency-domain specifications imposed by FCC masks and they must achieve a very small level of time-domain ISI in order to accommodate higher order modulation formats such as 256-QAM. It is well known that the optimum partitioning of the transmit and receive filters in the presence of additive white Gaussian noise in the communication channel is the so-called "matched" filter pair whereby the transmit and receive filter frequency responses are complex conjugates of one another, i.e.,

$$H_R(\omega) = H_T^*(\omega). \tag{2}$$

Using techniques presented in [5], 40-tap FIR matched transmit and receive filters were designed. Nonrecursive FIR structures were chosen since, in addition to having very regular architectures suitable for VLSI implementation, they can be highly pipelined to increase their throughput rate. The transmit matched filter was designed to meet various FCC mask criteria [4], the most stringent of which being a 40 MHz mask with a symbol rate of 35 MBd. The resulting filter has an excess bandwidth factor of 35%, an oversampling factor of $K = 4$, and a stopband attenuation of 53.8 dB (with ideal unquantized coefficients).

If the transmit filter coefficients are denoted by h_k, $k = 0, 1, \cdots, N-1$, then the corresponding receive matched filter coefficients are given by h_k, $k = N-1, \cdots, 1, 0$. For an oversampling factor of $K = 4$, the peak intersymbol interference distortion of the cascade of the transmit and receive matched filters is given by

$$\mathrm{ISI} = 20 \log_{10} \left(\frac{2 \sum_{k=1}^{(N/4)-1} \left| \sum_{i=0}^{N-1-4k} h_i h_{i+4k} \right|}{\sum_{k=0}^{N-1} (h_k)^2} \right). \tag{3}$$

(N is restricted to be a multiple of 4 (see [5]), thus, the summation limits in (3) are always exact integers.) Note that (3) is valid for the baseband cascade of the matched filters and does not incorporate any quadrature modulation and demodulation. Due to the finite stopband attenuation in practical matched filter designs, the modulation

and demodulation process will introduce additional ISI. The proposed modulator and demodulator architectures have an IF center frequency equal to $1/4$ the filter sampling rate, i.e., $\omega T' = \pi/2$ in Fig. 1. After incorporating the effects of the quadrature modulation and demodulation, the resulting ISI is given by

$$\text{ISI} = 20 \log_{10} (\max (\text{EVENISI}, \text{ODDISI})) \quad (4a)$$

where

$$\text{EVENISI} = \left(\frac{2 \sum_{k=1}^{(N/4)-1} \left| \sum_{i=0}^{(N/2)-1-2k} h_{2i} h_{2i+4k} \right|}{\sum_{k=0}^{(N/2)-1} (h_{2k})^2} \right) \quad (4b)$$

and

$$\text{ODDISI} = \left(\frac{2 \sum_{k=1}^{(N/4)-1} \left| \sum_{i=0}^{(N/2)-1-2k} h_{2i+1} h_{2i+4k+1} \right|}{\sum_{k=0}^{(N/2)-1} (h_{2k+1})^2} \right). \quad (4c)$$

The EVENISI and ODDISI terms correspond to the ISI in the in-phase and quadrature rails of the demodulator.

A. Filter Coefficient Optimization

A direct implementation of the 40-tap matched filter would require 40 multipliers, which would consume a substantial amount of silicon area and, hence, would not permit a single chip implementation. Furthermore, the maximum speed of operation would be severely limited due to the numerous multiply and accumulate operations required. In addition, implementing a fixed coefficient digital filter with multipliers is very inefficient. A much more efficient realization involves the use of a canonic signed-digit (CSD) representation for each of the coefficients. A CSD code represents the filter coefficients as sums and differences of several powers of two. Since power-of-two multiplications can be obtained for free in a dedicated hardware implementation, the use of a CSD representation results in a substantial reduction in hardware complexity.

A CSD coefficient optimization technique for conventional FIR filters is presented in [6]. However, the optimization problem for data transmission filters is complicated by the fact that time domain ISI constraints as well as frequency domain attenuation constraints are imposed on the design. The algorithm in [6] was modified [7] to incorporate the additional ISI constraints, and a 40-tap filter with CSD coefficients was designed. The coefficients were restricted to have at most 4 nonzero digits, thus, each coefficient can be realized in hardware with at most 3 adders and 4 hardwired shifts. The stopband attenuation of the optimized CSD filter is 53 dB, and the residual ISI given by (4a) is -55.9 dB. The baseband magnitude response of the ideal and CSD filters is shown in Fig. 2. The IF output spectrum of the modulator is shown in Fig. 3, along with the FCC mask for a 35 MBd symbol rate in a 40 MHz microwave radio channel. Note that only a very small amount of stopband attenuation is sacrificed by the filter with quantized coefficients, however, the hardware implementation of the CSD transmit and receive filters becomes an order of magnitude simpler than the original filters since each multiplier has been replaced with 3 adders.

It is readily apparent from Fig. 3 that the 40-tap filter design greatly exceeds the FCC mask specifications in the stopband. A 40 dB stopband attenuation with a much more gradual roll-off would have been sufficient and could have been accomplished with fewer filter taps. The primary motivation for increasing the stopband attenuation of the digital matched filters is to minimize the ISI degradation resulting from the transition bands and stopbands of the analog filters in the system. Ideally, the passbands of all analog filters in the system extend out to the stopband edges of the modulator output spectrum and have zero ripple and exactly linear phase. The transition bands and stopbands of the analog filters would then overlap with the stopband of the transmitted IF spectrum. The residual ISI of -55.9 dB resulting from the coefficient optimization of the digital filter will be degraded by any additional filtering in the system. However, if the stopband attenuation of the digital matched filters is large, then the transition bands and stopbands of the analog filters will have a negligible effect on the transmitted signal. But if the digital filters have a gradual roll-off with a smaller stopband attenuation, then the effect of the analog filters will be more pronounced and the ISI degradation will be greater.

In practice, it will probably turn out that the passband ripple and passband group delay distortion of the analog filters will have a much more serious effect on the ISI than the transition bands and stopbands. However, it was decided that the additional robustness of the ISI performance resulting from a larger stopband attenuation in the digital filter was worth the additional chip complexity.

B. Architecture Simplifications

Choosing the IF center frequency of the modulator and demodulator to be $1/4$ of the sampling rate, or equivalently, to be equal to the symbol rate $1/T$, results in substantial architecture simplifications. By selecting this center frequency, the cosine and sine waveforms needed in the mixing function can be sampled at 0°, 90°, 180°, and 270°, thereby producing samples of values 1, 0, -1, 0, for the cosine waveform and 0, 1, 0, -1 for the sine waveform. These values eliminate the need for high-speed digital multipliers and adders to implement the mixing functions in both the modulator and demodulator. Instead, a 2-to-1 multiplexer and an inverter can perform the mixing process in the modulator, and a 1-to-2 demultiplexer and an inverter can perform the mixing process

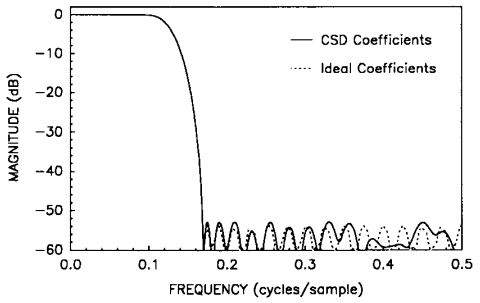


Fig. 2. Baseband magnitude frequency response of 40-tap CSD coefficient transmit filter.

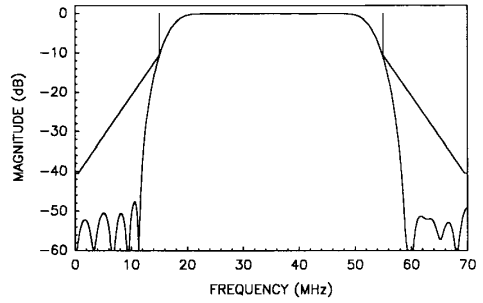


Fig. 3. Modulator IF magnitude response with 40-tap CSD coefficient transmit filter for 35 MBd symbol rate (140 MHz sample rate).

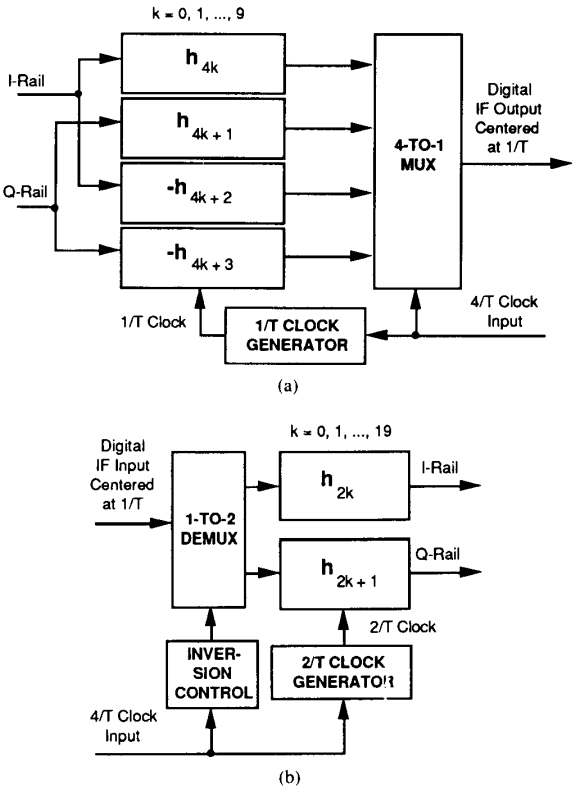


Fig. 4. Final all-digital architectures. (a) Modulator. (b) Demodulator.

in the demodulator. In addition, since half of the cosine and sine samples are zero, the two identical 40-tap FIR transmit filters required for the I and Q rails in the modulator can be replaced by only one 40-tap filter which can simultaneously process the data for both the I and Q rails.

A further simplification in the modulator architecture can be obtained by taking advantage of the fact that the transmit filter is an interpolating FIR filter with a 1:4 interpolation ratio. Thus, the single 40-tap filter can be broken down into four 10-tap "subfilters," which can process the I and Q data in parallel. Moreover, these 10-tap "subfilters" can be clocked at a rate equal to the symbol rate $1/T$, rather than the output oversampled clocking rate of $4/T$. Hence, a tremendous amount of hardware devoted to pipelining overhead can be avoided, since the clock period is increased by a factor of 4. Additionally, the inverter needed to implement the -1 multiplication in the mixing process can be eliminated by simply negating half of the 40 filter coefficients. Thus, the only hardware needed to implement the modulator are four 10-tap FIR filters, obtained from the 40-tap transmit filter, and a 4-to-1 multiplexer. The final modulator architecture is shown in Fig. 4(a), which implements the functions in the shaded portion of Fig. 1(a). It can be seen that while the input clock to the modulator is at a rate equal to $4/T$, internally over 90% of the modulator hardware is clocking at the much slower rate of $1/T$, thereby considerably easing the circuit design requirements.

Similar architectural simplifications can be achieved in the demodulator since the receive matched filter is a decimating filter with a 2:1 decimation ratio. The final demodulator architecture contains a 2-to-1 demultiplexer with inversion logic to implement the mixing process, and two 20-tap "subfilters" obtained from the 40-tap receive filter by selecting the even and odd tap coefficients. These "subfilters" are clocked at a rate of $2/T$ instead of the initial oversampled rate of $4/T$. As a result, one 20-tap "subfilter" outputs the in-phase symbol component, and the other 20-tap "subfilter" outputs the quadrature symbol component. Output samples occur every $T/2$ seconds (ideal for $T/2$ fractionally-spaced adaptive equalizers). Again, while the demodulator appears to be operating at a rate equal to $4/T$, internally over 90% of the demodulator hardware is clocking at a slower rate of $2/T$. The final demodulator architecture is shown in Fig. 4(b), which implements the functions in the shaded portion of Fig. 1(b).

C. System-Level Considerations

The D/A converter and A/D converter play key roles in determining the overall system performance due to their critical location within the flow of data. For the all-digital architecture in Fig. 1, the D/A converter is placed at the IF output of the modulator where the data rate is $4/T$, whereas for a typical analog architecture, the D/A's are in the baseband I and Q rails and thus operate at the symbol rate of $1/T$. For the prototype modulator chip, a max-

imum symbol rate of 35 MBd is projected. Hence, the D/A converter must be capable of operating at 140 MHz.

An unavoidable side effect of the D/A converter is the introduction of sin $(x)/x$ amplitude distortion into the transmit spectrum. Thus, a $x/\sin(x)$ compensation filter is required to equalize the sin $(x)/x$ frequency response roll-off of the D/A converter. A digital $x/\sin(x)$ compensation filter chip has been designed to operate with the modulator chip [8]. A digital compensation filter has the advantage that the $x/\sin(x)$ compensation is accurate for all data rates, whereas an analog compensation filter compensates the spectrum distortion only for a single data rate.

Special attention must also be given to the A/D converter in the demodulator. As shown in Fig. 1(b), the A/D converter is placed at the IF front-end of the demodulator where the data rate is $4/T$, whereas for a typical analog architecture, the A/D's are in the baseband I and Q rails and need only operate at the symbol rate of $1/T$. Therefore, to accommodate a symbol rate of 35 MBd, the A/D converter must be capable of operating at 140 MHz. The required wordlengths of the D/A and A/D converters is discussed in Section III.

The requirement to have the IF center frequency equal to the symbol rate greatly simplifies the digital chip architecture, but it does slightly complicate the system architecture. The majority of microwave digital radio systems in existence today use standard IF frequencies of 70 or 140 MHz, and thus, an additional mixer stage would be required to translate the IF to one of these standard frequencies. Furthermore, a fairly sophisticated IF filter is required after the first mixer stage to reject image frequencies. For example, with a 35% excess bandwidth factor and a 35 MBd symbol rate, the stopband-to-stopband edge bandwidth of the modulator output signal is 47.25 MHz (see Fig. 3) and the spectral separation of the next image band is only 22.75 MHz. Thus, the IF filters must have an approximately linear phase response, low passband ripple, 47.25 MHz passband bandwidth, and a stopband-to-stopband edge bandwidth of 92.75 MHz, which are fairly challenging specifications.

III. Pipelining and Wordlength Issues

Since speed was the primary consideration in the implementation of the prototype modulator and demodulator chips, fully parallel pipelined architectures were required. The transpose direct-form FIR filter structure with carry-save addition shown in Fig. 5 was chosen due to its inherent high-speed operation and its suitability for pipelining. Each filter coefficient in Fig. 5 was then replaced by its corresponding 4-digit CSD representation to obtain the final filter structure. Because of the architectural simplifications discussed in Section II-B, pipelining within the transmit filter was found to be unnecessary. However, for the demodulator receive filter, pipelining was found to be necessary since the receive filter is clocked at $2/T$, while the transmit filter is clocked at $1/T$. An example of the pipelining technique used in the transpose direct-form receive CSD filter is shown in Fig. 6. Pipeline registers are

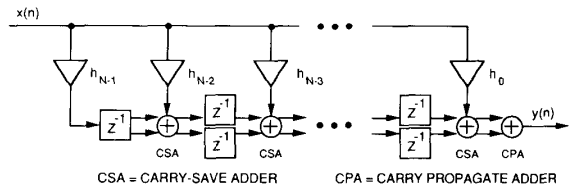


Fig. 5. Transpose direct-form filter structure with carry-save addition.

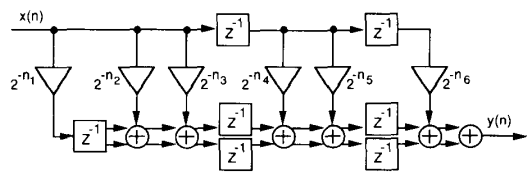


Fig. 6. Transpose direct-form CSD filter structure with pipelining.

inserted between every two adder stages. Note that, in general, further pipelining within the transmit and receive filters could be implemented if the system specifications should warrant the additional speed.

The adders within the prototype transmit and receive filters were implemented as carry-save adders so that carry signals were not required to ripple through the adders at each stage. At the end of each "subfilter" in the modulator and demodulator, pipelined carry ripple adders were used to merge the carry bits with the sum bits to obtain the final two's complement output.

Finite wordlength effects were also considered in the implementation of the transmit and receive digital filters. The tolerable levels of ISI within the overall modem becomes an important factor in determining the internal wordlengths of the modulator and demodulator, as well as the input and output wordlengths. A simulation program was written which emulates all of the bit-level operations that occur within the modulator and demodulator chip architectures. By varying the modulator and demodulator internal and input/output wordlengths, the finite precision effects on the ISI could be determined, and from these results, the appropriate wordlengths for the VLSI implementation were selected. For the simulation results that follow, an 8 b input I and Q symbol wordlength for the modulator was assumed. In addition, the modulator output was directly connected to the demodulator input. This latter assumption is equivalent to a distortionless transmission channel and perfect D/A and A/D conversion, therefore, the simulation results represent an upper bound as to the achievable performance in a practical modem implementation. The simulations calculated the resulting ISI SNR which is defined as

$$\text{ISI SNR} = 10\log_{10}\left(\frac{\text{Signal Power}}{\text{Quantization Noise Power}}\right) = 10\log_{10}\left(\frac{E\left[x(nT)^2\right]}{E\left[\left(x(nT)-x'(nT)\right)^2\right]}\right) \quad (5)$$

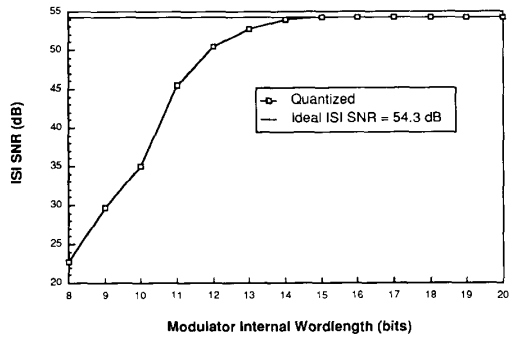


Fig. 7. ISI SNR of modulator/demodulator versus modulator internal wordlength.

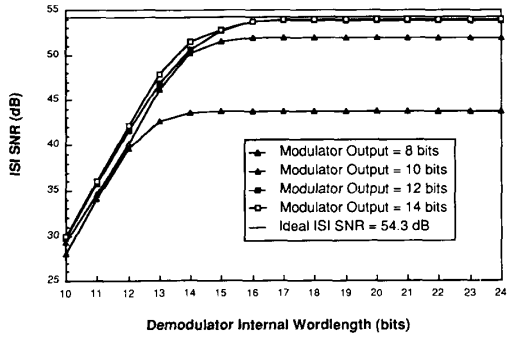


Fig. 8. ISI SNR of modulator/demodulator versus demodulator internal wordlength.

where $x(nT)$ are the transmit symbols and $x'(nT)$ are the receive matched filter output samples. The expectations in (5) were computed as time averages over 16K random input symbols of a 256-QAM signal constellation. The I channel and Q channel ISI SNR were computed separately and the lesser value was selected as the overall ISI SNR.

For the first simulation, all wordlengths were kept at their maximum values (i.e., no rounding or truncation errors occurred anywhere within the architecture). For this "ideal" case the ISI SNR was determined to be 54.3 dB. This is the maximum achievable performance of the finite wordlength architecture for the given set of CSD filter coefficients.

Next, the modulator internal wordlength was varied between 8 and 20 b and the modulator output and demodulator internal and output wordlengths were kept equal to their original full precision values. The resulting ISI SNR is plotted in Fig. 7. The SNR performance varies considerably for internal wordlengths between 8–14 b and shows little improvement when internal wordlengths over 14 b are used. Consequently, the internal wordlength of the prototype modulator was selected to be 14 b.

Next, the demodulator internal wordlength was varied between 10 and 24 b. For these calculations the modulator internal wordlength was fixed at 14 b, and various modulator output wordlengths (equal to the demodulator input wordlength) were used as parameters to generate a family of ISI SNR curves. The results, plotted in Fig. 8, show that while a demodulator internal wordlength of 14 b is sufficient for a modulator output wordlength of 8 b, a demodulator internal wordlength of 16 b provides satisfactory ISI SNR for up to 14 b of modulator output wordlength. Hence, an internal demodulator wordlength of 16 b was selected for the prototype demodulator.

In Fig. 9, the ISI SNR is plotted as a function of the output wordlength of the modulator, given that the internal wordlengths of the modulator and demodulator were fixed at 14 and 16 b, respectively. The results show that for a pair of ideal 8 b D/A and A/D converters the ISI SNR is 43.7 dB, and for a pair of ideal 10 b D/A and A/D converters the ISI SNR is 51.8 dB. As an additional feature of the modulator and demodulator chips, user-selectable rounding of the modulator and demodulator outputs from 8 to 14 b was implemented. Rounding results in a nontrivial increase in the ISI SNR over that obtained by straight truncation at the modulator and demodulator outputs. This increase in ISI SNR can be seen in Fig. 10 where the ISI SNR was measured while varying the demodulator output wordlength between 8 to 16 b. For these results the modulator output wordlength was fixed at 10 b. It can be seen that the increase in ISI SNR with rounding versus truncation is especially evident when low demodulator output wordlengths are used.

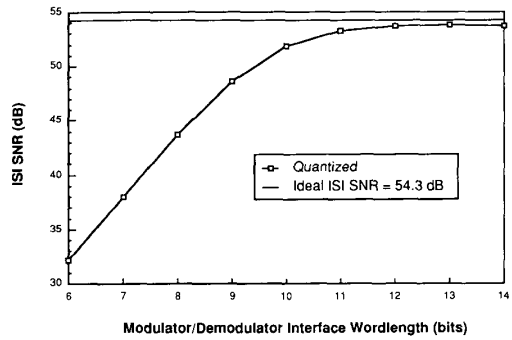


Fig. 9. ISI SNR of modulator/demodulator versus interface wordlength.

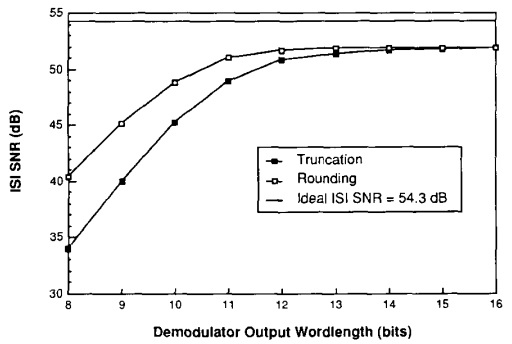


Fig. 10. ISI SNR of modulator/demodulator versus demodulator output wordlength.

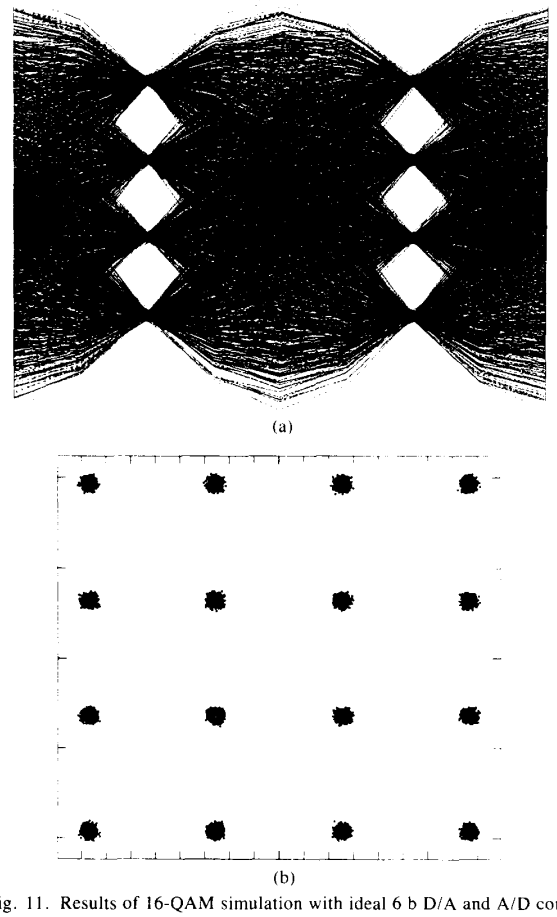


Fig. 11. Results of 16-QAM simulation with ideal 6 b D/A and A/D conversion (ISI SNR = 31.8 dB). (a) Eye diagram. (b) Symbol constellation.

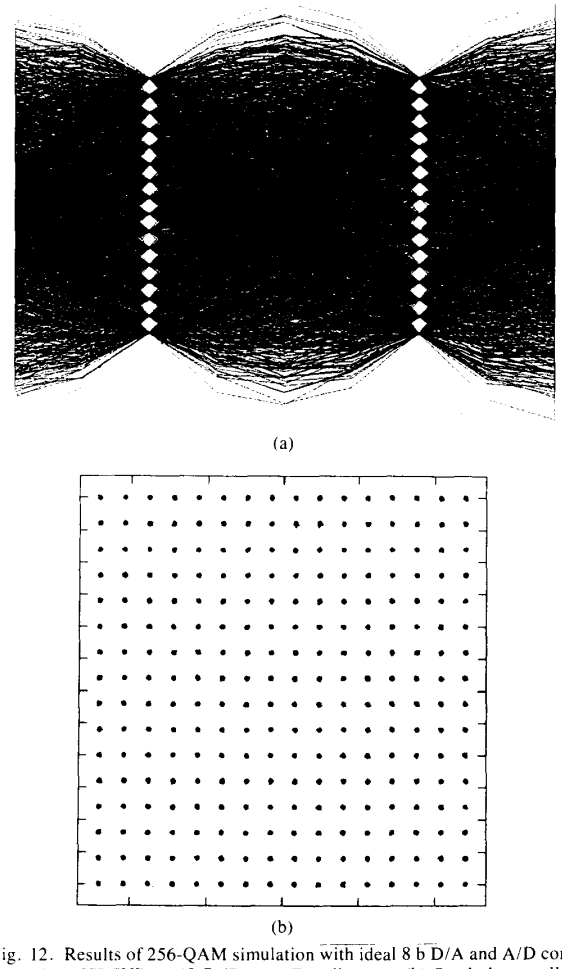


Fig. 12. Results of 256-QAM simulation with ideal 8 b D/A and A/D conversion (ISI SNR = 43.7 dB). (a) Eye diagram. (b) Symbol constellation.

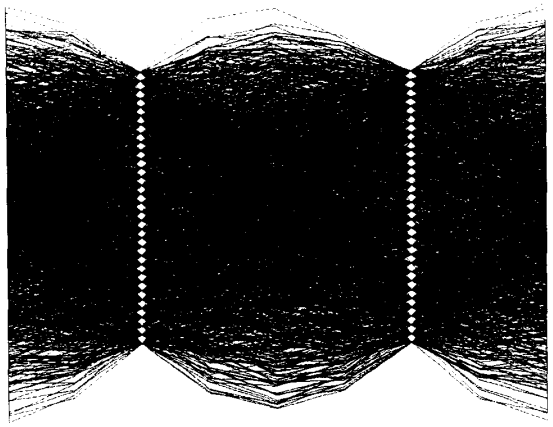
A. Simulation Examples

To demonstrate the versatility of the all-digital QAM modulator and demodulator chip set, various QAM formats were simulated, and the resulting eye patterns and symbol constellations at the output of the demodulator were plotted. For these simulations, the actual modulator/demodulator VLSI implementation wordlengths were used, i.e., a modulator input wordlength of 8 b, a modulator internal wordlength of 14 b, and a demodulator internal wordlength of 16 b. As before, the modulator and demodulator were connected back-to-back, thereby simulating an ideal distortionless channel (and also perfect clock and carrier recovery). The wordlength at the IF interface between the modulator and demodulator chips was varied to simulate the effects of finite precision D/A and A/D conversion.

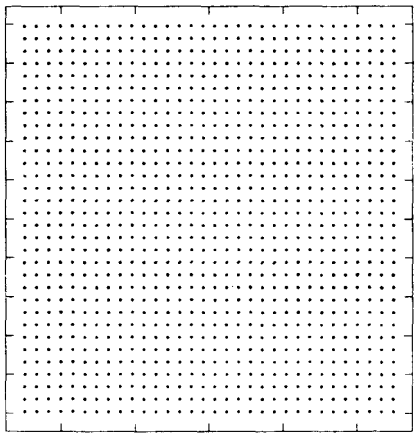
In the first example, a 16-QAM signal constellation was simulated with a 6 b D/A and A/D wordlength. An ISI SNR of 31.8 dB was measured and the resulting baseband eye diagram and symbol constellation at the demodulator output are shown in Fig. 11. In the second example, a 256-QAM input signal constellation was simulated with an 8 b D/A and A/D wordlength. An ISI SNR of 43.7 dB was measured and the demodulator eye diagram and symbol constellation are shown in Fig. 12. Finally, a 1024-QAM input signal constellation was simulated. An ISI SNR of 53.7 dB was measured with a 10 b D/A and A/D wordlength, and the corresponding eye diagram and symbol constellation are shown in Fig. 13. These results clearly indicate that very good ISI performance can be achieved without imposing unreasonable requirements on the D/A and A/D converter wordlengths.

IV. Conclusions

Several architectural simplifications and finite wordlength optimizations have been presented for implementing a high-performance all-digital quadrature modulator and demodulator which allow single-chip high-speed VLSI implementations. Prototype chips have been designed and submitted for fabrication to the TRW Microelectronics Center in a 1.25 μm CMOS process. These chips are projected to accommodate any symbol rate up



(a)



(b)

Fig. 13. Results of 1024-QAM simulation with ideal 10 b D/A and A/D conversion (ISI SNR = 51.7 dB). (a) Eye diagram. (b) Symbol constellation.

to 35 MBd and a wide variety of modulation formats such as M-ary PSK and M-ary QAM. Simulations indicate that satisfactory SNR performance can be achieved for 256-QAM modulation with 8 b IF D/A and A/D conversion, and therefore, IF sampling techniques, which have traditionally been feasible only in voiceband data modems, can now be applied in high bit-rate digital radio modem designs.

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