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A VLSI CHIP SET FOR REAL TIME VECTOR QUANTIZATION OF IMAGE SEQUENCES

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ABSTRACT

This paper describes the architecture and implementation of a VLSI chip set that vector quantizes (VQ) image sequences in real time. The chip set forms a programmable Single-Instruction, Multiple-Data (SIMD) machine which can implement various vector quantization encoding structures. Its VQ codebook may contain unlimited number of codevectors, N, having dimension up to K = 64.

Under a weighted least squared error criterion, the engine locates at video rates the best code vector in full-searched or large tree searched VQ codebooks. The ability to manipulate tree structured codebooks, coupled with parallelism and pipelining, permits searches in as short as O(log N) cycles. A full codebook search results in O(N) performance, compared to O(KN) for a Single-Instruction, Single-Data (SISD) machine. With this VLSI chip set, an entire video code can be built on a single board that permits realtime experimentation with very large codebooks.

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OVERVIEW

- MULTISPECTRAL COMPRESSION PROBLEM
- PHILOSOPHY <---> A NEED
- VX IMPLEMENTATION CHALLENGES
- VQ CHIP SET

COMPRESSION RESEARCH AT UCLA

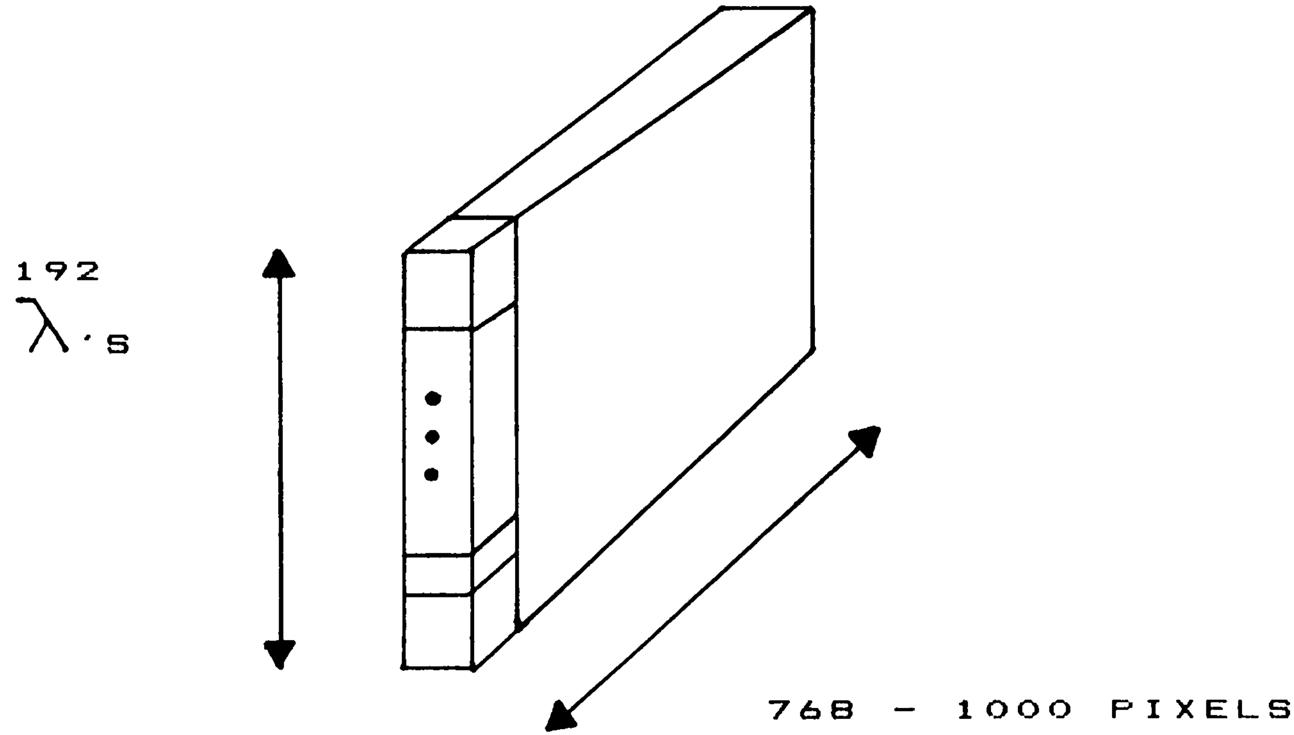
<u>ALGORITHMS</u>

- LOW RATE VIDEO
- SINGLE FRAME
- MULTISPECTRAL

<u>HARDWARE</u>

- APPLICATION SPECIFIC INTEGRATED CIRCUITS

MULTISPECTRAL COMPRESSION PROJECT (JPL)

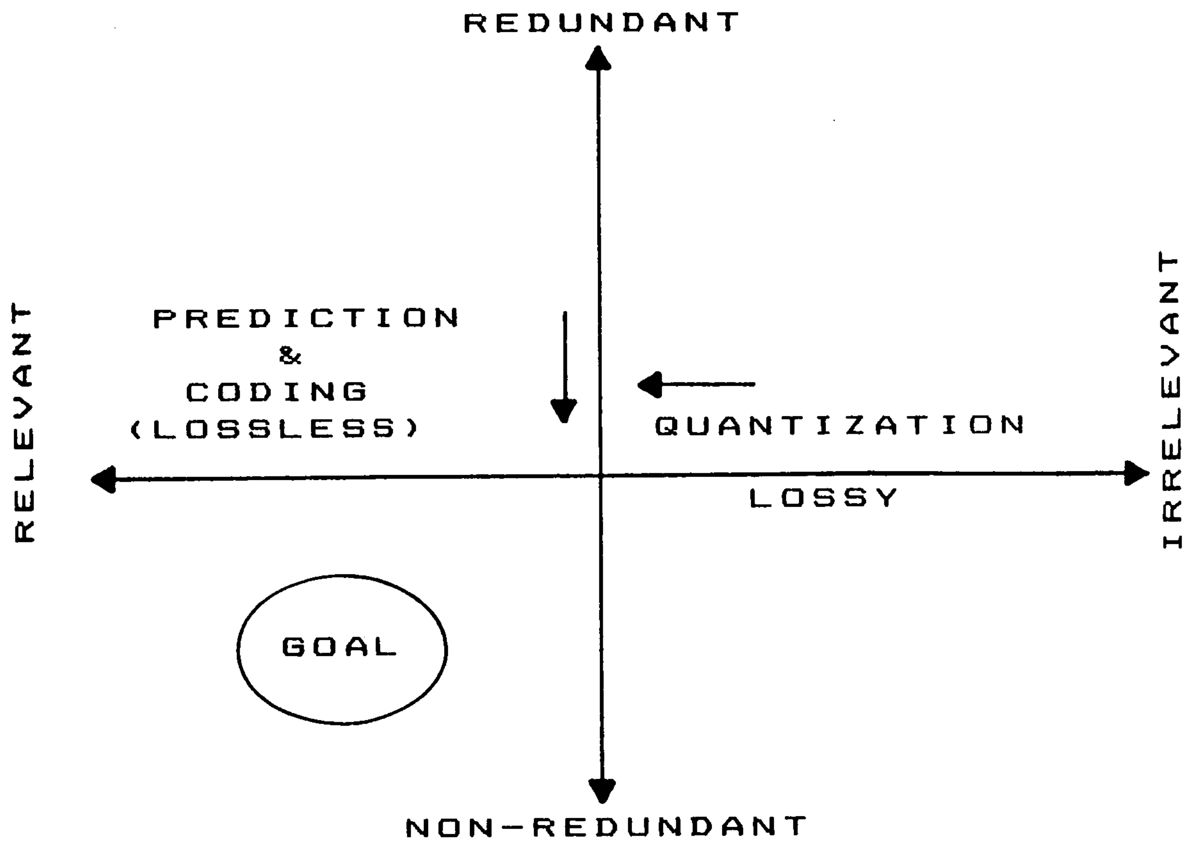


$$\frac{\text{50 MEGAPIXELS/SEC}}{\text{17 CHANNELS}} = \frac{3 \times 10^6}{\text{PIX/SEC/CH}}$$

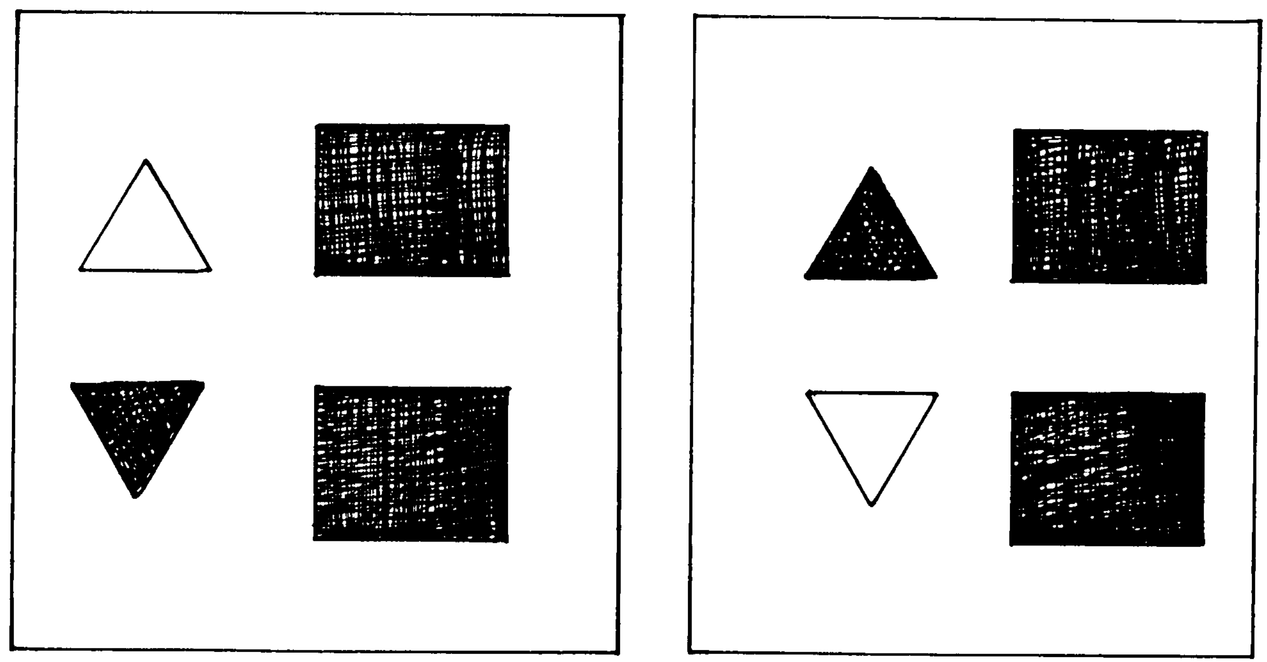
DESIRE OVER 50:1

--> UNDER 1/4 BITS/PIXEL

DATA COMPRESSION PROBLEM



DESIGNER'S PERCEPTIONS
VS.
USER'S NEEDS

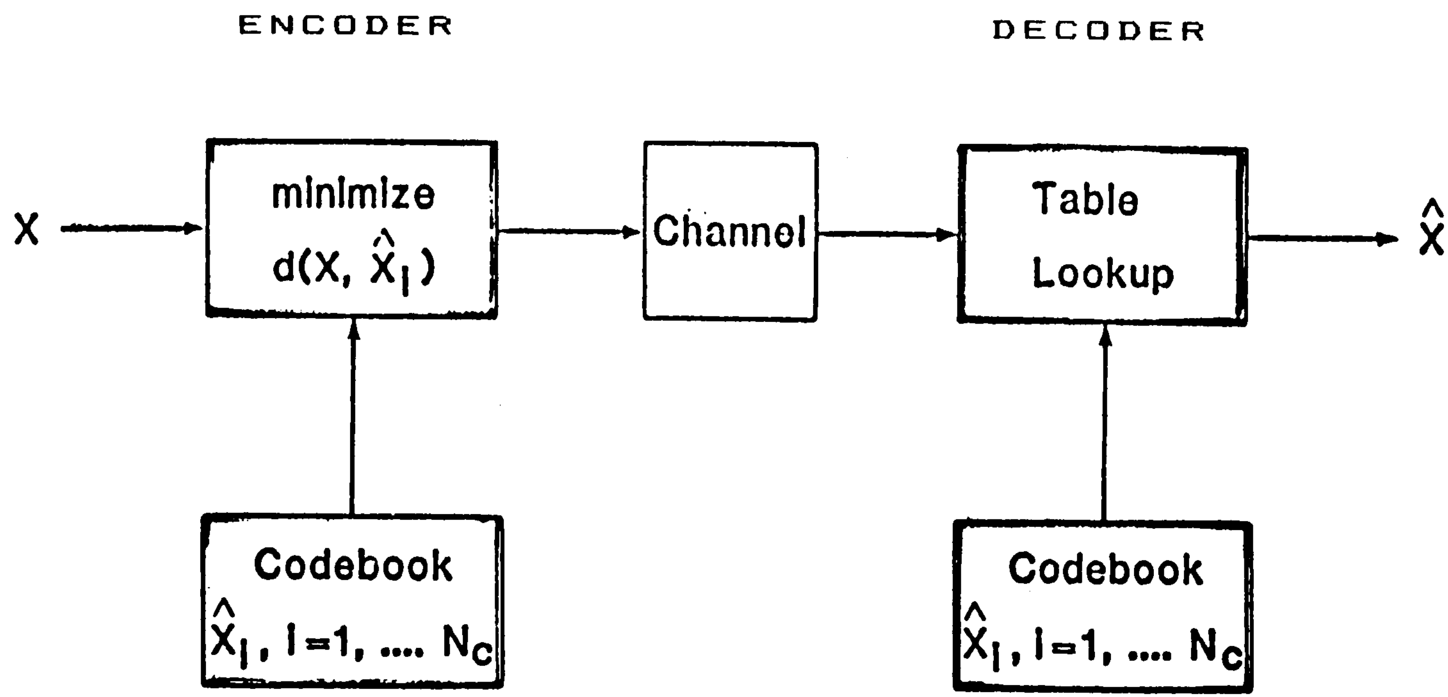


WHAT IS <u>RELEVANT</u>?

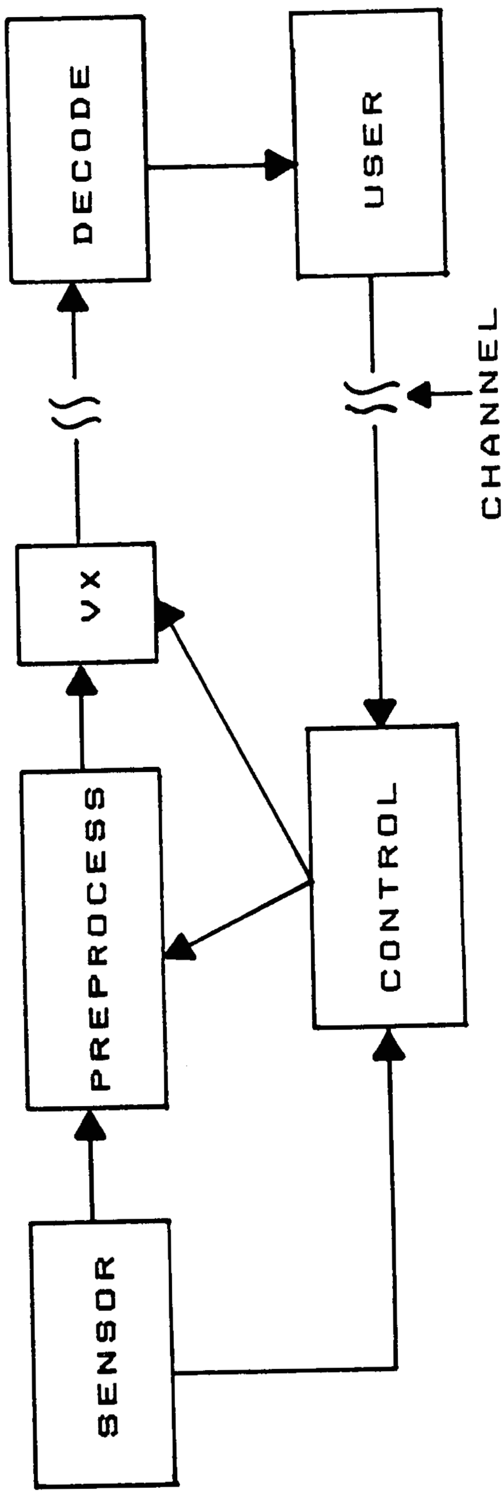
WHAT IS <u>REAL</u>?

D E P E N D S O N U S E R

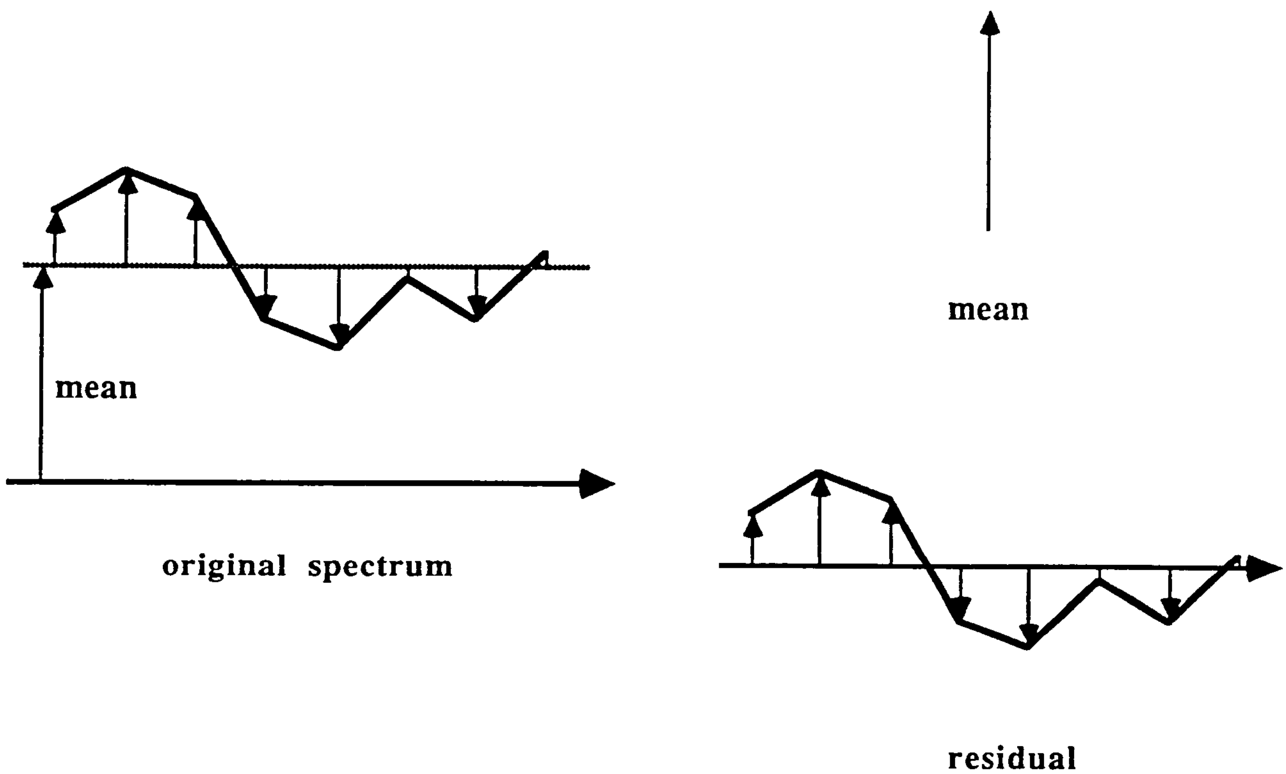
- MEAN SQUARE ERROR
- HAUSDORFF MEASURE
- HUMAN VISION SYSTEM MODELS
- MISSION SCIENTIST MODELS

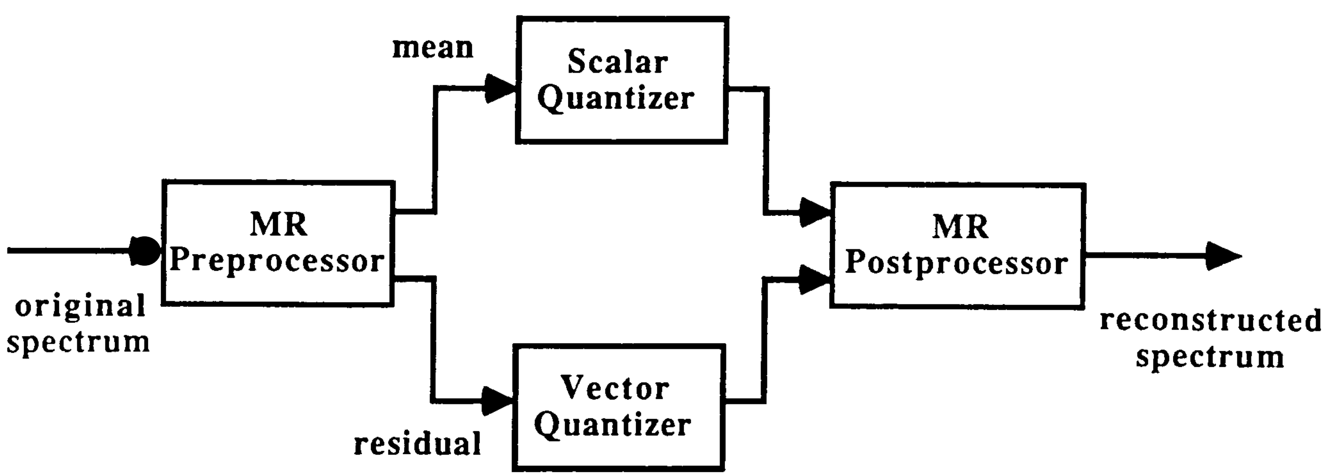

ENCODER
DECODER
X
minimize
d(X, X̂_l)
Channel
Table
Lookup
X̂
Codebook
X̂_l, l=1, ... N_c
Codebook
X̂_l, l=1, ... N_c

Basic VQ


DECODE
USER
CHANNEL
VX
PREPROCESS
CONTROL
SENSOR

Mean-Residual VQ Encoder (MRVQ)





DISTORTION COMPUTATION

Minimize squared error:

$\mathbf{x}$ = Source vector, $\hat{\mathbf{x}}^i$ = ith Code vector,

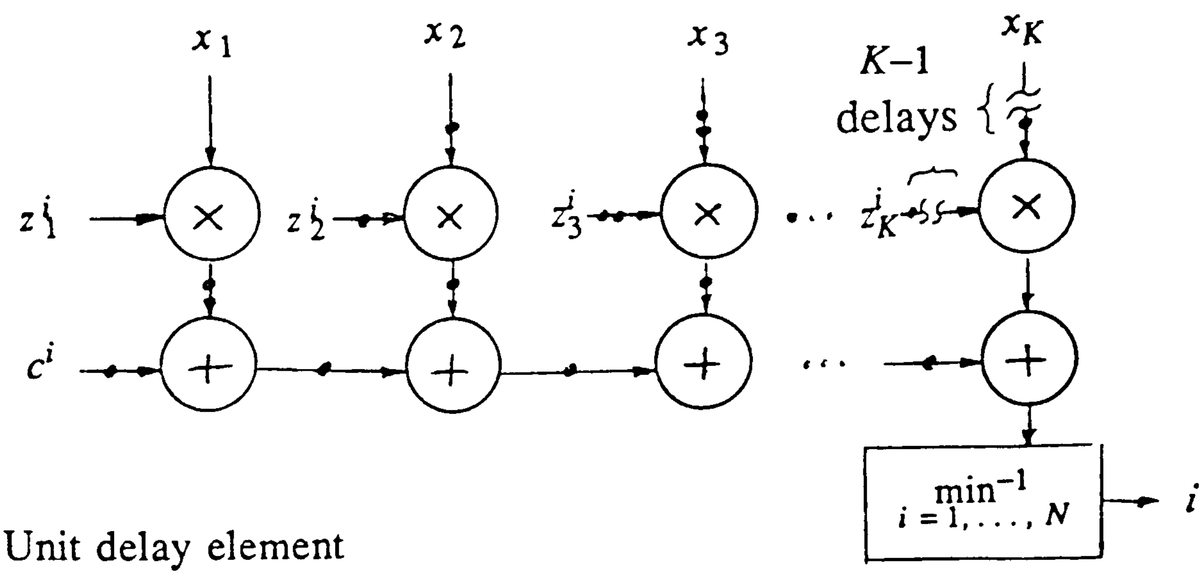
$$i = \min_{i=1,\ldots,N}^{-1} \left\{ \sum_{k=1}^{K} w_k \mid x_k - \hat{x}_k^i \mid^2 \right\},$$

$$= \min_{i=1,\ldots,N}^{-1} \left\{ \sum_{k=1}^{K} \frac{w_k (x_k)^2}{2} - \sum_{k=1}^{K} w_k \hat{x}_k^i x_k + \sum_{k=1}^{K} \frac{w_k (\hat{x}_k^i)^2}{2} \right\},$$

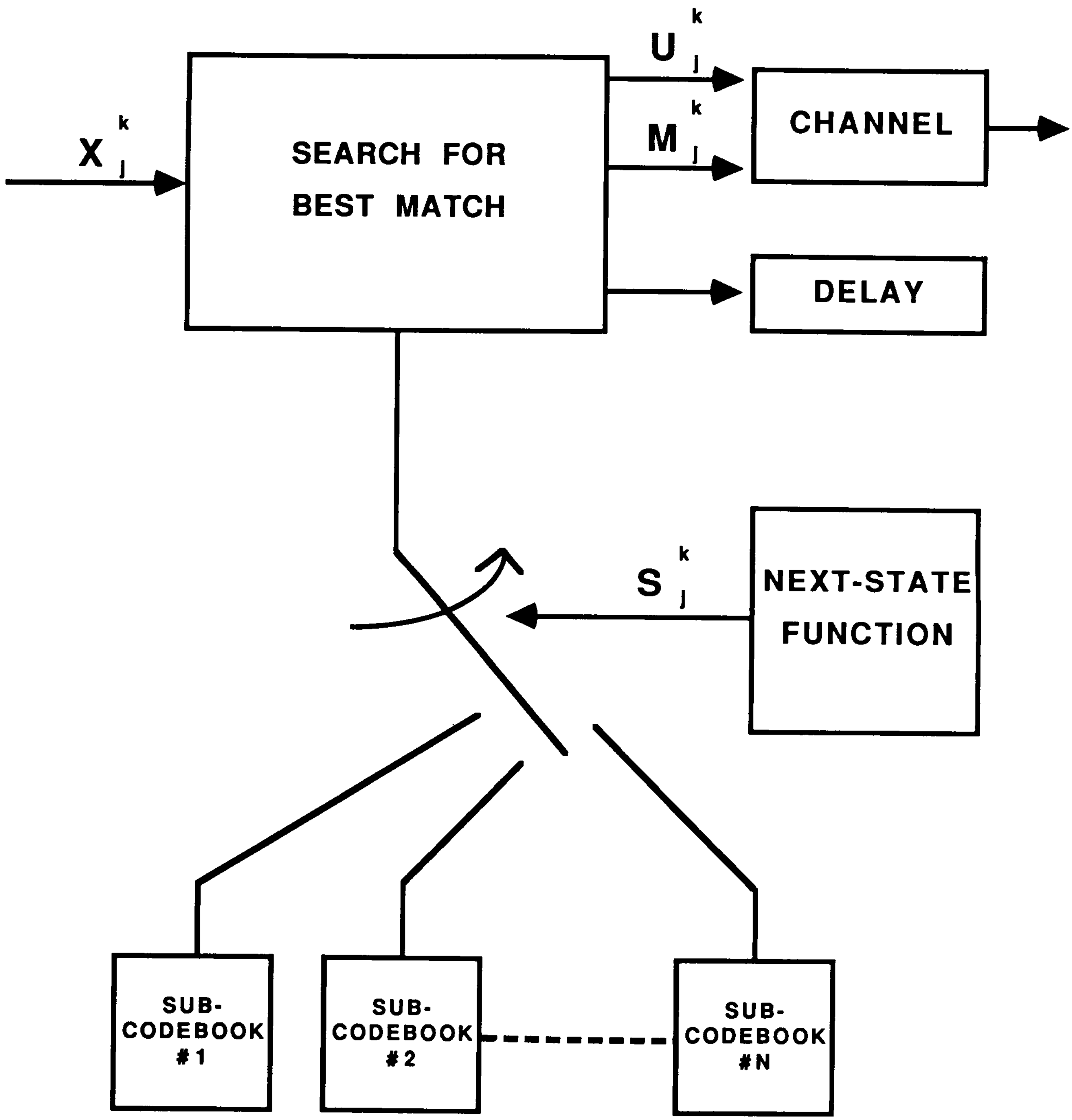
$$= \min_{i=1,\ldots,N}^{-1} \left\{ \sum_{k=1}^{K} z_k^i x_k + c^i \right\},$$

where

$$z_k^i \triangleq - w_k \hat{x}_k^i, \qquad c^i \triangleq \sum_{k=1}^{K} \frac{w_k (\hat{x}_k^i)^2}{2}.$$



• = Unit delay element



Basic Finite-State Vector Quantization Block Diagram.

PROBLEM: LIMITED SEARCH TIME

- Given:
  - 256x256 resolution image
  - 15 frames per second
  - 4x4 block size.

    → 983,040 pixels/sec
    → 61440 4x4 blocks/sec

  or 16.3 microseconds/block

- Assume:
  - Pipeline, 10 MHz clock, 1 distortion/clock

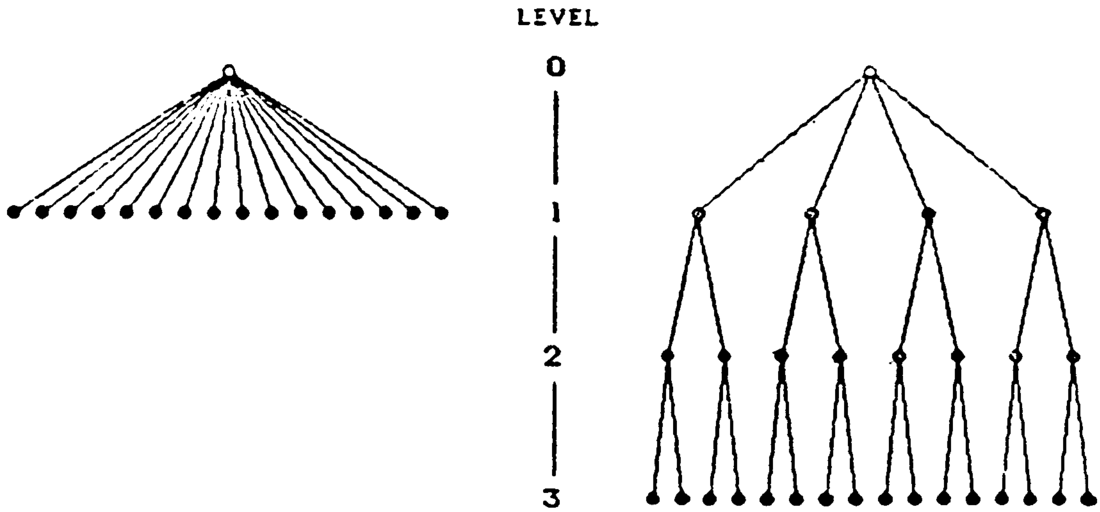
    → 163 distortion computations / block
    → 163 codevectors searched / block

THESE #'S VARY AT RESOLUTION, BLOCKSIZE, RATE, ETC. - BUT:

- Problem:

  → Prefer 4000+ codevectors in codebook
  → Must limit search through codebook

ONE SOLUTION: TREES



N search
N memory

$O(log\ N)$ search
$O(N)$ memory

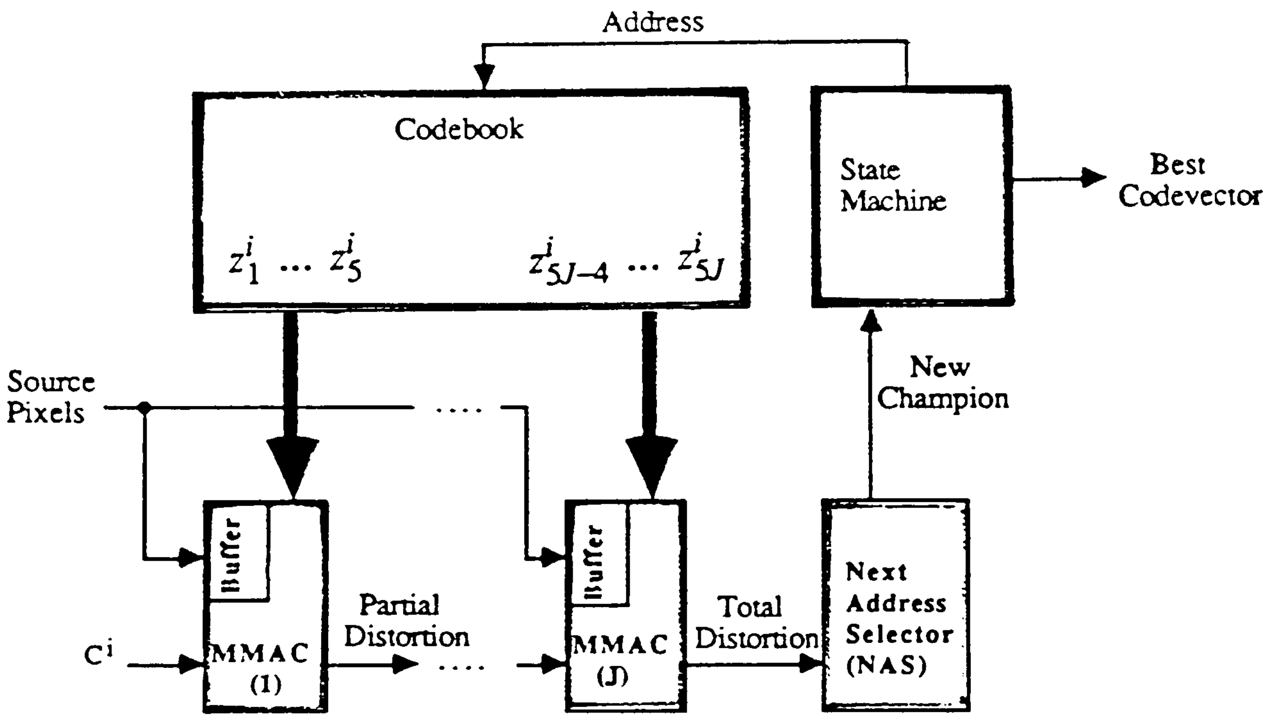
- Example

N = $4096 = 2^{12} = 2^5 \times 2^7$
Search = $2^5 + 2^7 = 160$
Memory = $2^5 + 2^5 \times 2^7 = 32 + 4096 = 4128$

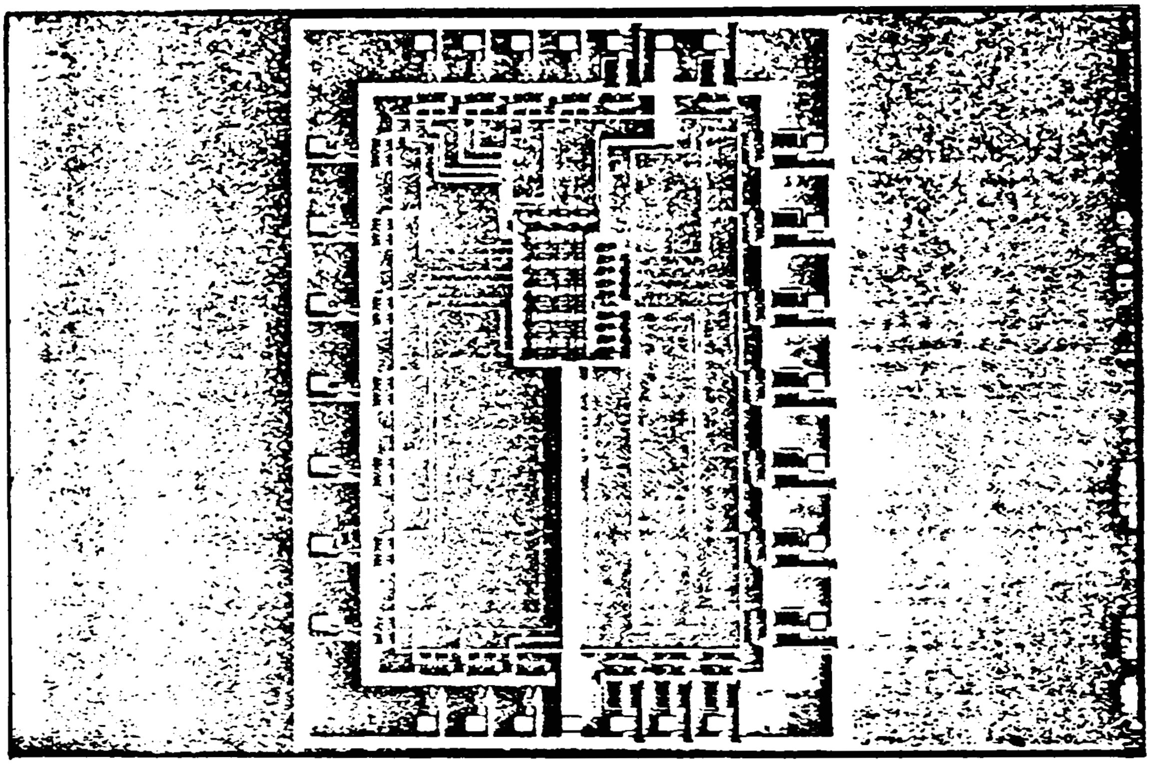
- Problem: data dependency

  - Minimize pipeline latency
  - Buffer to process several source vectors

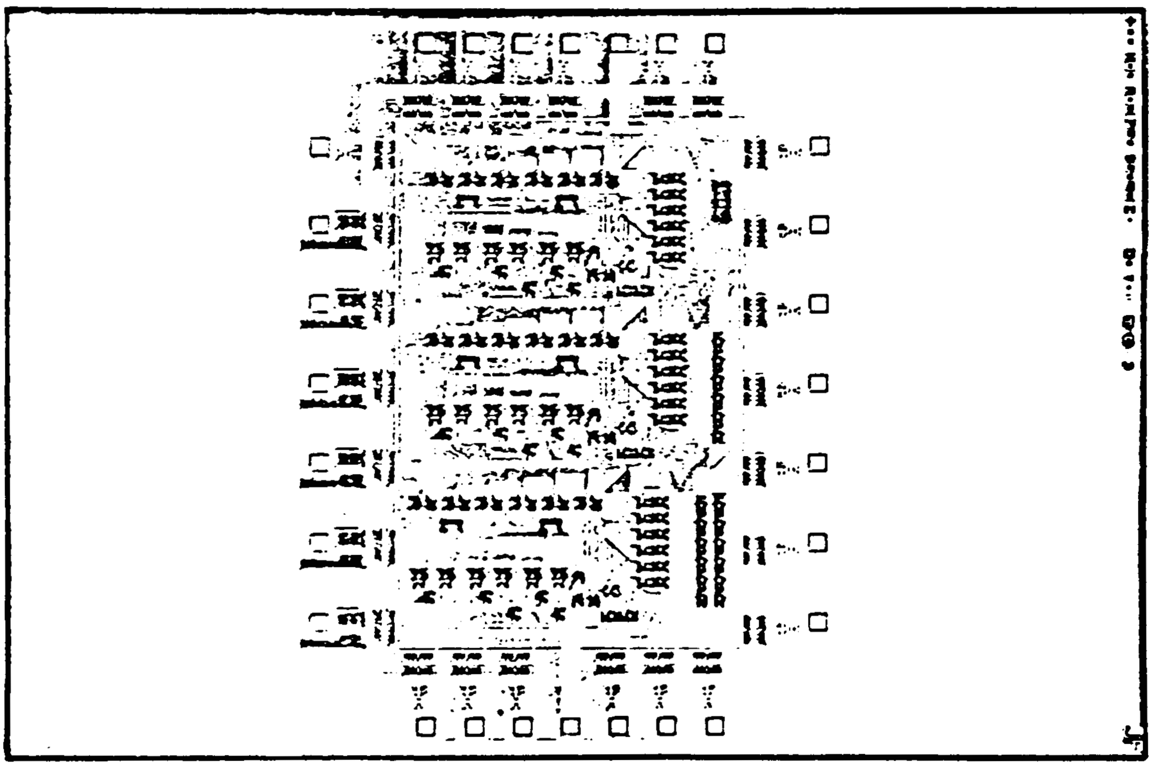
OVERALL SYSTEM



TALLY BLOCK (1/2)



NEXT ADDRESS SELECTOR



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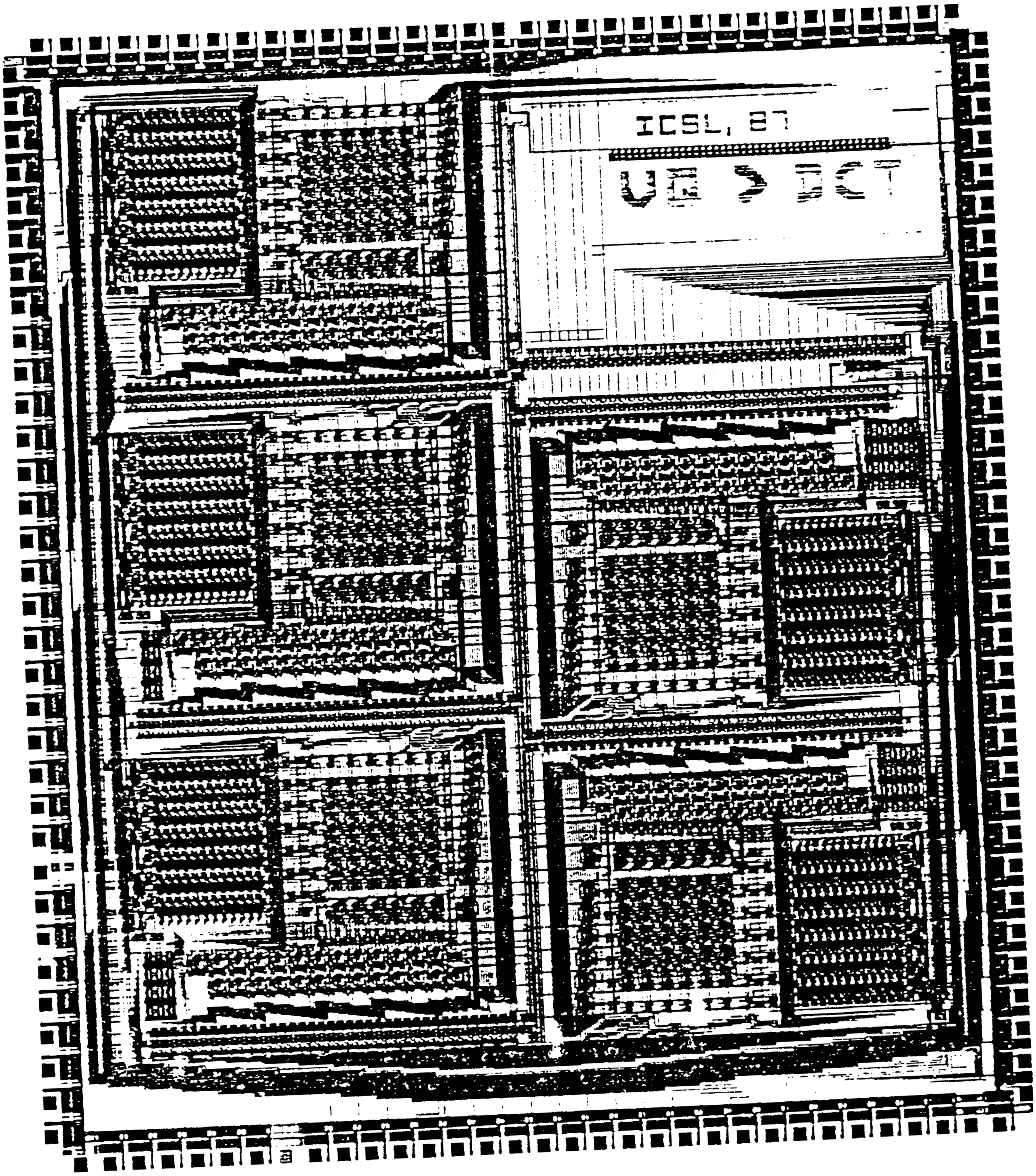

FEATURES

- SEARCH TREE STRUCTURED CODEBOOKS
  - VECTOR DIMENSION UP TO 64 PIXELS
  - CODEBOOK SIZE LIMITED BY MEMORY
  - ONE DISTORTION COMPUTATION PER CLOCK
  - 6 BITS + SIGN
- ARCHITECTURE
  - SYSTOLIC ARRAY
  - ON CHIP BUFFERING
    --> FULL PROCESSOR UTILIZATION
  - CARRY SAVE ADDER AND DYNAMIC MANCHESTER CARRY CHAIN
  - PIPELINED COMPARATOR
- MMAC IMPLEMENTATION
  - 3 MICRON CMOS (MOSIS)
  - 7900 X 9200
  - ABOUT 30000 TRANSISTORS
  - 10 MHz PROJECTED => 10^7 VECTOR DISTORTIONS PER SECOND
  - 132 PINS
- NAS IMPLEMENTATION
  - 3400 X 4600
  - 1376 TRANSISTORS
  - 28 PIN
  - 12 MHz

SUMMARY

- MULTISPECTRAL COMPRESSION ALGORITHMS UNDER STUDY
- WHAT IS RELEVANT?
- HIGH SPEED VX CHIP SET
  - 10 MEGADISTORTIONS/SEC
  - TREE CODEBOOKS (LARGE)
  - INEXPENSIVE TECHNOLOGY