A voltage-mode RF DAC for massive MIMO system-on-chip digital transmitters

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Abstract

As the number of antenna elements increases in massive multiple-input multiple-output-based radios such as fifth generation mobile technology (5G), designing true multi-band base-station transmitter, with efficient physical size, power consumption and cost in emerging cellular frequency bands up to 10 GHz, is becoming a challenge. This demands a hard integration of radio components, particularly the radio's digital application-specific integrated circuits (ASIC) with high performance multi-band data converters. In this work, a novel radio frequency digital-to-analog converter (RF DAC) solution is presented, that is also capable of monolithic integration into today's digital ASIC due to its digital-in-nature architecture. A voltage-mode conversion method is used as output stage, and configurable mixing logic is employed in the data path to create a higher frequency lobe and utilize the output signal in the first or the second Nyquist zone. This 12-bit RF DAC is designed in a 22 nm FDSOI CMOS process, and shows excellent linearity performance for output frequencies up to 10 GHz, with no calibration and no trimming techniques. The achieved linearity performance is able to fulfill the high requirements of 5G base-station transmitters. Extensive Monte-Carlo analysis is performed to demonstrate the performance reliability over mismatch and process variation in the chosen technology.

1 Introduction

Massive multiple-input, multiple-output (MIMO) wireless technology is a key in the fifth-generation (5G) mobile telephony standard to achieve higher information transfer capacity by employing spatial multiplexing and beamforming techniques. Information transfer capacity can be improved by increasing the bandwidth and by increasing the number of parallel data streams via spatial multiplexing and beamforming [9]. The massive MIMO-based 5G standard is exploiting multi-path propagation and spatial multiplexing to send and receive multiple data streams over the same radio channel by beamforming technique and hence increasing the system capacity and spectral efficiency [9].

As the number of antenna elements increases in massive MIMO radios, designing efficient radio base-stations covering multiple bands in existing, unlicensed, or emerging frequency bands up to 10 GHz [6], with efficient size, cost, and power consumption is becoming a challenge. This demands a hard integration of the radio components and specifically the digital ASIC with high-performance data converters. For instance, in downlink, monolithic integration of RF DAC and digital ASIC into "one" digital radio System-On-Chip (SoC) results in reduced power consumption as well as a considerable footprint reduction and thus the size of the radios. To achieve this, high performance data converters to fulfill the wireless infrastructure requirements with very high output bandwidth to cover

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multiple frequency bands, and in the same time, compatible with digital integration are highly demanded.

Figure 1 shows a block diagram of a possible implementation of a transmitter for 5G. There are multiple antenna elements (for instance 64), in order to form highly focused beams. Each branch mainly consists of a digital signal processing (DSP) block, RF DAC, power amplifier (PA) and band filter. Each branch delivers the pre-processed data stream with high power and proper phase difference to each antenna element. Depending on if the beamforming is digital, analog or hybrid, the phase adjustment between the branches are performed in digital, RF chain or both, respectively [23]. In Fig. 1(a), digital beamforming architecture is assumed which requires the same number of RF DACs as the number of antenna elements. In each branch, the baseband in-phase (I) and quadrature-phase (Q) data are fed to digital up-conversion block (DUC) where the data is interpolated and up-sampled to the RF DAC update rate, and also digital IQ modulation is performed. The numerically controlled oscillator (NCO) provides 0° and 90° shifted phase LO to the digital IQ modulator. There are advantages with digital IQ modulation, comparing to analog IQ modulation, such as, IQ imbalance can be digitally canceled and there is no LO feedthrough that falls into the carrier bandwidth. The real-valued digital signal is then fed to the RF DAC to be represented by an analog signal. The RF DAC directly synthesizes the signal in the desired RF frequency and there is no need for another frequency translation step. The sample frequency is provided by a high-performance phase-locked loop (PLL) to the RF DAC. If the RF DAC is used in mixing mode configuration, the LO frequency does not have to be higher than the output RF signal, which is a big advantage for this method, would otherwise require more than double the output frequency in conventional Nyquist DACs.

The rest of this paper is formatted as follows: In Sect. 2, digital transmitters employing RF DACs in literature are reviewed, in Sect. 3, the proposed RF DAC-based digital transmitter is described. Details of circuit implementation and simulation analysis and impact of non-idealities such as device mismatch induced errors are analyzed and presented in Sect. 4, and concluding remarks in Sect. 5.

2 Digital transmitter

In conventional analog transmitters with one to four antennas (as in 3G and 4G), a high performance DAC, in terms of linearity and noise spectral density, and an analog IQ modulator have been used. The DAC often is operating in the first Nyquist zone and the DAC output signal is in the sub-GHz range. The IQ modulator translates the analog signal to the desired RF band. As the number of antenna elements grows, for instance in LTE-A, to up to eight elements per radio, the integration of the baseband DAC and analog IQ modulator was more efficient in terms of overall radio size and cost [13, 14, 21]. In massive MIMO however, the number of antenna elements increases dramatically, and a digital transmitter with an RF DAC solution is more beneficial as there is no analog mixer limitation and therefore simultaneous multi-band operation becomes easier. In a digital transmitter with digital IQ modulator, the RF DAC converts digital data directly to RF signal which goes to the power amplifier (PA) and the antenna, simplifying the overall radio design and results in smaller area and cost. If in a radio system, the digital ASIC and the digital transmitter (including digital IQ modulator and the RF DAC) are implemented in separate chipsets, multigiga-bit serial data link (such as JESD204B) between the digital ASIC and the digital transmitter, requires a huge power consumption, both in the digital ASIC as the sender of high-speed serial data and the RF DAC as the receiver. If the RF DAC is integrated into digital ASIC (on the same die), it will be possible to save power and area by eliminating the serial link transceivers. The RF DAC can potentially fit in the same area as of the high-speed serial data link sender in digital ASIC, which implies no additional area is needed for monolithic integration of the RF DAC in digital ASIC [5].
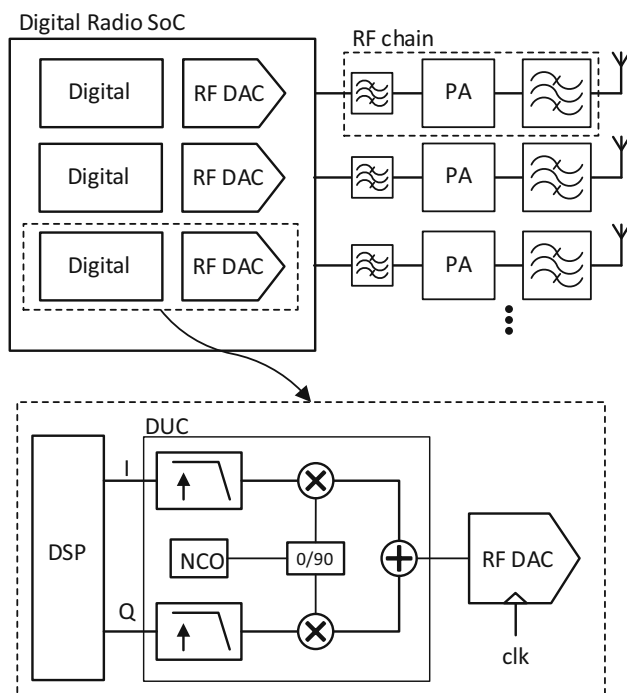
Fig. 1 Block diagram representation of a massive MIMO-based transmitter with monolithic integration of data converters into the digital Radio System-On-Chip

2.1 RF-sampling DACs

RF DAC or RF-sampling DAC, in this context, refers to DACs for which the sample rate is high and the DAC output is in RF domain [2, 3, 15, 18]. Depending on the architecture and implementation choices, the RF DAC can utilize first, second or even higher Nyquist zones to synthesize the signal at the desired RF frequency. In a zero-order hold RF DAC, the analog signal is reconstructed by means of pulse-amplitude modulation (PAM) of the digital input data using a rectangular pulse with duration of sampling period $T_s = 1/f_s$, and the frequency response is a *sinc*-weighted function with zeros at multiples of the sample frequency f_s. The sample rate in this case must be very high, for instance, more than 20 GHz to cover up to 10 GHz RF output within the first Nyquist zone. Higher Nyquist images of the DAC in this structure will have 10 to 20 dB less power and hence degraded dynamic range and dynamic linearity.

In mixing RF DACs, however, the PAM signal can be an oscillating pulse, for which the amplitude is modulated with the level of the input digital code which gives rise to the higher Nyquist images energy. The frequency response of the RF DAC will have high energy lobe at f_s or a multiple of f_s depending on the oscillating pulse duration. The higher Nyquist images of the digital data at f_s (or a multiple of f_s), will be the RF output signal of the RF DAC [5, 7, 12, 19].

3 Proposed RF DAC-based digital transmitter

In this work, a 12-bit resolution RF DAC solution for a digital radio transmitter is presented. The digital data is processed in the digital blocks and the sample rate is increased to the update rate of the RF DAC.

In general two approaches exist for implementing a mixing RF DAC depending on how the mixing operation in each cell of the DAC is performed, as discussed in [19]: at the data path as "mixing logic" or modulating the tail current as "series mixing" and therefore various oscillating PAM signals have been used for RF DAC implementation such as continues sinusoidal [7, 12], discrete oscillating PAM [20], or a bipolar rectangular [5, 19]. To implement the RF DAC in a process that is compatible with co-integration by digital ASIC, mixing logic approach is preferred due to the voltage headroom limitations and also the "digital-in-nature" characteristic of this method, so that the RF DAC actually benefits from process scaling.

3.1 RF DAC architecture

A top-level functional block diagram of the proposed RF DAC is shown in Fig. 2 which contains digital processing block for segmentation and decoding and a number of weighted unit conversion cells that are driven by the decoded input bits. Each conversion cell is constructed of data capturing and mixing logic, and voltage-mode conversion block. The positive and negative output of all conversion cells are combined and terminated in a transformer with differential 100 Ω load. The transformer at the load will help isolating the output voltage swing from the internal RF DAC nodes, as well as impedance matching if required. It will also help for common-mode isolation and required voltage headroom. There is a trade-off here between selecting on-chip or off-chip transformer. An off-chip transformer requires a large footprint and bond wire inductance can be challenging at higher frequencies. An on-chip transformer comes at the cost of larger chip area and larger power dissipation for the RF DAC output stage.

To implement the mixing logic function, the PAM signal is selected to be a bipolar pulse toggling between amplitudes $+A$ and $-A$ (Fig. 3b), where A is the level corresponding to the input digital code. This PAM signal can be generated by applying an exclusive NOR logic gate (XNOR) to the clock and the input bit as shown in Fig. 3(a and b).

## 3.2 RF DAC output stage in voltage-mode

Traditionally, current-steering DACs have been the choice for high speed application mainly because of the driving capability of the current sources in high speed operation and to avoid having buffer at the output stage of the DAC. Switching time variation which is input code-dependent is one source of non-linearity. Another one, which is the main limitations of dynamic performance in current steering DACs, is the finite output impedance of the unit current cell. This makes the DAC output impedance input code-dependent, and causes non-linearity [10, 16]. There are some techniques to overcome this limitation to some extent, for instance, by using bleeding current sources [5, 10], still the achievable linearity for sub-10 GHz operation is very limited.

In the proposed RF DAC solution, Voltage-mode (VM) conversion is used as the output stage of the RF DAC, as shown in Fig. 2 and each data bit, after passing through the mixing logic, is applied to the switches d and d_N. These switches are implemented by means of an inverter connecting the positive and negative terminals of the output to either V_{ref+} or V_{ref-} through the unit element resistors (R_u). Due to high speed switching capability of the CMOS

Fig. 2 Top-level functional block diagram of the proposed RF DAC for a digital RF transmitter with an off-chip Balun
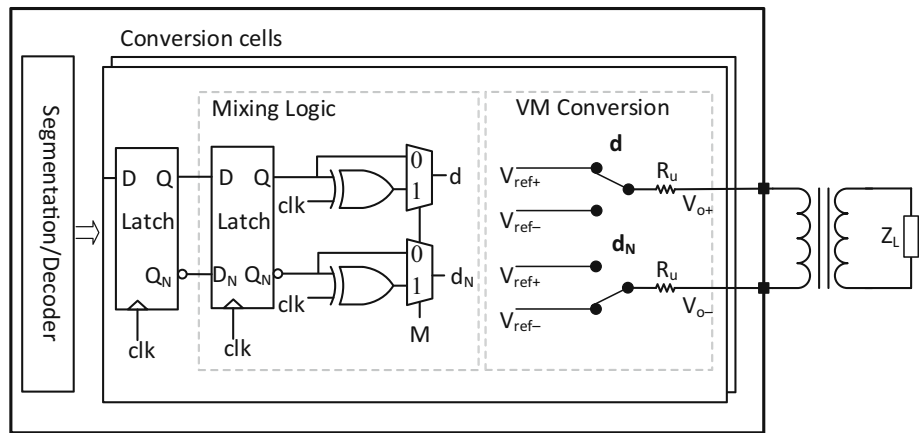
Fig. 3 **a** Mixing logic operation by XNOR-gating the input bit and the clock, **b** bipolar pulse amplitude modulation (PAM) to generate the RF DAC frequency response, and **c** simplified equivalent circuit at each clock phase
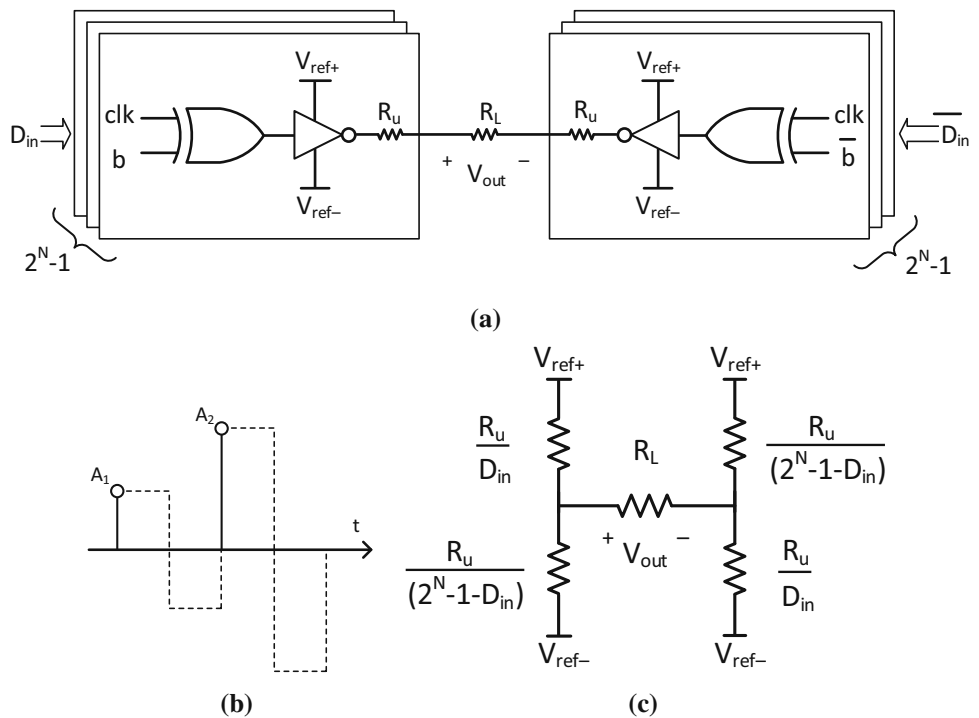
transistor in this technology, very high speed RF DAC operation will be possible. This switching speed will benefit from process scaling and will become even faster in advanced nodes.

3.2.1 Transfer function

The voltage-mode conversion and mixing logic is shown in Fig. 3(a). At each clock phase the output stage will become a resistor network as shown in Fig. 3(c), and the steady-state transfer function, output voltage versus input code, can be calculated investigating the half-differential Thevenin equivalent as:

$$V_{th} = \frac{D_{in}}{2^N - 1} \cdot \left(V_{ref+} - V_{ref-} \right),$$
$$R_{th} = \frac{R_u}{2^N - 1}. \tag{1}$$

The differential output voltage is then derived as

$$V_{out} = \frac{2D_{in} - (2^N - 1)}{(2^N - 1) + 2R_u/R_L} \cdot \left(V_{ref+} - V_{ref-} \right), \tag{2}$$

where D_{in}, is the input code, R_L is differential load virtually seen by the RF DAC output and R_u is the unit element resistor. In this architecture, the impedance seen from the output of the RF DAC, is always constant regardless of what input code is applied. That is, all the R_u resistors are either connected to positive or negative reference voltage

and hence the total output impedance is always constant and it does not contribute to the linearity degradation. This can be also observed from (2) where the output voltage is a linear function of the input code and there is no code-dependent load variation which was a limiting factor in current steering DACs.

However, switching time variation will still impact the non-linearity performance. The "on" resistance of the switches is negligible comparing to the individual unit element resistors in series ($R_u = 10$ kΩ), and therefore is ignored in (2) for simplicity. Unit element resistors are implemented in N+ Polysilicon material in this 22 nm FDSOI CMOS process. Each R_u has a width of 360 nm and a length of 7.6 μm and resistance of 10 kΩ. If resistance value of R_u is too small, and once all in parallel, comparable to the "on" resistance of PMOS and NMOS switches, there will be code-dependent load variations due to the differences of PMOS and NMOS transistor "on" resistance. The optimum unit element resistor is found by sweeping its value and the simulation shows that smaller values cause more non-linearity and larger values limit the achievable speed due to more parasitic capacitors and hence $R_u = 10$ kΩ seems to be a good compromise. The overall RF DAC core area is dominated by the unit element resistors. In 12 bit RF DAC, there are 4095 unit elements and each R_u has an area of 2.74 μm^2, in total becomes 0.00112 mm^2. Although this is only the area needed for resistors and not the complete design, it gives a good approximation of the required area and indicates that the proposed RF DAC area is very competitive, when compared to the state of the art RF DACs [5, 13, 14]. The NMOS and PMOS switches in each unit element are minimum sized (W = 300 nm, L = 20 nm) with m-factor of five (transistors M_{1-4} in Fig. 5).

3.2.2 Unit Element Resistors Mismatch and RF DAC Segmentation Scheme

Process and mismatch variation within RF DAC cells will cause errors in timing and amplitude accuracy in multi-bit RF DAC [11]. The unit element mismatch error can be modeled as an additive random variable, where the additive random variable's standard deviation depends on the desired value. According to Pelgrom's model [8, 17], the standard deviation of mismatch is inversely proportional to the area and hence more resistors in parallel decreases the mismatch.

In order to characterize the resistor mismatch behavior in the selected process, 22 nm FDSOI CMOS, a single nominal 10 kΩ Poly resistor with size of W = 0.36 μm and L = 7.6 μm is simulated with 1000 Monte-Carlo samples and the simulated resistance value is observed. As

discussed before, the unit element resistor value is selected as $R_u = 10$ kΩ given the trade-off between the output switching speed due to parasitic capacitance and being sufficiently large value compared to the "on" resistance of the switches.

The simulation is run in three different mode, first only mismatch, second only process and third with both mismatch and process variation and the one-sigma standard deviation values and mean values are listed in Table 1, where ϵ is a random error that represents the fluctuation around the nominal value of the resistor in Ω, and μ is mean value in Ω and σ is standard deviation of the resistor in percentage relative to the mean value.

In this work, the unit element conversion cells are weighted according to the segmented bits as shown in Fig. 4. The first six LSBs (L = 6) are fed to binary weighted unit element conversion cells, and the remaining MSBs (M = 6) are decoded into 63 unary bits, and corresponding cells are weighted as $2^L = 64$.

The same Monte-Carlo simulation is also run for the MSB, i.e., 64 resistors of 10 kΩ in parallel, and the result is shown in Table 2.

As expected from Pelgrom's model [8, 17], the mismatch variation (within die) is scaled with the square root of area, i.e., 64 parallel resistors have 64 times more area and hence the corresponding sigma is 8 times smaller ($0.16\% = 1.24\%/\sqrt{64}$), while the process variation (die-to-die) does not scale with area. With this segmentation scheme (M = 6, L = 6) the largest error which is on the LSB R_u (124 Ω) will be less than nominal value of the MSBs (156.25 Ω).

Although for the dynamic performance it is the mismatch variation only which is important, to ensure that it covers the worse cases, the simulations in the following sections are run with both mismatch and process variation indicating that the simulation result is conservative.

4 Implementation and simulation analysis

The proposed RF DAC solution is implemented in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and simulated with the spectre simulator engine. The transistor-level schematic diagram of a unit conversion

Table 1 One unit element resistor R_u with nominal value of 10 kΩ

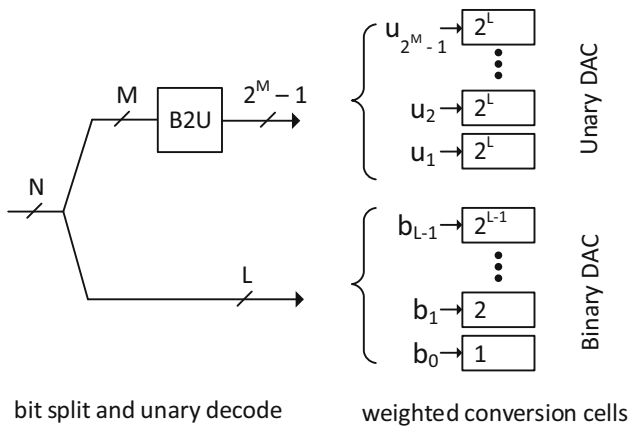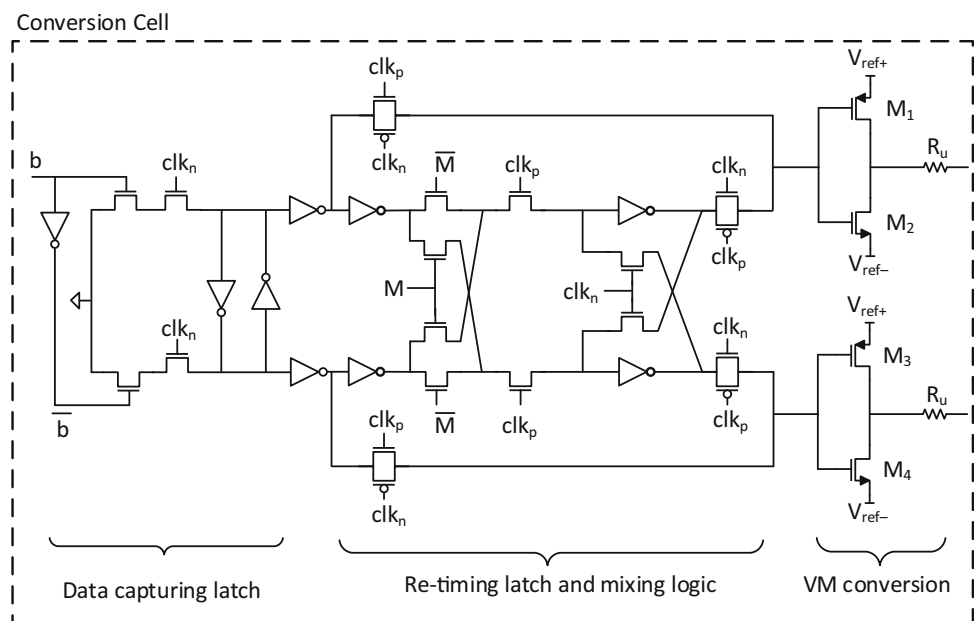|	Mismatch	Process	Mismatch and process
ϵ, Ω	124.1	699.1	665
μ, kΩ	10.01	10.03	10.03
σ, %	1.24	6.97	6.6

Fig. 4 Segmentation scheme and unit conversion cells weighting

Table 2 64 unit element resistors R_u in parallel with nominal value of $10k/64 = 156\Omega$

	Mismatch	Process	Mismatch and process
ϵ, Ω	0.249	10.92	10.38
μ, Ω	156.3	156.7	156.7
σ, %	0.16	6.97	6.6

cell, consisting of data capturing latch, re-timing latch and mixing logic, and voltage-mode conversion stage, is shown in Fig. 5. Signal b is the input bit to each cell using a differential clock signal clk_p and clk_n with 5-ps rise- and fall times. Signal M is selecting mixing or base-band mode

operation of the RF DAC. V_{ref+} and V_{ref-}, are the reference voltages to the output stage. V_{ref-} is 0 V and connected to ground and V_{ref+} is supplied from a 0.8 V stable power supply with minimum disturbances and large decoupling capacitors.

4.1 Impact of mismatch on performance

Process and mismatch variation will cause errors in timing and amplitude accuracy of the RF DAC and can degrade the performance. Amplitude error is dominated by the unit element resistors mismatch. To mitigate the mismatch error, potentially, a dynamic element matching (DEM) scheme can be adopted to average out the spurious, with the penalty on the increased noise floor due to randomization. The skew variation between different clocking routes to RF DAC unit elements are caused by the device mismatch and can also be averaged-out by randomization. The timing jitter (clock phase noise), however, changes stochastically at every sampling edge and for all unit elements, and is not mitigated by randomization technique. The simulation result in this work is without the use of dynamic element matching since the noise spectral density (NSD) requirement of the RF DAC in 5G base-station application is very tough and any increase in the noise level is undesired. It should also be mentioned that the RF DAC noise specification is affected by the PLL phase noise.

In order to analyze the impact of mismatch on linearity performance, extensive Monte-Carlo simulation is performed on the proposed RFDAC circuit and the result is presented in Sect. 4.4.

Fig. 5 Complete transistor-level schematic diagram of one conversion unit element cell, including the latches, mixing logic and voltage-mode (VM) conversion

4.2 Impact of resistor thermal noise

There are $2^N - 1$ resistors in parallel at each clock phase, connected to the reference voltages. The uncorrelated noise power is added from each resistor and the total noise power will be

$$\overline{I_{n,tot}^2} = \overline{I_{n,1}^2} + \overline{I_{n,2}^2} + \cdots = \frac{4kT}{\left(\frac{R_u}{2^N-1}\right)}, \tag{3}$$

$$\overline{V_{n,tot}^2} = \overline{I_{n,tot}^2} \left(\frac{R_u}{2^N-1}\right)^2 = 4kT\left(\frac{R_u}{2^N-1}\right), \tag{4}$$

which implies that the thermal noise power of all resistors in parallel, is divided by the total number of unit elements and will be $2^N - 1$ times smaller than single R_u.

4.3 Simulation setup

Simulation results confirms the discussion on linearity performance in the previous sections. A test case with a 10 GHz clock frequency (f_s) and RF_{out} up to 10 GHz, is set up and simulated. Differential load of 100 Ω, with 300 fF capacitive load, is used. In a complete system, the digital input base-band frequency is translated to the desired RF frequency, from DC to Nyquist frequency ($f_s/2$), by means of digital up-converter (DUC). Since implementing the NCO and DUC, is out of scope of this work, the input signal to the RF DAC is directly generated with proper frequency in the simulator. For RF signals within first Nyquist zone, the base-band mode of operation of the RF DAC is selected and for RF signals at second Nyquist zone, the RF DAC is configured to operate in mixing mode to get higher power level from the output signal.

4.4 Monte-Carlo analysis

As discussed before mismatch and process variation will impact the RF DAC performance. Particularly unit element resistors mismatch will result in degraded linearity performance. In order to analyze the unit element resistors mismatch impact, 100-point Monte-Carlo simulation is run and Fast Fourier transform (FFT) is performed on the output transient signal for each Monte-Carlo run. Third and fifth order intermodulation distortions (IM3 and IM5) are measured by two-tone test, each tone at −6 dBFS, and 15 MHz frequency spacing between tones. Figure 6 shows the worse-case IM3 and average IM3 performance and total output RF power in six different output frequencies. The worse-case IM3 better than 70 dBc for f_{out} up to 10 GHz is achieved with output RF power > 0 dBm. The IM3 and IM5 distribution of 100 Monte-Carlo simulation points is shown in Fig. 7 for three different output frequencies. The output spectrum for worse-case mismatch
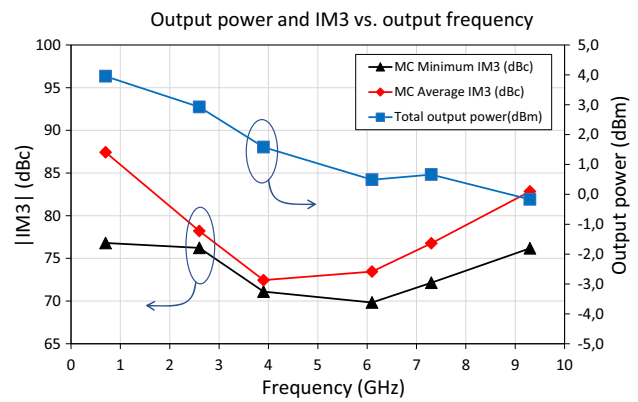

Fig. 6 P_{out} and IM3 performance in 100 Monte-Carlo points, for output signals from DC to f_s. The sample frequency is at 10 Gsps

corner, at 9.3 GHz output RF frequency is shown in Fig. 8 and demonstrates IM3 of 76 dBc while maintains excellent spurious free dynamic range (SFDR) in the Nyquist bandwidth of 5 GHz.

## 4.5 Parasitic capacitance of routing unit elements

To avoid the asymmetry between unit elements caused by the layout effects, the routing strategy should be selected in layout such that the parasitic capacitance of the metal wires connecting the unit elements to the differential output terminals are as similar as possible. One approach to keep the symmetry is to select a tree structure for output routing [22].

To consider this parasitics impact in our analysis, an experiment is done in which extra capacitance instances are added in the schematic of each cell, after each unit element resistor to account for the routing parasitic capacitance. This parasitic capacitance is swept up to 20 fF and the circuit is simulated in one of the worse Monte Carlo corners (f_{out}= 2.6 GHz) to observe the effect. One should note that 20 fF at each cell for parasitic capacitance is a very conservative choice and the parasitics are typically smaller than this value. In the worse case, IM3 is degraded with approximately 2 dB considering the parasitic capacitance of 20 fF. As expected going from schematic to layout the performance will be changed, however as simulations show, this performance degradation is within the expected range.

5 Comparison and conclusion

An RF DAC solution with capability to be monotonically integrated into digital system-on-chip, and complying with the area and power consumption constrains of massive

Fig. 7 IM3 and IM5 distribution of 100 Monte-Carlo points, for three different f_{out}: 2.6, 6.1 and 9.3 GHz. The sample frequency is at 10 Gsps
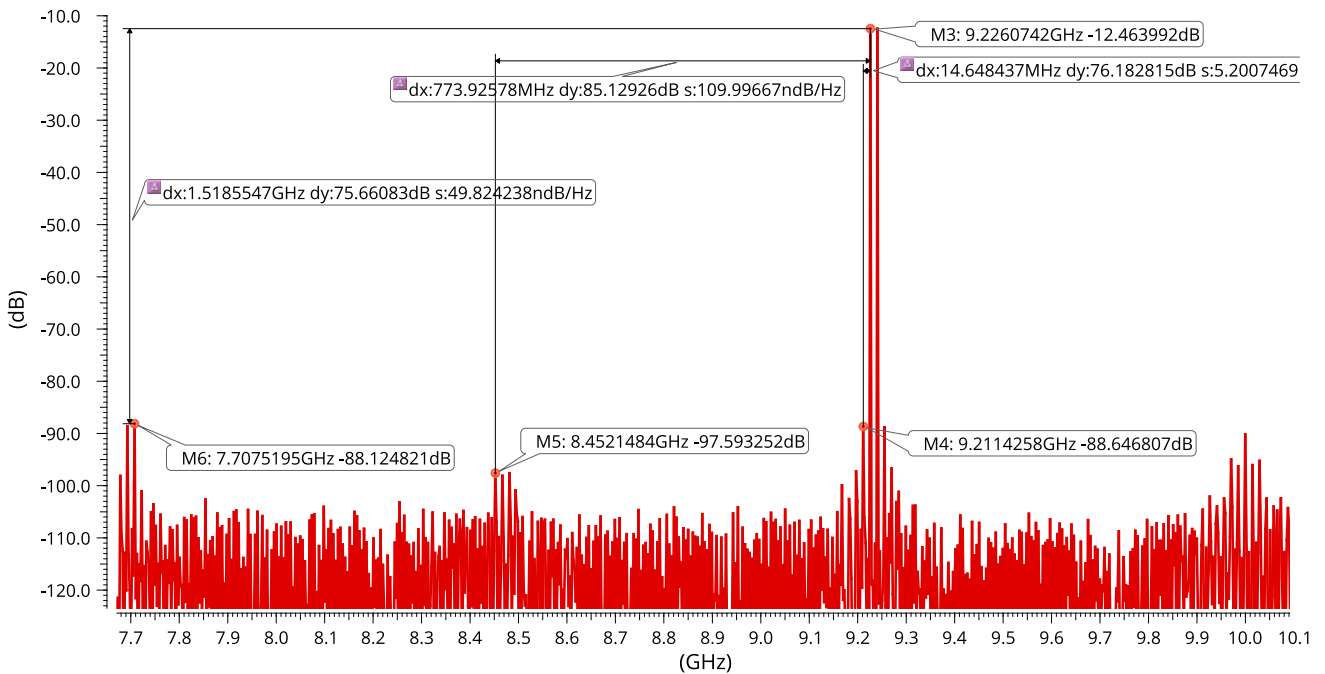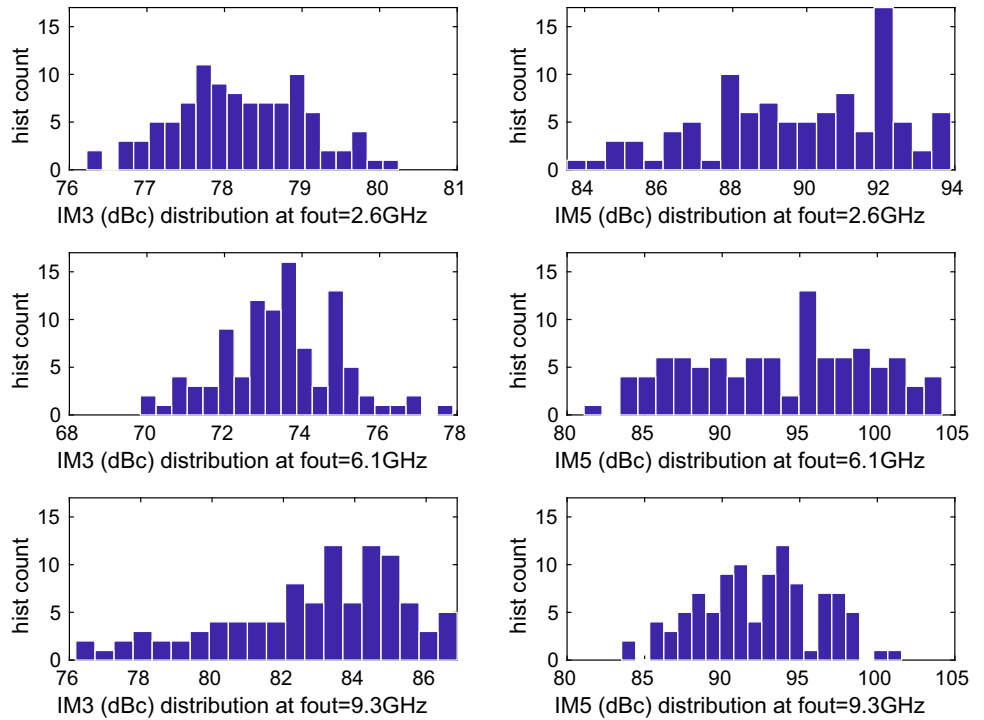
Fig. 8 Two-tone test spectrum for the worst-case mismatch corner at $f_{out} = 9.3$ GHz, demonstrating an IM3 of > 76 dBc. The sample frequency is at 10 GSps. Folded second and third harmonic distortion components are also marked in the plot and shows > 75 dBc SFDR within the Nyquist band

MIMO-based 5G transmitters in cellular communication, is described in this paper. A proof-of-concept of this architecture were designed and implemented by a 12-bit segmented RF DAC.

The impact of the major circuit imperfections is studied analytically in this work and it is shown in principle with the aid of extensive Monte-Carlo simulations, that in worse-case corners, the performance is still able to fulfill the upcoming 5G standard requirements. Since the

proposed RF DAC is very compact in size, it can replace high-speed serial data link block in a digital ASIC meaning that basically the monolithic integration of the RF DAC comes with no die-area increase for the digital ASIC in fully digital beamforming 5G architectures.

The proposed work is compared against some of the recent state-of-the-art RF DACs [1, 4, 11]. These RF DACs are implemented in current-steering architecture. There are non-idealities associated with the current source implementation as well. Finite output impedance of the unit element current sources causes harmonic distortion and mismatch between the unit element current sources causes timing and amplitude inaccuracy and hence harmonic distortion. To mitigate the finite output impedance of current-steering architecture, works in [1, 4, 11] utilize the bleeding current source technique proposed in [10], making the output impedance of the DAC independent of the input code. Moreover in a current-steering structure the mismatch can happen between unit current sources and also between the switches. The former causes amplitude error and the latter will cause timing error between the samples. These errors appear as spurious emission in spectrum of the DAC and hence limiting the dynamic linearity. The work in [11] utilizes calibration technique to mitigate the amplitude errors and utilizes Dynamic Element Matching (DEM) technique to mitigate the timing errors. In this way the randomization via DEM technique alleviates spurious problem without increasing the noise spectral density.

Using the aforementioned techniques, the work in [11] achieves IM3 better than 70 dBc up to 4.5 GHz output frequency and the work in [4] achieved IM3 better than 65 dBc up to 6.8 GHz output frequency, both in 16 nm CMOS technology. The proposed solution in this work has shown in simulations to be able to achieve better than 70 dBc IM3 in output frequencies up to 10 GHz in 22 nm CMOS technology without any calibration, trimming or compensation method.

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