A VOLTAGE SAG SUPPORTER UTILIZING A PWM-SWITCHED AUTOTRANSFORMER

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To My Parents,

My Loving Wife, Joo-Youn,

And My Daughters, Do-Young and Do-Yun.

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SUMMARY

The objective of this research is to develop a novel voltage control scheme that can compensate for voltage sag and swell conditions in three-phase power systems. Faults occurring in power distribution systems or facilities in plants cause the voltage sag or swell. If a fault occurs, it can damage the power system or user's facility. Sensitivity to voltage sags and swells varies within different applications. For sensitive loads, even voltage sags of short duration can cause serious problems in the entire system. Normally, a voltage interruption triggers a protection device, which causes shutdown of the entire system.

In order to mitigate power interruptions, this research proposes a scheme called "Voltage Sag Supporter utilizing a PWM (Pulse Width Modulation) - Switched Autotransformer." The proposed scheme is able to quickly recognize the voltage sag or swell condition, and it can correct the voltage by either boosting the input voltage during voltage sag events or reducing the input voltage during voltage swell events. Among existing methods, the scheme based on the inverter system such as dynamic voltage restorers (DVR) require an inverter, a rectifier, and a step-up down transformer, which makes the system expensive. AC converters can be used for the purpose of the research. However, they consist of two solid-state switches per one phase and include energy storage devices such as reactors and capacitors.

The switching device for the high voltage application is relatively expensive so that this research suggests a scheme utilizing only one switch for the output voltage control,

which makes the system more stable and cost effective. The proposed scheme can be applied at any voltage and provides cost and size advantages over existing methods due to the reduced number of switching components and no need of energy storage devices. This research includes many design issues such as a voltage controller, a voltage detection, snubber design, and a commutation logic for thyristors. Fast fault detection is essential for the high voltage application so that fault detection logics for each switch device are devised and implemented either in hardware or software based logic. Simulations and experiments have been carried out to verify the validity of the proposed scheme, and prototype experiments are being done to confirm the control scheme.

CHAPTER 1

INTRODUCTION

1.1 Background

A power distribution system is similar to a vast network of rivers. It is important to remove any system faults so that the rest of the power distribution service is not interrupted or damaged. When a fault occurs somewhere in a power distribution system, the voltage is affected throughout the power system. Among various power quality problems, the majority of events are associated with either a voltage sag or a voltage swell, and they often cause serious power interruptions.

A voltage sag condition implies that the voltage on one or more phases drops below the specified tolerance for a short period of time. A voltage swell condition occurs when the voltage of one or more phases rises above the specified tolerance for a short period of time. The causes of voltage sags and swells are associated with faults within the power distribution system. Users located a close distance to the fault experience voltage sags much greater in magnitude and duration than users located farther away, and as the electrical system recovers after removing the fault, voltage swells are produced throughout the system for short periods of time. Often all users who are served by the

power distribution system have power interruptions during a fault because of the effects of a voltage sag or voltage swell produced in the system by the fault. The objective of this research is to develop a novel voltage control scheme that can compensate for voltage sag and swell conditions in three-phase power systems.

Power systems supply power for a wide variety of different user applications, and sensitivity to voltage sags and swells varies widely for different applications. Some applications such as automated manufacturing processes are more sensitive to voltage sags and swells than other applications. For sensitive loads, even a voltage sag of short duration can cause serious problems in the manufacturing process. Normally, a voltage interruption triggers a protection device, which causes the entire branch of the system to shut down.

1.2 Problem Statement

In order to increase the reliability of a power distribution system, many methods of solving power quality problems have been suggested. The development and improvement of power switching devices capable of carrying large current with high voltage enable power electronics technologies to be applied to this area. In addition, self-commutable devices, i.e., gate turn-off device such as GTOs and high power IGBTs, give rise to a variety of schemes to mitigate power quality problems.

Much research has been performed in an effort to solve power quality problems. Many voltage mitigation schemes are based on inverter systems consisting of energy

storage and power switches. Large energy storage is required when it is necessary to supply real power, which makes these systems expensive.

The main goal of this research is the development of a voltage sag mitigation scheme with high reliability at low cost. This research proposes a scheme called "Voltage Sag Supporter utilizing a PWM - Switched Autotransformer." The proposed scheme is able to quickly recognize the voltage sag and swell conditions and can correct the voltage by either boosting the input voltage during voltage sag events or reducing the input voltage during voltage swell events.

Any power electronic switch in for high voltage applications is expensive, and the peripheral circuits such as gate drivers and power supplies are even more expensive than the device itself. The overall cost of power electronics-based equipment is nearly linearly dependent on the overall number of switches in the circuit topology. Hence, this research suggests a scheme that uses only one PWM switch with no energy storage. Since fewer components are required in this scheme, the system becomes more reliable and less expensive.

Existing methods of voltage sag mitigation using gate turn-off switches for PWM need at least two switches per phase. Other methods use a direct AC-AC converter topology. In addition to requiring at least two switches per phase, they require energy storing reactive components. Therefore, it should be clear that the proposed system having only one PWM switch per phase with no energy storage is a very low cost solution for voltage sag mitigation.

As a first step, this research reviews the statistical surveys of power quality problems in order to determine the specifications of the target system, and this research evaluates existing methods used to compensate for voltage sags and swells. Since the majority of voltage sag events occur under severe weather conditions, the voltage distribution of the system under lightning surge must be investigated. From the power quality surveys, it is known that most voltage sag events last for less than 2 seconds. Hence, it is necessary to operate this device only for a short period. Therefore, to increase the system efficiency and to provide the means of bypass of a short current, the system employs another switch in addition to the PWM switch, which is a bypass switch implemented with thyristors. The bypass switch is in the on-state most of time, and the PWM switch, which is actually a high voltage bidirectional AC switch, operates only during a voltage sag condition and regulates the output voltage according to the PWM duty-cycle.

In order to quickly and precisely control the output voltage or mitigate the input voltage sag, this research includes several design issues such as the design of the voltage controller, the voltage sag detector, and the snubber circuitry. To hasten the transition from bypass mode to PWM mode, i.e., from normal voltage mode to sag mitigation mode, this research suggests a commutation logic for the bypass switch that minimizes the commutation process.

The fault detection logic for switching devices and components are also presented. Fault situations in the sag supporter itself are analyzed, along with their resultant causes and effects, so that appropriate logic and detection circuits can be developed to maximize the reliability of the system. In order to quickly detect faults in the supporter and lessen

the burden of the voltage controller, hardware-based fault detection is preferred over those realized by software logic.

In order to test the performance of the system and to find any problems caused by using actual devices, prototype experiments were done and their results are presented.

1.3 Thesis Outline

A brief overview of the results of a literature survey related to voltage sag and mitigation devices are presented in Chapter 2.

In Chapter 3, this research proposes two schemes of voltage sag mitigation, the so-called “shunt type” and “series type” of topologies. The voltage distributions of the two schemes in the case of a lightning surge are analyzed using PSPICE simulations. In this chapter, the final mitigation scheme is chosen, and the basic configuration of the sag supporter system is presented.

To efficiently mitigate the voltage sag event with the proposed method, many system designs are required. In Chapter 4, design issues such as a snubber, filters, and a voltage controller etc. are explained. Simulation results of voltage sag and swell conditions are presented to show the fast control response and the well-regulated output voltage using the proposed scheme.

Chapter 5 describes the internal fault detection algorithm for each switching device as well as the other components in the system. To detect a device fault, each gate driver circuit is designed with a signal showing either a healthy or and faulty status. The

circuitry is implemented using a programmable logic device. The complete logic scheme for internal fault detection is explained in Chapter 5.

Experiments have been carried out to demonstrate the validity of the proposed scheme, and the results are presented in Chapter 6. In this chapter, the software routines for the voltage controller, and the hardware configuration, are briefly explained.

The conclusions and contributions resulting from this research work are summarized in Chapter 7, and recommendations for future research are also provided in this chapter.

CHAPTER 2

PREVIOUS WORK ON VOLTAGE SAG AND VOLTAGE SAG MITIGATION DEVICES

This chapter reviews the typical characteristics of voltage sag, and gives a brief review of previous work in power electronic systems for voltage sag mitigation.

2.1 Power Quality Surveys

With an increase in the use of sensitive loads, the power quality issues have become an increasing concern. Poor distribution power quality results in power disruption for the user and huge economical losses due to the interruption of production processes. According to an EPRI report, the economical losses due to poor power quality are $400 billion dollars a year in the U.S. alone [1]. A power disturbance can be classified as voltage sag, swell, over voltage, under voltage, surge, outage, etc. More widespread use of advanced power-line monitoring technology is enabling useful surveys of electric power quality that can be used to statistically characterize power quality problems. Three power quality surveys for North America had been done by the National Power Laboratory (NPL), the Canadian Electrical Association (CEA), and the Electric Power

Research Institute (EPRI) [2]–[4]. Table 2.1 shows summary of these three power quality surveys.

In each of the three surveys, the definition of a power disturbance event is different. For instance, "voltage sag" is defined as being less than 92% and 90% of nominal voltage for the CEA and the EPRI survey, respectively. In case of "voltage swell", the CEA defines it as the voltage level greater than 104% of nominal voltage, while that of the EPRI is 110%. The data of the three surveys was summarized by Duglas D. Dorr [5]. This paper shows the voltage sag events defined by 0% to 87% of nominal voltage comprise 68% of power disturbances, in which no filter was applied for NPL data. Where, no filter means that every power disturbance is recorded. In the NPL survey, the voltage range of 106% to 110% of nominal voltage is considered to be a voltage swell event. If the EPRI definition of voltage swell, greater than 110% of nominal voltage, is applied to the same data, it results in that voltage sags events having 0–87% consists of 93.3% of total event, and voltage sag having 50%–87% of nominal voltage consists of 70% of total disturbances.

In addition, the EPRI survey shows that in most of the cases (92%), the voltage sags have duration of less than 2 seconds and down to 40–50% of nominal voltage [6]. Besides the above three surveys, many papers have reported power quality surveys. The survey reported in [7] shows that 68% of the power disturbances were voltage sags, and these types of disturbances were the only cause of production losses. From power quality surveys, it can be concluded that voltage sags are the most common power disturbances

and main cause of power disruption. Therefore, this research focuses on voltage sags and their mitigation techniques.

Table 2.1 Summary of the CEA, NPL, and EPRI power quality survey.

Survey	Period	Number of Site	Measure Parameter	Voltage rating
CEA	1991 – 1994	550	Voltage	120 or 347 V
NPL	1990 – 1995	130	Voltage	-
EPRI	1993 – 1995	277	Voltage and Current	4.16 – 34.5 kV

2.2 Voltage Sag

A voltage sag is a momentary decrease of the voltage RMS value with the duration of half a cycle up to many cycles. Voltage sags are given a great deal of attention because of the wide usage of voltage-sensitive loads such as adjustable speed drives (ASD), process control equipment, and computers. In case of sensitive loads, even a shallow voltage dip can cause malfunctions and a stoppage of operation, which results in the loss of production.

2.2.1 Causes of Voltage Sags

Faults in systems and starting large motors create voltage sags. In case of starting large motors, the voltage sags are usually shallow and last a relatively long time. Faults

in the distribution or transmission line can be classified as single-line-to-ground (SLG), and line-to-line (L-L) faults. SLG faults often result from severe weather conditions such as lightning, ice, and wind. Animal or human activity such as construction or accidents also causes SLG faults. Lightning may cause flashover across conductor insulators and is the major source of SLG faults. Figure 2.1 shows a typical shape of voltage sag due to a short SLG fault. Many statistical power quality studies have been performed in various locations and show that most voltage sags are caused by SLG faults. SLG faults can occur at any place in the power system and are nuisance to industrial and commercial customers.

The magnitude of voltage sag can be expressed by the voltage divider model of voltage sag events as shown in Figure 2.2. With ignoring the load current, the sag voltage V_{sag} can be expressed as (2.1).

$$V_{sag} = \frac{Z_s}{Z_s + Z_f} \times V_s \tag{2.1}$$

Where, Z_s represents the source impedance at the point of common coupling (PCC) and Z_f represents impedance between the PCC to the location of the fault [8]. At the point of fault, the voltage is almost zero. Therefore, the impedance of Z_s and Z_f determines the magnitude of voltage dip, and the duration of voltage sags is determined by the fault clearance time of the protection device. From (2.1), it can be known that the fault occurs near to PCC, which causes deeper voltage sag.

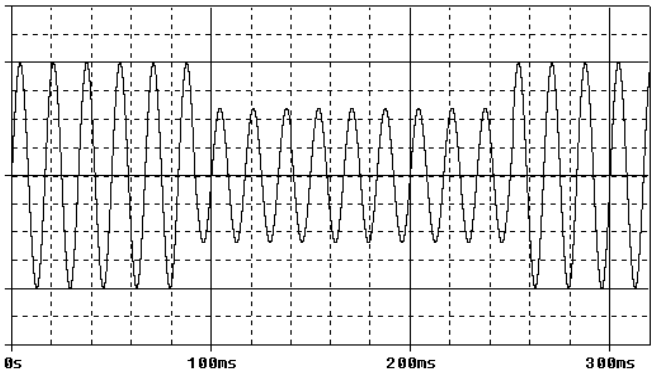


Figure 2.1. A shape of voltage sag due to SLG fault.

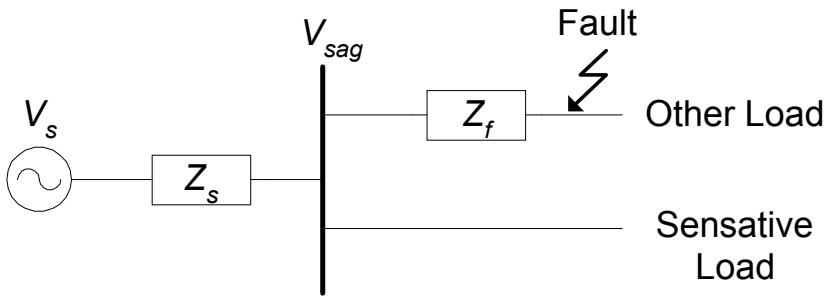


Figure 2.2. Voltage divider model for a voltage sag event.

2.2.2 Sensitivity of Voltage Sags

Figure 2.3 shows the Information Technology Industry Council (ITIC) curve that has been introduced to suggest a guideline for voltage quality in power distribution systems serving main computers, and it has become an industry reference for acceptable voltage tolerance. This curve specifies the voltage dip magnitude and the duration of the voltage sag for 120 V single-phase applications. The curve shows that a 10% voltage deviation is acceptable even if the voltage sag or swell remains for a long time, but a 30% voltage

drop for a time period longer than 0.5 second is not acceptable. This curve is useful for providing general insight into acceptable voltage quality. The SEMI–F47 [9] specifies the requirement of voltage quality for the voltage sag immunity of semiconductor manufacturing processing. Table 2.2 shows the duration and magnitude of voltage sag specified by the SEMI–F47.

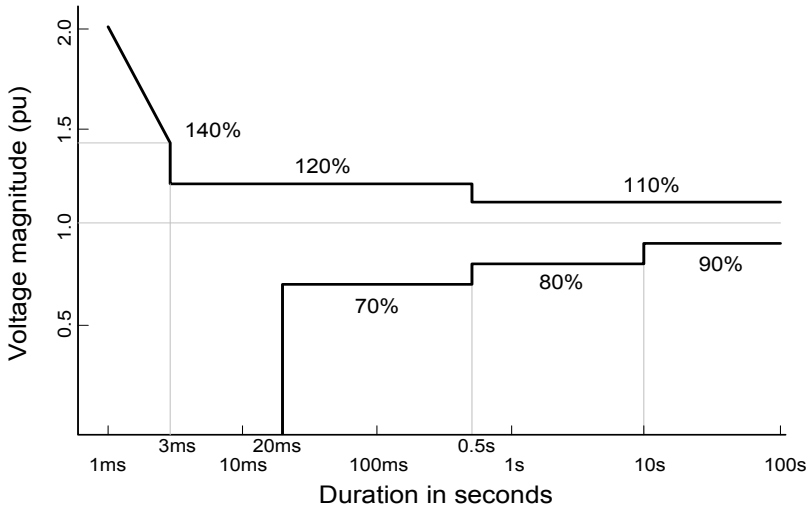


Figure 2.3. The ITIC curve.

Table 2.2 Recommended voltage for semiconductor industry.

Duration	< 0.05s	0.05s - 0.2s	0.2s - 0.5s	0.5s - 1.0s	> 10s
Magnitude	-	> 50%	> 70%	> 80%	> 90%

Voltage sags affect the performance of equipment and may trigger the system's protection circuit, which interrupts power. As a result of the loss of power, the process of work will stop. The voltage sag tolerance of devices varies widely, and the range can be

shown in Table 2.3 [8]. For instance, a value of X ms, Y% indicates that a voltage sag lower than Y% and longer than X ms causes a trip or malfunction of the equipment. This table does not show the tolerance range for specific devices. For reliable operation, the tolerance range should be higher than the average level.

In addition, many literature surveys have been performed to specify the threshold voltage that causes a trip or malfunction of the system. The research [10] shows that in case of ASD (adjustable speed drive), voltage sag with a duration of 12 cycles or more and lower than 20% voltage drop may trip out some ASD's involved in continuous processes. Program logic controller with computerized numerically controlled (CNC) machines can be disrupted with a sag of longer than 1 cycle and less than 86% of nominal voltage. However, the sensitivity highly depends on the equipment itself, and the survey of threshold voltage test says that some equipment has a threshold at 30% voltage.

Table 2.3 Voltage tolerance ranges of equipment.

	Voltage Tolerance		
Equipment	Upper Range	Average	Lower Range
PLC	20 ms, 75%	260 ms, 60%	620 ms, 45%
PLC input card	20 ms, 80%	40 ms, 55%	40 ms, 30%
5 HP AC drive	30 ms, 80%	50 ms, 75%	80 ms, 60%
Personal computer	30 ms, 80%	50 ms, 60%	70 ms, 50%

2.3. Voltage Sag Mitigation Devices

To better understand the most effective method of voltage sag mitigation, a brief review of existing methods is presented.

2.3.1 Tap Changers

Tap changers are the most cost-effective method for regulating the output voltage when the input voltage has a sag condition that exists for a relatively long period of time. It is possible to vary the output voltage by changing taps located in the primary or secondary side of a transformer. Most existing tap changers use mechanical moving parts to change the tap location. Usually, three or four cycles are needed to move the mechanical switch to the desired position. Therefore, its response is relatively slow [11]. To overcome this problem, thyristors have been used recently to replace the mechanical parts of the tap changer.

The simplified configuration of a thyristor tap changer is shown in Figure 2.4 to show the output voltage waveforms controlled by either phase control or discrete-level control. The output voltage waveforms generated by phase control are shown in Figure 2.5 (a). It can be seen from the figure that the voltage waveform controlled by the phase control contains a relatively high harmonic distortion component. To reduce the harmonic distortion, discrete-level control can be used. In discrete-level control, the thyristor pairs conduct during one cycle. However, to get many discrete voltage levels, it

is necessary to have many transformer taps, which means that it needs many thyristor pairs as well. This is another disadvantage of thyristor tap changers.

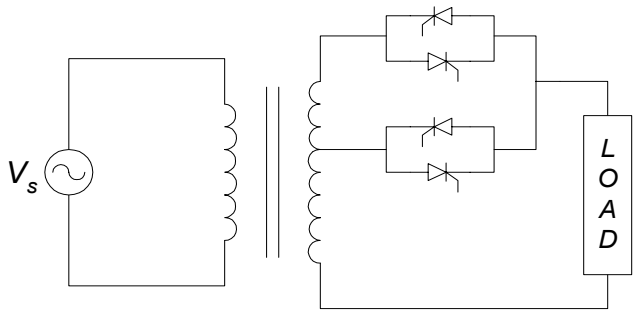
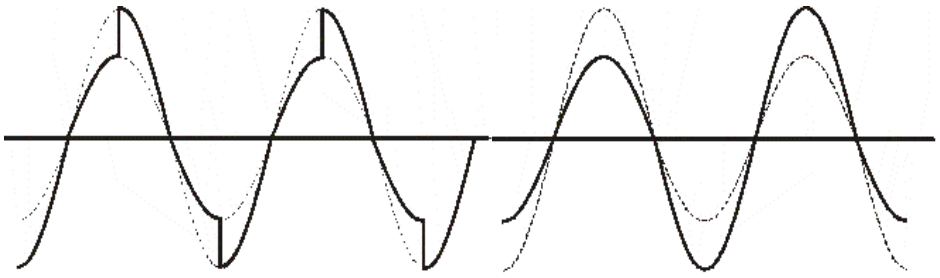


Figure 2.4. Thyristor tap changer using two thyristor pairs.



(a) Phase control (b) Discrete-level control

Figure 2.5. Output voltage waveforms of thyristor tap changer.

2.3.2 Flexible AC Transmission Systems (FACTS) Devices

FACTS devices have abilities of controlling active powers and reactive powers of the distribution system, which are able to maximize the utilization of existing lines. In addition, they can stabilize the voltage at point of common coupling and can reduce the

damping of the power oscillation. FACTS devices can be divided into three categories such as series controller, shunt controller, and combined controller [12].

- Series connected controllers: Static Synchronous Series Compensator (SSSC), Thyristor-Switched Series Capacitor (TSSC), Thyristor-Switched Series Reactor (TSSR), etc.
- Shunt connected controllers: Static Synchronous Generator (SSG), Static Var Compensator (SVC), Static Synchronous Compensator (STATCOM), Thyristor-Controlled Reactor (TCR), Thyristor-Switched Capacitor (TSC), etc.
- Combined controllers: Unified Power Flow Controller (UPFC), Thyristor-Controlled Phase Shifting Transformer (TCPST), etc.

Among the FACTS devices, many methods are based on inverter topologies such as STATCOMs. On the other hand, TSCs or TCRs based on thyristor switches use passive elements such as capacitors or reactors to change the reactive impendence of systems for controlling active and reactive powers. The inverter system gives more flexibility of controlling power and improving the power stability as well as control of the magnitude and phase of the voltage. Since this research mainly focuses on the mitigation of voltage sags, only the inverter based FACTS devices will be explained in the viewpoint of compensation of voltage sag events.

2.3.2.a Series Compensation Method

Recently, a dynamic voltage restorer (DVR) was introduced for mitigating a voltage sag [13]–[20]. The DVR shown in Figure 2.6 is based on an inverter system that has energy storage for supplying active power, an output filter to make more sinusoidal voltage, and a step up transformer.

The DVR is one of the FACTS devices that use the power electronics technology, especially inverter technology and is configured as a series-connected voltage controller. To control the output voltage of the DVR, the inverter supplies the missing load voltage using self-commutable electronic switches such as a gate turn-off thyristor (GTO), an insulated gate bipolar transistor (IGBT), or an insulated gate commutated thyristor (IGCT). The DVR injects the missing voltage in a series. Therefore, it can be called a series voltage controller, but the term DVR is commonly used now.

DVRs have a same configuration of SSSC. The DVRs can be operated with a relatively small capacitor to exchange reactive power or can supply active powers to loads with energy storage. The large capacitor bank, flywheel, superconducting magnetic device, and battery can be used for the energy storage.

The DVR, located between the supply and critical loads, has demonstrated excellent dynamic capability for mitigating voltage sags or swells. Each phase can be controlled independently, and the DVR can adjust the magnitude of the load voltage and the voltage phase angle as well. The advantages of the DVR are its fast response and ability to compensate for a voltage sag and a voltage phase shift using an inverter system.

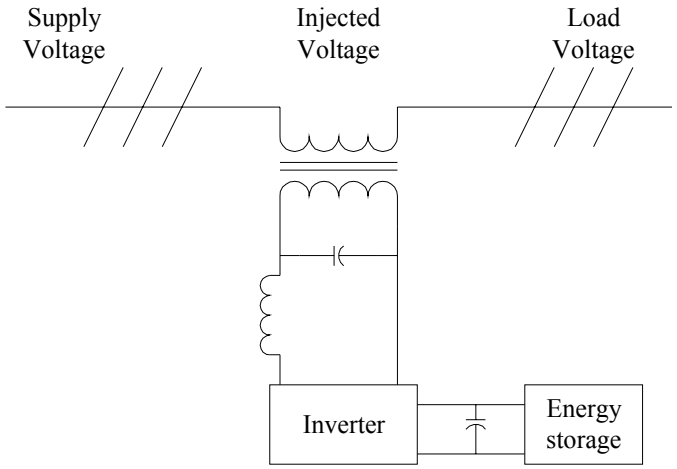


Figure 2.6. Configuration of a dynamic voltage restorer.

Three schemes can be used to generate the missing voltage in series with the source voltage for compensating the voltage sag such as,

i) In-phase voltage injection

ii) Phase-invariant voltage injection

iii) Phase–advanced voltage injection

In the in-phase voltage injection scheme, the injecting voltage has a same phase angle of the source voltage. Therefore, the magnitude of the injected voltage is the smallest among three compensation schemes. However, this scheme requires the largest active power. In case of the phase invariant voltage injection scheme, the DVR injects the missing voltage that keeps the magnitude of the voltage as well as the phase of the supply voltage. This scheme needs a large injected voltage and may cause over injection of reactive power. Since the size of energy storage is closely related to the requirement

of active power, various compensation methods to reduce the requirement of active energy have been proposed [21]–[22]. If the injected voltage is in quadrature with the load current, the DVR does not inject active power. This scheme is highly depends on the load power factor and can generate a sudden jump of the voltage phase angle. To avoid sudden phase angle jump, the phase of the injected voltage should be gradually changed at the beginning of the compensation as well as at the restoration in order to do not disturb the operation of sensitive loads. The high-speed PWM switching and output filter make it possible to achieve a fast response with less harmonic distortion. However, DVRs are relatively expensive because of the inverter systems, the inserting transformer, and energy storages that need to contain energy to supply active and reactive power for the missing voltage.

2.3.2.b Shunt Compensation Method

A distribution static synchronous compensator (D-STATCOM) is shown in Figure 2.7, which controls the load voltage in a shunt configuration. The DVR method injects a missing voltage, while the D-STATCOM injects a current to compensate the load voltage variation.

D-STATCOM mainly consists of the inverter circuit with X_{sh} coupling inductance, the leakage inductance of the transformer. Also, the D-STATCOM, a shunt-connected voltage controller, is connected to the critical load with system impedance [23]. The effectiveness of D-STATCOM depends on the source impedance Z_{th} and the fault level.

When the phase of the V_{sh} is in quadrature with the I_{sh}, without injecting real power the D-STATCOM can achieve the voltage sag mitigation. The shunt injecting current i_{sh} and V_L in Figure 2.7 can be expressed as (2.2).

$$I_{sh} = I_L - I_s = I_L - \frac{V_{th} - V_L}{Z_{th}}$$

$$V_L = V_{th} + (I_{sh} - I_L) \cdot Z_{th} \qquad (2.2)$$

Equation (2.2) shows that the compensation voltage is closely related to the impedance Z_{th}. The complex power developed in the D-STATCOM controller to support the load voltage is given as (2.3).

$$S_{th} = V_L I_{sh}^* \qquad (2.3)$$

Notice that the impedance Z_{th} is connected in parallel with the load impedance. When a short occurs near the load, the equivalent impedance Z_{th} becomes a small value. Hence, from (2.2) it can be known that the D-STATCOM is then required to generate a large reactive current I_{sh} to support the load voltage V_L. This is why the D-STATCOM controller is rarely used as a voltage sag supporter. The D-STATCOM controller is often used for power factor correction, voltage flicker mitigation, and active filtering.

From the operation principles of DVR and D-STATCOM, it can be known that both devices have an ability of the absorbing or generating of reactive power. However, it is

necessary to have large power energy storage to inject active power. Several researches have compared the performance of the DVR and the STATCOM and power rating with various fault voltage levels. These studies show that the power rating of the series voltage injection method such as the DVR is lower than the shunt current injection method such as the STATCOM.

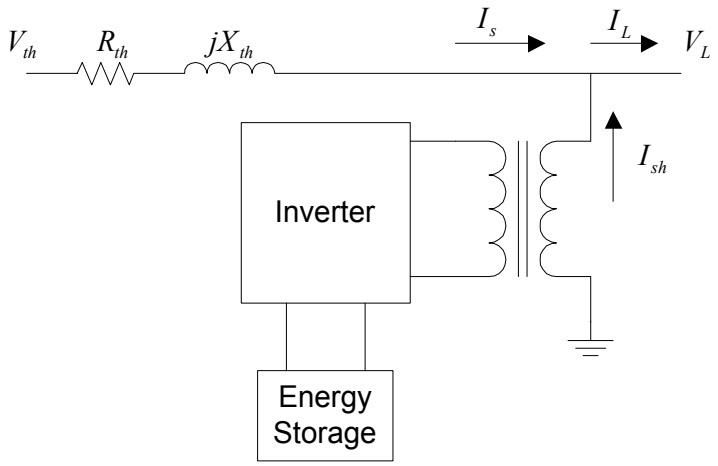


Figure 2.7. Schematic of a D-STATCOM.

2.3.2.c Combined Compensator

The unified power flow controller (UPFC) shown in Figure 2.8 is the combination of the static synchronous series compensator (SSSC) and the shunt compensator (STATCOM) with a common DC-link energy storage capacitor. The UPFC can control reactive and real power. Therefore, the UPFC can maximize the power line capability and reduce power loss in the system [24]. The operating modes of two voltage source inverters (series, shunt) in the UPFC can be summarized as follows.

The shunt compensator has two modes. One is the VAR control mode, in which it controls the reactive power according to an inductive or capacitive VAR reference, and the other is automatic voltage control mode. In this mode, the compensator regulates the transmission line voltage at the connection as a constant value by changing the shunt converter reactive current, and this mode is normally used in practical applications.

There are five possible control modes in the serial compensator [12]: bus voltage regulation and control, direct voltage injection, phase angle shifter, line impedance emulation, and automatic power flow control. In many possible control modes, the automatic power flow mode is used in majority of practical applications. In this mode, the magnitude and the angle of the injected voltage is controlled with respect to the line current, the series compensator controls real and reactive power in the line. Using a closed-loop control, the series converter independently controls real and reactive power with desired values regardless of changes of the power system. Since this research mainly focuses on mitigating voltage sags not controlling the power flow, the UPFC can be regarded as an expensive alternative solution for voltage sag compensation.

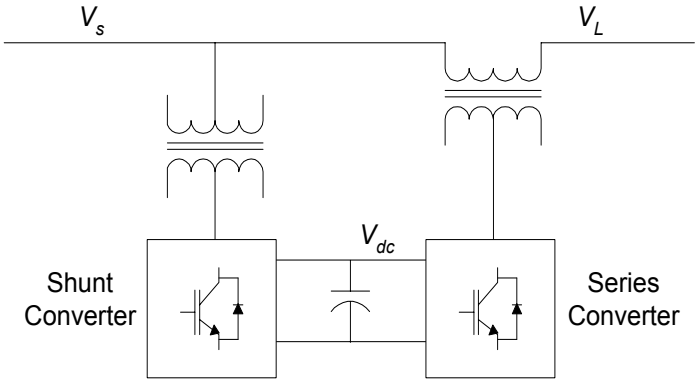
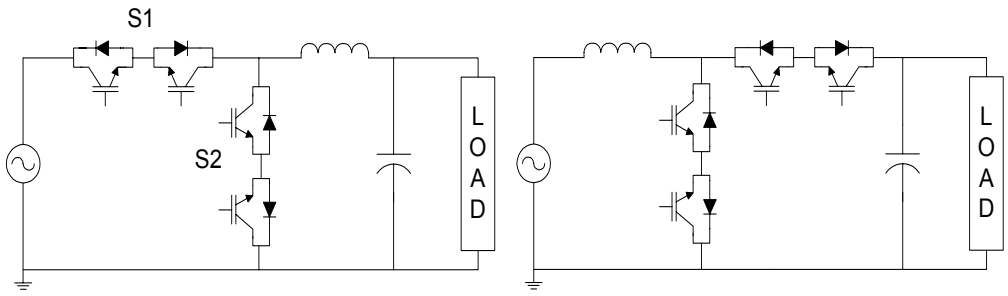


Figure 2.8. Configuration of a UPFC.

2.4 AC Converters

Various AC converter technologies have been proposed for AC output voltage control [25]–[35]. The well-known DC to DC conversion technology has been adapted to AC to AC conversion technology. Also, mature PWM technology is used to regulate the output voltage as constant values during sags or swells. The AC converter topology can be classified as buck, boost, and buck-boost type, and its role is step-down, step-up, and step-up/down, respectively. The ratio of input voltage to output voltage can be expressed as D, $1/(1-D)$, and $-D/(1-D)$, respectively. D represents duty-cycle. Since the phase of the output voltage of the buck-boost type AC converter is inversed with respect to the phase of the input voltage, the buck-boost type converters are not desirable for line conditioner [28]. The buck and boost type are used to only step-down and step-up function, respectively.

Figure 2.9 shows the buck and the boost topology for a single-phase application. AC converters consist of two solid-state switches per one phase, and reactive elements such as a capacitor and an inductor are used for step-up or step-down operation. Since the current in the AC converter flows in both directions, static switches and diodes that are serially connected to allow both directions current. Switches S_1 and S_2 operate complementarily; hence, it is necessary to provide a turn-on delay between S_1 and S_2 switching to avoid the short circuit.



(a) Buck AC converter. (b) Boost AC converter.

Figure 2.9. AC converter topologies.

One example of an output voltage control scheme based on AC converters is shown in Figure 2.10, in which the LC filter is included to generate a more sinusoidal output voltage. A buck type converter with a boosting transformer may be one of several possible voltage sag mitigation schemes. This topology is similar to that of the DVR shown in Figure 2.6. In this scheme, the AC converter replaces the function of the inverter in the DVR topology, which generates the missing voltage. Because the AC converter does not need a large DC link capacitor, it makes the overall system less expensive.

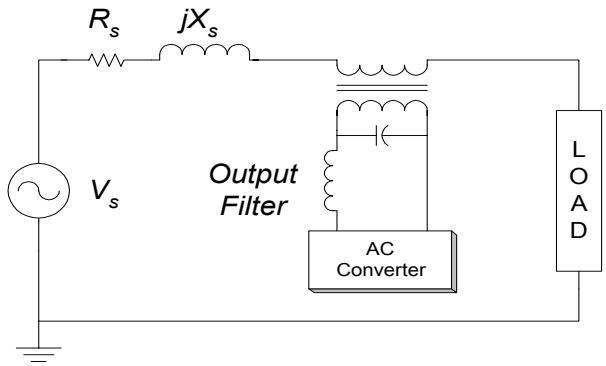


Figure 2.10. Voltage regulation scheme using an AC converter.

2.5 Modified Scheme

Besides above schemes, several topologies for voltage sag mitigations have been proposed [36]–[37]. In [36], the inverter-based topology so called Dynamic Sag Corrector (DySC) is presented as shown in Figure 2.11. This topology is capable of bypass mode and voltage boost mode. During the voltage boost mode, the missing voltage is added to the input voltage to generate the output voltage. In [37], a PWM AC converter-based scheme is presented, in which an autotransformer is used to boost the input voltage. Same as [36], the output voltage is obtained by summation of the input voltage and the missing voltage generated by the AC converter. In the scheme of [37], same as AC converters, two switch pairs are used for single-phase application.

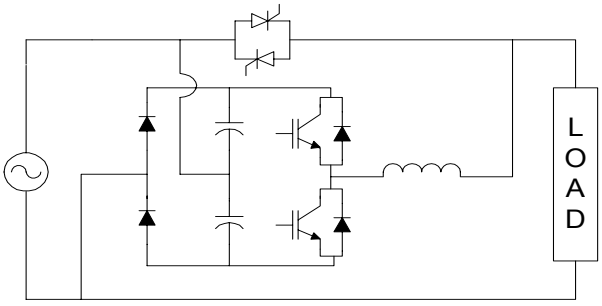


Figure 2.11. Single phase DySC topology.

2.6 Chapter Summary

In this chapter, the causes and effects of voltage sags have been briefly reviewed. It was known from various power quality researches that most of power quality problems are voltage sag events, and they can cause serious power distribution problems.

A summary of the state of the art methods proposed for voltage sag mitigation has been presented in this chapter. It has been shown that many kinds of methods can be used for the purpose of this research, and the PWM scheme has been successfully used the voltage sag mitigation devices, such as FACTS devices and AC converters. These various schemes for mitigating the voltage sag have been reviewed to determine the direction of the research.

From result of the literature survey, it was known that the FACTS devices show a fast control response. However, the cost of the system is relatively expensive due to inverter systems and large energy storage for supplying active power. Also, it was known that the PWM AC converter could be used for cost-effective solution for this research. It was shown that buck type converter with a boosting transformer and boost type converter were successfully applied for voltage sag mitigation of single-phase and three-phase applications. It was noted that the AC converter topology uses two switches per one-phase application.

CHAPTER 3

SELECTION OF

VOLTAGE SAG MITIGATION TOPOLOGY

3.1 Selection of Compensation Method

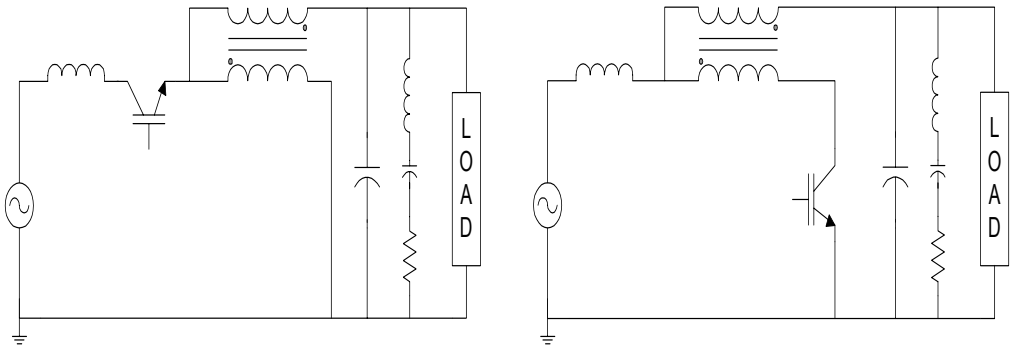
The literature survey done in the previous chapter showed that tap changers, DVRs, and AC converters are some of the better existing voltage compensation solutions. However, tap changer topology has a slow response time for mechanical switching units. Tap changers using thyristors have high harmonic distortion for phase control units and the high cost for discrete-level control units. These disadvantages make this technology unattractive for this research. The DVR topology is also unattractive as a solution for large power systems because of the high cost. Hence, this research focuses on the AC converter topology shown in Figure 2.9 as the basis for a new voltage sag compensator and further study. For example, a voltage sag compensator can be realized using the topology shown in Figure 2.10 with a buck AC converter and a boosting transformer.

Eliminating the electrical switches reduces the cost and complexity of the system. The AC converters in Figure 2.9 need two switch pairs per phase. One switch pair consists of two switches conducting current in both directions. The AC converter

topology is an inexpensive approach for low voltage and low power implementation, but the switch used for high voltage system is expensive. The switch cost is a significant portion of the overall system cost in this research. Therefore, minimizing the number of switches significantly reduces cost.

Reducing the number of switches has a high priority in this research. The series type and shunt type voltage compensators are shown in Figure 3.1 (a) and (b), respectively. These schemes have only one switch, and an autotransformer is used for a boosting transformer instead of a two-winding transformer.

The schemes can be classified as either "shunt type" or "series type." The names are based on how the injecting voltage is added to the output voltage. In the shunt type scheme, the switch is located before the autotransformer, and the developed voltage is injected in a shunt manner. In the series type scheme, the switch is located after the autotransformer, and the developed voltage is serially added to the supply voltage.



(a) Shunt type (b) Series type

Figure 3.1. Shunt type and series type compensators.

3.1.1 Comparisons between Series type and Shunt type Compensation

The autotransformer shown in Figure 3.2 is used in the proposed system to boost the input voltage instead of a two winding transformer. The autotransformer does not offer electrical isolation between primary side and secondary side, but this autotransformer has advantages of high efficiency with small volume.

The relationship of the autotransformer voltage and current is shown in Figure 3.2 and expressed as (3.1), where a is the turns ratio. In this research, the transformer with ratio $N_1 : N_2 = 1 : 1$ is used to boost up to 50% voltage sag. $N_1 : N_2$ is common notation for the turns ratio of a two-winding transformer. From equation (3.1), it can be known that the turns ratio of an autotransformer is defined by $N_1 : (N_1+N_2)$, which is 1 : 2 in this case. However, in order to easily recognize that the autotransformer has same turns of primary and secondary side, the term of "1 : 1 turns ratio" is used for convenience of later analysis.

As the turns ratio equals 1 : 1, the magnitude of the load current I_H (high voltage side) is same as that of the primary current I_1 (low voltage side). Therefore, so that from Equation (3.1) it can be known that $V_H = 2V_L$ and $I_L = 2I_H$.

The series type and shunt type topologies are compared to determine the best topology for high voltage implementation. Initially, the magnitudes of the switch current and the voltage across the switch are compared to understand the advantages of a particular topology. It is assumed that the autotransformer has a 1 : 1 turns ratio and a 100% duty-cycle of the switch.

In the series type topology, since the switch is located in the autotransformer's primary side, the magnitude of the switch current equals the load current, whereas in the shunt type topology, the switch current is two times the load current. Based on the magnitudes of the switch currents in both topologies, the series type compensator is found to be a better choice.

Because voltage sag conditions occur only a few times, and the duration of a 92% voltage sag event is less than 2 seconds as shown in the previous chapter, this voltage sag supporter works only a few seconds and remains off-state most of its operation time. Since the switches in the voltage sag supporter remain in the off-state most of the time and must withstand the voltage across it, the voltage across switch should be considered. The magnitude of voltage across the switch in the off-state is an important factor to decide a topology because it affects the expected lifetime of the switch.

In the shunt type topology, the voltage across the switch in the off-state is equal to one half of the input voltage, while in the series type case, the voltage across the switch in the off-state is equal to the magnitude of the input voltage.

In summary, the series type topology has the advantage of lower switch current, and the shunt type topology has the advantage of lower off-state voltage. Since the voltage across the switch is a more important factor for deciding overall system safety, the shunt type topology is chosen for the voltage compensation scheme. The voltage sag supporter will operate during severe weather conditions such as lightning. To determine the final topology, effects of surge voltage during a lightning strike must be considered. Voltage

distributions of the system under lightning surge condition are simulated, and results are given in Section 3.3.3.

$$\frac{V_L}{V_H} = a = \frac{I_H}{I_L}, \quad a = \frac{N_1}{N_1 + N_2} \tag{3.1}$$

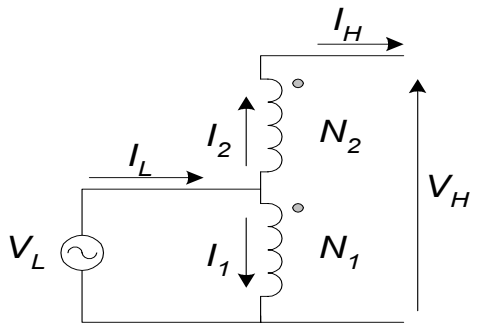


Figure 3.2. Voltage and current relation in an autotransformer.

3.2 Configuration of the Proposed System

It is now necessary to introduce a new configuration and control logics that are suitable for normal operating conditions as well as voltage sag conditions. To do that, a thyristor is connected to the load side to serve as a bypass switch. Design issues of the proposed system will explain in detail in next chapter. This research suggests a scheme for mitigating voltage sag as shown in Figure 3.3.

The proposed system consists of a PWM switch block, a bypass switch block, output filters, an autotransformer, and a voltage controller. Two kinds of switches are present in this system, a IGBT and a thyristor. The IGBT operates only during a voltage sag

condition and regulates the output voltage corresponding a PWM duty-cycle. A thyristor is used as the bypass switch in an inverse parallel configuration. This bypass switch connects the input power to the load unless the sag condition is present. The efficiency of the voltage compensator is very high because during normal operation power passes only through the thyristor.

In the proposed voltage sag supporter, an autotransformer having a 1 : 1 turns ratio is used for boosting the input voltage. To filter out the switching noise and reduce harmonics, output filters (a main capacitor filter and a notch filter) are attached to the output side. To suppress the over voltage when the power switches are turned off, RC snubber circuits are connected across every IGBT and thyristor.

In this research, the input voltage is about 15 kV RMS, and rated voltage of the IGBT and thyristor are 6500 V. Therefore, it is necessary to serially connect the switches to withstand the input voltage. Circuit simulations are done to determine the total number of serially connected IGBTs for PWM switch and thyristors for static bypass switch. Because the snubbers are serially connected, they have a function of dynamic voltage sharing as well as the role of a turn-off snubber.

The proposed voltage sag supporter starts the PWM switching when the input voltage becomes lower than 90% of nominal voltage, i.e., this compensator does not operate if the input voltage remains within 10% deviation of the nominal value. The 10% deviation is inferred from the investigations of the voltage quality studies in Chapter 2 and Figure 2.3. In Figure 2.3, it is shown that a 10% voltage dip is allowable even the dip exists longer than 10 seconds. Therefore, under normal conditions, i.e., bypass mode

can be defined as the magnitude of the input voltage is higher than 90% of nominal voltage. During normal conditions, the bypass switch remains on.

On the other hand, when the sensing circuit detects more than 10% voltage sag, the voltage controller immediately commands turn-off process (commutation) of bypass switch and then commands the IGBTs to start PWM switching to regulate the output voltage.

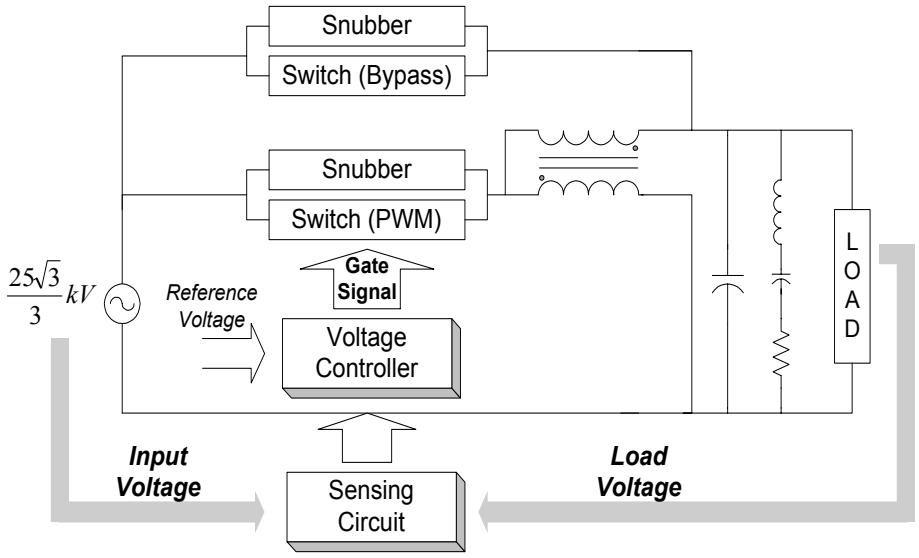


Figure 3.3. Basic configuration of the proposed voltage compensation scheme.

3.3 Comparison of the Voltage Magnitude of Series type and Shunt type

This section compares the peak voltage magnitude of the shunt and the series type during lightning surge. To better understand the voltage distribution in the system during the lightning surge, configuration of the IGBT switch block should be known first.

3.3.1 Bridge Configuration

The IGBT switch block consisting of diodes, a switch, and a snubber, which is so–called a bridge configuration is shown in Figure 3.4. The bridge configuration allows current flow in both directions by using just one switch. The switch configuration shown in Figure 2.9 (a) and (b) for AC converters is equivalent to the bridge configuration, except that it uses two switches connected in a common emitter configuration for each switch pair S_1 and S_2. The diode bridge arrangement is used to achieve bi-directionality at the lowest cost. When the switch is on, a positive current flows in the path $D_1 \rightarrow SW \rightarrow D_4$, and a negative current flows in the path $D_3 \rightarrow SW \rightarrow D_2$. When the switch turns off, the current in the switch changes its path to the RC snubber noted as R_{snub} and C_{snub}.

In this research, the magnitude of the input three-phase line-to-line voltage is 25 kV RMS, which is equivalent to 14.4 kV (20 kV peak) line-to-neutral single-phase voltage. Therefore, to keep the peak voltage of the switch under the rating of the switch, seven bridges are connected in series, operating as one AC switch.

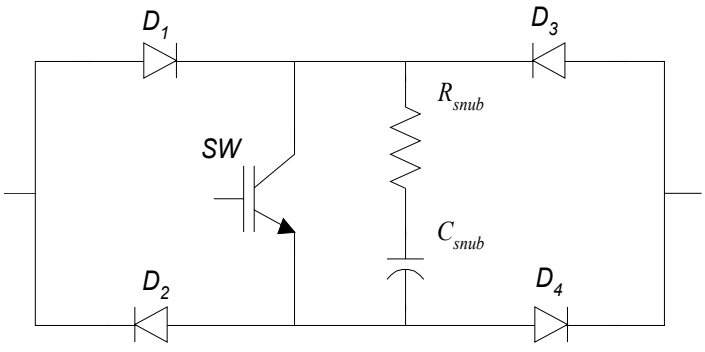


Figure 3.4. AC Switch with IGBT and snubber in bridge configuration.

3.3.2 Entire System Configuration

Figure 3.5 shows the actual circuit configuration. The inductor located between the input voltage source and switches represents source impedance. In Figure 3.5, it is shown that IGBT switch blocks and back-to-back connected thyristor switch pairs are serially connected to withstand the voltage across the switches. The total switch number of serial connection is seven and four for IGBT and thyristor, respectively. To determine the total number of IGBT switch pairs, circuit parameters such as the source impedance, the transformer leakage inductances, and minimum PWM duty-cycle are considered. More details are explained in the next section dealing with design of the RC turn-off snubber.

To determine the total number of thyristor pairs, it is necessary to check the condition when the largest voltage exists across each thyristor pair. During PWM mode, thyristor pairs should withstand a voltage difference between the output voltage and the input voltage. The maximum voltage across the thyristor occurs at 50% voltage sag. Since the output voltage is controlled to have nominal magnitude of the input voltage, the voltage across the thyristor pairs is 50% of the nominal voltage, which results in about 10 kV peak across the thyristor. Considering safety factors and over voltage condition, quantity four thyristor pairs (with each thyristor rated at 6.5 kV) are selected for the serial connection.

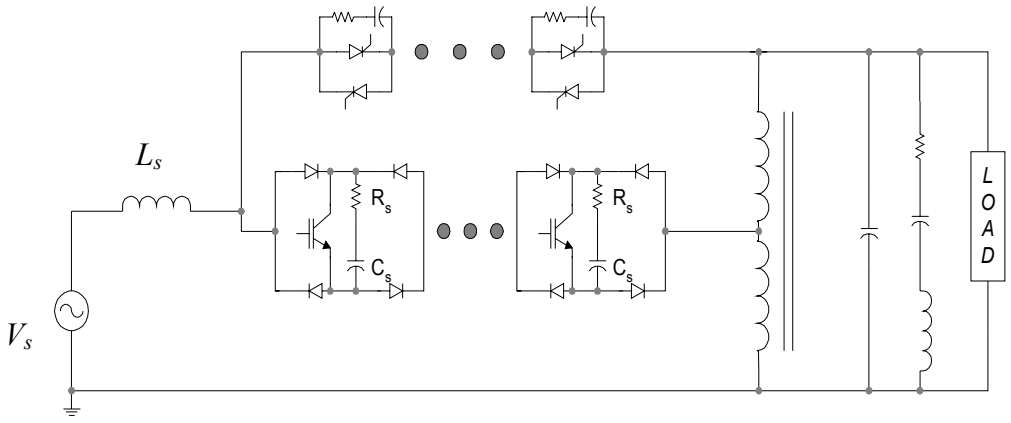


Figure 3.5. Overall system configuration showing serially connected switches.

3.3.3 Voltage Distribution during Lightning Surge

In the previous section, it was shown that the shunt type topology shows less voltage stress than the series type, while in the viewpoint of current stress in the series type was lower than the shunt type. These facts are inferred from the current and voltage relation of the autotransformer as shown in Figure 3.2.

To finalize the topology of the voltage mitigation device, it is necessary to examine the voltage distribution in the system during normal as well as abnormal conditions. During bypass mode under normal condition regardless of compensation types, the thyristor pair has a few volts showing the thyristor turn-on voltage drop. However, the voltages in the PWM switch (IGBT) corresponding to two compensation types have different voltage levels. The IGBT switch block has a bridge configuration with the RC turn-off snubber as shown in Figure 3.4, which works as a RC charging circuit similar to a rectifier circuit in inverter systems. When power is applied to the system, the capacitor

in the IGBT RC snubber will charge up, and it will stop charging when the diode in the bridge configuration becomes a reverse bias. If the energy in the source impedance L_s is ignored, the snubber capacitors charge up to the peak input voltage for series type and to a half of the peak input voltage for shunt type. For instance, considering the 20 kV input voltage and seven serially connected IGBT switch blocks, the capacitor charging voltage becomes 20 kV / 7 / 2 = 1.5 kV for the shunt type and 20 kV / 7 = 3 kV for the series type.

6.5 kV rating IGBTs are used in this research. The series type has a 3 kV peak voltage across the IGBT during normal condition. Therefore, it seems that the series type has enough voltage safety margins. However, 3 kV was obtained only under normal condition. Peak voltage across the IGBT and thyristor under abnormal condition should be considered as well. Lightning in power system is main cause of voltage sag events, and this voltage sag mitigation device has a more chance to operate under such a severe weather condition. Therefore, it is required to investigate the voltage across PWM and bypass switches during lightning surge.

In the proposed system, to protect the system from over voltage, MOVs (Metal Oxide Varistor) are placed in several places such as the input side, across the switch block, and the output side. A MOV has a non-linear V-I (Voltage-Current) characteristic, which can be realized by changing its resistance according to the voltage across the device. If the voltage across a MOV exceeds a certain level, the MOV offers a shunt path of the surge current, which suppresses the surge voltage. Several models of a MOV have been proposed to show the frequency dependent characteristic [38]–[42]. It is the

characteristic that the peak voltage of a MOV occurs before the peak of the current especially for fast front surge. In addition, MOVs show the characteristic that the maximum discharge voltage of MOVs is varied by the rising time of the surge current. The discharge voltage for a given current level is increased by 6% as the rising time of the surge current decreases from 8 μs to 1.3 μs [38]. To represent these effects, the IEEE W.G. 3.4.11 [38] suggested a model that has two non-linear resistors and R-L filters. However, this model has a difficulty in finding the parameters in the model. An inductor is required to show the frequency characteristic of MOVs. Datasheet for MOVs does not have enough of the actual voltage and current time response curves to determine the inductance value.

In simulations, MOVs are modeled as nonlinear resistors, because the main purpose of the simulation is to find out the peak voltage not the frequency response. In addition, the simulation uses a surge having a fixed time response, thus it is not necessary to model MOVs to have a different response for the surge having a different time response. The voltages across the IGBT switch and the thyristor are investigated under following three conditions. There exist two modes of PWM corresponding to IGBT ON and OFF, while the thyristor remains off in PWM mode.

- BYPASS mode (IGBT off, Thyristor on)
- PWM mode with IGBT ON (IGBT on, Thyristor off)
- PWM mode with IGBT OFF (IGBT off, Thyristor off)

Figure 3.6 shows the lightning surge waveform used for simulations, which has 140 kV peak voltage of 1.2 / 200 μs pulse duration. A typical surge voltage waveform has duration of 1.2 / 50 μs with a certain peak surge voltage. 1.2 μs is the time of reaching zero value to peak in the ascending slope, and 50 μs is the time of reaching from the peak to a half value in the descending slope. In simulations, it was assumed that the lightning surge exists relatively longer than conventional one with higher peak value of 140 kV in order to check the voltage distribution at worst case.

Where, the peak voltage is limited to 70 kV due to the MOV clamping. MOVs having 15.3 kV MCOV rating (maximum continuous operating voltage) have a maximum discharge voltage ranging from 40 kV to 63 kV corresponding to the surge current ranging from 1.5 kA to 40 kA with 8 / 20 μs duration [42]. As mentioned earlier, the discharge voltage of the MOV for the fast front surge such as 1 μs is higher than that for conventional surge current such as 8 μs. Therefore, 70 kV peak is chosen for the clamping voltage of the MOV.

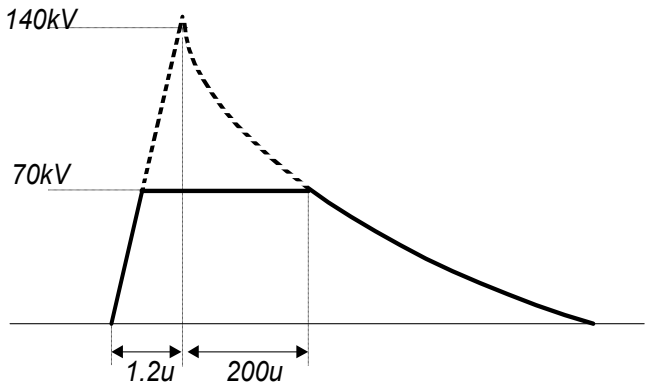


Figure 3.6. Lightning surge voltage waveform having 1.2 / 200 μs with 140 kV.

Figure 3.7 (a)–(c) show the equivalent circuits for lightning surge simulations. In bypass mode as shown in Figure 3.7 (a), thyristors are modeled as a resister to represent the turn-on voltage drop in the thyristors. The IGBT does switching during PWM mode. Therefore, there exist two states, which are IGBT ON and IGBT OFF. Two states of the PWM mode are described as "PWM mode with IGBT ON" and "PWM mode with IGBT OFF." In case of PWM mode with IGBT ON as shown in (b), the IGBT switch is modeled as a resistor to represent on-voltage drop in the IGBT. Figure 3.7 (c) shows the equivalent circuit during PWM mode with IGBT OFF. Since both IGBT and thyristor remain off, no resistor is required to show the turn-on voltage drop.

Stay capacitances of the transformer C_{st_trans} are taken account into the simulations. There exist stray capacitances of winding to winding, and that of winding to core. The junction capacitances of the diodes C_{dj} in the switch block and that of the anti-parallel diode C_{gj} in the IGBT are considered. Table 3.1 shows parameters used in lightning surge simulations.

Table 3.1 System parameters used in the lightning surge simulations.

Parameter	Value	Parameter	Value
R_{th}	100 Ω	R_{trans}	1.7 Ω
C_{th}	10 μF	$L_{leakage}$	20 mH
R_{snub}	49 Ω	C_{snub}	4 μF
C_{filter}	1.5 μF	C_{st_trans}	1 nF
C_{gj}	5 nF	C_{dj}	5 nF

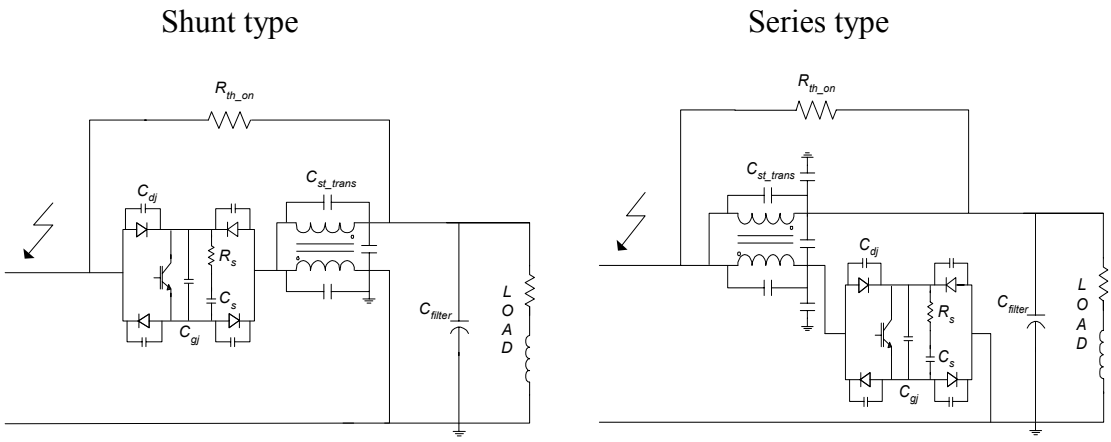
The voltage waveforms across the IGBT or/and the thyristor are shown from Figure 3.8 to 3.11. Figure 3.8 shows the IGBT voltage waveforms during bypass mode. In Figure 3.8 for series type, it can be seen that the peak value reaches around 7 kV. On the other hand, in case of shunt type the peak value remains lower than 5 kV, which is lower than the breakdown voltage of 6.5 kV rating IGBT. The leakage inductance of the autotransformer has a role to suppress the peak voltage across the IGBT. The higher leakage inductance, the lower peak voltage across the IGBT. In these simulations, the initial capacitor voltages of the RC snubber capacitor are selected as 1.5 kV, 3 kV, as explained in Section 3.3.3, for shunt and series type, respectively.

From Figure 3.7 (a), in case of series type, the secondary side of the transformer can be considered as a short circuit by ignoring the voltage drop occurring in R_{th_on}. In addition, with ignorance of the leakage components of the transformer, the primary side of the transformer also can be considered as a short circuit, hence only the RC snubber absorbs the lightning surge having 70 kV. On the other hand, from Figure 3.7 (b) for shunt type, it can be known that the voltage across the switch is 70 kV / 2 = 35 kV. Since the voltages in the primary and secondary sides of the ideal transformer withstand equally 35 kV, the peak surge voltage across the IGBT switch becomes 35 kV. This can explain why the shunt type has lower peak voltage than series type. Under real conditions, there always exist leakage components. With above assumption about no leakage components in the system, the voltage of the ideal transformer is zero for series type and 35 kV for shunt type. However, under real conditions, the voltage for the series type in the ideal transformer is not zero. The transformer voltage is lower than 35 kV corresponding to

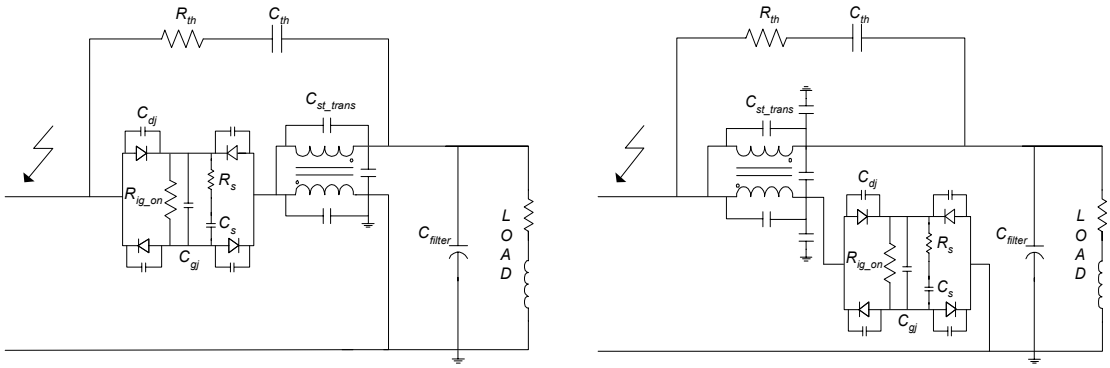
the 70 kV surge because of the impedance of IGBT turn-off snubber. Therefore, more than 35 kV is across the RC snubber. On the other hand, the voltage in the ideal transformer is always 35 kV in shunt type. There exist voltage drop in the leakage components, so that the voltage difference across the snubber becomes less than 35 kV. It means that the applied voltage across the snubber for shunt type is lower than that of series type. Therefore, the shunt type shows lower voltage across the IGBT than series type. Figure 3.7 (b) shows the equivalent circuits for PWM mode with IGBT ON. The IGBTs are modeled as a resistor. The IGBT can be considered as a short path, regardless of the compensation topologies, thus the equivalent circuit for two types can be thought identical each other. Figure 3.9 (a) shows the thyristor voltage waveforms without MOV across the thyristor. In the simulations, the MOV surge arrestor having same characteristic of that in the input side is implemented in the output side. If there is no arrestor, the output voltage will reach 140 kV due to the voltage boosting of the autotransformer. Figure 3.9 (a) shows that the voltage across the thyristor reaches over 17 kV, which exceeds the rating voltage of 6.5 kV thyristor. To suppress over voltage across it, a MOV is installed across the thyristor branch. It is clearly shown in Figure 3.9 (b) that the peak voltage across thyristor with the MOV is lower than 5 kV. The voltage across the thyristor shows positive and then changes to negative. Since the output voltage is limited by the MOV at the output side, the voltage across the thyristor, which is the voltage difference between the surge and the output voltage, has a positive value at the beginning of the surge. Even after the surge voltage becomes zero, there still exists

the surge current in the system. It results in the positive output voltage. Therefore, the voltage across the thyristor changes to a negative value.

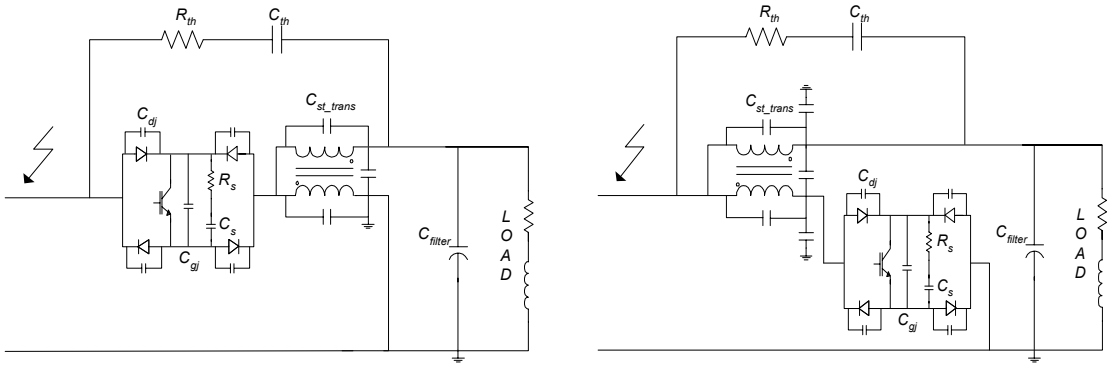
Figure 3.7 (c) shows the equivalent circuits during PWM mode with IGBT OFF. Figure 3.10 shows the voltage waveforms during this mode. Upper figures of Figure 3.8 (a) and (b) show the voltage across the IGBT, and bottom figures show the voltage across thyristor. From Figures 3.10 (b) for series type, it can be seen that without MOV across the thyristor, the voltage rises up around 17 kV, and the IGBT voltage also reaches almost 10 kV. In the case of shunt type, Figure 3.10 (a) shows that the maximum peak voltage is 17 kV and 7.8 kV for thyristor and IGBT, respectively. From Figure 3.10, it can be known that regardless of the compensation type, the voltages across the thyristor have the same peak values. Since the MOV at the output side clamps the output voltage at the same voltage levels for two compensation types, the magnitudes of the voltage across the thyristors are the same. Figure 3.11 (a) and (b) show the voltage waveforms of shunt type and series type, in which to suppress the over voltage across the thyristor, a MOV is attached in parallel with the thyristor branch. The initial voltage of the snubber capacitor is 4 kV, which is chosen from the assumption that the lightning surge occurs after the IGBT switch remains a certain period of turn-off. From Figure 3.11 (a) for shunt type, it can be known that the peak voltage of the IGBT and thyristor are lower than 6.5 kV. After implementing the MOV across the thyristor branch, the peak voltage across the IGBT becomes less than 6.5 kV. Since the MOV at the thyristor branch provides alternative current path during the surge, it results in less IGBT snubber current during the surge event.



(a) Bypass mode (thyristor on, IGBT off)

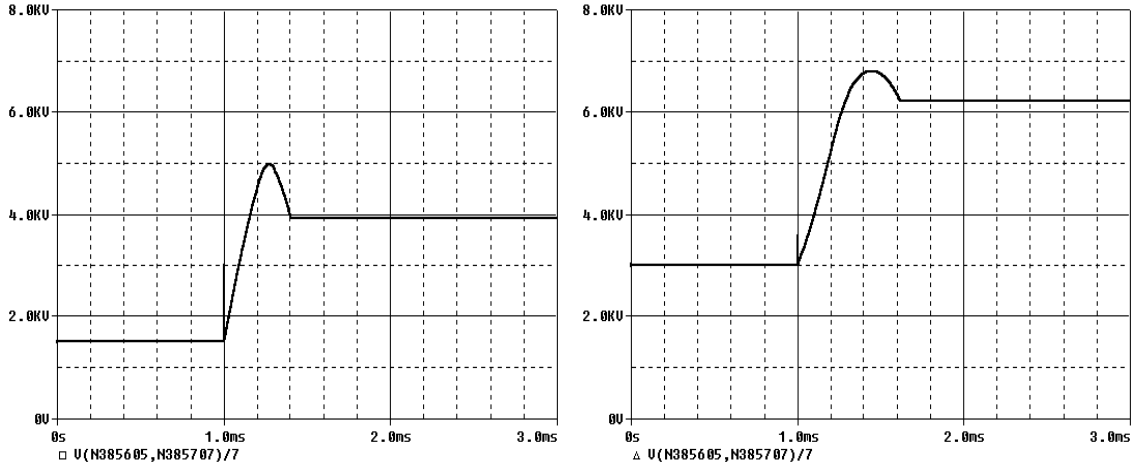


(b) PWM mode with IGBT ON



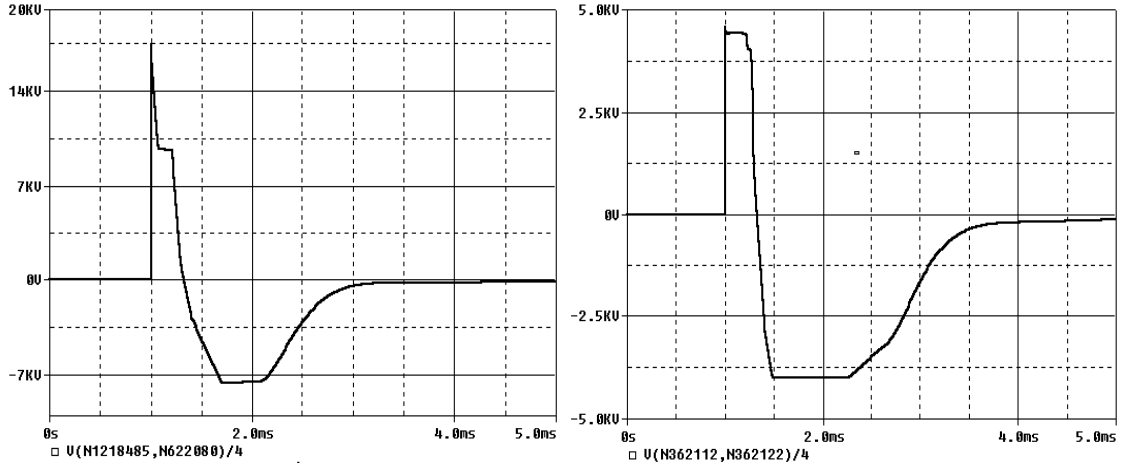
(c) PWM mode with IGBT OFF

Figure 3.7. Equivalent circuit for lightning surge simulations.



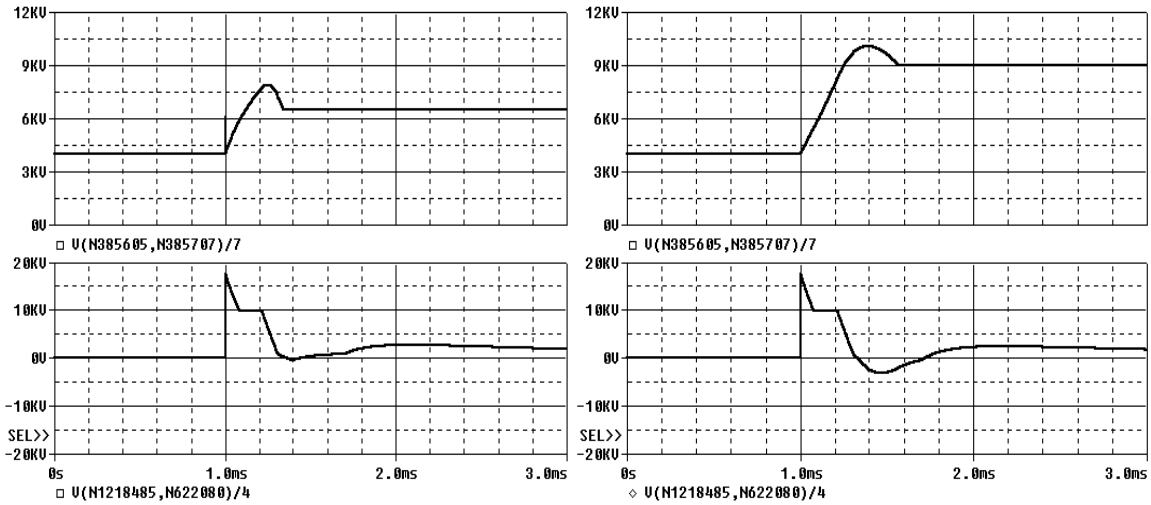
(a) Shunt type (b) Series type

Figure 3.8. Voltage waveforms across one IGBT switch block for the lightning surge during bypass mode (thyristor on, IGBT off).



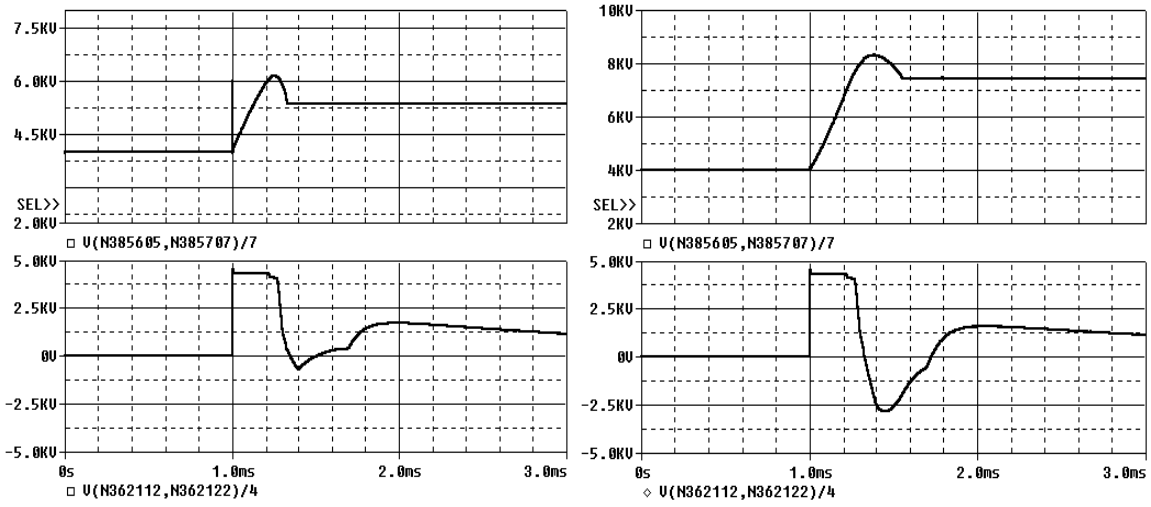
(a) Without MOV (b) With MOV

Figure 3.9. (a) Voltage waveforms across one thyristor block without MOV across the branch during PWM mode with IGBT ON, (b) Voltage waveforms across one thyristor block with MOV across it.



(a) Shunt type (b) Series type

Figure 3.10. Voltage waveforms across one IGBT switch block of the lightning surge during PWM mode with IGBT OFF (from the top-downwards voltage across IGBT and thyristor).



(a) Shunt type (b) Series type

Figure 3.11. Voltage waveforms across one IGBT switch block of the lightning surge during PWM mode (IGBT OFF) with MOV across thyristor (from the top-downwards voltage across IGBT and thyristor).

3.4 Chapter Summary

A novel configuration of a voltage sag mitigation device based on PWM switched autotransformer has been proposed. The proposed system consists of a PWM switch block, a bypass switch block, an autotransformer, a voltage controller, and filters. To reduce total system cost, only one PWM switch was implemented in the system. In addition, to increase the system efficiency and increase the short circuit capability, a bypass switch using thyristors was implemented. Serially connected PWM switch blocks and bypass switch blocks were used to withstand over voltage during the transient condition. It was shown that the switch block has an AC bridge configuration, which is able to conduct AC load current in both directions.

Two different schemes so called shunt type and series type have been suggested, and voltage distributions during lightning surges were examined by simulations. During normal condition, the series type has sufficient voltage safety margin (3 kV peak voltage for 6.5 kV rating IGBT). However, the lightning surge simulations showed that the voltage across the IGBT during surge condition exceeded the breakdown voltage of the IGBT. Simulations showed that a MOV was needed in parallel with the static bypass assembly to protect the thyristor from the voltage breakdown during lightning event that occurs while the proposed system is in PWM mode.

CHAPTER 4

DESIGN OF SYSTEM

The shunt type compensation method was chosen for this research in the previous chapter, based on the fact that the shunt type shows less voltage stresses during normal and surge conditions. Many design issues are involved in developing this research. This chapter explains each design issue starting from voltage detection methods.

4.1 Voltage Detection Methods

Voltage detection is important because it determines the dynamic performance of the proposed scheme. The magnitudes of the input and output voltages determine the PWM duty-cycle and the starting and the ending moment of compensation. Therefore, precise and fast voltage detection is an essential part of the voltage sag supporter. Several voltage detection methods have been documented for use in various voltage compensation schemes, which can be categorized as below:

i) Average method

ii) RMS detection method

iii) DQ transformation or positive-negative sequence detection method

iv) Peak detection method

v) Using signal processing

Among above methods, many approaches use the DQ transformation of the voltage in the synchronous reference frame [43]–[44], and another approach uses positive and negative voltage components for the input and output voltage waveforms. Signal processing techniques such as the Fast Fourier Transformation (FFT) and the Wavelet Transformation can be used to detect voltage sag [45]. However, to get accurate information of the voltage magnitude, the FFT can take up to one cycle of the fundamental frequency. Using the Wavelet transformation, it is possible to detect a sudden change of the supply voltage, however there is a difficulty of real-time implementing due to a large amount of data processing [45]. In the following section, the characteristics and problem with the DQ transformation are explained.

4.1.1 DQ Transformation for Voltage Detection

The DQ transformation theory has been used in motor drive applications for many years, and it can be adapted for detecting voltage sags. The values of DQ transformation are calculated using (4.1), in which three-phase values are transformed to stationary two-axis values V_{ds}, V_{qs}, and then these values are transformed to dq values in the rotating frame. Where, the angle θ is obtained by PLL (Phase-Locked Loop). Equation (4.1.a)

defines the transformation from three-phase system a, b, c to dq stationary frame. In this transformation, phase A is aligned to the q-axis that is in quadrature with the d-axis. The transformed values in the dq rotating frame can be obtained by (4.1.b). The theta (θ) is defined by the angle difference between the phase A to the q-axis.

$$T_s = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \quad \begin{bmatrix} V_{qs} \\ V_{ds} \end{bmatrix} = T_s \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.1.a}$$

$$T_r = \begin{bmatrix} \cos\theta & \sin\theta \\ \sin\theta & -\cos\theta \end{bmatrix}, \quad \begin{bmatrix} V_{qr} \\ V_{dr} \end{bmatrix} = T_r \begin{bmatrix} V_{qs} \\ V_{ds} \end{bmatrix} \tag{4.1.b}$$

If three-phase parameters such as currents and voltages are balanced, the value of the DQ transformation results in DC constant values. In addition, the resulting DC values make voltage controller design easier. Figure 4.1 shows three-phase voltages and their dq-axis values for the balanced voltage sag. Figure 4.1 (bottom) shows the resulting DQ values. It is clearly shown that regardless of the voltage sag, the value in d-axis remains zero, and the q-axis component instantaneously indicates the change of the voltage magnitude. The DQ transformation uses instantaneous values. Therefore, the detection time is much faster than other methods such as average, RMS, and peak detection. However, for the unbalanced voltage sag, this DQ transformation method does not show the instant change of DC values. The output of the DQ transformation has a 120 Hz ripple component, which is twice of the frequency of the source voltage. Figure 4.2

shows the voltage waveforms of the unbalanced three-phase system, in which only phase A has a voltage sag. The resulting DQ values, shown in Figure 4.1 (bottom), show 120 Hz ripples in both d-axis and q-axis value.

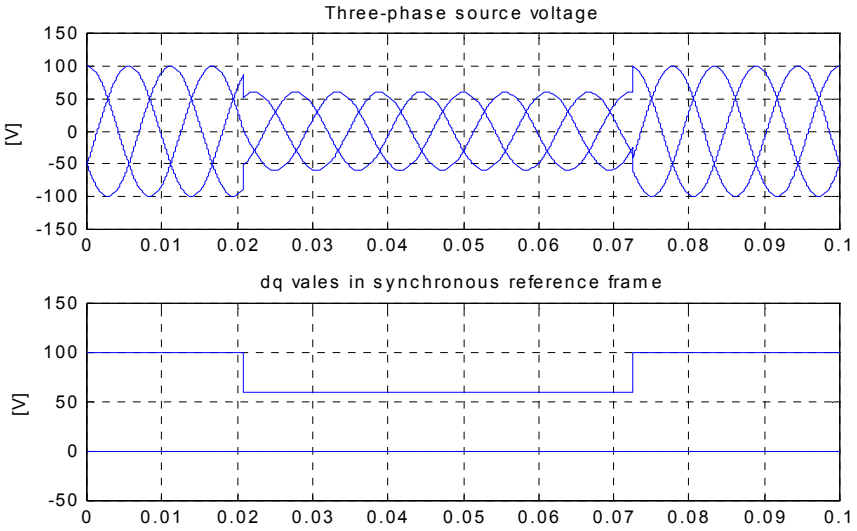


Figure 4.1. The result of DQ transformation of balance three-phase voltage.

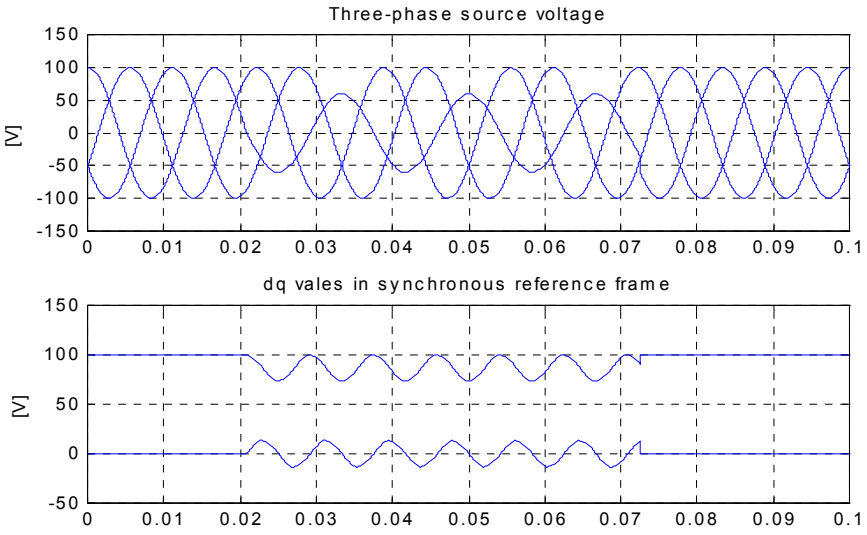


Figure 4.2. Resulting values of DQ transformation of unbalance three-phase voltage.

Another approach of measuring the voltage magnitude is to determine the components of positive and negative sequences of unbalanced three-phase system using (4.2).

$$T_{pn} = \frac{1}{3}\begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}, \quad \begin{bmatrix} V_p \\ V_n \end{bmatrix} = T_{pn}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{4.2}$$

and $a = e^{j\frac{2\pi}{3}}$

V_p and V_n represent instantaneous magnitude and angular position of the resultant voltage vectors of positive and negative components, respectively. For unbalanced three-phase system, it can be shown that the positive and negative sequences also have 120 Hz ripple components, and it can be explained as follows.

The measured voltage in the stationary frame can be expressed as (4.3), which has two rotating components that rotate in positive and negative directions with the synchronous speed. Where, V_{dq}^{p} and V_{dq}^{n} represent the voltage magnitude of positive and negative component, respectively.

$$V_{dqs} = e^{j\omega t}V_{dq}^{p} + e^{-j\omega t}V_{dq}^{n} \tag{4.3}$$

Multiplying $e^{j\omega t}$ and $e^{-j\omega t}$ to each component gives the following equation in the rotating frame.

$$\overline{V}_{dq}^{p} = V_{dq}^{p} + e^{-j2\omega t} V_{dq}^{n}$$

$$\overline{V}_{dq}^{n} = V_{dq}^{n} + e^{j2\omega t} V_{dq}^{p} \qquad (4.4)$$

In (4.4), it can be seen that the positive and negative components in the rotating frame have DC values and 120 Hz components. It is desirable to remove the 120 Hz ripple component and determine the DC value for these two components. To get the DC values, a 120 Hz notch filter is recommended to remove the 120 Hz ripple component from the positive and negative transformation [46] or a low-pass filter having its cutoff frequency lower than 120 Hz. The filtering using a 120 Hz notch filter or a low-pass filter cause delay in the voltage detection, hence it slows down the detection time, which results in delay in overall response time.

4.1.2 Peak Voltage Detection Method

The DQ transformation or the positive-negative transformation method offers a fast detection time for a three-phase balanced system. However, to get the DC component in the rotating frame for the unbalanced system, it is necessary to remove the 120 Hz ripple component, which makes the detection response sluggish.

To control and detect the voltage sag, the voltage compensator of this research requires only the peak values of input and output voltages. Therefore, a simple method called the "peak detection method" [47] is used. In addition, the DQ transformation needs three-phase information, while the peak detection method needs only a single-

phase value. It is necessary to mention that a low-pass filter having 300 Hz cutoff frequencies, which is needed for eliminating measurement noises, is attached in the sensing circuit. As previously mentioned, the filtering for DQ transformation causes detection delay. Comparing the detection time, it is found that the detection time of the peak detection method is nearly same as DQ transformation with a 120 Hz notch filter. The peak detection method is implemented as shown in Figure 4.3, and Equation (4.5) shows the peak detection method.

$$(V_m \sin \theta)^2 + (V_m \cos \theta)^2 = V_m^2 \qquad (4.5)$$

The process of measuring the peak magnitude can be explained as follows. The single-phase line-to-neutral voltage is measured, and the cosine value of this voltage is determined using a 90^o phase shifter. Assuming a fixed value (60 Hz) for line frequency, the 90^o-shifted value can be found by either an analog circuit or by digital signal processing. In this research, the 90^o-delayed value was obtained in the control program. Both components of voltage are squared and summed to yield V^2_m. Obtaining the square root of V^2_m results in the magnitude of the detected voltage. Figure 4.4 shows the voltage measurement using the peak detection method.

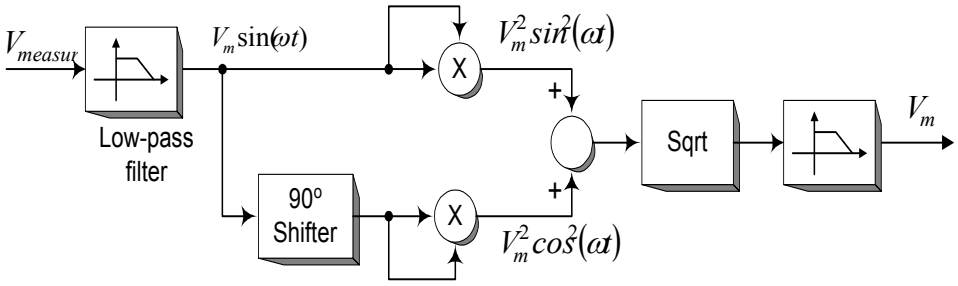


Figure 4.3. Voltage measurement using the peak detection method.

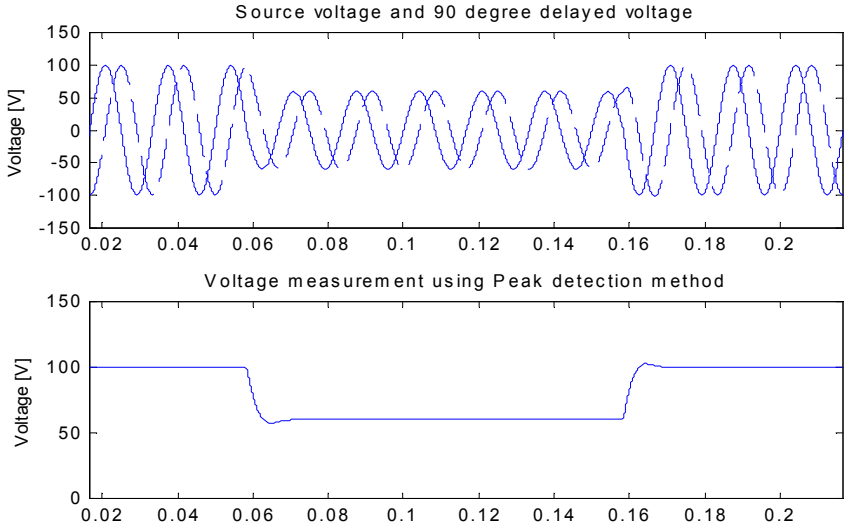


Figure 4.4. Measured voltage waveforms using the peak detection method.

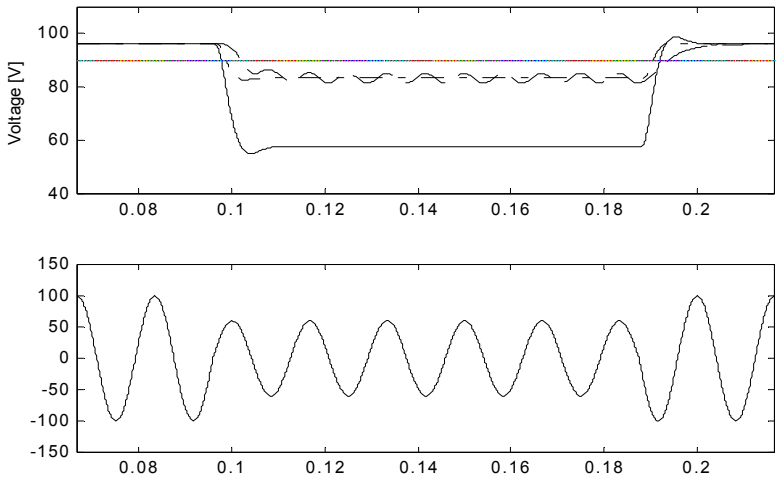
Figure 4.5 compares the detection time of voltage measurement, in which following three configurations are implemented.

Case 1: Peak detection method with a 2nd order low-pass filter having 300 Hz cutoff frequency

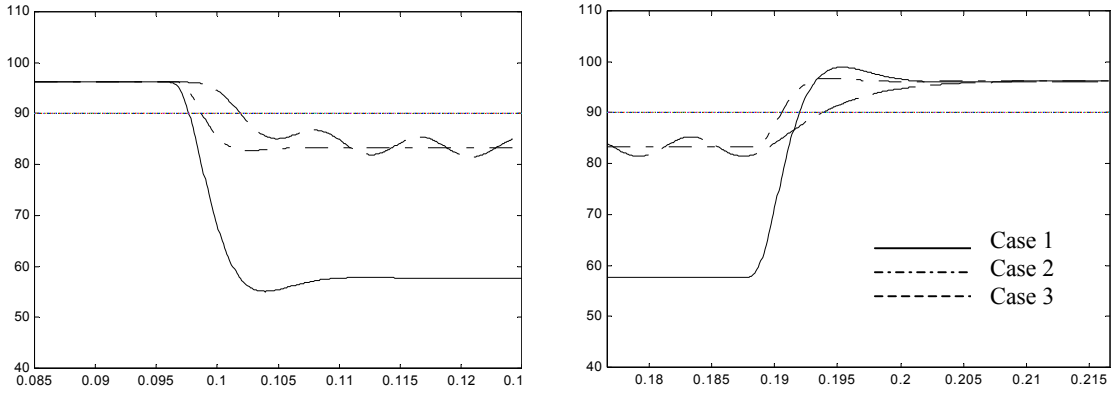
Case 2: DQ transformation with a 2nd order low-pass filter having 50 Hz cutoff frequency

Case 3: DQ transformation with a 120 Hz notch filter

The extended waveforms during starting and recovering voltage sag are shown in Figure 4.5 (b) and (c), respectively. The normalized voltage has a 40% voltage dig during sag event. The peak magnitude of voltage is slightly lower than the normalized voltage due to the attenuation caused by the low-pass filtering. From the figure, it can be shown that the measured value by the peak detection method changes between 100 to 74, which follows the peak value of the voltage. However, the measured value of the DQ transformation changed between 80 to 100, which is mean value of the variation during the voltage sag. In case 3, even a 2nd order low-pass filter is used, the measured value has a significant 120 Hz ripple component. From the extended waveforms, it can clearly be seen that the detection time of the peak detection and the DQ with a notch filter is almost same. In the simulation, the angular position of the voltage for the DQ transformation is obtained without errors. However, it should be mentioned that if there exists a error in detecting the angular position, the calculated peak value of voltages is decreased due to the misalignment between the stationary and the rotating frames.



(a)



(b) (c)

Figure 4.5. Comparison of voltage detection time for various detection methods.

4.2 Voltage Controller

The voltage controller based on a Proportional Integral (PI) controller is shown in Figure 4.6. The input of the PI controller is the voltage error between the voltage reference and the load voltage. K_p is the proportional gain, and K_i is the integral gain.

To avoid the wind-up phenomenon, the difference between the limiter output and input is fed back to the PI controller input, which provides an anti-wind-up scheme. The integral action accumulates the error and causes the wind-up phenomenon. If the wind-up phenomenon is not corrected, a large voltage overshoot can occur at the moment of voltage recovery, which can be explained as follows. When the voltage measurement circuit detects the recovery of the input voltage, the output of the PI controller should decrease as quickly as possible to reduce the amount of voltage overshoot. In the case where the PI output (duty-cycle) reaches its maximum value, but the voltage error is not zero, the output of integral controller will continue to increase. When the controller detects the recovery of the input voltage, the PI output will decrease, but the PI reference output increases too much; it takes time to reduce the accumulated error.

To achieve faster response, a feed-forward scheme is used. The difference between the voltage reference and the measured input voltage is added to the output of the PI controller. For the incoming voltage sag, the output of the feed-forward instantaneously becomes positive, and this feedback is added to increase the actual duty-cycle of the IGBT switch, and vice versa. The feed-forward control scheme gives the base value of the duty-cycle. The feed-forward control is an effective way to speed up the response time at the beginning of the voltage sag and reduce the overshoot at the moment of voltage recovery.

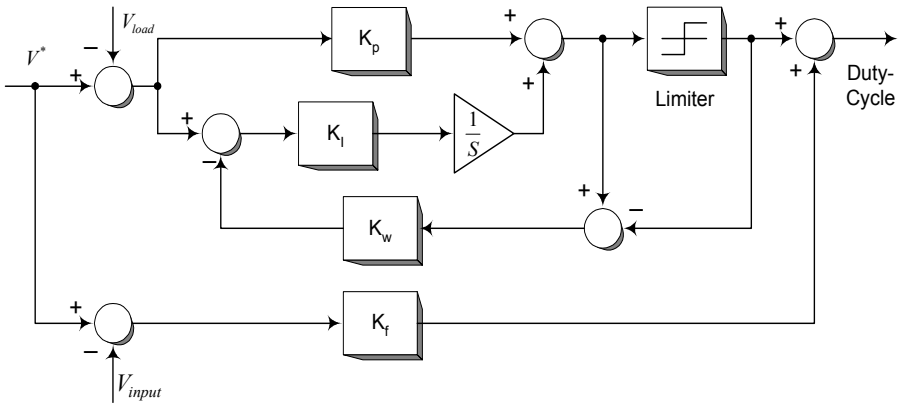


Figure 4.6. Output voltage controller based on PI controller.

4.3. Snubber Design

4.3.1 Role of Snubber

The AC switch in a bridge configuration was shown in Figure 3.4. The bridge has a turn-off snubber circuit across the IGBT switch that consists of a resistor and a capacitor. The snubber suppresses the peak voltage across the IGBT switch when the IGBT turns off. When the IGBT switch turns off, the current flowing in the IGBT in the on-state instantly diverts to the snubber circuit. The energy stored in the current path is transferred into the snubber capacitor and resistor.

To determine the snubber values, the system parameters should be known first and are shown in Table 4.1. The normal current of the system is 60 A RMS, and its maximum value is chosen as 120 A RMS. The line-to-line voltage is 25 kV RMS, hence the peak of phase voltage is about 20 kV.

In addition, as mentioned in the previous chapter, seven serially connected switch blocks are used. In this research, a 400 A / 6500 V rating IGBT switch is used. Even the break down voltage of the IGBT is 6500 V, the IGBT manufacturer recommends that the maximum voltage across the IGBT should not exceed 5000 V because each component of the snubber has thermal variation and the tolerance of components especially snubber capacitors. The values for the snubber resistor and capacitor are chosen to prevent the peak voltage across the IGBT from exceeding 5000 V during the IGBT off-state.

Table 4.1 Parameters of the system.

Phase	3 ϕ	Maximum Load Current	120 A
Input Voltage	25 kV	Load	2.5 MVA
Power Factor	0.8	Maximum operation time	3 seconds

4.3.2 Selection of the RC Values

To determine the snubber resistor and capacitor components, the value of the resistor is examined at first. The resistor has two roles. One is to dampen the energy transfer to the capacitor when the IGBT turns off, and the other is to limit the capacitor discharge current when the IGBT turns on. From the IGBT datasheet, it can be found that the maximum peak repetitive current is 800 A. From the second role for limiting the initial discharging current of the capacitor, the resistor value is selected by from 5000 V / 800 A = 6.25 Ω, so that the resistor value is chosen to be 7 Ω.

At first, the capacitor value is selected based on the 7 Ω resistor. The worst condition, i.e., the condition of the highest snubber voltage, occurs when the load current is greatest, and maximum IGBT turn-off time, i.e., the shortest on-time. In other words, the voltage of snubber capacitor increases during the IGBT is turned off because the energy is transferred or charged to the snubber capacitor during turn-off time and will be charged rapidly for the maximum load current.

Using the simplified circuit shown in Figure 4.7 (a), firstly the minimum IGBT duty-cycle is determined. In Figure 4.7, the AC switch is shown as one IGBT switch, and the block marked "snubber" represents the RC snubber circuit. When the IGBT is on, the load voltage equals $2 \cdot V_{in}$, and the load voltage is $2 \cdot V_{in} - 2 \cdot V_{snub}$ when the IGBT is off (where V_{snub} is the voltage across the snubber and D represents the duty-cycle). Assume that the source impedance L_s is ignored for simplicity. Then, the average output voltage can be given as (4.6).

$$\begin{aligned} V_{out} &= D \cdot V_{on} + (1 - D) \cdot V_{off} \\ &= D \cdot 2V_{in} - (1 - D) \cdot 2V_{in} \cdot \tfrac{1}{2} = 2V_{in}(\tfrac{3}{2} D - \tfrac{1}{2}) \end{aligned} \tag{4.6}$$

In (4.6), the average voltage during IGBT turn-off is calculated as V_{in}. The value of V_{in} is determined by the shape of the snubber voltage shown in Figure 4.7 (b). During the turn-off period (*1-D*), the load voltage is $2 \cdot V_{in} - 2 \cdot V_{snub}$, because the voltage having the magnitude of V_{in}–V_{snub} at the primary side of the transformer is boosted twice by the 1 to 1 autotransformer. Assume that the input voltage is constant during turn-off time as the

IGBT switching frequency is high enough. Where, the snubber voltage V_{snub} is not a constant value, which varies during the IGBT off-state period as shown in Figure 4.7 (b). V_{snub} has a shape that the initial voltage drop equals about V_{in}, and the maximum peak value should be less than 5000 V.

In this research, the system independently controls the single-phase voltage, which has 20 kV peak-to-peak single-phase voltage corresponding to the 25 kV line-to-line RMS voltage. It is assumed that seven serially connected AC switches, maximum 120 A load current, and predetermined 7 Ω snubber resister. The initial voltage drop in equivalent snubber value can be calculated as $120 \times \sqrt{2} \times 2 \times 7 \times 7 = 16.7$ kV, which is similar to a 90% of nominal voltage (0.9×20 kV ≈ 18 kV), where it is considered that V_{in} has a 10% voltage sag. In the above calculation, the worst case is assumed that the peak value of the maximum load current of 120 A ($120 \times \sqrt{2}$), and as the current of input side in the autotransformer is twice the load current, the peak load current is multiplied by two in the equation. Also, the first seven comes from the 7 Ω, and the second seven comes from seven switches in series.

The highest snubber voltage occurs at the condition of the minimum on time, in other words maximum turn-off time. When the input voltage has minimum voltage sag, which generates this condition. In this system, the minimum allowable voltage is 0.9 pu (per unit) so that the voltage having 90% voltage sag is chosen as the worst case.

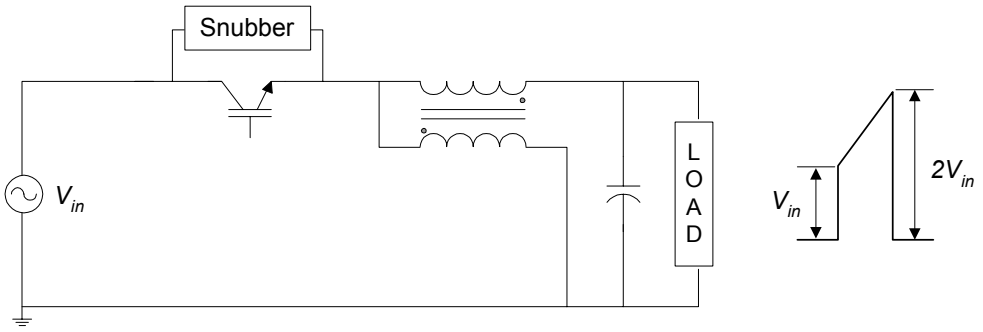
In Figure 4.7 (b), the highest voltage has a $2V_{in}$. Each switch needs to have less than 5000 V across it. Therefore, the worst case acceptable peak value for the entire series of

switches is 7 × 5000 = 35 kV, which is similar to $2V_{in}$ in the case of the 10% voltage sag condition (2 × 0.9 × 20 kV ≈ 36 kV ≈ $2V_{in}$).

The average voltage value of $2 \cdot V_{in} - 2 \cdot V_{snub}$ is equal to $-2 \cdot V_{in} \times 1/2$. From Figure 4.7 (b), it can be known that the snubber voltage increases from V_{in} to $2V_{in}$ during the turn-off, so that the initial value of $2V_{snub}$ equals $2V_{in}$, and the final snubber value is $2V_{snub}$, which equals $4V_{in}$. As this value is subtracted from $2V_{in}$, which remains the triangular snubber voltage shape with the $-2V_{in}$ peak value. Therefore, the average value becomes $-2 \cdot V_{in} \times 1/2$.

The minimum turn-on time is determined from (4.6), which gives a 75% duty-cycle. In cases where the 1.5 kHz switching frequency and D = 75%, the IGBT is in the on-state for 500 μs and in the off-state for approximately 170 μs. The approximate capacitance value of the snubber is determined by two conditions. The first condition is that the peak voltage during the IGBT off-state should be lower than 5000 V, and the second condition is that the capacitor voltage needs to discharge lower than 10% of its charged value during the IGBT turn-on. When the minimum IGBT on-state time is greater than 2.5 × RC, which means 500 μs > 2.5 × RC → C < 28.5 μF, the second condition is satisfied, which results in 20 μF snubber capacitor.

A 7 Ω resistor and a 20 μF capacitor are derived only from the condition of restricting the initial discharge current and discharge time of snubber circuit, respectively. Therefore, it is necessary to check whether or not the selected snubber values can prevent the IGBT voltage from exceeding 5000 V.



(a) (b)

Figure 4.7. Simplified diagram of the shunt voltage compensator.

4.3.3 Equivalent Circuit during IGBT turn-off

A diagram of the equivalent circuit when the IGBT is off is shown in Figure 4.8, and from this diagram the voltage and current relation can be expressed as (4.7).

$$V_{sag} = 2L_s \frac{di_{load}}{dt} - 2R_{snub} \cdot i_{load} - \frac{2}{C_{snub}} \int i_{load}\, dt + V_2 - L_2 \frac{di_{load}}{dt} - R_2 i_{load}$$

$$V_{in} = 2L_s \frac{di_{load}}{dt} + 2R_{snub} \cdot i_{load} + \frac{2}{C_{snub}} \int i_{load}\, dt + V_1 + L_1 \frac{di_{load}}{dt} + R_1 i_{load} \qquad (4.7)$$

Where V_1 and V_2 are the voltages of the ideal transformer in the primary N_1 and secondary N_2. R_1 and R_2 are the primary and secondary resistance, respectively, L_1 and L_2 are the primary and secondary leakage inductance, respectively, and L_s is the source inductance. By manipulating (4.7) with the assumptions that $V_1 = V_2$, $R_1 = R_2$, and $L_1 = L_2$

(because of the 1 : 1 turns ratio transformer), (4.8) can be derived. A diagram of the equivalent circuit with equivalent parameters is shown in Figure 4.9.

$$V_{in} - V_{sag} = 4L_s \frac{di_{load}}{dt} + 4R_{snub} \cdot i_{load} + \frac{4}{C_{snub}} \int i_{load} dt + 2L_1 \frac{di_{load}}{dt} + 2R_1 i_{load} \qquad (4.8)$$

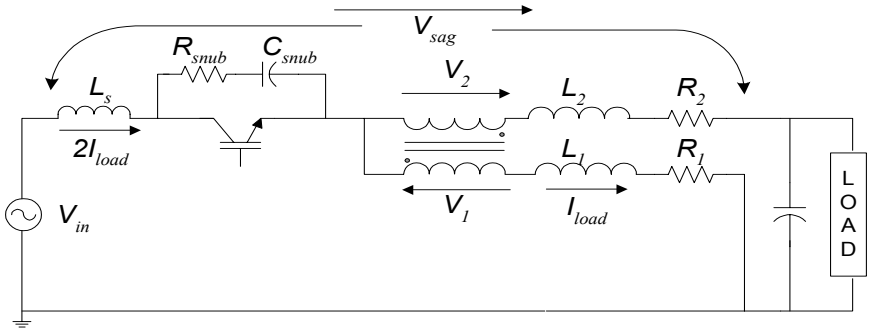


Figure 4.8. Equivalent circuit diagram during the IGBT is off.

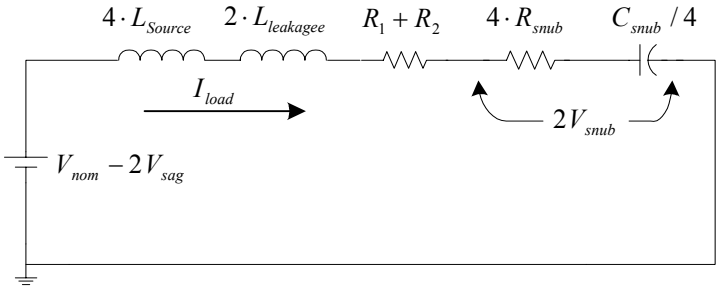


Figure 4.9. Simplified equivalent circuit during IGBT turn-off showing equivalent parameters.

The equation for the snubber voltage can be derived from Figure 4.9, which is a second order equation, hence there exist two possible cases, under-damped and over-

damped. From the previously determined values of R = 7 Ω and C = 20 μF, it is known that the circuit response is under-damped. The snubber capacitor voltage can be found as (4.9), where θ and K are determined by the initial conditions. The initial conditions are as follows. The initial snubber current is twice the load current, and the initial snubber capacitor voltage is zero with the assumption that most capacitor energy is discharged when the IGBT is on.

$$v_c(t) = V_s + Ke^{-at} \cdot \cos(\omega_d t - \theta) \qquad (4.9)$$

where, $\theta = \tan^{-1}\left(\frac{C\alpha V_s - I_{load}}{C\omega_d V_s}\right)$, $K = -\frac{\sqrt{C^2 V_s^2 \omega_0^2 - 2I_{1oad} C\alpha V_s + I_{load}^2}}{C\omega_d}$

$$\alpha = R_{tot} \Big/ (2 \cdot L_{tot}), \omega_0 = \frac{1}{\sqrt{L_{tot} \cdot C_{tot}}}, \omega_d = \sqrt{\omega_0^2 - \alpha^2},$$

$$V_s = V_{nom} - 2V_{sag}, \; L_{tot} = 4 \cdot L_s + 2 \cdot L_{leakage},$$

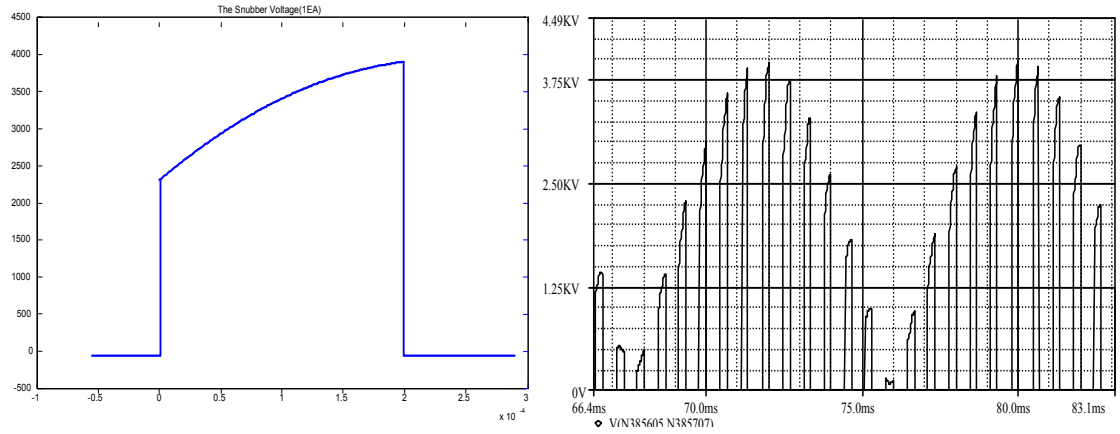
$$C = C_{snub}/4, \text{ and } R_{tot} = 2 \cdot R_1 + 4 \cdot R_{sunb}$$

The snubber voltage is expressed as (4.10) that is summation of the voltages in the resistor and the capacitor. The magnitude of the source voltage is $V_{nom} - 2V_{sag}$, where V_{nom} = 20 kV (nominal voltage) and V_{sag} = 2 kV. V_{sag} represents the magnitude of voltage dip. The maximum snubber voltage occurs when the IGBT turn off time is the longest, in other words, minimum voltage sag condition or minimum turn-on time. In this research, the minimum allowable sag is 10%, which is equal to 2 kV.

$$v_{snub} = \left[i(t) \times R_{snub} + v_c(t) \right] / 2$$

$$i(t) = CKe^{-\alpha t} \left[-\alpha \cos(\omega_d t - \theta) - \omega_d \sin(\omega_d t - \theta) \right] \qquad (4.10)$$

The voltage across each snubber is shown in Figure 4.10 (a). Figure 4.10 (b) shows one cycle waveform simulated using PSPICE®. Because a sinusoidal current flows through the AC switch, the envelope of the voltage waveform across the switch is also sinusoidal. The peak voltage occurs when the load current through the switch is at its maximum value. From the figures, it can be known that the peak voltage is below 5 kV using the selected resistor and capacitor values.



(a) (b)

Figure 4.10. Voltage across the IGBT using parameters of R_S = 7 Ω, C_S = 20 μF, L_s = 10 mH, and $L_1 = L_2$ = 20 mH.

4.4 Design of Output Filters

To reduce harmonic components of the output voltage, two filters are used. One is a notch filter and the other is a capacitor filter. Usually less than 5% THD (Total Harmonic Distortion) of the voltage is required in power system. To select the filter values, firstly the equivalent circuit is derived as shown in Figure 4.11. In Figure 4.11, the total effective inductance L consisting of the source impedance and the leakage inductances of the transformer represents $4L_{source} + 2L_{leakage}$. The PWM effect is included in the source voltage as shown in Figure 4.11 (beside source voltage), in which the envelope of the voltage has the magnitude of $2V_{in}$, and during IGBT off times, the voltage has a magnitude of twice that of the snubber voltage is subtracted from $2V_{in}$.

From Figure 4.11, it can be observed that the combination of the effective inductance L and the output capacitor filter named C_{filter} form a low-pass filter. As the source and leakage inductance work as a low-pass filer, it seems large source impedance is preferred to reduce the harmonics. The leakage inductance helps to reduce the harmonics, but the source inductance does not. Because the source voltage can have a significant voltage distortion due to the voltage change by current ripples in the source impedance, and the voltage distortion will increase as the source impedance goes higher. The notch filter with a center frequency of the PWM switching is added to reduce harmonics, especially the PWM switching harmonics; it consists of a resistor, an inductor, and a capacitor in series. The impedance of the filter is given by (4.11).

$$Z = R + j(\omega L - \frac{1}{\omega C}) \qquad (4.11)$$

The LC resonance frequency, occurring when the imaginary part is equal to zero, $f = 1/2\pi\sqrt{LC}$ is tuned to the PWM switching frequency. It is possible to have many combinations of the inductor and the capacitor, which is tuned to the resonance frequency. However, the frequency response of the notch filer is different from each other for various combinations of the inductance and capacitance. To select the capacitor value of the notch filter, the common design rule such as generally the capacitor kVA chosen to 25%–30% of the total kVA rating is considered. Since the output filer is always energized regardless of the operation mode either PWM mode or the bypass mode, it is desirable that the output capacitor has a lower capacitance. The capacitor reactive power (VAR) is given by (4.12).

$$VAR = \frac{V^2}{X} \tag{4.12}$$

Using (4.12), the total capacitance is obtained by (4.13), where V = 15 kV, frequency = 60 Hz, 0.3 from 30%, and 2.5 MVA for three-phase VA. In the calculation, 2.5 MVA is divided by three to get a single-phase VA.

$$C = \frac{1}{2\pi \cdot 60} \div \frac{(15\times 10^3)^2}{2.5\times 10^6 \times \frac{0.3}{3}} \cong 3\mu F \tag{4.13}$$

There exist two capacitors in the output filters. One is the main capacitor filter, and the other is the capacitor in the notch filter. The notch filter is capacitive below the center frequency of the filter and inductive above the center frequency. At 60 Hz, since the notch filter works as a capacitor, it can be considered that there exist two parallel-connected capacitors. Therefore, the total 3 μF capacitance is equally divided. The main capacitor filter and the capacitor in the notch filter each have a capacitance of 1.5 μF. The bode diagrams of the notch filer and total system, which has a 10 mH source impedance and 20 mH leakage inductance, are shown in Figure 4.12 (a) and (b), respectively. Figure 4.12 (b) shows that the output filter consisting of the capacitor and the notch filter has a low-pass filtering effect whose cutoff frequency exists around 300 Hz and provides a shunt path for the frequency at 1.5 kHz of the IGBT switching frequency.

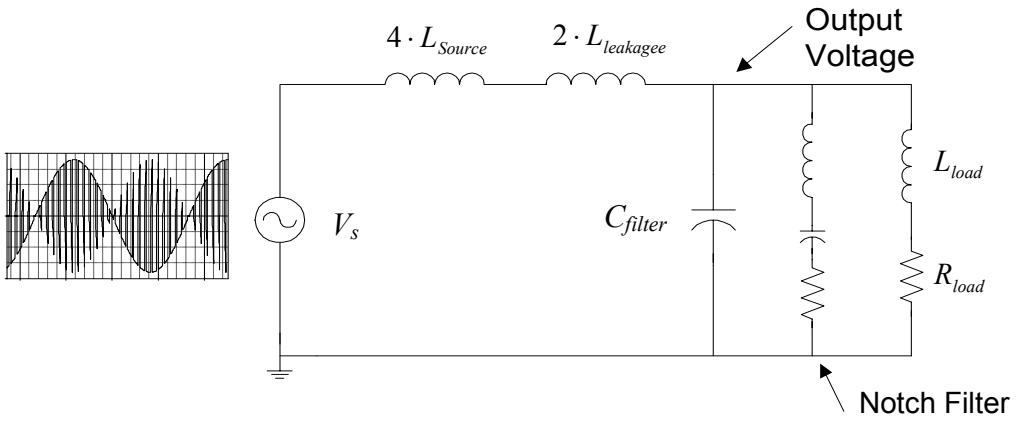
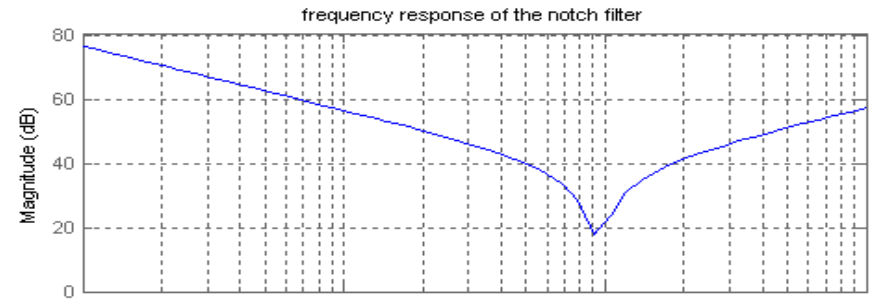
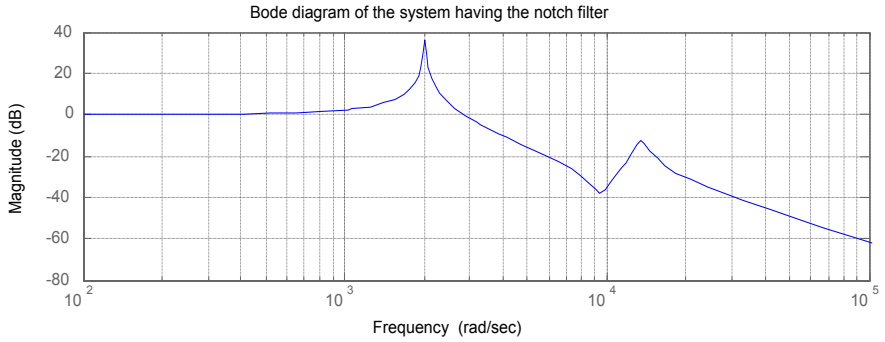


Figure 4.11. Equivalent circuit for selecting filter values.



(a)



(b)

Figure 4.12. Bode diagrams: (a) notch filter and (b) system having the notch filter and capacitor filter.

4.5 Thyristor Commutation Scheme

4.5.1 Thyristor Commutation Logic using Thyristor Current and Input Voltage

The thyristor is on during the normal voltage condition, connecting power from the input to the load. To get a fast dynamic response, the static bypass switch is turned off as soon as the voltage controller detects a sag condition. In other words, the IGBT should be turned on as fast as possible to regulate the output voltage to avoid producing a worse

voltage sag condition on the load. However, the thyristors are not self-commutable devices, i.e., they cannot be turned off by their gate signals.

There are two ways to turn off (commutate) thyristors. They can be turned off by either forced commutation or natural commutation. In forced commutation, the commutation logic or circuit imposes a reverse voltage bias across thyristors, which turns them off within a few microseconds. In natural commutation, the thyristor naturally reaches the off-state after the current in the thyristor becomes zero. In this research, the thyristor commutation method is determined by the polarities of the input voltage and thyristor current. The commutation logic is explained as follows.

The arrow in Figure 4.13 shows the direction of positive current flow. It is assumed that the input voltage is positive and a normal voltage condition exists. When a voltage sag event occurs, the voltage controller commands the thyristor gating to stop and commands the IGBT to initiate PWM switching. As the IGBT begins switching, the voltage at point ② is higher than the input voltage at point ① (because of the voltage boosting by the autotransformer). Thus, reverse bias is applied across the thyristor, and it turns off quickly. This means that turning-on the IGBT forces commutation of the thyristors if the input voltage and the thyristor current are both positive, i.e., they have the same polarity.

However, in the case of a negative voltage and a positive current (i.e., different polarities), turning on the IGBT causes more forward voltage bias to the thyristor because the voltage at point ② is lower than that of point ①. Hence, turning on the IGBT cannot commutate the thyristor when polarities are different. Therefore, once a voltage sag

event occurs and the thyristor gate signals are removed, the IGBT gate signal should remain in the off-state until the thyristor current becomes zero.

The commutation logic for the current flowing in the negative direction is explained in the same manner. The commutation logic can be summarized as follows:

- Turn on the IGBT if the polarities of the thyristor current and the input voltage are the same.
- Keep the IGBT off, if the polarities are different and begin PWM after the thyristor current becomes zero.

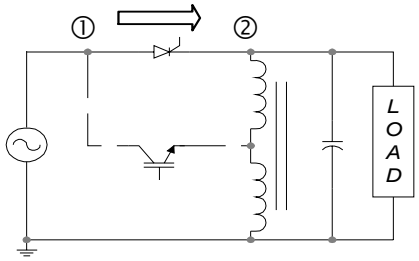
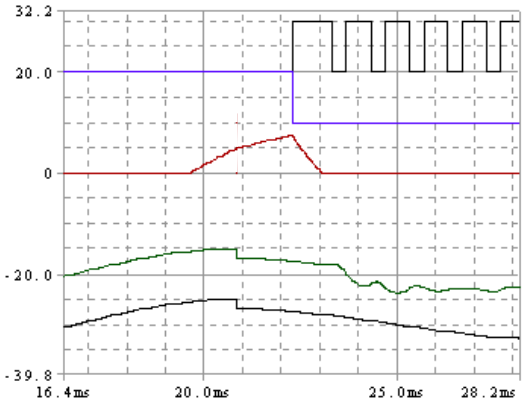


Figure 4.13. Commutation scheme showing the positive thyristor current.

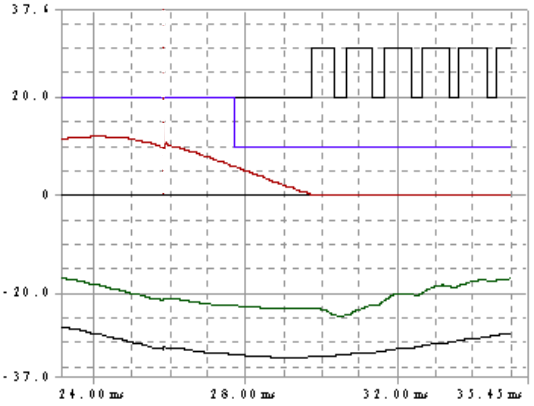
There exist four different cases according to the polarity of the current and voltage, for instance positive voltage and negative current, or positive voltage and positive current. In Figure 4.14 (a)–(d), from top the IGBT gate signal, the thyristor gate signal, the thyristor current, the input voltage and the load voltage are shown. For the simulation, a 100% duty-cycle of thyristor gate signal is used. If thyristors are latched, they can remain on-state without gate signals. Therefore, after latching it is not necessary

to generate the gate signals of the thyristors. However, to simplify the control logic, the thyristor gate signal that has a certain duty-cycle is continuously fired in this study.

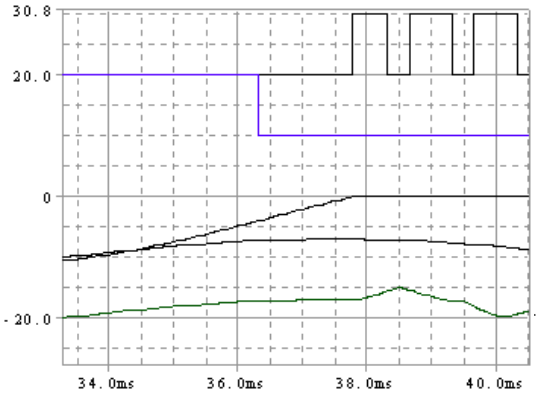
It is clearly shown in Figure 4. 14 (a) and (d) that in cases of the same polarity either positive or negative, turning on the IGBT makes forced commutation, while for the different polarity as shown in (b) and (c), natural commutation is carried out.



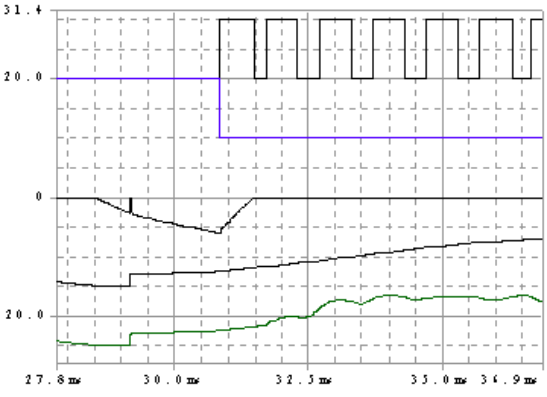
(a) Positive current and positive voltage



(b) Positive current and negative voltage



(c) Negative current and positive voltage



(d) Negative current and negative voltage

Figure 4.14. Thyristor commutation scheme for four different cases (from the top-downwards IGBT gate signal, thyristor gate signal, thyristor current, input voltage, and load voltage).

4.5.2 Thyristor Commutation Logic using Input Current and Input Voltage

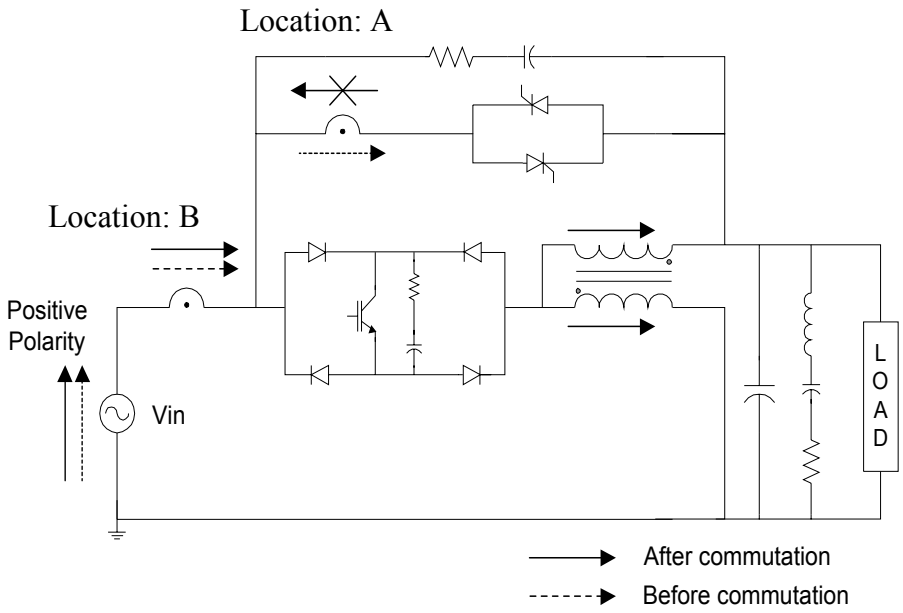
The thyristor commutation logic explained earlier needs a current sensor in the thyristor branch to check the polarity of the thyristor current. When the current sensor is present in the thyristor branch (Location: A), it should have a voltage-isolation rating that can withstand high input voltages such as 20 kV peak to peak for the input voltage of this proposed system. In this voltage sag configuration, there exists a well-isolated bushing terminal that serves as the input power terminal for the user. In power distribution systems, utilities commonly use an inexpensive 600 V AC-rated current sensor at the base of the input power terminal (Location: B) to sense current in their applications. If the current sensor can be moved from the thyristor branch to the input terminal, it will enable the use of an inexpensive current sensor in this application as well. Therefore, it is necessary to determine the commutation logic using the input current.

The commutation logic can be explained using Figure 4.15. Assume that the input current polarity is positive. Similar to the commutation logic explained earlier, when the polarities of the input current and input voltage are the same, turning on the IGBT imposes a reverse bias across the thyristor. In the case of different polarities, the commutation logic can be explained as follows. First, assume that the input voltage is negative, and the input current flows through the thyristor with positive polarity. When the voltage controller detects the voltage sag event, the thyristor gating is stopped and the IGBT gating is kept off because turning on the IGBT cannot turn off the thyristor. With the elimination of the thyristor gating, the positive thyristor current (same as the input current) will naturally become zero. The input current will then continue to flow (even

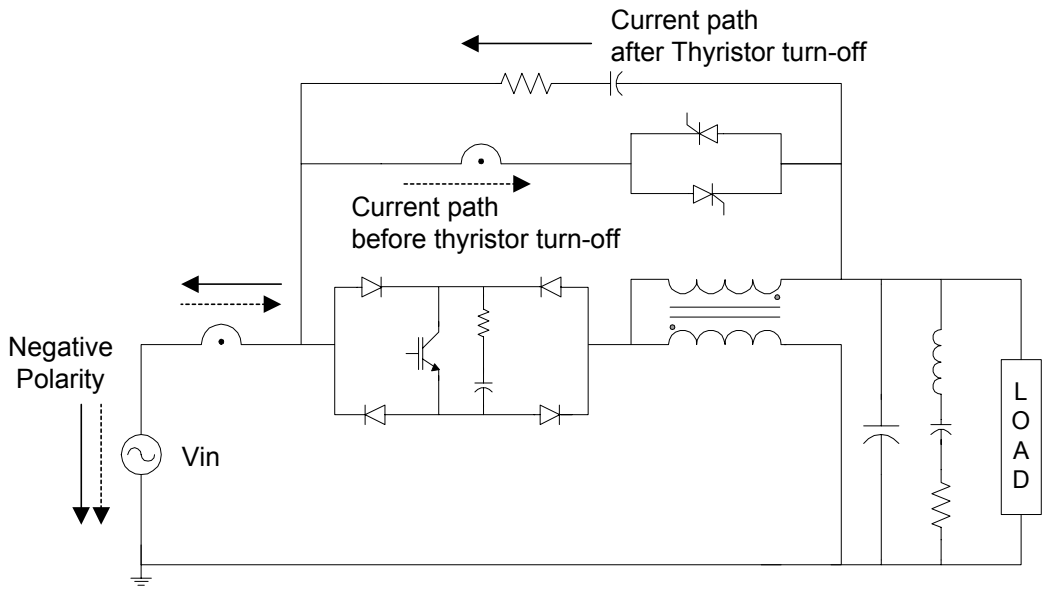
though the thyristors is off) through the thyristor snubber circuits. This means that the polarity of the input current becomes negative, i.e., the polarity of the input voltage and the input current become the same.

In the previous commutating logic, which is based on actual thyristor current, it is necessary to check whether or not the thyristor current becomes zero before starting IGBT switching. In this commutation logic (based on the input current), it becomes an equivalent condition to check whether or not the current and the voltage have the same polarity before initiating IGBT switching. Therefore, the commutation scheme can be summarized as a simple logic.

- Start PWM after the polarity of the input current and polarity of the input voltage become the same.



(a) Same polarity



(b) Different polarity

Figure 4.15. Showing the relation of the input current and the thyristor current to use the input current for the thyristor commutation logic.

4.6 Simulation Results

To verify the validity of the proposed system, simulations are performed using PSPICE under various voltage dip and swell conditions. Figure 4.16 shows the input voltage and the output voltage waveforms for the input voltage having a 20% voltage sag. The nominal input voltage is 20 kV peak to peak, and the load current is 120 amperes. The sag condition begins at 41.7 ms and stops at 135 ms. From Figure 4.16, it can be seen that the output voltage is well regulated with a nominal 20 kV peak to peak by the proposed scheme.

The voltage waveforms for the input voltage having a 40% voltage sag are shown in Figure 4.17. The output voltage for the 40% sag condition has a lower ripple than the 20% sag case. The duty-cycle of a 40% voltage sag is higher than that of 20%, so that the current ripple of the input current becomes less, which results in lower voltage ripple. From the figure, it can be shown that the output voltage becomes the desired 20 kV within a half cycle. There exists a voltage overshoot at the instant of voltage recovery caused by the detection delay in the voltage measurement. The delay in the voltage detection time is proportional to the magnitude of the voltage dip. Therefore, the deeper voltage dip the higher voltage overshoot.

Figure 4.18 shows the voltage waveforms for a 20% voltage swell. The input voltage swell condition starts at 41.7 ms and stops at 135 ms. The figure shows that the output voltage is well regulated with the proposed system. Even the proposed system focuses on the voltage sag mitigation, this simulation result shows that the proposed system has a excellent control response of the voltage swell condition as well.

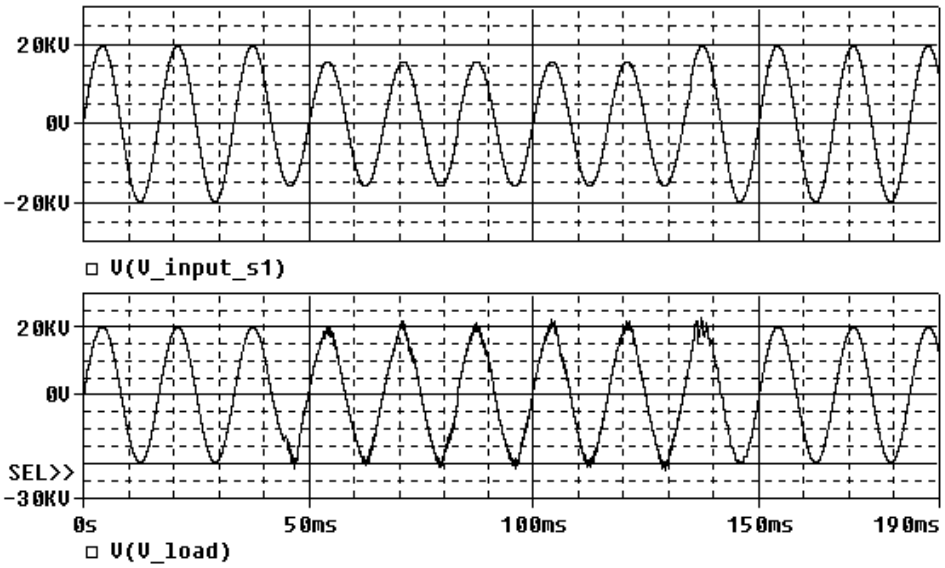


Figure 4.16. Output voltage waveform when the input voltage has 20% sag.

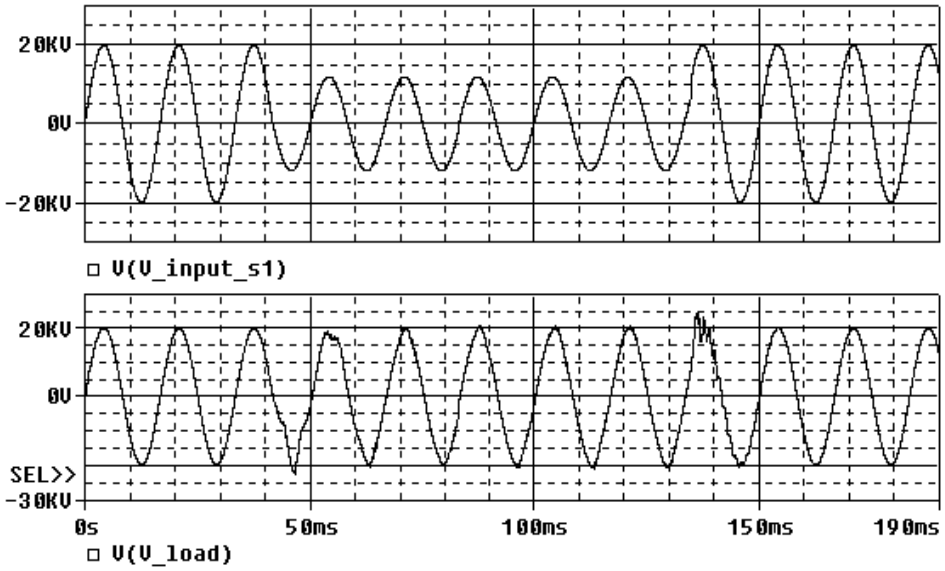


Figure 4.17. Output voltage waveform when the input voltage has 40% sag.

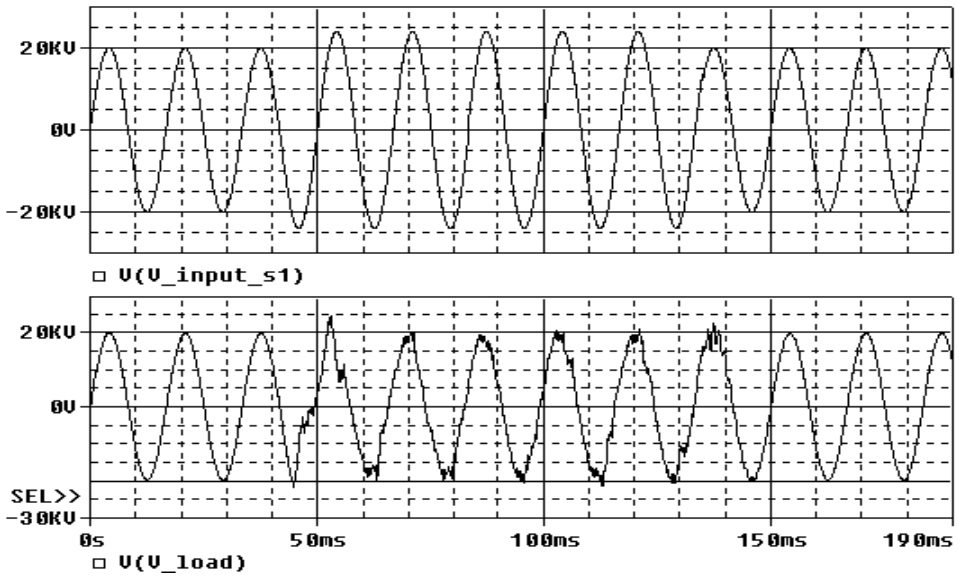


Figure 4.18. Output voltage waveform when the input voltage has 20% swell.

4.7 Chapter Summary

In this chapter, various design issues for the proposed system were presented. At first, existing voltage detection methods were evaluated, and the peak detection method has been selected based on the evaluation of each method. Among existing methods, it was shown that the method relying on the DQ transformation requires three-phase voltage information, and the output of the DQ transformation has 120 Hz ripples in the case of an unbalanced three-phase supply. The voltage detection time of the peak detection method was almost same as that of the DQ transformation with a 120 Hz notch filter due to the delay associated to a low-pass filter in the voltage measurement and the notch filter.

The voltage controller, based on a PI controller, was implemented and to get fast response and avoid wind-up, the controller has a feed-forward and an anti-windup scheme. In this research, an IGBT switch block having a bridge configuration is used and it has a RC snubber circuit to suppress over voltage during turn-off. The RC snubber values have been selected in order to suppress the turn-off voltage to be lower than the forward blocking voltage limits of the IGBT.

To get a fast transition from bypass mode to PWM mode, a thyristor commutation logic has been proposed. It was shown that the commutation depends on the polarities of the input voltage and the thyristor current. It was verified by the simulations that the proposed voltage sag supporting scheme can regulate the output voltage with quick reaction and high precision during voltage sag and swell conditions.

CHAPTER 5

FAILURE DETECTION AND PROTECTION LOGIC

This chapter describes the fault detection and protection logic. In the previous chapters, this research has so far focused on verifying the performance of the proposed system and the system design. The investigation now shifts its focus to the implementation of the proposed scheme.

Usually prior to experiments, it is necessary to have a fast and reliable fault protection circuit. In addition, the proposed voltage sag supporter is to be used in a high voltage application and has a novel topology. Therefore, having a fast acting and accurate fault detection logic is important. The first part of this chapter discusses the possible failures in the system and proposed post-fault procedures, and the second part explains the failure detection logic using signals from IGBT and thyristor gate drivers.

5.1 Gate Signals

The configuration of the system has been explained in Chapter 3 and 4. From the viewpoint of hardware, the system can be divided into following categories: switches and their gate drivers, controller board, sensors, autotransformer, and filters. To determine

the kind of fault that can occur, and what kind of protection logic will be implemented in gate drivers and the controller, all possible failures of components consisting of the total system have to be considered.

The gate signals corresponding to PWM and bypass modes are shown in Figure 5.1, where from top to bottom appear the thyristor gate signal, the thyristor mode signal, the PWM signal, and the reed-relay signal are shown. The thyristor mode signal shows the on/off status of thyristor generated from the controller, where high or low stands for thyristor ON and OFF, respectively. This signal is used to interlock the gate signals of the thyristor and the IGBT to avoid short circuit between these devices. In other words, the IGBT PWM signal cannot be activated during the thyristor on mode due to the interlock circuit using the thyristor mode signal. In this research, there exist two ways to turn on the thyristor. One is the gate driver circuit using transistors, and the other is using the reed relay circuit. The reed relay provides an alternative firing mechanism for the thyristor in order to prepare for the situation of no power in the driver circuit or a malfunction of the gate circuits. The reed relay used in this research has a normally closed contact, so that it remains in the closed state without a turn-off signal. The gate drivers of the IGBT and the thyristor each have one-pair of fiber optic links consisting of a transmitter and a receiver for a gate signal and a feedback signal. The fiber optic links are used to obtain high voltage isolation between the power and the controller circuit. It should be mentioned that if there exists misconnection or disconnection in the fiber optic cable, the fault signal does not show up in the controller board. Hence, it is always

necessary to check the existence of the feedback signal. Possible failures about IGBTs, thyristors, and other components are summarized in Table 5.1, 5.2, and 5.3.

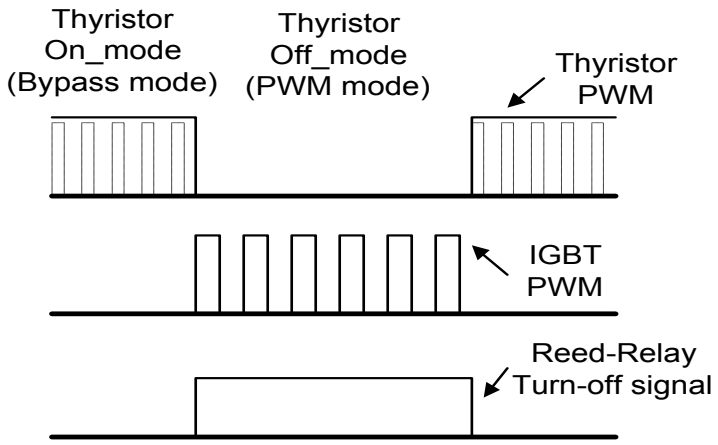


Figure 5.1. Gate signals corresponding to PWM and bypass mode.

5.2 Faults in IGBT Switch Block

The IGBT switch block is the most important, and it seems the most vulnerable part of the system due to the high voltage and current stress across the switch block. This section describes possible failures and actions for faults related to the IGBT switch block.

5.2.1 Summary of Possible Failures and Detection Method related to the IGBT Switch Block

Table 5.1 summarizes possible failures, causes of failures, results of the failure, how to detect, and actions for the faults in the IGBT switch block. The overall IGBT switch block consisting of the gate driver, the power supply, and diodes, and the RC snubber etc,

is shown in Figure 5.2. Comparing conventional inverter systems for low voltage application, there is a difference in this IGBT switch block. Firstly, a fiber optic cable is used for gate signal and feedback signal. Secondly, to obtain isolated power for each IGBT switch block, the power for the gate driver is generated from the RC charging circuit located in parallel with the RC snubber circuit. The capacitor inside the power supply is charged through the power resistor noted as R_{power}.

Based on possible failure modes in Table 5.1, it is concluded that the IGBT gate driver needs detection circuits for under voltage of the power supply and over voltages across the switch. Table 5.1 shows that in order to detect a shorted snubber resistor or an opened IGBT, detection for desaturation is preferred. Usually, the desaturation detection can be used to find a short circuit of the switch. (checking the V_{ce} after turning on the switch). However, the desaturation circuit is not implemented because there is limited space available on the gate driver. In addition, these faults seem to occur rarely and can be detected by another detection circuit such as over voltage sensing.

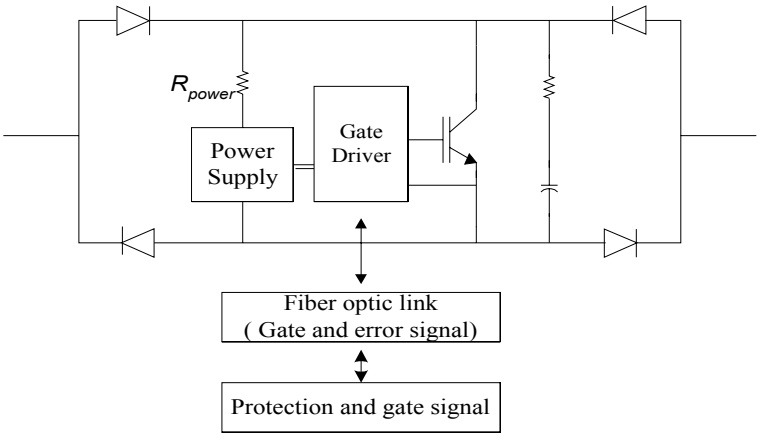


Figure 5.2. IGBT switch block showing the power supply and gate driver.

5.2.2 Procedure after Detecting Faults related to the IGBT Switch Block

This section describes processes after the controller recognizes faults in the IGBT switch block. It should be mentioned that even it the fault occurs in any one of the serially connected switch blocks, the gate signal of that block is not inhibited. In this research, the switch blocks are serially connected. When the controller detects the fault signal in any one switch of the serially connected switch pairs, whole gate signals are blocked. In the case that only one switch remains off-state while rest of blocks are turned on, the entire input voltage will appear across the block. Therefore, blocking only one switch having the fault results in excessively high over voltage across it.

If faults occur during the bypass mode, the controller keeps thyristors turned on and it sends a short pulse to check the status of the switch block having the fault. If the fault exists consecutively for several times, the controller inhibits starting of voltage sag supporting. On the other hand, if faults occur during the PWM mode, the controller does the following actions. First, it inhibits all IGBT gate signals, and turns on thyristors. Secondly, the switch block having the fault is examined with a short gate pulse while monitoring the feedback signals.

5.3 Faults in Thyristor Switch Block

Thyristor pairs are used to bypass the input power to the output at high efficiency. In addition, they are used to provide a short current path because they have a capability of withstanding a large short current. Even though thyristors themselves are robust devices,

there exists a possibility of failures in the thyristor block due to malfunctions in peripheral circuits. This section describes possible failures and actions for corresponding faults related to the thyristor block.

5.3.1 Summary of Possible Failures and Detection Method related to Thyristor Switch Block

Table 5.2 summarizes possible failures and detection methods in thyristor block consisting of the gate driver, the power supply, and the snubber etc. The thyristor driver has circuits for detecting under voltage of the power supply and the reed relay feedback circuit. A shorted or opened IGBT switch itself can be detected by detection functions in the gate driver such as over voltage and under voltage of power supply.

On the other hand, in order to detect a shorted or opened thyristor, it is necessary to have information about currents. Figure 5.3 shows the location of current transformers CT_1 to CT_3. A shorted thyristor during the PWM mode can be detected using CT_2. The existence of thyristor current during PWM mode means that the system has a shorted thyristor. A thyristor failed open can be detected during the bypass mode using the fact that there is no thyristor current during this mode. However, in this research, thyristor snubbers are implemented in parallel with each thyristor pair. Therefore, even if a thyristor has failed open, there can exist current flowing via the CT_2. This may arise due to the current through the snubber R_{th} and C_{th} with the assumption that only one CT exists in one of the serially connected thyristor branches, and the fault occurs in outside of the thyristor branch having the CT_2. An alternative way of determining that thyristor has

failed open is to compare the magnitudes of the input voltage and the output voltage during normal condition using the PTs (Potential Transformer) with the assumption that there is no fault in the sensing circuits.

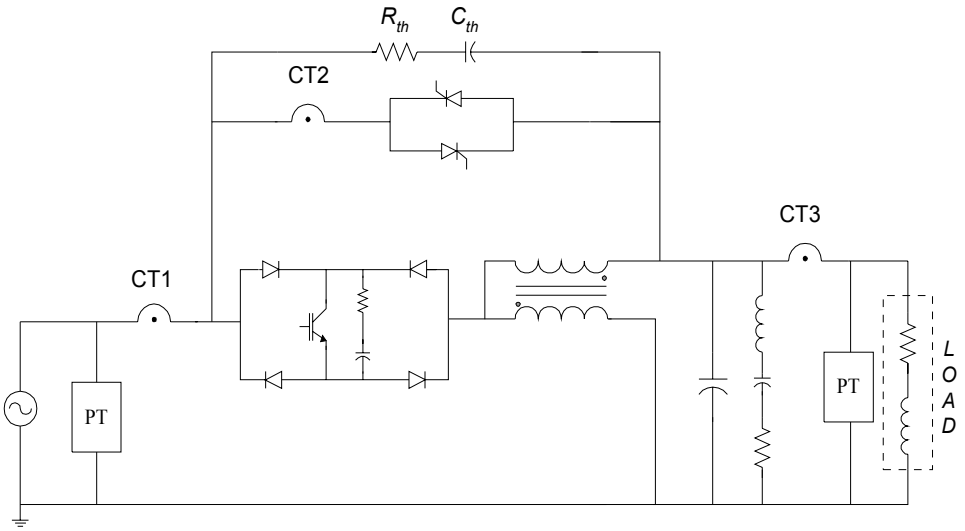


Figure 5.3. Sensors for the purpose of control and protection.

5.3.2 Procedure after Fault Detection in Thyristor Gate Driver

When a fault occurs during the bypass mode, at first the controller prohibits starting the sag support to avoid a short circuit between the IGBT and the thyristor, and then, the feedback signal of the thyristor gate driver is periodically checked. If faults occur during PWM mode, the voltage sag supporting is inhibited. The reed relay remains closed during the bypass mode and will open at the beginning of the PWM mode. Therefore, it is necessary to check whether the relay is actually off in the PWM mode.

After the input voltage has recovered, the thyristor pairs should be turned on to bypass the input power. Thus, if the fault still exists after turning on the thyristors, only the reed relay circuits can turn on the thyristors. If both the thyristor gate driver and the reed relay do not work, it is necessary to turn on the VCB (vacuum circuit breaker) in order to bypass the input power instead of the thyristors. The VCB, which is not shown in Figure 5.3, is implemented in parallel with the thyristor pair.

5.3.3 Faults in Components

The possible failures except the IGBT and thyristor switch blocks are summarized in Table 5.3. Using the current transformer CT_1 through CT_3, failures in the autotransformer, the capacitor filter, and the notch filter can be detected. If the current magnitude of the CT_1 and CT_3 are different from each other during the bypass mode, it is an indication that there exist failures in filters or the autotransformer. By comparing measured values from each sensor, failures of sensors can be detected. During the bypass mode, the measured voltage using the input voltage sensor and the output voltage sensor should be identical with the assumption that no error is present in the switches. In order to check the sensing circuits, the DC offset of the sensors can be used, in which sensing circuits include sensors themselves and interface circuits such as scaling and A/D converter etc. The DC offset value of the sensing circuit should be the center value of the measurable voltage range. For example, when the input ranges of the A/D converter is 0 V–3.3 V, the center value of the A/D converter usually is selected as 1.65 V. The offset

calculation of sensors will be explained in Chapter 6 in detail. Back-up power using a battery is employed in the control board to prepare for power interruption. The watchdog timer in the DSP will reset the controller if the controller stops working due to the noise caused by high voltage and high current switching.

Table 5.1 Summary of possible failures and detection method related to IGBT switch block.

Possible failure	Cause of failure	Result of failure	How to detect	Action
IGBT gate driver				
Loss of fiber optic signal	- Disconnection - Low voltage in power supply	- Loss of control	- Shape of FB signal	1
Over temperature (Heat sink)	- Operating condition	- Damage device	- Temperature sensor using RTD (Resistor Temperature Detector)	1
Power supply for IGBT				
Under voltage	- Tolerance in a power resistor	- Increase IGBT loss	- Under voltage	1
Resistor (fail open)	- Component failure due to over voltage - Disconnection	- No power	- Under voltage	1
No voltage	- Resistor open - Capacitor short - Open circuit in charging path	- No power	- Under voltage	1
Over voltage	- Fault in other blocks (Snubber value)	- Increase power loss in resistor - Damage power supply resistor		-
Components				
Snubber Resistor (fail open)	- Over heat - Over voltage - Over current	- No snubber action - Over voltage during PWM mode (load current flows through the power supply resistor)	- Over voltage	1

(Continued on the following page)

Table 5.1 (cont.)

Possible failure	Cause of failure	Result of failure	How to detect	Action
Snubber Resistor (fail short)		- Large capacitor discharge current	- Desaturation	1
Snubber capacitor (open)		- No snubber action - Over voltage in power supply - Over voltage across IGBT during PWM	- Over voltage	1
Snubber capacitor (fail short)		- No power in bypass mode	- Under voltage of power supply	1
Diodes (fail open)	- Mechanical disconnection	- Output voltage distortion (Loss of voltage control)	- No current in IGBT path during PWM - Voltage waveform during PWM	1
Diode (fail short)	- Over voltage - Excessive high power dissipation	- No snubber action during IGBT off - Difficulty in voltage control	- No voltage across IGBT during IGBT turn-off	-
IGBT (fail open)	- Rupture inside the device	- Over voltage across IGBT due to no discharge path of snubber capacitor	- Over voltage - Desaturation	1
IGBT (fail short)	- Over voltage - Excessive high power dissipation	- Over voltage at other IGBT blocks - No voltage in power supply	- Under voltage of power supply - Over voltage protection located in other IGBT blocks	1
Other conditions				
Over voltage (PWM mode)	- Open in snubber circuit - Over load condition	- Damage IGBT	- Over voltage during PWM	1
Heavy load	- Load condition	- Over voltage during PWM		

1. No sag support (Stop PWM and turning on thyristor)

Table 5.2 Summary of possible failures and detection method related to thyristor block.

Possible failure	Cause of failure	Result of failure	How to detect	Action
Thyristor gate driver				
Loss of fiber optic signal	- Misconnection - Low voltage in power supply	- Loss of control - Low output voltage - Damage of the snubber circuit due to over voltage	- Shape of FB signal	2
Over temperature (Heat sink)	- Long lasting heavy load	- Damage devices	- Temperature detection by RTD - Protected by fuse	1
Reed Relay				
Impossible to open	- Over current - Loss of reed relay turn-off signal	- No sag supporting - Generate short path in thyristor and IGBT	- FB signal of reed relay	2
Power supply for thyristor				
Under voltage	- CT failure - No load	- Low supply voltage	- Under voltage of power supply	2
No voltage	- Misconnection - CT failure	- No power - No control	- Under voltage of power supply	2
Over voltage	- Large current due to heavy load	- Voltage stress of circuits in the power supply		-
Components				
Snubber resistor (fail open)	- Over heat - Voltage stress	- No snubber action - Voltage spike during commutation - High dv/dt	- No current in thyristor branch during PWM on-off	3

(Continued on the following page)

Table 5.2 (cont.)

Possible failure	Cause of failure	Result of failure	How to detect	Action
Snubber resistor (fail short)		- Large capacitor discharge current	- Large capacitor discharge current	3
Snubber capacitor (fail short)		- Not serious problem	-	-
Thyristor (fail open)	- Short circuit that melts internal part	- Decrease output voltage during bypass mode	- Output voltage magnitude is different from that of the input voltage due to voltage drop in snubber circuit during bypass mode - No thyristor current during bypass mode	1
Thyristor (fail short)	- Over voltage - Over current - Failure in reed relay circuit	- Different voltage sharing between switch blocks during off-state	- Thyristor current exists during PWM mode	2

1. Stop thyristor gating and turning on VCB (vacuum circuit breaker)
2. Inhibit voltage sag support
3. Keep sag supporting and request maintenance

Table 5.3 Summary of possible failures and detection method related to sensors and control board.

Possible failure	Cause of failure	Result of failure	How to detect	Action
Sensors				
Loss of input voltage	- Disconnection - Error in sensing circuits - Loss of power supply - Sensor fault	- Incorrect sag support mode	- Comparing measured value with that of the output voltage sensor during bypass mode	1
Loss of output voltage	- Same above	- Malfunction in output voltage control (over voltage)	- Comparing measured value with that of the input voltage sensor during bypass mode	1
Loss of current signal	- Same above	- Fault in thyristor commutation process - Possibility of generating short path due to turning of IGBT - Impossible to realize the over current protection logic	- Detection logic is same as that of voltage sensor	2
DSP				
No power	- Power supply fault - No line power	- Loss of control	- Back-up power	1
CPU malfunction	- CPU disruption - Disruption in supply voltage	- Loss of control	- Reset by WD (watchdog) timer	-

(Continued on the following page)

Table 5.3 (cont.)

Possible failure	Cause of failure	Result of failure	How to detect	Action
Interface circuit				
Malfunction of sensing circuit	- Disconnection - Sensing device failure such as ADC and op amps for scale and offset	- Same result as that of loss of sensing signal	- Same method of the each sensing signal failure - Offset calculation comparing with 1/2 of input voltage range	1

1. Do not start voltage sag support
2. Wait half cycle to commutate thyristor or rely on one normal signal of input or thyristor current sensors

5.4 Fault Detection Logic

In the previous sections, possible failures, causes, and detection methods have been mentioned. It has been shown that the IGBT and the thyristor have failure detection circuits on their driver boards, while failures in the sensor circuits, thyristors, the transformer etc. are detected through software-based logic.

This section describes the fault detection logic of the IGBTs, the thyristors, and the reed relays based on feedback signals from the gate drivers. Implementation using hardware is preferred in order to get fast fault detection and protection. Therefore, the protection logics of the IGBT gate driver and the thyristor gate driver are realized using logic circuits, whereas failures in the relay are detected through control software. There exist time delays between the gate signal and feedback signal in the IGBT and thyristor driver circuit, but the propagation delay in the logic circuits and gate drive circuits is reasonably short. However, the turn-on delay of a reed relay is about 2 ms due to its mechanical moving part. This means that at least 2 ms is necessary to determine the status of the relay contact. Measuring the 2 ms delay using hardware involves many gates. Therefore, a software routine is preferred to check the status of the relay.

The overall fault detection circuits are shown in Figure 5.4, and protection logic for each block is explained in the next section. As mentioned earlier, when any one of the IGBT blocks has a fault, the gate signals to all IGBTs are inhibited. The status of each IGBT block is passed on to the controller through a data bus. The controller then generates a short pulse to determine whether the fault exists repetitively or not. To examine an individual IGBT switch block, the PWM selection signals [0–2] are used.

Any fault in the IGBT, the thyristor, or the relay generates an external interrupt that informs the fault occurrence to the main controller. The status of each device is connected to the controller using the latches, so that the controller can discriminate where the fault occurs.

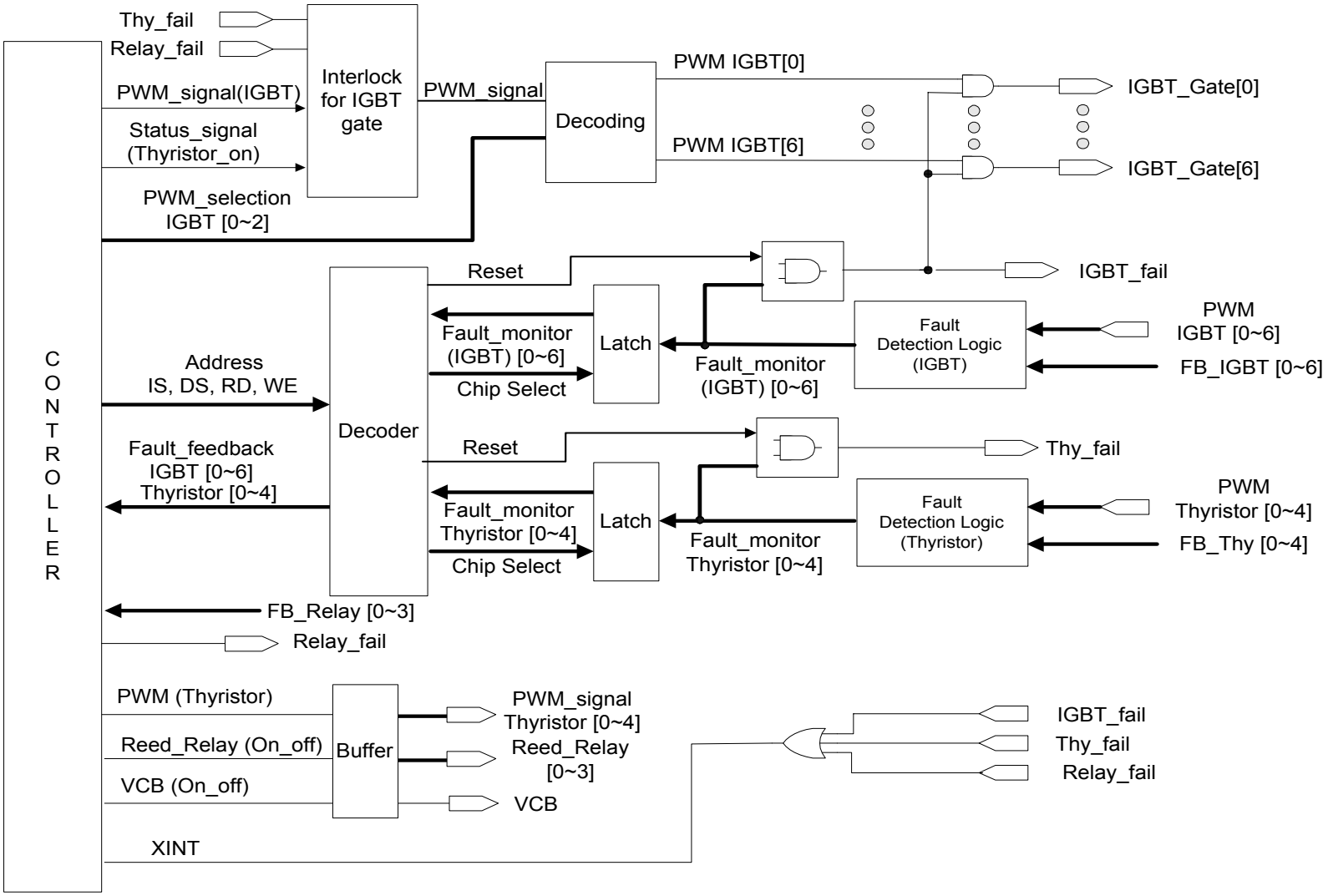


Figure 5.4. Overall hardware block diagram for fault detection.

5.4.1 Fault Detection Logic for the IGBT using Signals from its Gate Driver

The complete IGBT detection logic is shown in Figure 5.5 and consists of two parts: One is fault detection during the bypass mode, and another is that of the PWM mode. These modes are distinguished by the PWM_ON_OFF signal. The PWM_ON_OFF signal becomes high or low level for the bypass and PWM mode, respectively. During bypass mode, the value of the PWM_ON_OFF signal is high, hence the output of the fault detection logic, which has logic for detecting during PWM mode (shown as the square shape) is ignored by the NOT gate. The PWM_ON_OFF signal is identical to the thyristor on-off signal used for interlocking of the IGBT gate during thyristor ON mode. If a fault occurs, the FB_IGBT signal assumes a high-level.

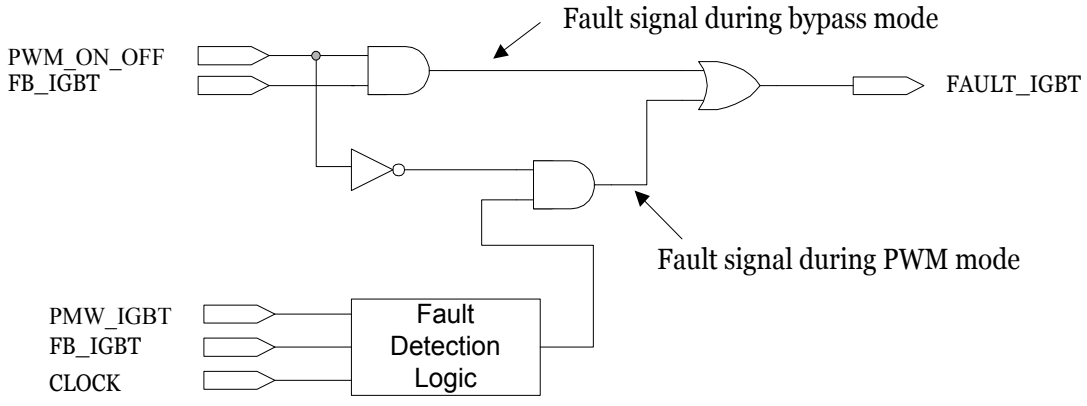


Figure 5.5. Overall IGBT fault detection circuit for bypass and PWM mode.

The feedback (FB) signal during the PWM mode is different from that during the bypass mode, which is shown in Figure 5.6. As shown in the figure, the feedback signal

is designed to generate a short pulse at the positive edge of the PWM signal to inform its healthy status to the controller. When a fault occurs, the feedback signal becomes a high level, which is same as bypass mode. Therefore, if a fault occurs, the FB signal becomes a long pulse. Hence, the fault can be detected by checking the pulse duration of the signal.

To get high voltage isolation, fiber optic links are used for sending the PWM signals and receiving the FB signals. When there exists misconnection or disconnection of the fiber optic link, the FB signal will remain at a low-level. Therefore, faults during the PWM mode can be expressed as one of the following two conditions.

1. The feedback signal longer than 5μs.
2. No feedback signal after the PWM signal is sent to the gate driver.

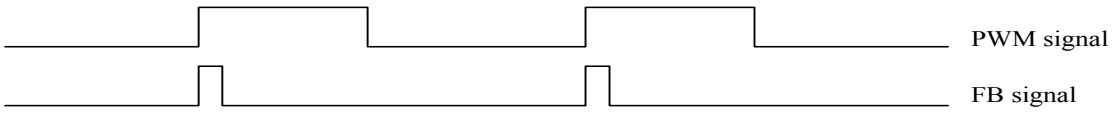


Figure 5.6. The PWM signal and the FB signal having a short pulse corresponding to a rising edge of the PWM signal.

Figure 5.7 shows the circuit for checking the duration of the feedback signal, in which the clock, the PWM, and the FB signal are used. The JK FF (Flip-Flop) has a characteristic that the output of the FF toggles at the rising edge of the clock signal if the both J and K inputs are high level. As shown in Figure 5.7, the JK FF output is

connected to input of the next JK FF to work as the clock signal. Therefore, by changing the total number of flip-flops, this circuit can detect various durations of the FB signal. In this research, the total number of the FF is chosen to detect a pulse longer than 5 μs.

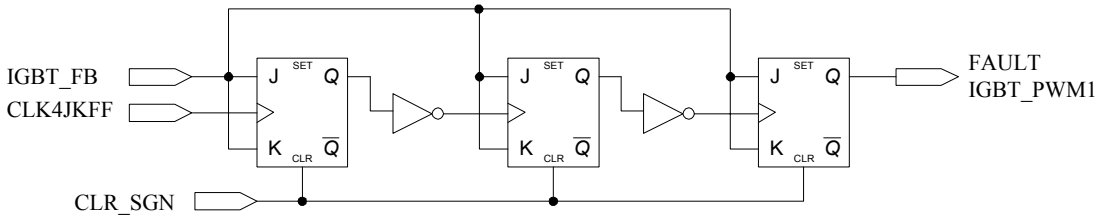


Figure 5.7. The logic circuits for checking the duration of the FB signal.

To check the existence of the FB signal, the logic and circuit shown in Figure 5.8 is used. Using the D FF with the FB signal and the PWM signal, the existence of FB signal can be checked. The IGBT FB signal is connected to the input of D FF, and the delayed PWM signal is used for the clock signal. The D FF has a characteristic that the output becomes the input of the D FF at the rising edge of the clock signal. In the healthy status, the FB signal should appear after the rising edge of the PWM signal. Therefore, at the rising edge of the delayed PWM signal, the output of D FF is a high-level. If a FB signal does not exist at the rising edge of the clock signal, the D-FF output remains at low-level, which generates an IGBT fault signal.

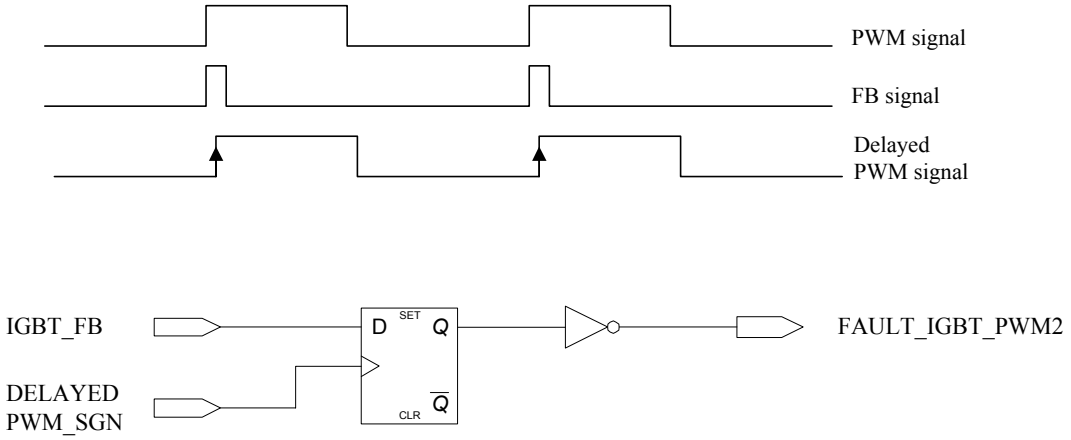


Figure 5.8. Logic circuit and related signals for checking the existence of the IGBT FB signal.

5.4.2 Fault Detection Logic for the Thyristor using Signals from its Gate Driver

The thyristor fault detection logic and signals used are shown in Figure 5.9 and Figure 5.10. The feedback signal of the thyristor resembles the thyristor gate signal, while the IGBT feedback signal is a short period signal in synchronized with the rising edge of the PWM signal. In Figure 5.9, from top the thyristor gate signal, the feedback signal, and the exclusive OR (ExOR) signal of the gate and the feedback signal are shown. The feedback signal of the thyristor is identical to the gate signal, and there exists small time delay in the actual circuit.

In this research, the thyristor gating pulse has a fixed duration about 30 μs. If the thyristor current remains above the latching current level, the thyristor can remain in an on-state without a gate signal. Therefore, after the current reaches the latching current

level, the controller does not need to generate thyristor gate signals. However, to control the thyristor gate signal with above control manner, the polarity of the thyristor current should be known. Hence, to simplify the thyristor control logic, a short gate pulse of 10 kHz switching frequency is continuously applied to the gates.

Thyristors have higher surge current capability than that of IGBT and have less voltage stress in the proposed scheme. In addition, if the FB signal resembles its gate signal, it is possible to implement the gate and logic circuit with simple and less components. Therefore, the FB signal identical to the gate signal is used.

The fault detection logic of the thyristor is shown Figure 5.10. Using the earlier IGBT fault detection circuits, the JK FFs are in use to measure the duration of the FB signal. This logic differs from the IGBT logic in that the exclusive OR (ExOR) signal between the gate signal and the FB signal is used as an input of the JK FF. If there is no fault, the ExOR signal shows only a short pulse indicating the delay between the two signals. Whenever the feedback signal does not resemble the gate signal (which means a fault occurs), the resulting ExOR signal will have long period. Therefore, if the duration of the ExOR signal is longer than predetermined periods, the JK FF output located in last stage becomes high. Changing the total number of the JK FFs can easily modify the periods. Besides the circuit shown in Figure 5.10, the thyristor gate driver has the circuit that generates a high level of FB signal when there is a fault. There exists one problem caused by using the FB signal resembling its gate signal. If a fault happens during the thyristor on time, as the FB signal resembles the on signal, the fault logic can not detect the fault occurrence until the thyristor on signal becomes low-level, i.e., not identical

each other. The thyristor on signal remains 30 μs, so that maximum detection delay is 35 μs with assumption that the predetermined period of the ExOR signal is 5 μs. Since the thyristor has a big surge current capability, it seems that 35 μs delay in detection is allowable. On the other hand, the IGBT fault detection circuit is designed to detect faults within 10 μs. Using the ExOR signal makes the circuit simple. In case of the IGBT, to check the existence of the FB signal, additional circuits such as delay generating circuit and D flip-flop etc. are necessary. However, if the ExOR signal is used to measure the pulse duration, it is possible to check the existence of thyristor FB signal without additional circuits. When there is no feedback signal, the ExOR signal will become a long pulse having 30 μs. Therefore, there is no need for additional circuits to check the existence of feedback signals.

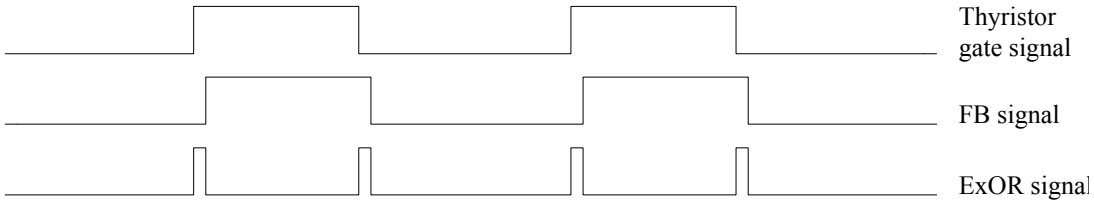


Figure 5.9. The exclusive OR signal between the thyristor gate signal and its FB signal.

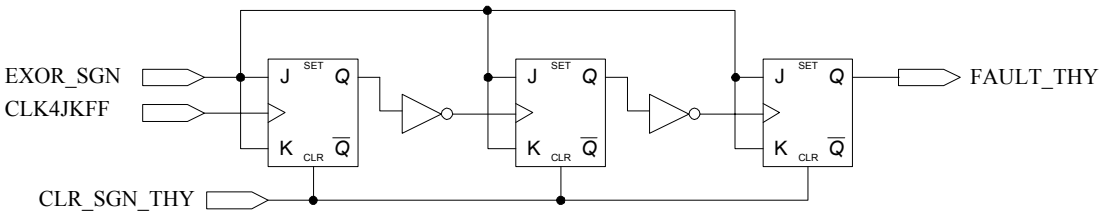


Figure 5.10. Logic and logic circuit for checking faults in thyristor gate driver.

5.4.3 Fault Detection Logic for Reed Relay Circuit

Figure 5.11 shows the reed relay off signal and its feedback signal. The delay time of relay is about 2 ms due to the mechanical movement. The relay used in this research has a normally closed contact. Therefore, this relay remains in close state without a turn off signal. To open the relay, the voltage controller generates the relay off signal during the PWM mode as shown in Figure 5.11. The turning off signal of the relay becomes high at the beginning of the PWM mode and remains high during the mode.

If there exist faults in the relay circuit, which means that the relay remains in on-state during PWM mode in spite of turn-off command, turning on the IGBT results in the short circuit between the IGBT and the thyristor branch. Therefore, before turning off the relay, it is necessary to know whether the relay actually in off-state or on-state. The status of the relay is determined as follows. After sending the relay off signal from the controller, the controller checks the FB signal using a digital input port. If the FB signal does not go high for some time after sending off signal, the controller recognizes it as the fault of the reed relay circuit.

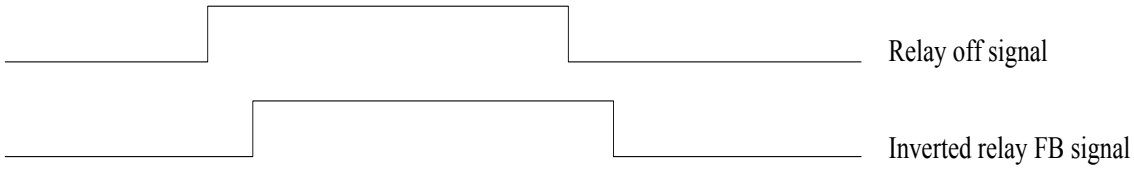


Figure 5.11. Reed-relay off signal and its FB signal.

5.5 Chapter Summary

This chapter provides a summary of the faults and analyzes each fault based on risk of occurrence, risk of causing damage to system, and possible corrective actions. The analysis included examining detection circuitry reliability and its potential effect on overall system reliability. In some cases, a component has a much higher risk of failing a particular way, than other ways. For example, thyristors used in the static bypass switch are enclosed under pressure in a "press pak" container. This device package rarely fails in an open state but can fail shorted if thermally or voltage overstressed. Therefore, the failure analysis was more concerned with detecting a shorted device than a rare open device.

As a result of fault analysis, each IGBT gate driver included the circuits for detecting under voltage for the power supply, steady-state over voltage across each IGBT switch, transient over voltage across each IGBT switch, and feedback signals that indicate the health of the IGBT control circuitry. To show the healthy status of the IGBT, the gate driver was designed to send a short pulse that is synchronized with the PWM gating signal. By checking the shape of the FB signals, it is possible to detect faults in the gate drivers. Each thyristor driver includes a detection circuit for under voltage of the power supply and feedback signals that indicate the health of the driver control circuitry as a result of fault analysis. To show healthy status of the thyristor control, the driver was designed to return a duplicate feedback signal for each (Reed Relay turn-on and thyristor turn-on command) signal sent to it.

Faults occurring in the system are detected by software-based and hardware-based logics. The hardware-based logic uses circuitry to detect faults in the IGBT and thyristor gate drives. The software-based fault detection has been suggested to find faults in relays and components such as sensors or power devices.

CHAPTER 6

EXPERIMENTAL VALIDATIONS

This chapter explains the configuration of the hardware and software used in the development of a voltage sag mitigation device, and experimental results are provided.

6.1 Experimental Setup

To verify the control logic, experiments have been carried out with the experimental setups as shown in Figure 6.1. Figure 6.1 shows schematic of the entire system. The actual test setup is shown in Figure 6.2. For the purpose of laboratory experiments low voltage of 120 V was used, while as shown in the test setup, actual high voltage devices and their gate drivers for high voltage application are used in the test setup. The experimental setup consists of a voltage sag generator, switch blocks, controller, filters, load, and sensing parts. Table 6.2 shows the specification of power the devices. The 6500 V, 400 A high voltage IGBT made by EUPEC is used for the PWM switch.

For high voltage application, it is necessary to connect in series the IGBT PWM switches and the thyristor bypass switch, but only one IGBT and one pair of thyristors are used in this experimental verification to simplify the hardware setup. The load is made of

a power resistor and an inductor, which simulates 3 A load current. The inductor in the notch filter has been made by winding wires around a magnetic core, and the inductance value was measured by an LCR meter in the motor laboratory. As mentioned in Chapter 5, the switching frequency of the IGBT and the thyristor is 1.5 kHz and 10 kHz having a 30% duty-cycle, respectively.

A digital signal processor (DSP) is used to implement the control algorithm. The DSP TMS320LF2407 is selected for the main controller. The control program can be developed by either an Assembler or C-language. The program is presently being developed using C-language because of its easiness of debugging and programming. An emulator XDS 510PP is used for debugging and downloading the control program, and the program named CODE COMPOSER™ is used to compile program and generate output file of C source program [48]–[49]. In the real implementation, the control program will be recorded in the flash EEPROM of the DSP. However, during the development phase, using the emulator makes it easy to debug the program. For instance, the emulator can monitor internal variables and set break points inside the program for the purpose of debugging.

There exist two voltage sensors made by ABB at the input side and the load side, which are used for monitoring voltage sags and also serve as feedback for load voltage regulation. There are two current sensors for measuring the thyristor current and the input current. The current sensor in the thyristor branch has a role in checking the current polarity and magnitude to determine thyristor commutation logic. For over current protection, the input current sensor is implemented.

The DSP chip has 16 A/D converters (ADC) inside. Each ADC has a resolution of 10 bit with ± 2 LSB max error. The ADC conversion time is less than 500 ns. An accurate voltage measurement is the most important factor for precise voltage control. Therefore, commercial ADC (AD7874) is used, which is a 12 bit 4 channels ADC with ± 1 LSB max error. Comparing the resolution such as 10 bit and 12 bit and the maximum error such as ± 2 LSB and ± 1 LSB, it can be known that AD7874 has a much higher resolution. Also there is another factor of increasing the precision of the measurement. In case of ADCs in the DSP, the input voltage range should be between 0 V and 3.3 V, while the input voltage range of AD7874 is ± 10 V. Therefore, this higher measurable input voltage range gives much higher resolution. Currents are measured by the ADCs in the DSP, because the ADCs in the DSP provide good enough resolution of measuring current polarity and the magnitude. To reduce problems caused by difference of ground potentials in the sensing circuits, the differential amplifiers are inserted at the first stage of the sensing circuit having gain of one. A second order low-pass filter having 300 Hz cutoff frequencies is implemented at the next stage of the differential amplifier, to reduce noise of the sensed signals for both the measurements of voltage and current. In the case of voltage sensing signal, the signal after the low-pass filter is connected to the A/D converter, AD7874. On the other hand, scaling and level shift stage are necessary to measure the current signals. Since these current signals are measured by the ADCs inside the DSP, it requires the current signal to have ranging from 0 V to 3.3 V.

Based on the voltage and the current feedbacks, the DSP generates gate signals for the IGBTs, the thyristors, and the reed relay. The gate signals are transmitted through

fiber optic cables that are connected to the gate drivers of each device. The DSP checks the status of the IGBT, the thyristors, and the reed relay using the feedback signal from the fiber optic cables connected to the respective gate driver boards. The use of fiber optic link gives high voltage isolation between the high voltage side and low voltage side such as the control board and increase noise immunity. The driving current of a fiber optic transmitter is set at a relatively high level in order to generate the strong gating signal having a form of light that can reach the receivers on the gate driver boards, since the control board is located far from the PWM and bypass switches. A D/A converter (DAC) is used to show internal variables of the control program. The DAC has 4 channels and 12 bit resolution.

Table 6.1 Specifications of power devices used in experiments.

Component	Rating	Component	Rating
Diode	4500 V, 350 A	Capacitor	4000 V, 30 μF
IGBT	6500 V, 400 A	Resistor	8 Ω
Thyristor	6500 V, 2590 A		

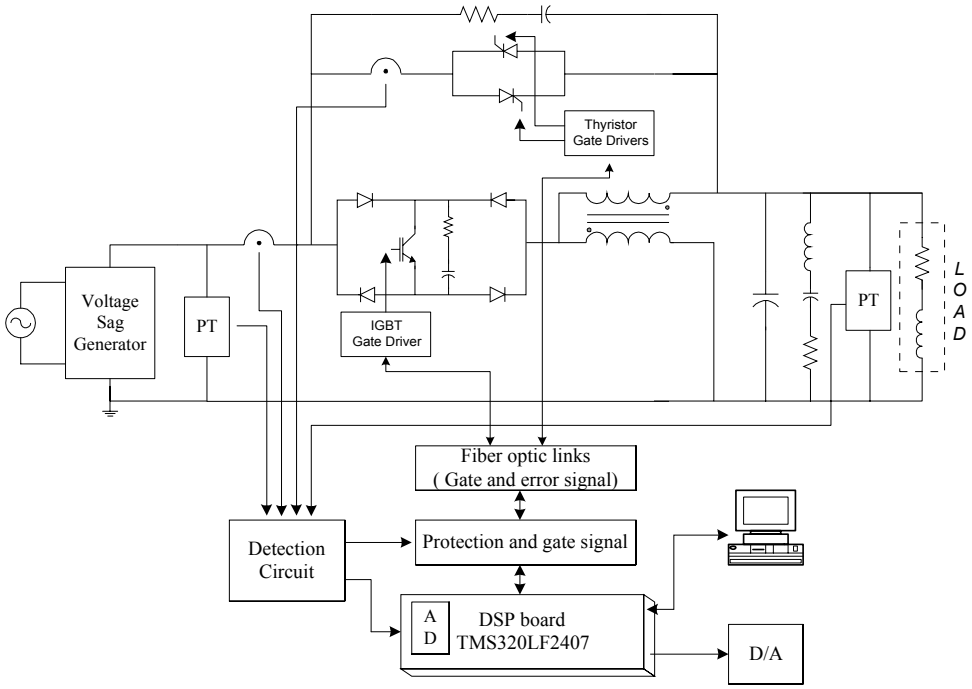


Figure 6.1. Schematic of experimental setup.

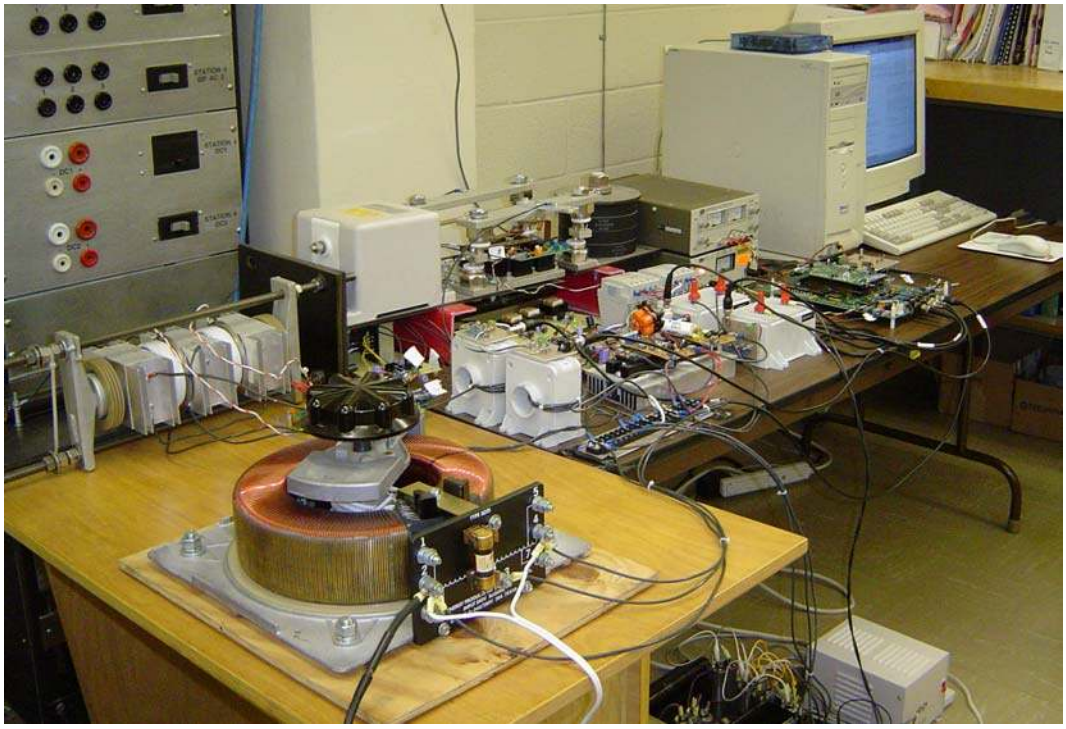


Figure 6.2. Experimental setup using high voltage devices.

6.2 Voltage Sag Generator

To simulate a voltage sag event, a voltage sag generator shown in Figure 6.3 has been developed. This sag generator consists of two IGBT switching blocks, a variable transformer (Variac), gate drivers, and logic circuit. To simplify the hardware circuits and increase reliability, commercially available IGBT gate drivers were used. This gate driver has a protection circuit for short circuit condition and provides a voltage isolation of the control circuit from the power circuit using a built-in optocoupler.

The switching block has a bridge configuration that is the same configuration of the main IGBT PWM switch. Upper IGBT switch block is connected to the top tap of the Variac, and lower IGBT switch block is connected to the middle tap of the Variac. The magnitude of the voltage dip can easily be changed by varying the tap location of the Variac. In the IGBT switch block, in order to decrease the voltage spike during turn-off, a RCD (resistor, capacitor and diode) snubber is used.

The logic circuit in the controller generates IGBT gate signals corresponding to the command of voltage sags. To simulate bypass mode, the logic circuit generates turn-on signal for S_1 and turn off signal for S_2. When the voltage sag command occurs, the logic circuit gives turn on signal for S_2 and turn-off signal for S_1. To avoid a short circuit due to the turning on both S_1 and S_2 switches, dead time is applied. To generate the dead time, a delay circuit using a resistor and a capacitor are used, and to avoid the variation in dead time caused by the variation of RC values, a relatively long dead time of 20 μs is selected. The IGBT gate driver for the sag generator has protection circuits. When a fault occurs, the gate signal is inhibited by the latch circuit in the driver about 1.5 ms.

However, the gate signal will be resumed if there exists an input gate signal after a latching period of 1.5 ms. In this research, the IGBT gating is generated by logic circuits only, so that it is necessary to keep the gate-off for any fault in order to prevent a short circuit between S_1 and S_2. Therefore, to keep the gate-off regardless of gate signals, an additional latch circuit with reset (made of NAND gates) is implemented.

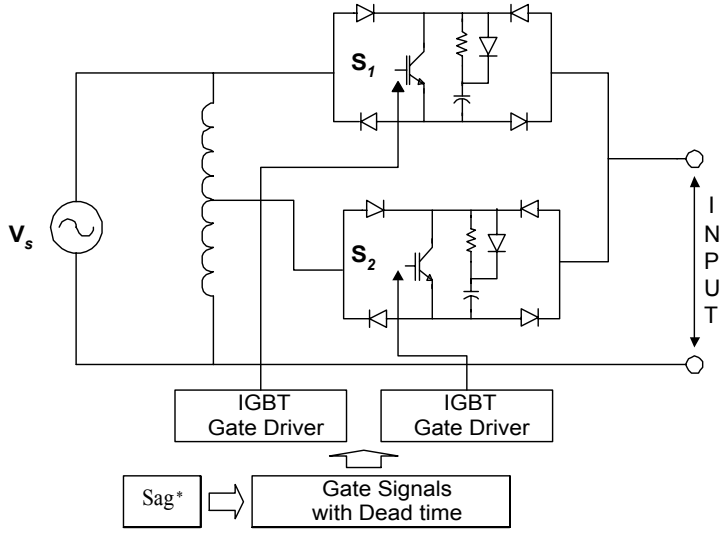


Figure 6.3. A voltage sag generator using an autotransformer and IGBT switch blocks.

6.3 Control Board

Figure 6.4 shows the target board. The target board consists of power supply part, sensing circuit (for voltage, current, and temperature), EPLD circuit, gating circuits including buffer and fiber optics receiver and transmitter, and memory. The target board and the DSP board are connected using connectors. Figure 6.5 shows the picture of the control board after the DSP evaluation module board (EVM) is mounted on the target

board. The DSP evaluation board made by Spectrum Digital is used, which has a DSP chip and GAL (Generic Array Logic) for address decoding, memory, and D/A converter etc. This EVM board includes peripheral circuits for communication.

The DSP board employs a 40 MHz Texas Instrument TMS320LF2407 DSP, which is a 16 bit fix point 3.3 volt DSP capable of 30 MIPS performance. This DSP is designed especially for motor drive applications and embedded systems. TMS320LF2407 is a family of TMS320F240 (5 V DSP). To realize a one-chip micro-controller for motor drive systems, this DSP has PWM ports, I/O pins, and encoder interface circuits etc. It has on chip memory up to 32k words of flash EEPROM and has 544 words dual access RAM and 2k words of single access RAM. There exist 16 PWM ports in which the total 16 PWM ports consist of two sets of 6 PWM ports and 4 individual PWM ports. The PWM port can also work as an I/O port. In this research, unlike three-phase motor control, only one PWM signal for each device is necessary for each switching device. Therefore, unused PWM ports are assigned as I/O ports.

Using the emulator, the control program is loaded into the DSP on the EVM board. The peripheral circuits for voltage sag mitigation are implemented in the target board. To increase noise immunity, the target board is designed to have four layers. To reduce the board size and to have flexibility of the logic design, the EPLD device (EPM7160SLC84) capable of 3200 usable gates made by ALTERA®, is used. A programmable logic device (PLD) can integrate many logic gates into one chip. There are two EPLD chips on the target board. One EPLD mainly deals with the fault detection logic and gate signals of the IGBT, and the other EPLD is involved in the fault detection logic of the thyristors and

address decoding. Software called MAX+PLUS® is used for developing logic and recording the EPLD. This software can be downloaded from the ALTERA website at no charge. The cable name "ByteBlaster™" is used for recoding the logic into an EPLD chip, and the schematic of the ByteBlaster is also provided in the ALTERA manual [50].

The control board is powered by external ± 12 V and + 5 V power supplies. These power supplies also provide the powers for the voltage sensors. Most ICs on the target board are 5 V devices. However, there are other voltage levels such as 3.3 V and –5 V for power of the DSP peripheral circuit and the A/D converter. A linear 3.3 V regulator steps down from 5 V to 3.3 V, and –5 V is derived from –12 V using a zener diode.

The status of faults is displayed by LEDs, and the target board has a latch circuit to recognize an external command for user interface. Even though, it is not shown in Figure 6.5, another board for external relays is used to generate ON/OFF signals for a vacuum circuit breaker, and external input and output signals.

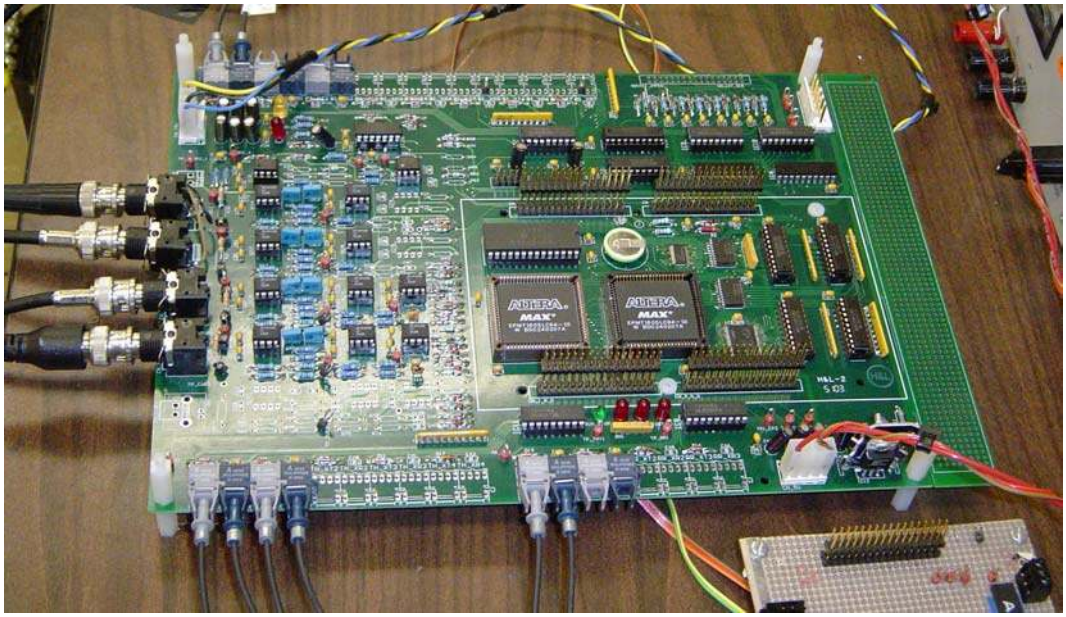


Figure 6.4. The control board having sensing, logic array, and circuits for gate signal etc.

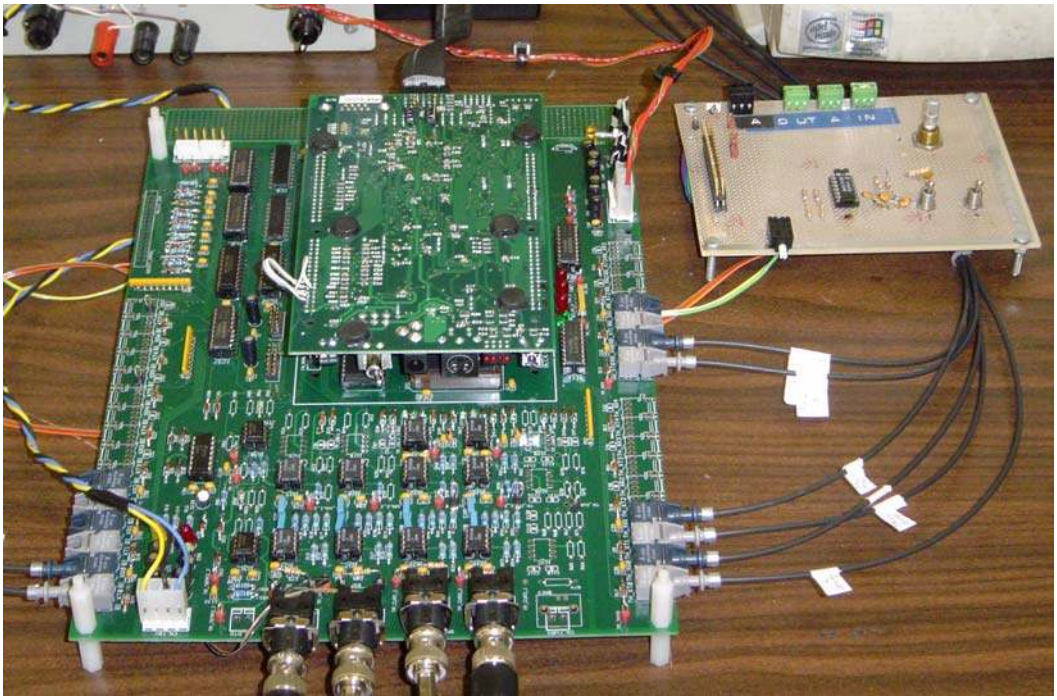


Figure 6.5. The control board with the EVM board mounted on the top.

6.4 Switch Blocks

The bi-directional PWM switch block consisting of a high voltage IGBT, eight stud diodes, and a snubber circuit (resistor and capacitor) is shown in Figure 6.6. The eight power stud diodes are mounted on bus bars that are inter-connected together so that four pairs of diodes are physically in series. The IGBT gate driver is mounted on the IGBT, and the IGBT is located in the center of Figure 6.6. The controller sends an optically transmitted signal to the driver receiver, and the driver converts the optical signal to a gate voltage that turns the IGBT ON/OFF. This gate driver also sends a short pulse that is optically transmitted back to the control through the fiber optic feedback cable in order to tell that there is no problem in the circuits.

An example of back-to-back connected thyristors and gate driver circuits are shown in Figure 6.7. In this example, it is necessary to have a gate driver for each thyristor since the ground potentials of cathodes of each thyristor are different from each other. In this research, the thyristor switch block has four pairs of back to back connected thyristors in series with one another and has five gate drivers controlling all four thyristor pairs. In cases where two thyristors have a common cathode connection, a single gate driver can be used to control both devices. Each thyristor gate driver has two active pulse circuits and one passive normally closed reed relay contact gating circuitry. The active pulse circuits are necessary for turning all the thyristors instantaneously on together after an input voltage sag event. The passive normally closed contact gating circuit connects the cathode of a thyristor within a back-to-back pair to the gate of the opposite thyristor within that same pair. The passive gating is necessary to provide low cost, highly

reliable, and low power gating. The RC snubber circuit for the thyristor pair is located behind the thyristor pairs. The small circuit board in front of the thyristor assembly monitors the status of the reed relay contact.

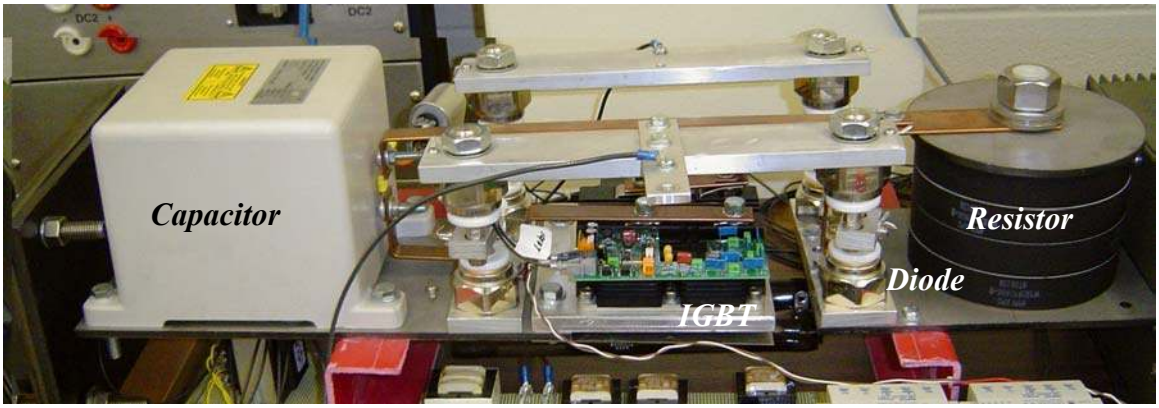


Figure 6.6. IGBT switch block.

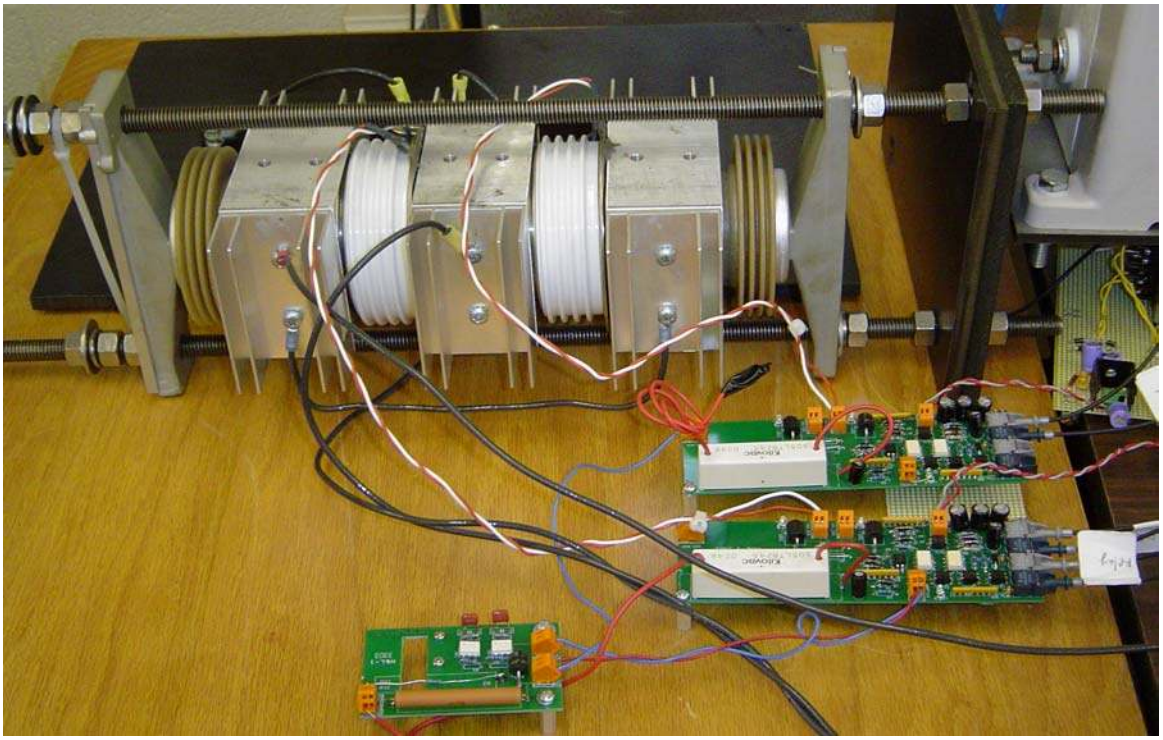


Figure 6.7. Thyristor switch block.

6.5 Control Program Software

The flow chart of main control loop is shown in Figure 6.8. In the main control loop, at the start, the variables, control registers of the program, and interrupt vectors are initialized. To calculate the A/D offsets of the AD7874 and A/D converters of the DSP, only the A/D interrupt (INT) generated by the event manager is enabled. The start of the A/D conversion is executed by the event manager with specific time interval. The period of the A/D INT is set to about 130 μs that is 1/128 of 60 Hz. Since the voltages and currents are sinusoidal, many consecutive A/D conversions for the A/D input does not give the correct sensor offset, which is only the mean value of that period of A/D conversions. To get a reasonable mean value using consecutive A/D conversion, the conversion should be carried out many times to have several cycles of the voltage or the current. However, this is not good way to calculate the A/D offset. Hence, the offsets are calculated using the A/D interrupt routine generated every 1/128 of one cycle (60 Hz).

During one cycle of voltage and current, the results of A/D conversion are added, and then the controller repeats this process for several cycles such as 32 or 64 cycles. Averaging the measured values with the total number of cycles gives the offset of each A/D channel. After calculating the A/D offset, the A/D INT is disabled, and the main control program goes into an infinite waiting loop. The PWM service routine and the timer 2 interrupt service routine are carried out every 200 μs and 1 ms, respectively. In timer 2 INT routine, external inputs and outputs are checked.

Overview of the function of interrupts is shown in Table 6.2. INT 1 is assigned to an external interrupt, which has the first priority. The DSP recognizes the external interrupt when the voltage level of XINT port becomes low. Any failure in switches and relay generates the external interrupt signal via the EPLD logic circuit. Rapidly to check faults of IGBTs and thyristors, the control board is designed to have the ports that show the occurrence of any fault of IGBT or thyristor. As explained in Chapter 5, the status of switches is connected to latch circuits. Therefore, the DSP can determine where the fault occurs and can diagnose the device having the fault. There can exist several interrupt sources for one interrupt. In case of INT2, there are two sources of timer period interrupt. One timer interrupt is assigned to generate 200 μs period for the PWM service routine, and the other is used for 1 ms timer interrupt. Figure 6.9 shows flowchart of the PWM service routine. To simplify the software structure, the 1 ms routine can be moved to other service routines such as INT 3 for timer 2 interrupt. However, to place related routines in the same interrupt service routine, the 1 ms interrupt service routine is not moved into INT 3. Using the 1 ms interrupt, the DSP counts the time period to inhibit restarting of PWM after the recovery of voltage sag event.

The PWM service routine has a role in generating the PWM signals. In this routine, the peak values of the input voltage and the output voltage are calculated and updated. If there is no sag condition, the DSP keeps the thyristors on, i.e., generating gating signal of the thyristors, and then escapes the routine. If the peak value of the input voltage is lower than the voltage sag limit, the control loop checks whether the commutation process is done or not. If the commutation done bit is set, the PI voltage controller generates the

duty-cycle of the IGBT. As shown in the thyristor commutation logic, the commutation process depends on the polarity of the input voltage and the thyristor current. Therefore, A/D conversion of the thyristor current is carried out.

End of the commutation processes is determined by the magnitude of the thyristor current. A zero current in the thyristor means end of the thyristor commutation. In this case, the commutation done bit is set, and the PI control routine is carried out at next PWM interrupt service routine. If the current and the voltage have the same polarity, the controller generates a 50% duty-cycle for the forced commutation process, and for the different polarity, the duty of the IGBT has a zero to wait the thyristor current becomes zero by natural commutation. At next PWM service routine, the magnitude of thyristor current will be checked again to determine whether the commutation process is done or not.

Table 6.2 Overview of function of interrupts.

Interrupt	Function
INT 1	External interrupt
INT 2	PWM interrupt service routine
INT 3	Timer 2 interrupt
INT 6	A/D conversion interrupt

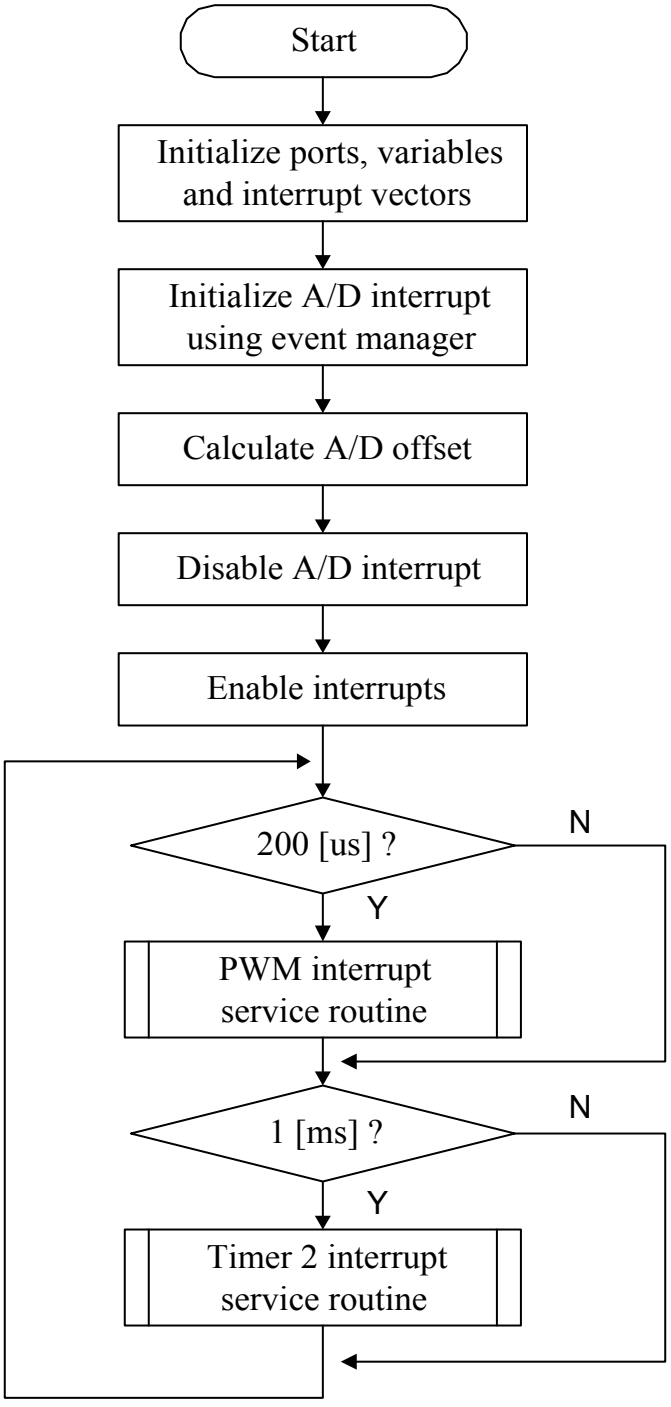


Figure 6.8. Flow chart of main loop.

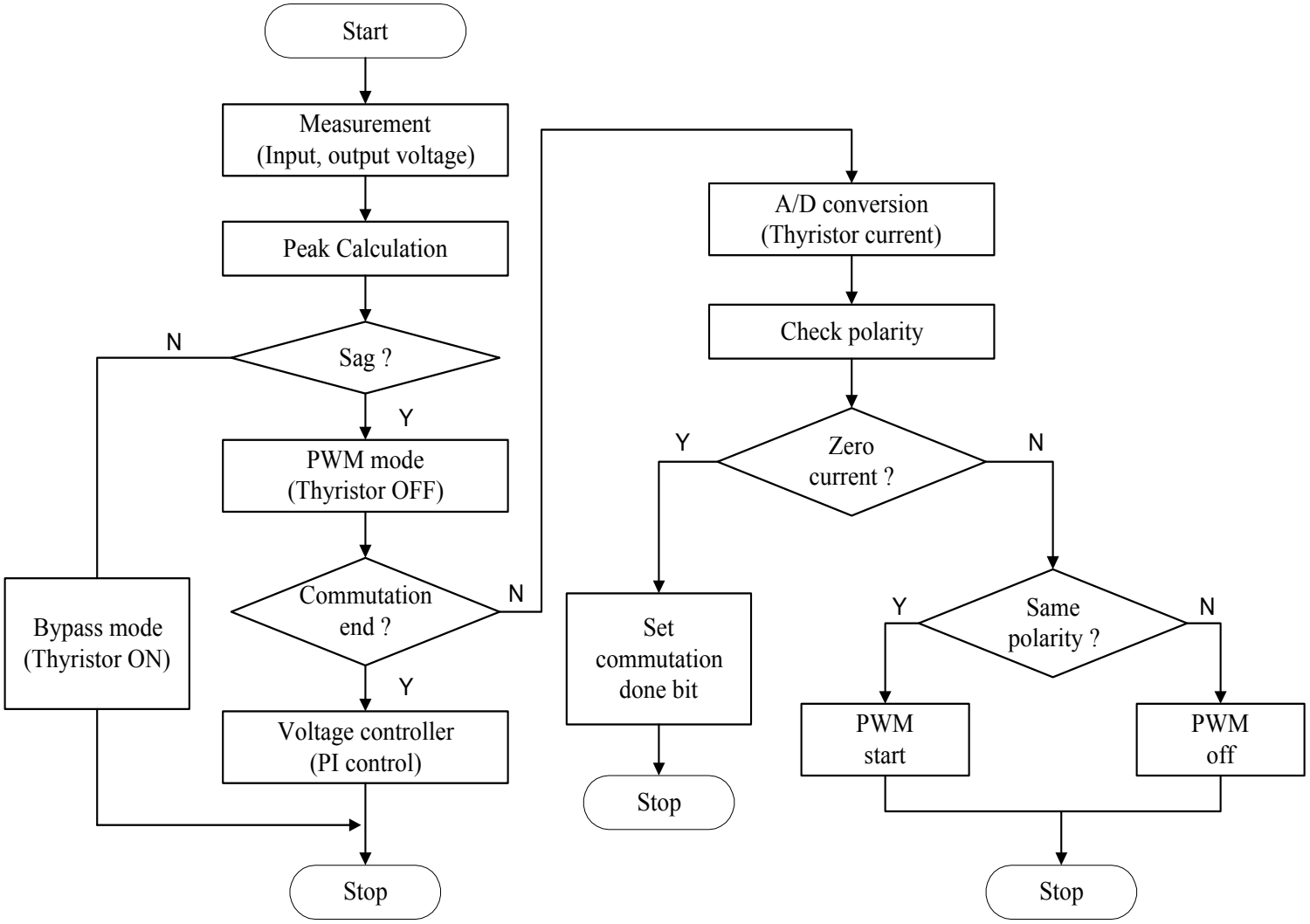


Figure 6.9. Flow chart of PWM interrupt service routine.

6.6 Experimental Results

Figure 6.10 shows the input voltage and the gate signals. From the top down appears the input voltage having a sag, the IGBT gate signal, the thyristor gate signal, and the relay signal. As explained in Chapter 5, it can be shown that after completing the thyristor commutation logic, the PWM switch starts to regulate the output voltage. The thyristor current during voltage sag event is shown in Figure 6.11. From the top down appears the input voltage, the PWM signal, the thyristor gate signal, and the thyristor current. The polarities of the input voltage and thyristor current in Figure 6.11 are the same, so that the controller starts PWM to commutate thyristors. It is clear that within a few microseconds, the thyristor current becomes zero.

The output voltage for the input voltage having a 20% sag, is shown in Figure 6.12. It is clear that the magnitude of the output voltage is well regulated using the proposed method. This corresponds well with the simulation results. The output voltage for a 40% input voltage dip is shown in Figure 6.13. The output voltage has some over voltage at the moment of voltage recovery.

Using D/A converters, the input and the output voltage, and the voltage error are shown in Figure 6.14. The input voltage, the magnitude of output voltage, the output voltage, and the voltage error are shown. It is shown that the voltage error becomes zero within a half cycle after the voltage sag occurs. It is clear that the output voltage remains constant during the sag event. Figure 6.15 shows the magnitude of the input voltage, the input voltage, the magnitude of the output voltage, and the output voltage. It is shown that the magnitudes of the voltages are well detected by the peak detection method.

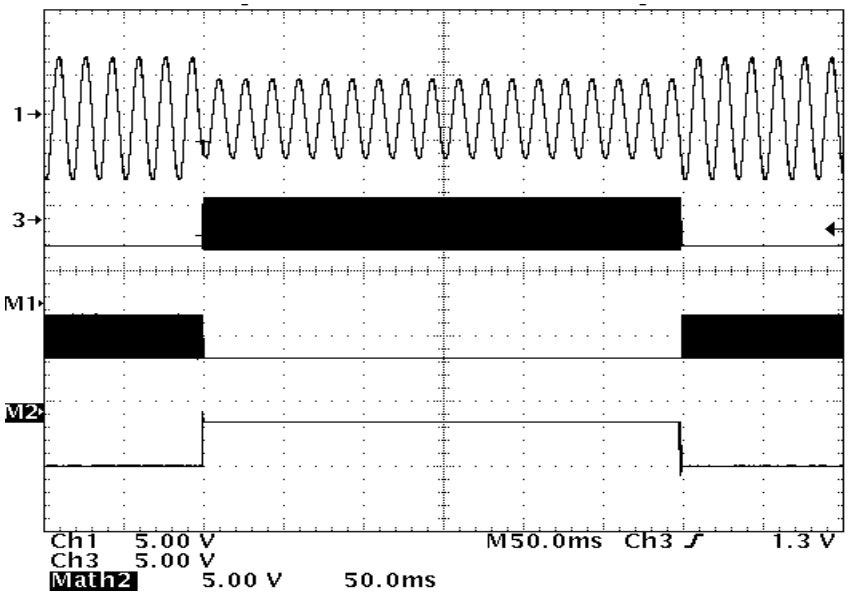


Figure 6.10. Gate signals corresponding to voltage sag event (from the top-downwards input voltage [135 V/div], PWM signal, thyristor gate signal, and relay signal).

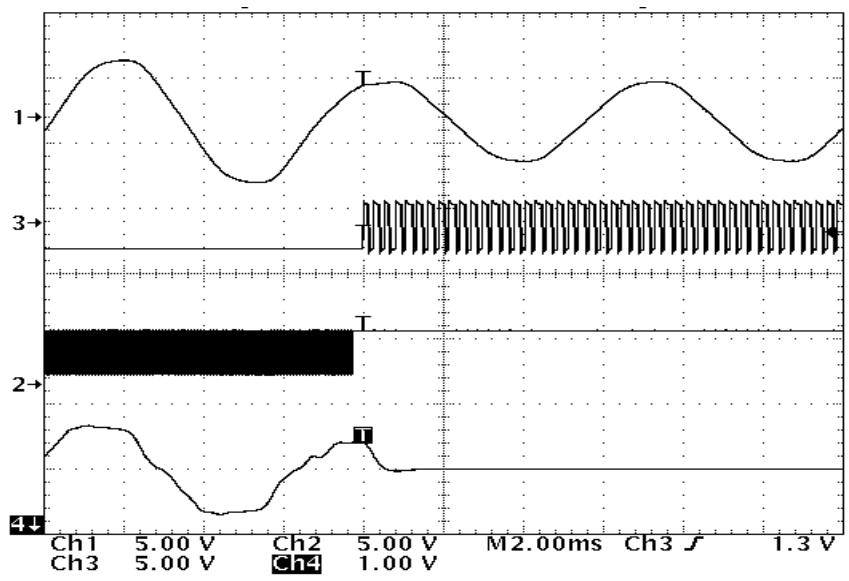


Figure 6.11. Thyristor current and related gate signals (from the top-downwards input voltage [135 V/div], PWM gate signal, thyristor gate signal, and thyrsitor current [4.5 A/div]).

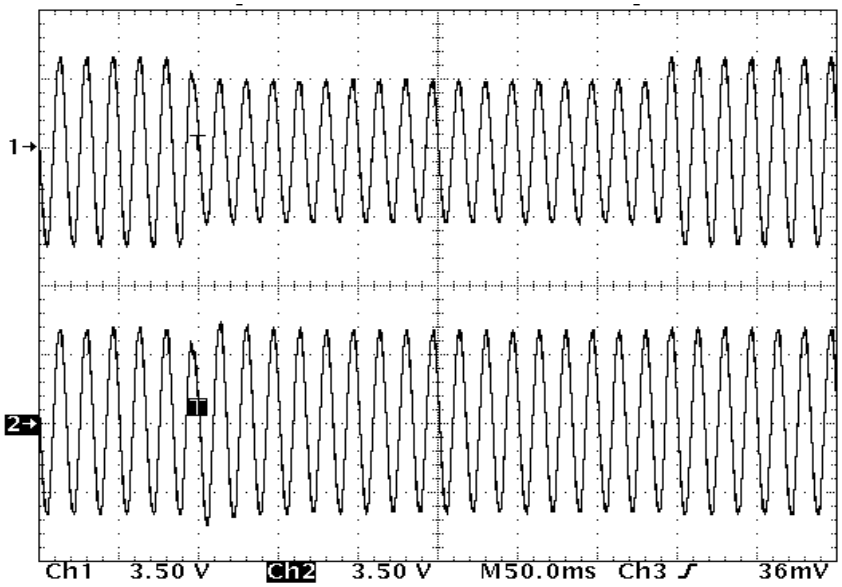


Figure 6.12. Output voltage and input voltage having 20% voltage sag (from the top-downwards input voltage [86.5 V/div], and output voltage [86.5 V/div]).

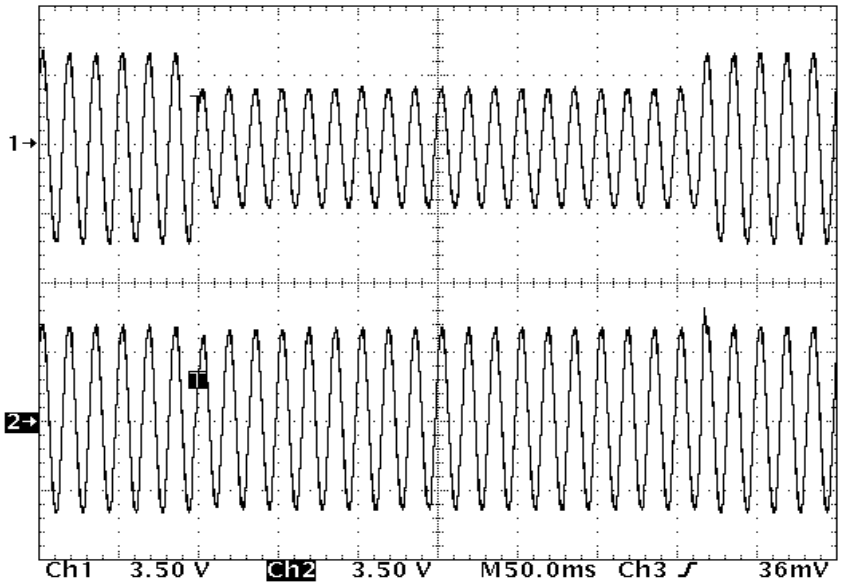


Figure 6.13. Output voltage and input voltage having 40% voltage sag (from the top-downwards input voltage [86.5 V/div], and output voltage [86.5 V/div]).

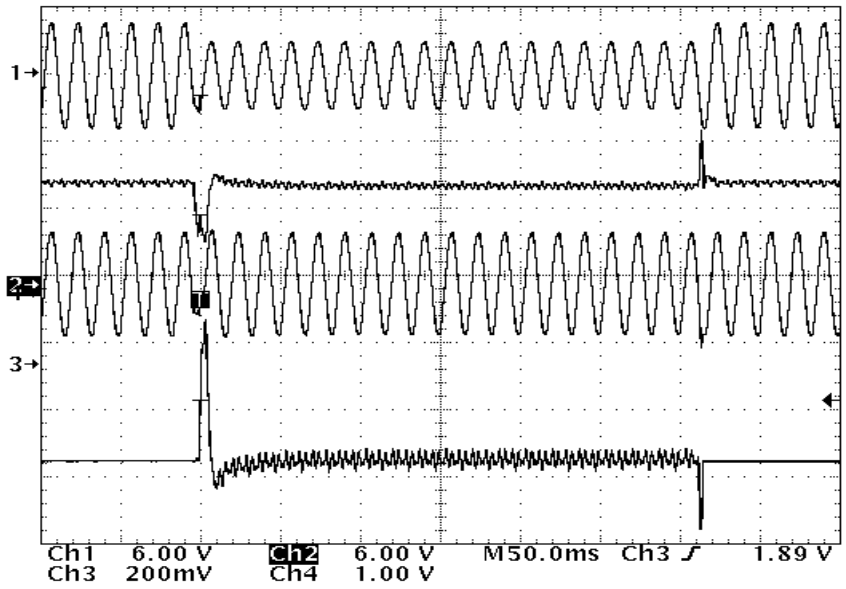


Figure 6.14. Voltage error signal and the magnitude of output voltage

(from the top-downwards input voltage [155 V/div], magnitude of output voltage [30 V/div], output voltage [155 V/div], and error of voltage magnitude [20 V/div]).

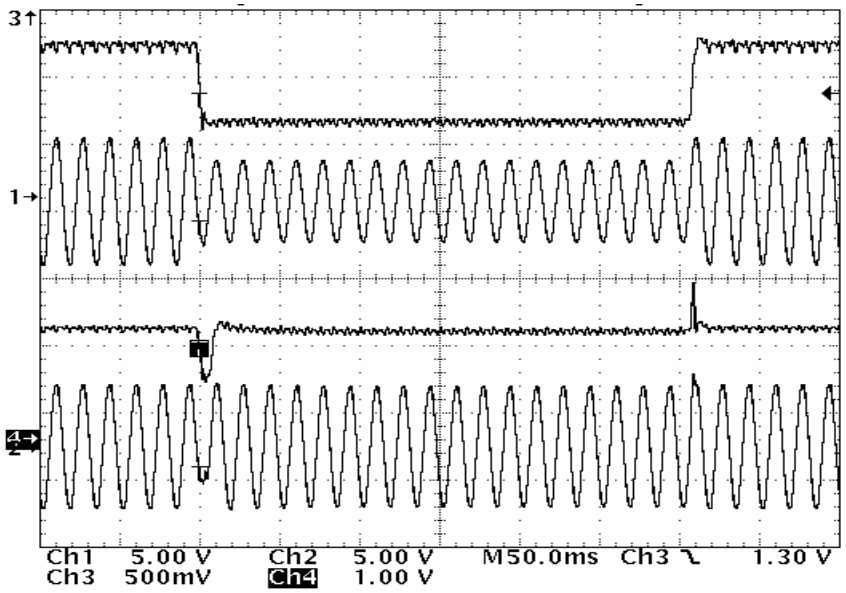


Figure 6.15. Input and output voltage and its magnitude,

measured by peak detection method

(from the top-downwards magnitude of input voltage [60 V/div], input voltage [127 V/div],magnitude of output voltage [30 V/div], and output voltage [127 V/div]).

6.7 Chapter Summary

To demonstrate the validity of the proposed scheme, the proposed voltage sag supporter based on a PWM-switched autotransformer has been implemented. The experiments have been performed under low voltage conditions. However, actual high voltage switches and their gate drivers were used, and the protection logics for the switch devices were implemented. The control board includes functions such as sensing, PWM generation, and memory etc. To precisely control the output voltage, the voltages were measured by a commercial 12 bit A/D converter, while the currents are detected by the A/D converters of the DSP. To generate voltage sag events, the sag generator using two IGBT switch blocks and an autotransformer was devised.

The assignment of the interrupts, the software routines of the voltage controller and main loop were explained. The PWM routine includes the subroutines ranging from recognizing sag condition to the post-process of voltage recovery. Similar to the simulation results, the experimental results showed that the proposed scheme controls the output voltage fast and accurately for the different voltage sag conditions.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusions

The purpose of this research was to develop a voltage sag mitigation device with low cost and high reliability. The scheme consisting of only one PWM switch and an autotransformer has been proposed. Given this topology, a more cost-effective and reliable sag supporter has been achieved primarily by reducing the number of switching components. In addition, by eliminating energy storage components the system is less expensive than many existing solutions.

A literature survey and a discussion of various existing methods were presented. The usage and operation principles were addressed, and deficiencies in the existing methods were mentioned, as well. The use of PWM-switched self-commutating devices gives rise to many possibilities for controlling the voltage and regulating power. From the literature survey, it was found that FACTS devices such as DVRs and STATCOMs yield good performance in controlling the output voltage.

This research has as its first priority, the development of a low-cost system that has a performance that is competitive to the FACTS devices. Therefore, an alternative topology from an inverter-based system was devised. Low cost was realized by using the proposed scheme that contains only a single switch and an autotransformer.

To determine the best solution, two circuit topologies were investigated: the "series type" and the "shunt type." It was concluded that the shunt type topology is a better choice because of the lower voltage stresses across the PWM switch (IGBT). From the voltage and current relation in an autotransformer, the current through the IGBT in the shunt type is twice of that in the series type. However, the voltage stress during an abnormal condition such as a lightning surge is a more significant factor in selecting the topology. Therefore, the shunt type was chosen for this work. The basic configuration, having a bypass switch was presented to increase the efficiency of the system during the bypass mode.

A voltage detection method known as "peak detection" was chosen to be the most appropriate for the application under study. This method was chosen since methods relying on a DQ transformation require three-phase voltage information, and the output of the DQ transformation has a 120 Hz ripple in the case of an unbalanced three-phase supply. It was shown that because of the filtering of the 120 Hz ripple, there is no difference between the detection time of the DQ method and that of the peak detection method. Next, a voltage controller based on a PI controller was presented, and it was shown that the controller that includes feed-forward and anti-windup results in a fast dynamic response and an acceptable output voltage overshoot.

The IGBT switch block and the snubber design were also presented in Chapter 4. The IGBT switch is surrounded by an AC rectifier bridge, and therefore only one active switch is necessary to conduct load current in both directions. The IGBT snubber circuit limits the transient voltage across the IGBT during the off-state, and it was shown that the selected snubber circuit values suppress the turn-off voltage to a level below the forward voltage limits of the device.

When the voltage controller detects the sag condition, the transition from bypass mode to PWM mode must be done as quickly as possible. Since the thyristors are not self-commutable devices, the commutation depends on the condition of the input voltage and the thyristor current. The commutation logic for the thyristor was proposed, and simulations were done under various conditions of the input voltage and the thyristor current for positive and negative polarities. The commutation logic using the input current and the input voltage provides a low-cost solution, because the current sensor located at the input terminal requires a lower voltage isolation level than that located in the thyristor assembly. The commutation logic utilizing the input current used the fact that before turning off the thyristor, the polarity of the thyristor current and the input current are same.

The simulations have been done to show that the proposed voltage sag supporter scheme regulates the output voltage with quick reaction and high precision during voltage sag events. It was also shown that because of the voltage detection delay, there exists an output voltage overshoot transient at the moment of the voltage recovery.

Software-based and hardware-based fault detection logic was next presented in Chapter 5. An EPLD logic circuit (hardware-based) was implemented to detect faults in the IGBT and the thyristor gate drivers during PWM and bypass mode. Additionally, software-based fault detection was implemented to signal faults in the relay and components such as sensors and thyristors. Since the switches are serially connected, the gate drivers do not inhibit the individual gate signal even if there exists a fault or short circuit. Prohibiting the individual gate signal without turning of all the series switches causes an over voltage in the device that is blocking. A software routine in the voltage controller, which includes recognizing sag condition, and the process of recovery, were explained.

To simulate voltage sag events, the sag generator using two IGBT switch blocks and an autotransformer was designed. To demonstrate validity of the proposed scheme, experiment was carried out, and the results were presented in Chapter 6.

7.2 Contributions

This research can be divided into two phases. In the first phase, this research focused on followings (i) Devising voltage sag mitigation scheme with low cost, (ii) Investigating performance of the proposed system, (iii) Design the each component to meet design specifications. The second phase focused on the implementation of the proposed scheme including system protection. The second phase includes followings (i) Investigating possible faults in the system, (ii) Design driver circuits with protection circuits and their

power supply scheme capable of high voltage isolation, (iii) Design control board, (iv) Experimental validations of the proposed scheme under realistic conditions.

Based on the research described in the chapters about design, a patent application titled "Voltage SAG and Over-voltage Compensation Device with Pulse Width Modulating Switch Connected in Series with Autotransformer" has been submitted. The main contributions of current research work to the field of voltage sag mitigation are summarized as follows:

- A comprehensive literature survey of voltage sag mitigation methods and a comparison of these methods have been presented.
- A method for voltage sag mitigation using a PWM switch and an autotransformer is proposed. It was shown that it has a fast response while regulating the output voltage with high precision.
- A design methodology for the RC turn-off snubber for the IGBT is presented and is verified through simulations.
- Various voltage detection methods have been surveyed and evaluated. The peak detection method has been chosen as a result of the research.
- A voltage controller based on PI control has been proposed, in which a feed-forward and anti-wind-up scheme are added to get a fast dynamic response.
- A thyristor commutation logic using the input voltage with the thyristor current or the input current is proposed.
- A fault detection logic based on either hardware or software is proposed.

7.3 Recommendations for Future Research

So far, a cost-effective voltage sag mitigation method and its control logic have been proposed and investigated. The performance of the scheme has been verified by simulations and experiments using a low voltage (120 V). It is necessary to confirm the validity of the proposed system under a high input voltage. The following tasks need to be completed before a high voltage can be applied to the proposed system. It is necessary to check the nonlinearity of voltage distribution caused by the serial connection of IGBTs and thyristors. Using simulations, the voltage across the PWM switch corresponding to the variation of the snubber capacitor and the resistor was checked. Gate signals having a different delay time (which is caused by different time delays in hardware circuits involved in gate driver) were used. Even though the simulation result showed that the peak voltage during IGBT turn-off remains below the forward blocking voltage of the 6.5 kV rating IGBT, it is nevertheless necessary to check the voltage distribution across multiple series IGBTs for 25 kV system.

A protection circuit such as over current protection should work fast and precisely under high voltage condition. In the laboratory condition, the current transformers for measuring the input current and the thyristor current are located near the control board, but in the 25 kV case the sensors can not be placed near the control board. BNC cables or twisted wires with a relatively long distance are used to transmit the current signals. Therefore, it is likely that the signals will be corrupted by electrical noise caused by a high voltage switch in the 25 kV application. In order to get noise-free signals, fiber optic cables can be considered to transmit the signal using additional A/D converters

located near current sensors. There are two boards as shown in Figure 6.5. One is a commercially available EVM board having 16 bit DSP, and the other is the control board designed based on as a results of this research. The 16 bit DSP shows a fast and precise control performance of the voltage sag mitigation. In real product, many additional programs, such as user interface and communication program will be necessary. Therefore, to improve the performance, it might be considered to use a 32 bit DSP.

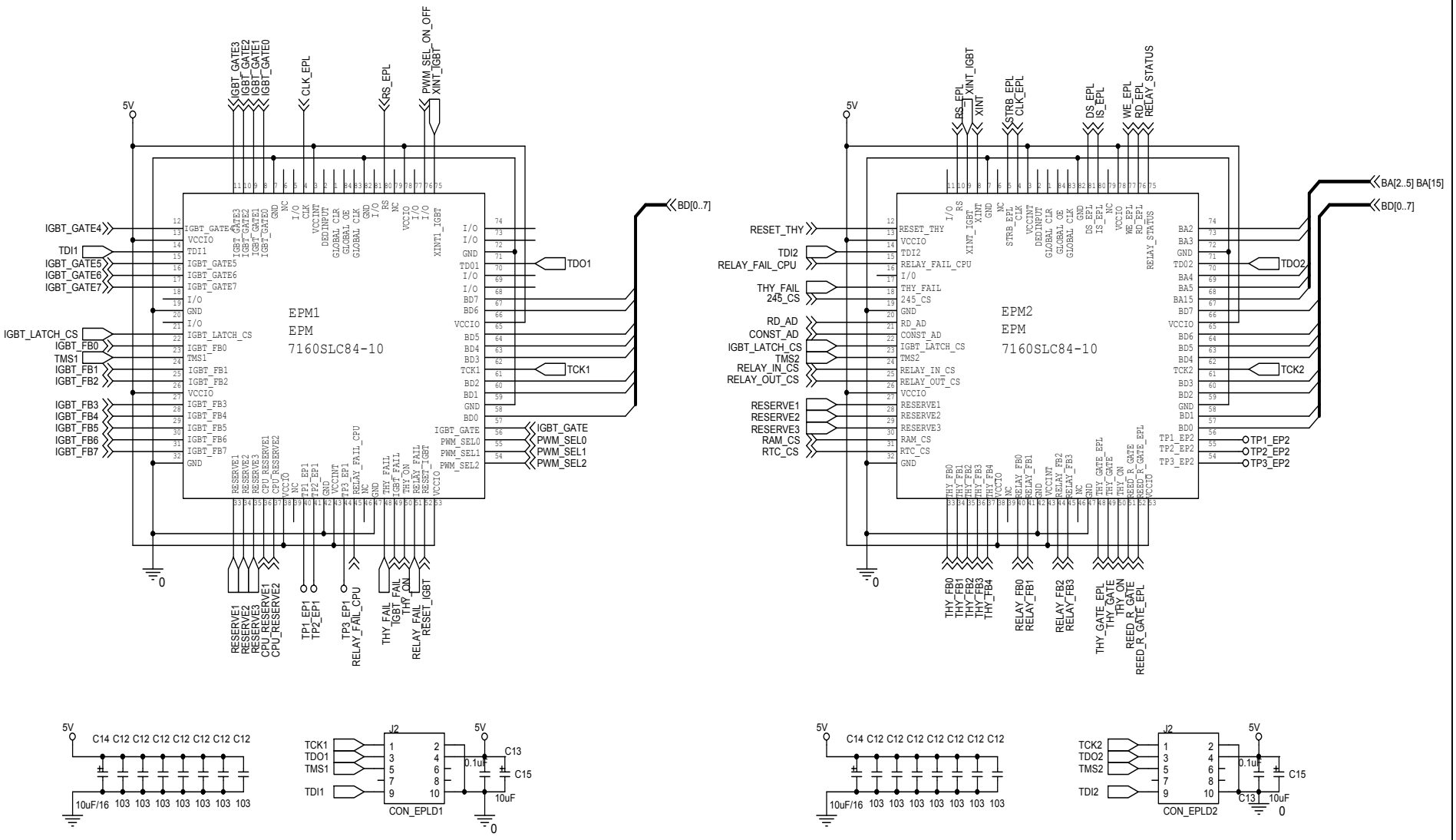
In addition, it is preferable to realize the controller using one board instead of two boards. Some circuits in the control board can replace the circuits in the EVM board. For example, the EPLD logic circuit, which works for fault detection and address decoding, can replace the GAL in the EVM board, because the GAL does the same function of address decoding for the devices in the EVM board. The control board also has buffers for address and data bus. Remaining circuits in the EVM board for control purposes are D/A converters, communication, and the DSP with its peripheral circuits. Therefore, it does not need to use the EVM board if the above circuits such as DA converters are implemented in the control board.

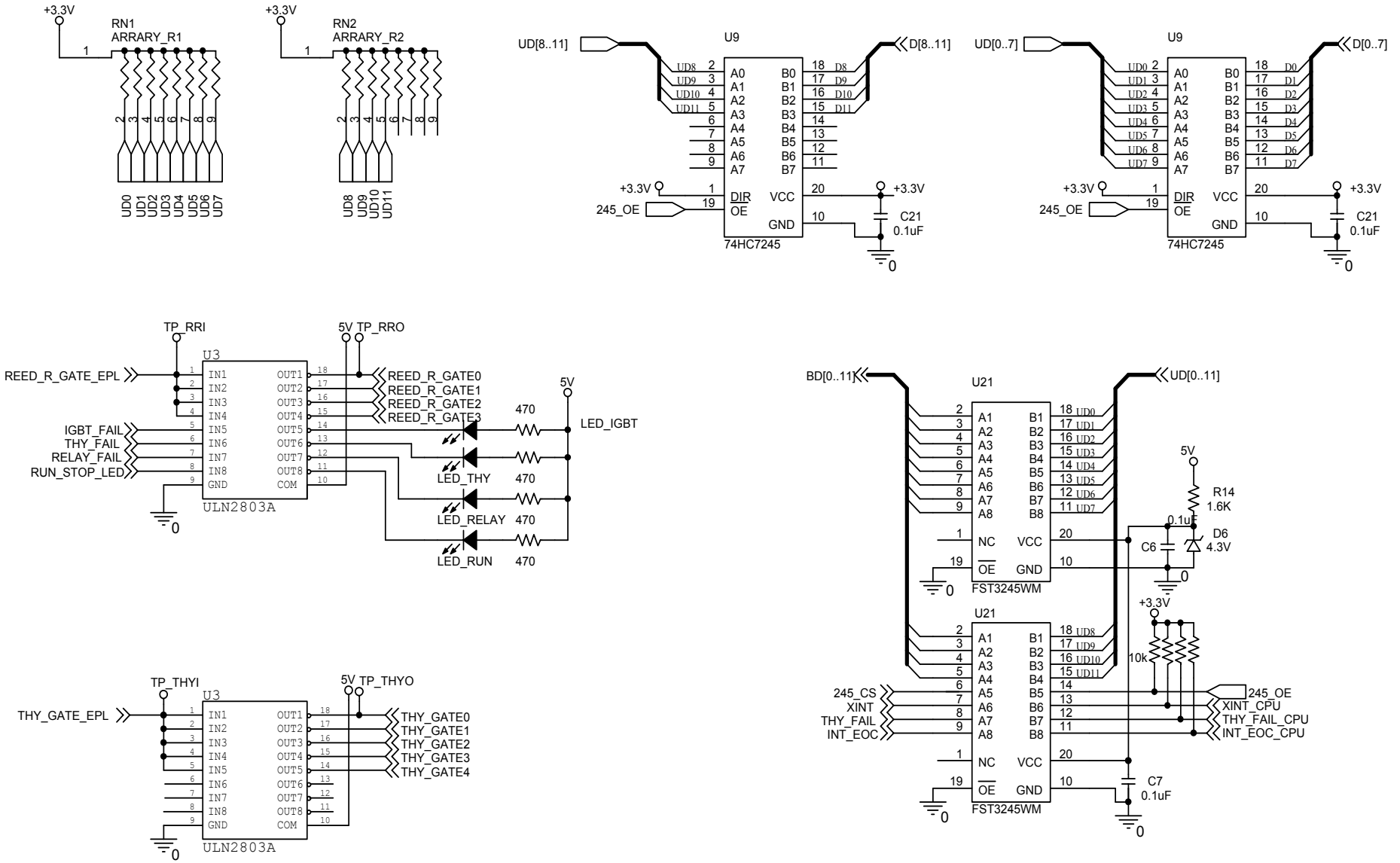
It has been shown by simulation and laboratory experimental results that when the magnitude of the voltage sag becomes deeper, the overshoot at the voltage recovery becomes higher because of the detection delay. Many approaches for reducing this voltage overshoot have been experimented with, but the proposed system still shows some amount of overshoot. This problem should be considered in future to improve the performance of the proposed scheme.

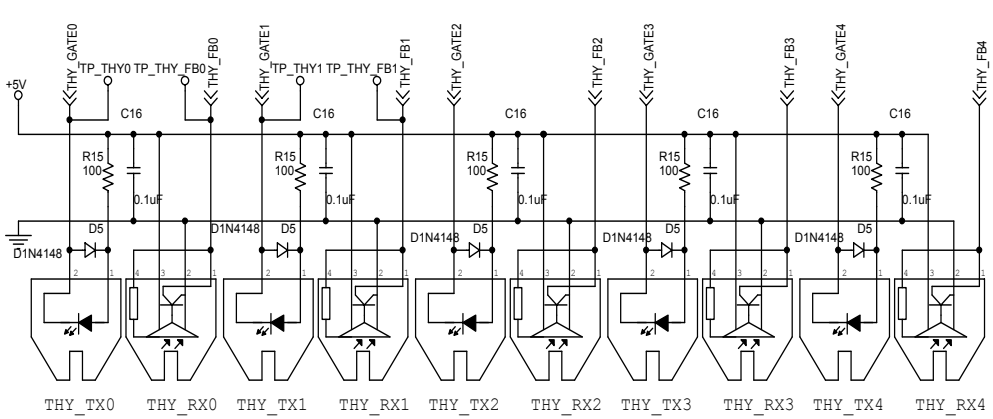
APPENDIX

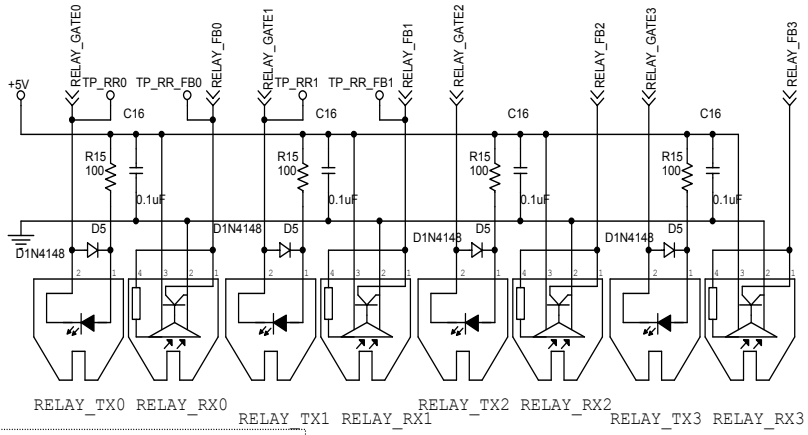
SCHEMATIC OF THE CONTROL BOARD

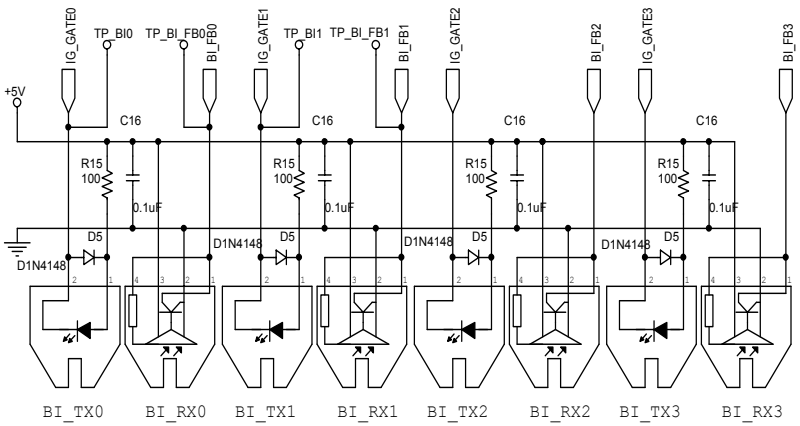
This appendix shows the schematic of the control board used for the experimental validations. This control board includes EPLDs, sensing circuits (voltage, current, and temperature), external memory, and digital I/O etc.

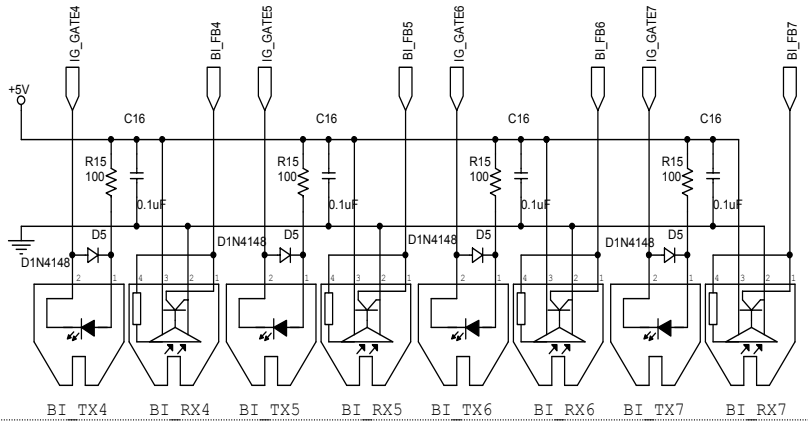

EPM1
EPM
7160SLC84-10
EPM2
EPM
7160SLC84-10
5V
IGBT_GATE3
IGBT_GATE2
IGBT_GATE1
IGBT_GATE0
CLK_EPL
RS_EPL
PWM_SEL_ON_OFF
XINT_IGBT
BD[0..7]
IGBT_GATE4
TDI1
IGBT_GATE5
IGBT_GATE6
IGBT_GATE7
IGBT_LATCH_CS
IGBT_FB0
TMS1
IGBT_FB1
IGBT_FB2
IGBT_FB3
IGBT_FB4
IGBT_FB5
IGBT_FB6
IGBT_FB7
TDO1
TCK1
IGBT_GATE
PWM_SEL0
PWM_SEL1
PWM_SEL2
RESERVE1
RESERVE2
RESERVE3
CPU_RESERVE1
CPU_RESERVE2
TP1_EP1
TP2_EP1
TP3_EP1
RELAY_FAIL_CPU
THY_FAIL
IGBT_FAIL
THY_ON
RELAY_FAIL
RESET_IGBT
XINT
STRB_EPL
CLK_EPL
DS_EPL
IS_EPL
WE_EPL
RD_EPL
RELAY_STATUS
BA[2..5] BA[15]
RESET_THY
TDI2
RELAY_FAIL_CPU
THY_FAIL
245_CS
RD_AD
CONST_AD
TMS2
RELAY_IN_CS
RELAY_OUT_CS
RESERVE1
RESERVE2
RESERVE3
RAM_CS
RTC_CS
TDO2
TCK2
TP1_EP2
TP2_EP2
TP3_EP2
THY_FB0
THY_FB1
THY_FB2
THY_FB3
THY_FB4
RELAY_FB0
RELAY_FB1
RELAY_FB2
RELAY_FB3
THY_GATE_EPL
THY_GATE
THY_ON
REED_R_GATE
REED_R_GATE_EPL
C14 C12 C12 C12 C12 C12 C12 C12
10uF/16 103 103 103 103 103 103 103
J2
CON_EPLD1
CON_EPLD2
0.1uF
C13
C15
10uF
0


+3.3V
RN1
ARRARY_R1
UD0
UD1
UD2
UD3
UD4
UD5
UD6
UD7
RN2
ARRARY_R2
UD8
UD9
UD10
UD11
U9
UD[8..11]
D[8..11]
74HC7245
245_OE
C21
0.1uF
UD[0..7]
D[0..7]
TP_RRI
5V TP_RRO
U3
REED_R_GATE_EPL
REED_R_GATE0
REED_R_GATE1
REED_R_GATE2
REED_R_GATE3
IGBT_FAIL
THY_FAIL
RELAY_FAIL
RUN_STOP_LED
LED_IGBT
LED_THY
LED_RELAY
LED_RUN
470
ULN2803A
TP_THYI
5V TP_THYO
THY_GATE_EPL
THY_GATE0
THY_GATE1
THY_GATE2
THY_GATE3
THY_GATE4
BD[0..11]
U21
FST3245WM
R14
1.6K
C6
0.1uF
D6
4.3V
10k
245_CS
XINT
THY_FAIL
INT_EOC
245_OE
XINT_CPU
THY_FAIL_CPU
INT_EOC_CPU
C7
0.1uF

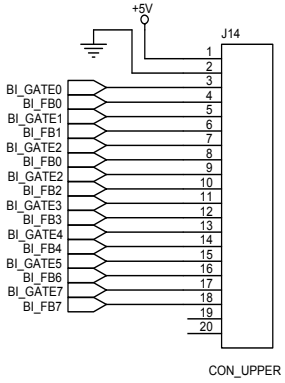


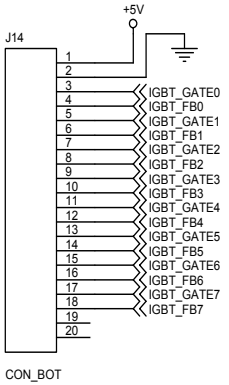


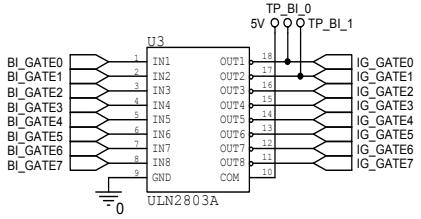


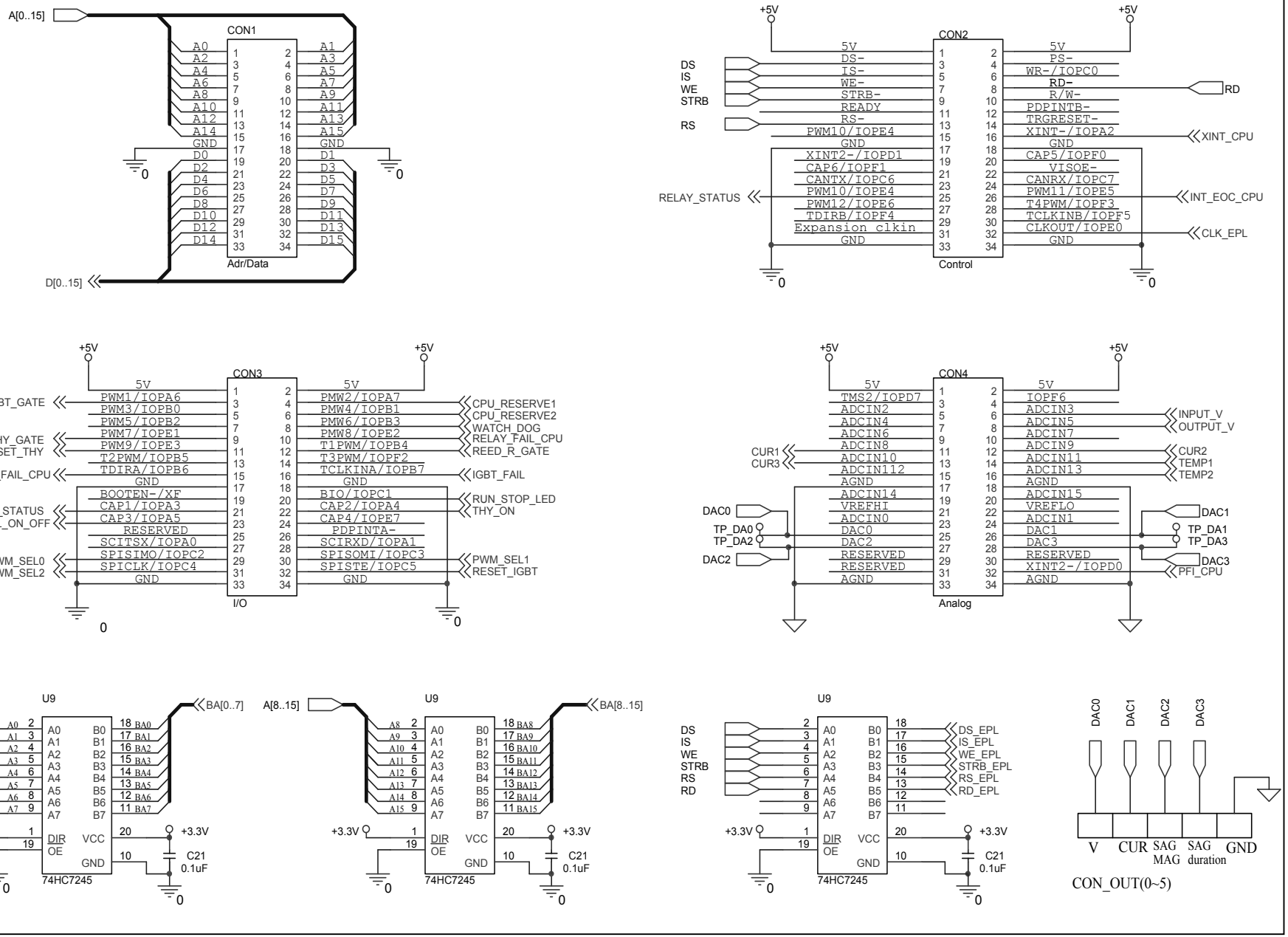


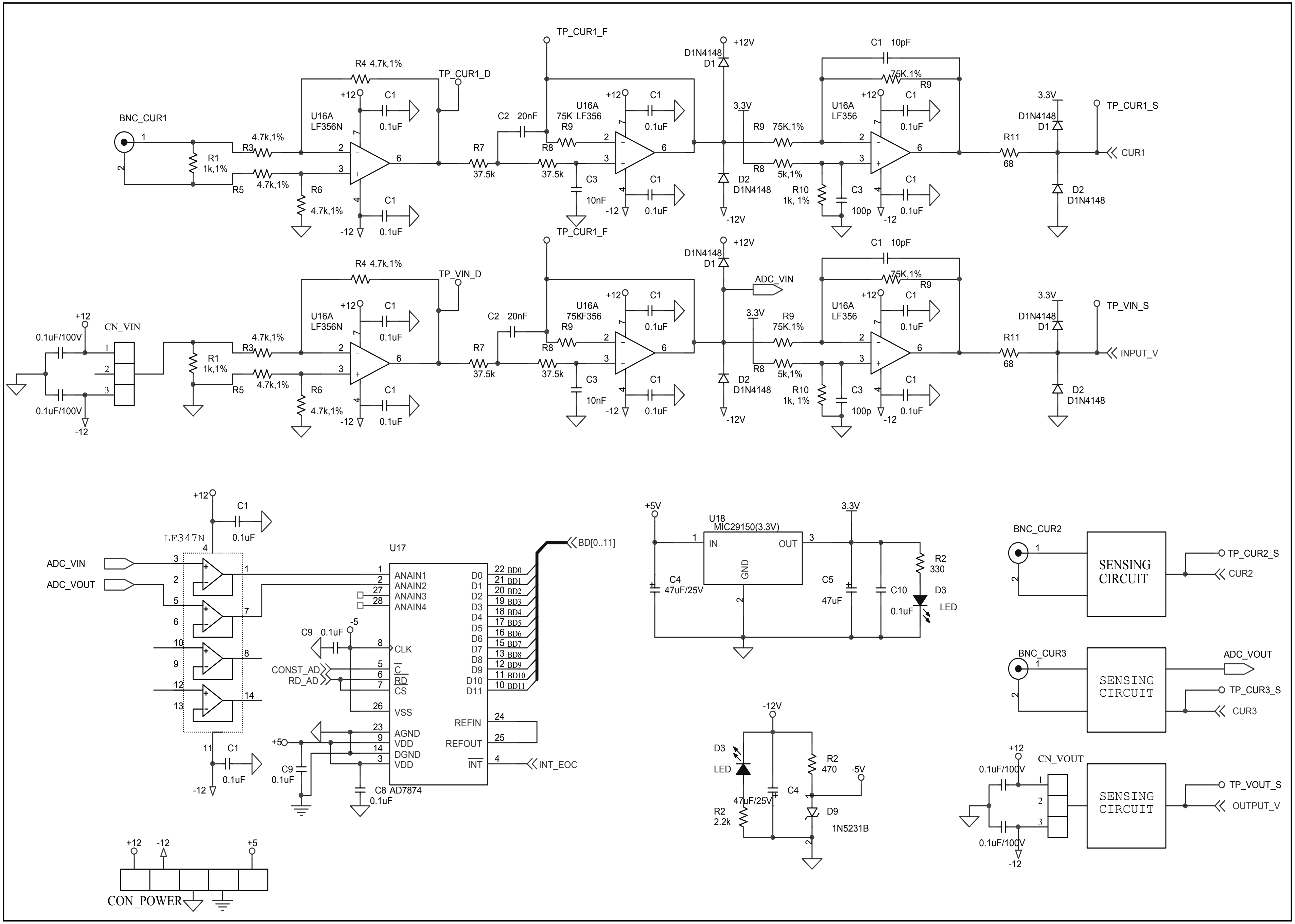
UPPER FIBER OPTIC BOARD

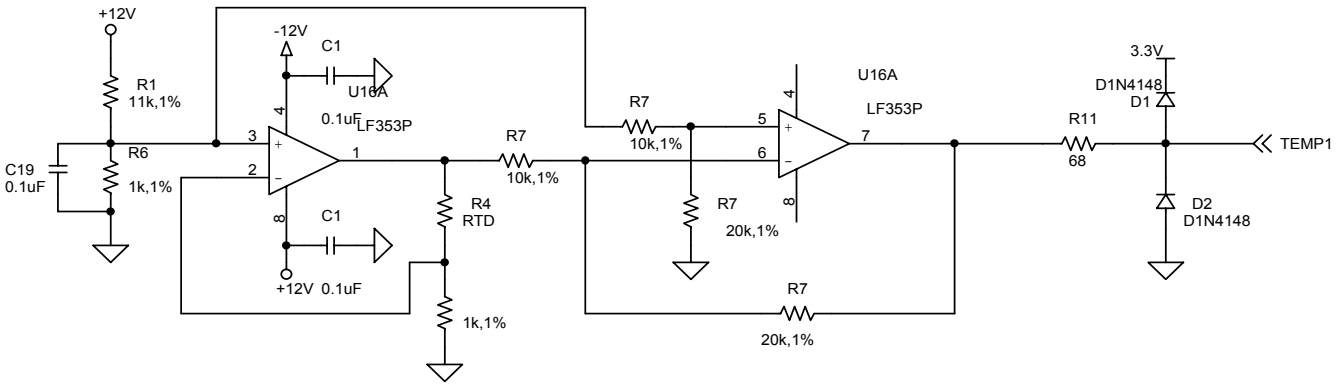


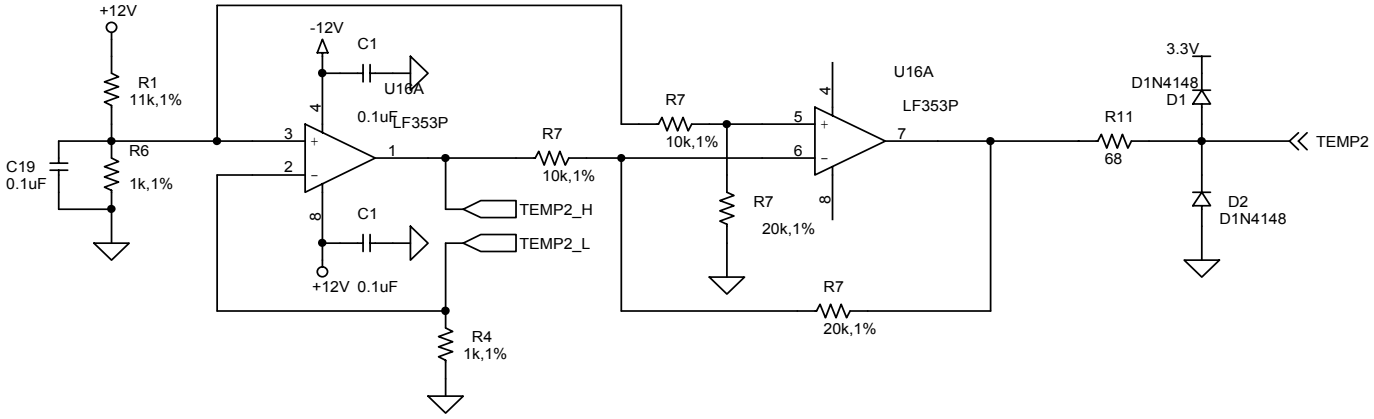


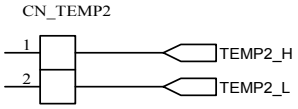


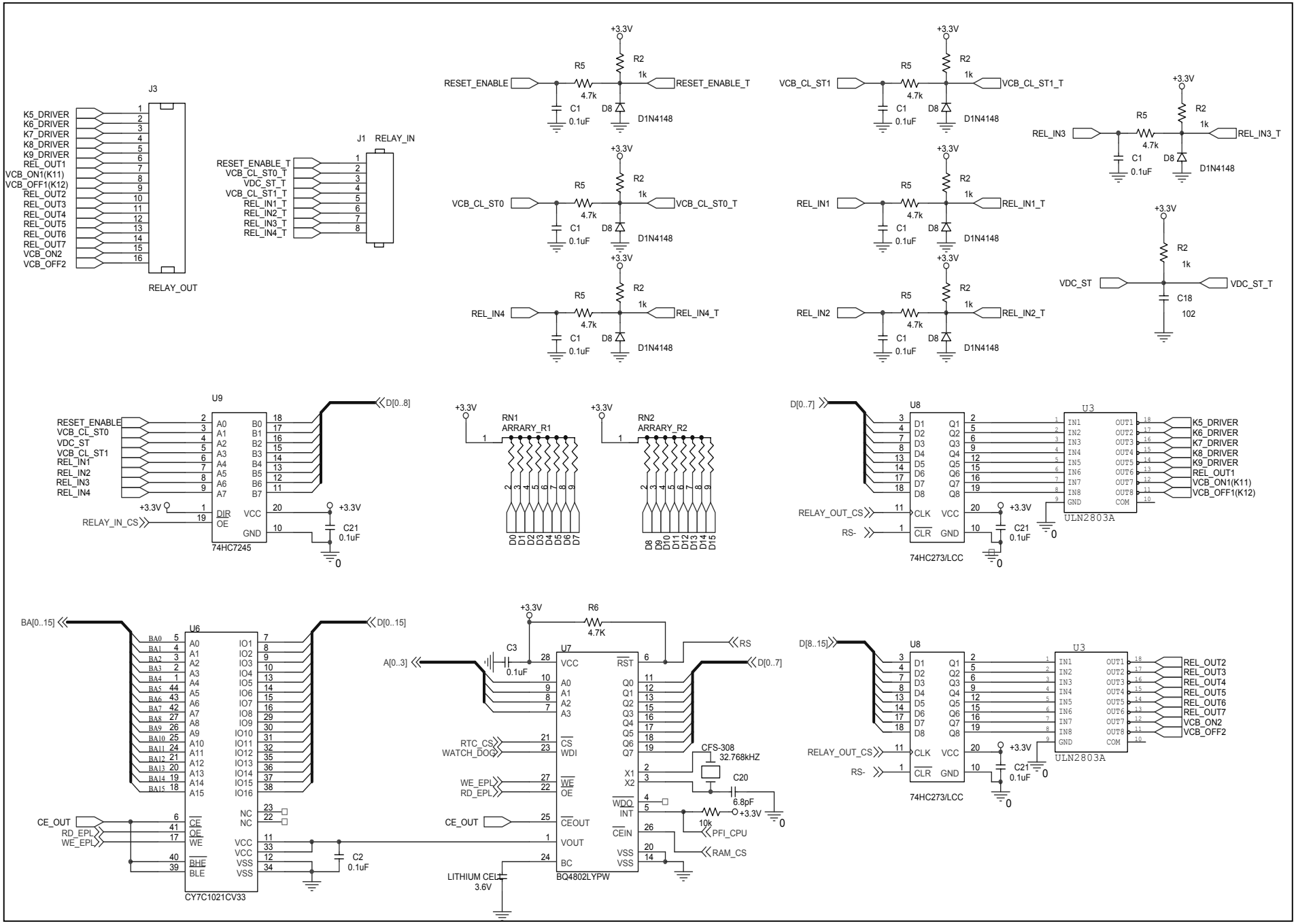

A[0..15]
CON1
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 GND GND D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
Adr/Data
D[0..15]
0
+5V
CON2
5V 5V DS- PS- IS- WR-/IOPC0 WE- RD- STRB- R/W- READY PDPINTB- RS- TRGRESET- PWM10/IOPE4 XINT-/IOPA2 GND GND XINT2-/IOPD1 CAP5/IOPF0 CAP6/IOPF1 VISOE- CANTX/IOPC6 CANRX/IOPC7 PWM10/IOPE4 PWM11/IOPE5 PWM12/IOPE6 T4PWM/IOPF3 TDIRB/IOPF4 TCLKINB/IOPF5 Expansion clkin CLKOUT/IOPE0 GND GND
DS IS WE STRB RS
RD XINT_CPU RELAY_STATUS INT_EOC_CPU CLK_EPL
Control
CON3
5V 5V PWM1/IOPA6 PWM2/IOPA7 PWM3/IOPB0 PWM4/IOPB1 PWM5/IOPB2 PWM6/IOPB3 PWM7/IOPE1 PWM8/IOPE2 PWM9/IOPE3 T1PWM/IOPB4 T2PWM/IOPB5 T3PWM/IOPF2 TDIRA/IOPB6 TCLKINA/IOPB7 GND GND BOOTEN-/XF BIO/IOPC1 CAP1/IOPA3 CAP2/IOPA4 CAP3/IOPA5 CAP4/IOPE7 RESERVED PDPINTA- SCITSX/IOPA0 SCIRXD/IOPA1 SPISIMO/IOPC2 SPISOMI/IOPC3 SPICLK/IOPC4 SPISTE/IOPC5 GND GND
IGBT_GATE THY_GATE RESET_THY THY_FAIL_CPU RELAY_STATUS PWM_SEL_ON_OFF PWM_SEL0 PWM_SEL2
CPU_RESERVE1 CPU_RESERVE2 WATCH_DOG RELAY_FAIL_CPU REED_R_GATE IGBT_FAIL RUN_STOP_LED THY_ON PWM_SEL1 RESET_IGBT
I/O
CON4
5V 5V TMS2/IOPD7 IOPF6 ADCIN2 ADCIN3 ADCIN4 ADCIN5 ADCIN6 ADCIN7 ADCIN8 ADCIN9 ADCIN10 ADCIN11 ADCIN112 ADCIN13 AGND AGND ADCIN14 ADCIN15 VREFHI VREFLO ADCIN0 ADCIN1 DAC0 DAC1 DAC2 DAC3 RESERVED RESERVED XINT2-/IOPD0 AGND AGND
CUR1 CUR3 DAC0 TP_DA0 TP_DA2 DAC2
INPUT_V OUTPUT_V CUR2 TEMP1 TEMP2 DAC1 TP_DA1 TP_DA3 DAC3 PFI_CPU
Analog
A[0..7]
U9
A0 A1 A2 A3 A4 A5 A6 A7
A0 A1 A2 A3 A4 A5 A6 A7 B0 B1 B2 B3 B4 B5 B6 B7
BA0 BA1 BA2 BA3 BA4 BA5 BA6 BA7
BA[0..7]
DIR OE VCC GND
+3.3V
C21 0.1uF
74HC7245
A[8..15]
A8 A9 A10 A11 A12 A13 A14 A15
BA8 BA9 BA10 BA11 BA12 BA13 BA14 BA15
BA[8..15]
DS IS WE STRB RS RD
DS_EPL IS_EPL WE_EPL STRB_EPL RS_EPL RD_EPL
DAC0 DAC1 DAC2 DAC3
V CUR SAG MAG SAG duration GND
CON_OUT(0~5)


BNC_CUR1
R1 1k,1%
R3 4.7k,1%
R5 4.7k,1%
R6 4.7k,1%
R4 4.7k,1%
U16A LF356N
TP_CUR1_D
TP_CUR1_F
C2 20nF
R7 37.5k
R8 37.5k
R9 75K
U16A LF356
C3 10nF
D1N4148 D1
D2 D1N4148
+12V
-12V
3.3V
R9 75K,1%
R8 5k,1%
R10 1k, 1%
C3 100p
C1 10pF
75K,1% R9
R11 68
TP_CUR1_S
CUR1
CN_VIN
0.1uF/100V
TP_VIN_D
ADC_VIN
TP_VIN_S
INPUT_V
LF347N
ADC_VOUT
U17
ANAIN1
ANAIN2
ANAIN3
ANAIN4
CLK
CONST_AD
RD_AD
CS
VSS
AGND
VDD
DGND
REFIN
REFOUT
INT
INT_EOC
C8 AD7874
C9 0.1uF
BD[0..11]
+5V
U18
MIC29150(3.3V)
IN
OUT
GND
C4 47uF/25V
C5 47uF
C10 0.1uF
R2 330
D3 LED
-12V
R2 470
-5V
D9 1N5231B
R2 2.2k
BNC_CUR2
SENSING CIRCUIT
TP_CUR2_S
CUR2
BNC_CUR3
TP_CUR3_S
CUR3
CN_VOUT
TP_VOUT_S
OUTPUT_V
CON_POWER


+12V
-12V
C1
U16A
0.1uF
LF353P
R1
11k,1%
R6
1k,1%
C19
0.1uF
R4
RTD
1k,1%
R7
10k,1%
R7
20k,1%
U16A
LF353P
3.3V
D1N4148
D1
R11
68
TEMP1
D2
D1N4148


+12V
-12V
C1
U16A
0.1uF
LF353P
R1
11k,1%
R6
1k,1%
C19
0.1uF
R4
1k,1%
R7
10k,1%
R7
20k,1%
U16A
LF353P
3.3V
D1N4148
D1
R11
68
TEMP2
D2
D1N4148
TEMP2_H
TEMP2_L


CN_TEMP2
1
2
TEMP2_H
TEMP2_L


J3
K5_DRIVER
K6_DRIVER
K7_DRIVER
K8_DRIVER
K9_DRIVER
REL_OUT1
VCB_ON1(K11)
VCB_OFF1(K12)
REL_OUT2
REL_OUT3
REL_OUT4
REL_OUT5
REL_OUT6
REL_OUT7
VCB_ON2
VCB_OFF2
RELAY_OUT
J1 RELAY_IN
RESET_ENABLE_T
VCB_CL_ST0_T
VDC_ST_T
VCB_CL_ST1_T
REL_IN1_T
REL_IN2_T
REL_IN3_T
REL_IN4_T
+3.3V
R5
4.7k
R2
1k
RESET_ENABLE
RESET_ENABLE_T
C1
0.1uF
D8
D1N4148
VCB_CL_ST1
VCB_CL_ST1_T
REL_IN3
REL_IN3_T
VCB_CL_ST0
VCB_CL_ST0_T
REL_IN1
REL_IN1_T
REL_IN4
REL_IN4_T
REL_IN2
REL_IN2_T
VDC_ST
VDC_ST_T
C18
102
U9
74HC7245
RESET_ENABLE
VCB_CL_ST0
VDC_ST
VCB_CL_ST1
REL_IN1
REL_IN2
REL_IN3
REL_IN4
D[0..8]
RELAY_IN_CS
DIR
OE
VCC
GND
C21
0.1uF
RN1
ARRARY_R1
RN2
ARRARY_R2
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D[0..7]
U8
74HC273/LCC
RELAY_OUT_CS
RS-
CLK
CLR
U3
ULN2803A
K5_DRIVER
K6_DRIVER
K7_DRIVER
K8_DRIVER
K9_DRIVER
REL_OUT1
VCB_ON1(K11)
VCB_OFF1(K12)
BA[0..15]
U6
CY7C1021CV33
CE_OUT
RD_EPL
WE_EPL
C2
0.1uF
A[0..3]
U7
BQ4802LYPW
R6
4.7K
C3
0.1uF
RS
RTC_CS
WATCH_DOG
WE_EPL
RD_EPL
CFS-308
32.768kHZ
C20
6.8pF
10k
PFI_CPU
RAM_CS
LITHIUM CELL
3.6V
D[8..15]
REL_OUT2
REL_OUT3
REL_OUT4
REL_OUT5
REL_OUT6
REL_OUT7
VCB_ON2
VCB_OFF2

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