Research article

A wet-etch method with improved yield for realizing polysilicon resistors in batch fabrication of MEMS pressure sensor

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Abstract

Purpose – The purpose of this paper is to present a selective wet-etching method of boron doped low-pressure chemical vapour deposition (LPCVD) polysilicon film for the realization of piezoresistors over the bulk micromachined diaphragm of (100) silicon with improved yield and uniformity.

Design/methodology/approach – The method introduces discretization of the LPCVD polysilicon film using prior etching for the grid thus dividing each chip on the entire wafer. The selective etching of polysilicon for realizing of piezoresistors is limited to each chip area with individual boundaries.

Findings – The method provides a uniform etching on the entire silicon wafer irrespective of its size and leads to economize the fabrication process in a batch production environment with improved yield.

Research limitations/implications – The method introduces one extra process step of photolithography and subsequent etching for discretizing the polysilicon film.

Practical implications – The method is useful to enhance yield while defining metal lines for contact purposes on fabricated electronic structures using microelectronics. Stress developed in LPCVD polysilicon can be removed using proposed approach of discretization of polysilicon film.

Originality/value – The work is an outcome of regular fabrication work using conventional approaches in an R&D environment. The proposed method replaces the costly reactive ion etching techniques with stable reproducibility and ease in its implementation.

Keywords Resistors, Silicon, Films (states of matter), Batch manufacturing

Paper type Research paper

Introduction

In the fabrication of polysilicon piezoresistive pressure sensor using silicon bulk micromachining, polysilicon resistors are realized on the silicon diaphragm in full or half wheatstone bridge configuration (Akhtar *et al.*, 2003a). A large number of arrays of the diaphragm are accommodated on the silicon wafer in case of the batch fabrication of the sensors. The number of arrays increases with the size of the silicon wafer. In order to make the fabrication process cost effective, wet etching is used for the delineation of polysilicon resistors in a selective manner. Employing standard photolithography, pattern of the polysilicon resistors is protected with photoresist and the exposed polysilicon is etched out from the entire silicon wafer either using reactive ion etching (RIE) or wet etching. However, in the wet process, fast etching takes place on the wafer edge. The etching process starts from the wafer edges and moves towards the center of the wafer for a uniform thick polysilicon layer. This results into resistors with over-etching, particularly, near the

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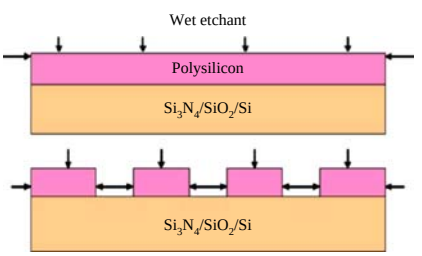
wafer edges, and leads to low yield. Non-uniformity in the polysilicon resistor's values is the outcome of low yield. Handling of selective etching process also becomes a tricky workmanship with practically no control over reproducibility. In order to overcome the non-uniform wet etching of polysilicon, dry etching is used to enhance the yield by uniform etching of polysilicon. In the dry etching process selectivity of polysilicon in respect of under layers of silicon nitride and silicon dioxide is poor, owing to which a fine control on the recipe for dry etching and etching time need to be optimized very accurately. Besides, the dry etch process is not a cost effective. The unavoidable stress developed in the low-pressure chemical vapour deposition (LPCVD) polysilicon during its deposition, the entire silicon wafer becomes oval and a non-uniform etching takes place during RIE. With the growing demand of sensors in a number of varieties of applications, a great deal of efforts is to reduce their manufacturing cost with improved reliability and reproducibility. The wet-etching method is easy to implement particularly for a larger number of wafers in a batch fabrication environment and offers minimum controlling parameters and much cheaper input infrastructure as compared with RIE.

A method of uniform wet etching of polysilicon has been devised and implemented in the present work for the realization of piezoresistors of boron doped polysilicon over the silicon diaphragm in the batch fabrication of pressure sensor. A 2 inch diameter silicon wafer has been considered as a model size in order to show the capability of the proposed method. Blanket wet etching has been carried out purposely to compare it with the proposed method. The method is economic and easy in its implementation. The methodology of the process is outlined in the next section, which is followed by the fabrication process adopted for the sensor fabrication. Relevant results of uniformly defined polysilicon resistors with statistical data of resistors values are presented. The results are discussed with conclusion in the end.

Methodology of wet-etching process

There are two situations of wet etching of polysilicon thin layer on the silicon nitride/silicon dioxide capped silicon wafer as shown in Figure 1; blanket wet etching of polysilicon film with protected patterns of resistors over the entire surface, and second, discretization of polysilicon layer and then wet etching of each unit simultaneously. In the previous situation etching rates of polysilicon is higher on the wafer edges and a non-uniform etched pattern of remaining polysilicon is resulted. The size of arrows shown in Figure 1 schematically shows the rate of etching which is higher on the corners and slow on the flat surface. The discretization of the polysilicon layer into small segments prior to the actual delineation of polysilicon resistors, enhances corners in a distributed manner on the entire polysilicon surface. The each small independent island of polysilicon establishes its own etch rate according to its surface area and provides a better control over the etching mechanism. By selection a uniform area of each island on the entire polysilicon surface, a uniform etching rate can be established. The geometry influence on the wet-etching rate has been extensively studied in the literature (Koehler, 1999). Parameters related to reaction and diffusion mechanisms of wet chemical etching are strong functions of geometries to be etched out. Fringing of reaction rates around sharp corners in the geometry enhances the etching rates. With the decreasing dimensions of the structures to be defined by wet etching, more involved etching mechanisms have been encountered in the recent studies (Yamamura and Mitani, 2008).

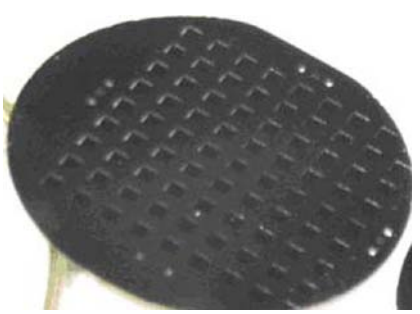
Figure 1 Schematic details of blanket etching of polysilicon and discretization of entire layer into small segments to establish uniform etching rate



Fabrication process

In the fabrication of polysilicon piezoresistive pressure sensor, starting silicon wafer is a double sided polished (100) oriented with a size of 2-8 inch diameters in a batch of few tens in numbers in a commercial fabrication foundry. The size of silicon wafer as such does not affect the fabrication process rather it brings the cost down by producing larger number of sensor chips in one cycle of fabrication process. Silicon wafer is first oxidized and silicon nitride is deposited using LPCVD to provide a mask for subsequent anisotropic etching in aqueous KOH for diaphragm realization. The details of the process sequence can be found out elsewhere (Akhtar *et al.*, 2003a). The array of etched cavities is shown in Figure 2. In order to delineate piezoresistors on the diaphragm, LPCVD polysilicon layer is deposited on the opposite surface of etched cavity. The polysilicon film is boron doped in order to adjust its sheet resistivity for required resistor's value. A blanket doping of boron is conducted by diffusion process with prior optimized diffusion parameters. At this stage back to front alignment process becomes important to align placement of polyresistors on the diaphragm which is on the other side of the surface. A double-sided mask aligning system is one solution, which is not cost effective. A novel and cost effective procedure has been used for this purpose (Akhtar *et al.*, 2003b). The method is also useful to control the diaphragm thickness in addition to provide facility for back to front alignment. The polyresistors thus defined and protected using photoresist are required to be selectively delineated by etching unwanted polysilicon from rest of the silicon surface. The area defined for each unit of sensor which is 4×4 mm with a diaphragm size of 2×2 mm, has been the size of each array which has been

Figure 2 Cavity arrays on one side of the silicon wafer realized in 45 percent KOH at 80°C till holes are emerged on the wafer edges as shown



repeated in 9 × 9 matrix on a 2 inch diameter silicon wafer. The grid defining the boundary of each sensor chip has been used for discretizing the polysilicon layer into islands of a 4 × 4 mm size by selectively etching of polysilicon from the location of grid as shown in Figure 3. The entire polysilicon film has been divided into discrete segments of 4 × 4 mm. An additional step of photolithography has been however introduced for polysilicon discretization. A larger view of the polysilicon islands is shown in Figure 4. The equal size of islands of polysilicon resembles with the size of sensor chip and therefore does not require any additional mask. This ensures uniform etching rates on each island while delineating polyresistors using wet-etching solution. A commercial grade poly etch solution from M/s GCC, USA has been used in the present work. Once islands are defined on the doped polysilicon surface, resistors are patterned using photolithography and wet etching is carried out for selective removal of unwanted polysilicon from each island at a uniform rate. A clear visibility of underlying silicon nitride layer on the entire surface helps for complete removal of the polysilicon. The resistors thus realized were tested in order to establish uniformity in the values of fabricated resistors.

Relevant technological details are mentioned as follows:

- polysilicon etchant: 95 percent PolyEtch (LTM grade) from M/s GCC, USA;
- thickness of thermal oxide – 0.5 μm;
- thickness of LPCVD silicon nitride – 0.15 μm at 780°C;
- thickness of LPCVD of Polysilicon – 0.5 μm at 620°C;
- boron doping of polysilicon – 1,050°C for 40 min in N_2 ambient followed by borosilicate glass removal in 10 percent HF;
- photoresist used – S1813 with MF312 developer;
- photoresist thickness – 1.0 μm; and
- designed line width of polysilicon resistor – 10.0 μm.

Figure 3 The other side of silicon wafer with LPCVD polysilicon patterned by selective wet etching to delineate each sensor chip. The whole area of doped polysilicon has been discretized into small area segments of 4 × 4 mm

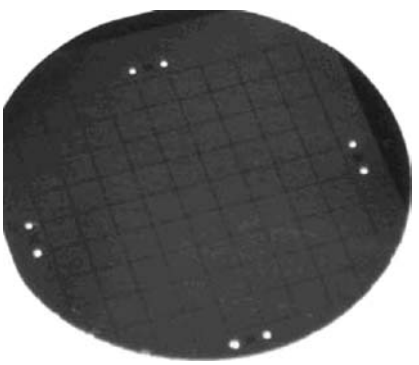
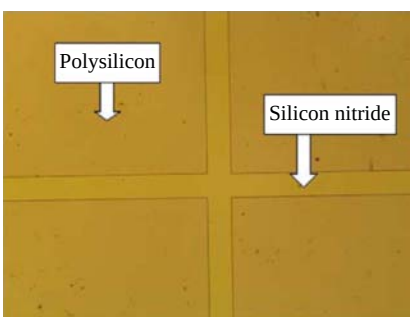


Figure 4 An enlarged view of discretized polysilicon pattern on silicon wafer with cavity array on the other side



Results

In process details of polysilicon resistors fabricated using wet etching of polysilicon after discretizing the polysilicon film have been recorded. Figure 5 shows the silicon wafer surface carrying polysilicon resistors in wheatstone's bridge configuration on the silicon diaphragm. Arrays of cavity are on the other side of the silicon surface. The polysilicon resistors are delineated using proposed wet-etch method. A uniformly distributed polyresistors can be seen on the entire silicon surface with clear visibility of under lying silicon nitride film. More details of the fabricated resistors are shown in Figure 6(a)-(c), where dimensions of the resistor coincide with the designed values. No undercut is found in the layout of the polyresistor. A closer view of the polyresistors on the silicon nitride bed has been shown in Figure 7. A comparison of the etching process of blanket and discretized polysilicon has been made on the basis of resistors dimensions and their values over the entire surface of the wafer. Typical measurement of the line width of polyresistor near the wafer edge has been shown in Figures 8 and 9 using blanket and discretized method of etching, respectively. The resistor width is decreased from 10.0 to 4.6 μm in case of blanket etching of the polysilicon film owing to enhanced over etch. The width of resistor defined using the proposed method has been found of 9.0 μm, which is very close to the designed value. The proposed method of wet etching enables to reduce over etching of resistors even on the wafer edge. The over etching of polysilicon resistors during the process of their realization using wet etching has been further shown in Figure 10. The width of the resistors is etched out completely at some of the locations on the wafer surface, which leads to zero values of the fabricated resistors. The over etching of polysilicon resistors on the silicon wafer is accounted maximally for the reduced yield in the fabrication of sensor chips. A reproducible method for realizing uniform polysilicon resistors is a crucial requirement for a sensor foundry. The proposed method introduces a viable and cheaper technique to provide uniform and reproductive polysilicon resistors in the fabrication of micro sensors at large-scale.

Figure 5 Silicon wafer carrying arrays of polysilicon resistors over the diaphragm after wet etching

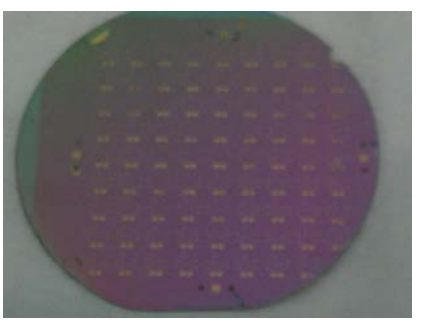
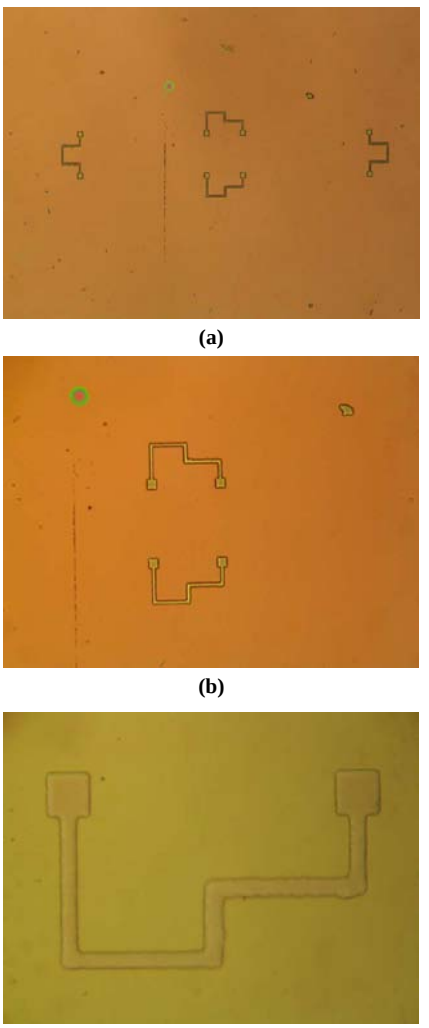


Figure 6 Polysilicon resistors patterned over the diaphragm after selective wet etching of polysilicon using proposed wet-etch method depicting resistors geometry



Notes: (a) Group of four (b) two in the group and (c) single

Figure 7 Enlarged optical view of polysilicon resistors on silicon surface over the arrays of diaphragms showing clarity between polysilicon resistors and the silicon nitridelayer

Figure 8 Resistors dimensions on the edge of silicon wafer after wet etching of blanket polysilicon

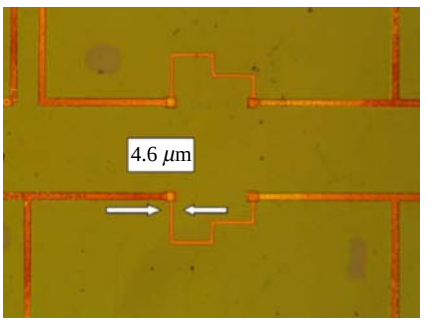


Figure 9 Resistors dimensions on the edge of silicon wafer after wet etching of discretized polysilicon

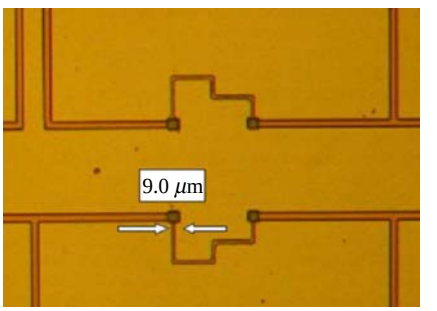
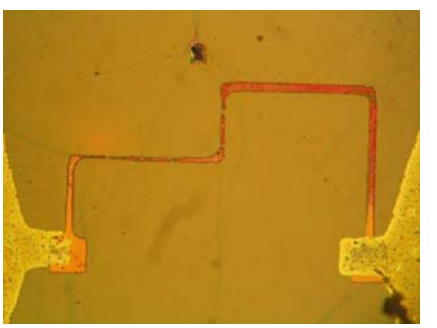


Figure 10 Typical details of over-etched resistors near the wafer edge during blanket polysilicon etch



Discussion

LPCVD polysilicon is an important sensing material in realizing microelectromechanical systems based sensors in general. Besides, being used for piezoresistors over the moving diaphragm, sacrificial layer-roles are immense owing to its technological compatibility with the prevailing microelectronics processes. It is well known about the stresses developed in the LPCVD polysilicon film, which modifies the flatness of the silicon wafer during the fabrication process and therefore introduces problems in the vacuum holding of the wafers (Bhushan and Koinkar, 1996; Matsuo *et al.*, 2004; Murarka and Retajczyk, 1983). Incorporation of discretization of polysilicon film is useful to minimize stress induced curvature effects in the silicon wafer. Apart from this, uniform etching of the polysilicon has been shown in this work as a major advantage for yield improvement and reproducibility. The results of measured values

of the fabricated polyresistors using both approaches of ploysilicon etching; discretized and blanket, are shown in Figures 11 and 12, respectively. More uniform resistor values can be seen on the wafer treated with discretized method of polysilicon etching. The blanket etching of polysilicon results into non-uniform resistor's values as shown in Figure 12. Owing to over etching in case of blanket etching, resistors on the edges sometimes are completely etched away, resulting into no resistor's values. A 2 inch diameter silicon wafers carrying sensor chips in 9 × 9 matrix with a diaphragm size of 2 × 2 mm have been considered in the above cases. The resistor's values were measured using commercial probe system with attached programmable instruments. Except polysilicon etching, rest of the fabrication process was maintained similar on both the wafers. The improved yield due to proposed method of wet etching has been determined experimentally in this work. The process has been extremely useful in the batch fabrication of piezoresistive pressure sensors based on bulk micromachining. The over etched width of the polysilicon increases the resistor's value. The enhanced values of the polysilicon resistors, shown in Figure 12, match with extra etching near the wafer edge. In case of blanket etching, etching of polysilicon starts from the edges of the wafer and slowly moves towards the center of the wafer. Discretization of the polysilicon film offers individual edges to each segment which is also an individual chip of the sensor, thus making it a novel method as compared to conventional approaches.

Figure 11 Measured polyresistor's values in 9 × 9 matrix arranged on a 2 inch diameter silicon wafer, fabricated employing proposed wet-etch method

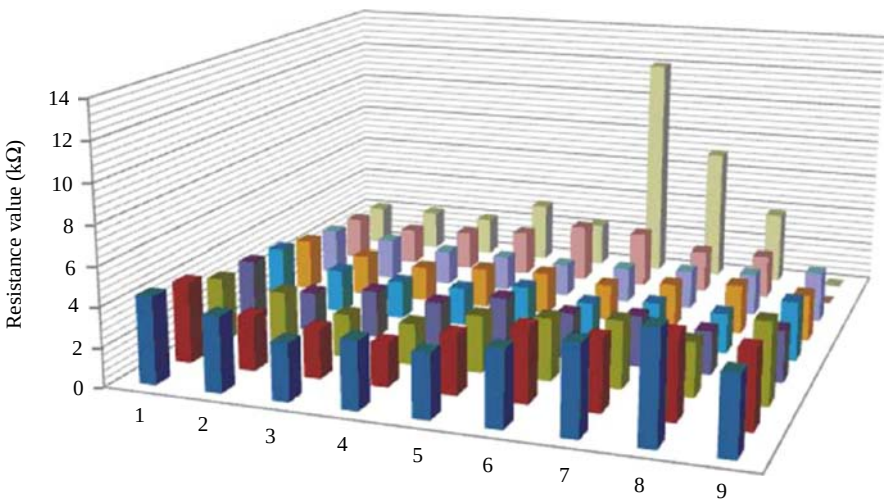
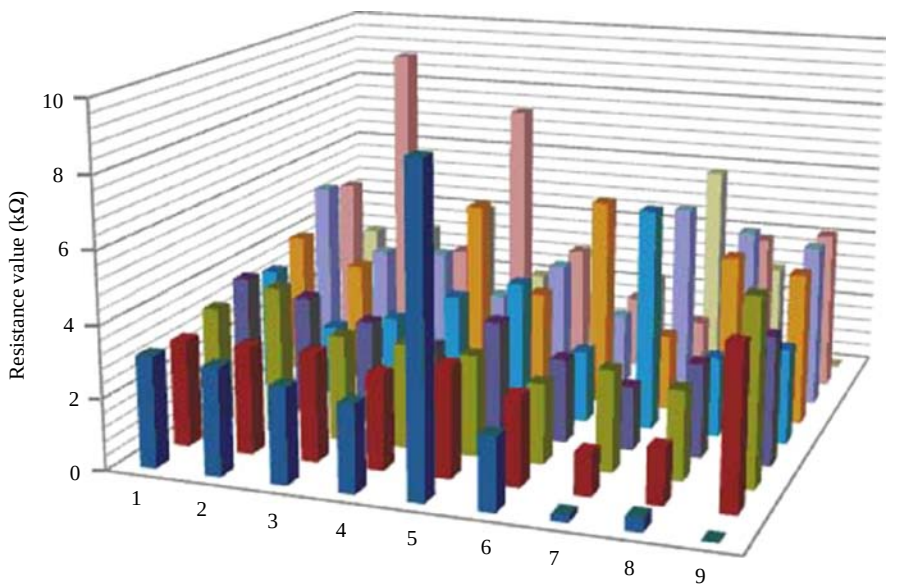


Figure 12 Measured polyresistor's values in 9 × 9 matrix arranged on a 2 inch diameter silicon wafer, fabricated employing blanket polysilicon etch method



Conclusion

The realization of polysilicon resistors over the diaphragm plays a crucial role due to yield in the fabrication of pressure sensor on large-scale. The proposed method of wet chemical etching with a prior discretization of the polysilicon film has resulted into enhanced uniformity in the resistors values and provides ease in its reproducibility. A comparison with conventional wet etching has been performed over a 2 inch diameter wafer for the superiority of the proposed method. The method is applicable for metal line delineation in case of microelectronics manufacturing.

References

Akhtar, J., Dixit, B.B., Pant, B.D. and Deshwal, V.P. (2003a), "Polysilicon piezoresistive pressure sensors based on MEMS technology", *IETE Journal of Research*, Vol. 49 No. 6, pp. 365-77.

Akhtar, J., Dixit, B.B., Pant, B.D., Deshwal, V.P. and Joshi, B.C. (2003b), "A process to control diaphragm thickness with a provision for back to front alignment in the fabrication of polysilicon piezoresistive pressure sensor", *Sensor Review*, Vol. 23 No. 4, pp. 311-5.

Bhushan, B. and Koinkar, V.N. (1996), "Microtribological studies of doped single-crystal silicon and polysilicon films for MEMS devices", *Sensors and Actuators*, Vol. 57, pp. 91-102.

Koehler, J.M. (1999), *Etching in Microsystem Technology*, Wiley-VCH, New York, NY.

Matsuo, N., Kawamoto, N. and Hamada, H. (2004), "Internal stress in polycrystalline Si film recrystallized by excimer laser annealing", *Japanese Journal of Applied Physics*, Vol. 43 No. 2, pp. 532-3.

Murarka, S.P. and Retajczyk, T.F. Jr (1983), "Effect of phosphorous doping on stress in silicon and polycrystalline silicon", *Journal of Applied Physics*, Vol. 54 No. 4, pp. 2069-72.

Yamamura, K. and Mitani, T. (2008), "Etching characteristics of local wet etching of silicon in HF/HNO_3 mixtures", *Surface and Interface Analysis*, Vol. 40 Nos 6/7, pp. 1011-3.

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