A WIDE DYNAMIC RANGE HIGH-Q HIGH-FREQUENCY BANDPASS FILTER WITH AN AUTOMATIC QUALITY FACTOR TUNING SCHEME

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Ajay Kumar

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A WIDE DYNAMIC RANGE HIGH-Q HIGH-FREQUENCY BANDPASS FILTER WITH AN AUTOMATIC QUALITY FACTOR TUNING SCHEME

Approved by:

Professor Phillip E. Allen, Adviser
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Paul E Hasler
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor James Stevenson Kenny
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Ronghua Pan
School of Mathematics
Georgia Institute of Technology

Professor David C. Keezer
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 17 December 2007

To my Parents

& my Wife,

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SUMMARY

This work addresses the problems associated with poor dynamic range and the quality factor instability of a high-Q, high-frequency, continuous-time bandpass filter. Some improvements to the existing transconductor design and an implementation of a new, reliable, quality tuning algorithm have been proposed to address the above mentioned problems. In order to formulate the problem statement, which can help and serve the society, wireless transceiver requirements has been kept in mind.

State-of-the-art superheterodyne transceiver architecture uses passive, surface acoustic wave (SAW) filters (DR ∼70 dB) for radio frequency (RF), image reject (IR), and intermediate frequency (IF) filters. The IF SAW filters are 20 dB more linear than an on-chip continuous time filters (DR = 40∼50 dB). The on-chip continuous-time filters also suffer from quality factor instability problem, however, they can generate gain, whereas the SAW filters introduce a 3∼13 dB of insertion loss. The loss from SAW filters also increases with bandwidth.

The goal of this research is to circumvent the poor dynamic range and quality factor instability problem of the on-chip continuous times filter, and take a step further towards the single chip solution of the wireless transceivers. In order to quantify the contribution and the improvements in performance, a 100 MHz biquad bandpass filter is designed with DR $>$ 60 dB, and gain∼20 dB, using an ultra-linear transconductor in BiCMOS process. The linearity of the stand alone transconductor is more than 80 dB and its 3 dB cut-off frequency is close to 1.5 GHz.

The new transconductor circuit employes a local negative feedback loop, to achieve high linearity, while maintaining its high cut-off frequency. Instability in the quality-factor(Q) of the filter is solved using a novel quality-factor tuning scheme. It uses the phase characteristics of the filter to extract the quality factor information and tunes the same by modulating the phase characteristics inside a second-order phase locked loop system. The

accuracy and performance of this new Q-tuning loop is determined by the dead-zone of the phase frequency detector (PFD), and the delay mismatch between the reference and the filter output signal. An ultra-low dead-zone (± 50 pS) pre-charge based digital PFD circuit has been developed and special attention has been given to the delay matching between the two signal paths.

Thus, this research work presents a wide-dynamic range, high-Q, high-frequency band-pass filter circuit with an reliable automatic tuning scheme to meet the requirements of the present and future wireless communication devices.

CHAPTER I

INTRODUCTION

The twenty first century is referred to as the Electronic Age in the development of the human race, where we have the ability to perform and control everyday activities electronically. We prefer to have a smart wireless communication device and controller. This urge has motivated the researcher to constantly refine the architecture and the components of wireless transceivers; and develop miniaturized, power-optimized, and cost-effective solutions. These goals are achieved by taking the transmitter and the receiver architectures simultaneously to the next level of system integration. Primarily, there are two architectures available for wireless transceivers:

- Superheterodyne
- Direct-Down Conversion

Both architectures are subsequently divided based on their implementation. The superheterodyne architecture has been the preferred choice for transceiver design, since its invention by Edwin H. Armstrong in 1917 [1], because of its simplicity and insensitivity to component and environmental variations. A block diagram of a superheterodyne receiver is shown in Figure 1.1. In this architecture, the entire signal band is first down-converted from radio frequency (RF) to an intermediate frequency (IF) using a fixed local oscillator (LO) and a RF mixer. Then, the desired channel is selected from the signal band using a mixer with a variable LO at the IF stage, which is implemented either in the analog or the digital domain. The two-stage modularity reduces the performance requirements on the individual components, so that they are reliable and easy to design [2].

Thus, the superheterodyne transceiver architecture is modular, reliable, and easy to design, but it requires several off-chip components, such as duplexer/RF filter, IR filter, and IF filter. Therefore, it is difficult to get a single-chip solution based on this architecture.

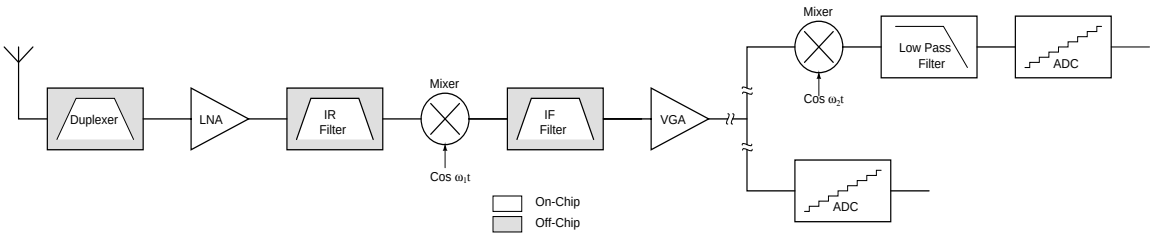

Figure 1.1: Block diagram of the superheterodyne receiver.

The direct-down conversion receiver architecture was developed for system integration, where the goal was to minimize the number of off-chip components. A block diagram of a direct-down receiver is shown in Figure 1.2. It only requires the duplexer as an off-chip component. It also circumvents the problem of the image lying at $2\omega_{IF}$ away from the channel. However, direct translation of the spectrum from radio frequency to zero frequency creates a number of other issues that did not exist in the superheterodyne receiver, such as DC offset, even harmonic inter-modulation (IM_2), flicker noise ($\frac{1}{f}$), and local oscillator leakage. It also requires a fine-pitched variable LO for the RF mixer to select the channel at the RF stage, a linear mixer to reduce the distortion (mixers are nonlinear circuits), and a fast sample-and-hold circuit. The stringent requirements on these blocks make them power hungry and complex. Together, these problems make this architecture unreliable and difficult to implement in a cost-effective manner [3]. The solutions to these problems are beyond the scope of this work and hence will not be discussed further.

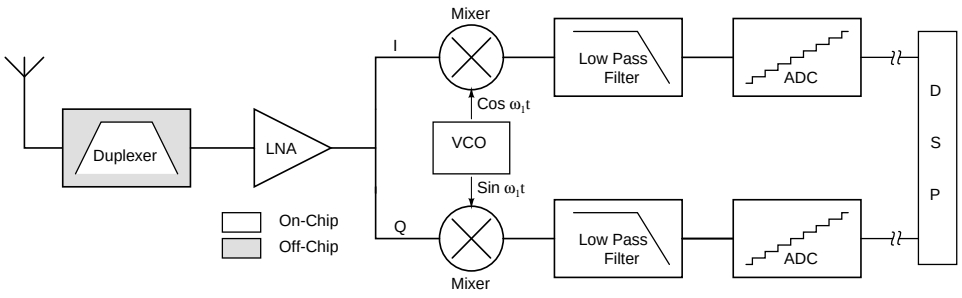

Figure 1.2: Block diagram of the direct-down conversion receiver.

A duplexer is used right after the antenna in both receiver architectures. It is employed to provide isolation between the transmit and the receive bands and minimize any leakage of

the transmit signal into the receive band, as this leakage can saturate the low noise amplifier (LNA) of the receive path. Since the duplexer comes first in the receive path, it should have large dynamic range (*e.g.*, GSM receive signal can range from -102 dBm to -15 dBm) with minimal loss. Any loss from the duplexer is critical to the system performance, as its loss directly adds to the noise figure (NF) of the system. The duplexers are implemented using surface acoustic wave (SAW) or bulk acoustic wave (BAW) devices [2, 4, 5, 6].

The duplexer is followed by a LNA in the receive path. The LNA is the first gain block in the receive path and its noise performance is as critical as the duplexer. The noise from the later stages is not as critical, because its effects are mitigated by the gain from the LNA.

An active or passive mixer follows the LNA in the receive path. A mixer is a non-linear circuit, that performs the frequency translation from radio frequency (RF) to an intermediate frequency (IF). It adds and subtracts the input RF frequencies with a local oscillator ($\omega_{LO} = \omega_{RF} - \omega_{IF}$). The two RF frequencies, one located at ω_{RF} (desired signal) and the other at $\omega_{RF} - 2\omega_{IF}$ (image frequency), produce the output signal at the same intermediate frequency (ω_{IF}). Therefore, sometimes in a superheterodyne architecture, an image-reject filter (IR Filter) precedes the mixer to suppress any undesired signal from the image frequency [7]. At present, IR filters are implemented using SAW technologies [4, 5]. There have been some attempts to replace this filter with a monolithic solution [8, 9].

In a superheterodyne architecture, the output of the mixer is first filtered using a channel select filter, known as an IF filter, before being amplified by a variable gain amplifier (VGA). The IF filter selects the desired channel from the receive signal band. At present, all IF filters are also implemented using SAW technologies. This work focuses on replacing this off-chip, passive, SAW IF filter with an active, integrated, monolithic solution. Upon completion of this work, the superheterodyne receiver architecture will move a step closer to a single-chip solution.

There are several other applications for high-frequency bandpass filters, *e.g.*, FM receivers, front-end of a high-speed analog-to-digital converter (ADC), hard-disk drive applications, etc. The underlying core component of a '$G_m - C$' bandpass filter is a linear transconductor circuit, which can also be used as the gain stage in a digital variable gain

Table 1.1: Wireless standards and their IF filters.

Standard	$f_{downlink}$	**Channel BW**	ω_{IF}	**Q**
GSM	869-894 MHz	200 kHz	10 MHz	50
	925-960 MHz	200 kHz	10 MHz	50
	1805-1880 MHz	200 kHz	20 MHz	100
	1930-1990 MHz	200 kHz	20 MHz	100
IS-95	869-894 MHz	1.25 MHz	70 MHz	56
	1930-1990 MHz	1.25 MHz	70 MHz	56
	2120-2170 MHz	1.25 MHz	70 MHz	56
Bluetooth	2402 ∼2495 MHz	1MHz	70 MHz	70
HomeRF	2402∼ 2495 MHZ	1 MHz/3.5MHz	70/140 MHz	70/40
EDGE	921-960 MHz	200 kHz	10 MHz	50
	1805-1880 MHz	200 kHz	20 MHz	100
	1930-1990 MHz	200 kHz	20 MHz	100
W-CDMA	1805-1880 MHz	5 MHz	220 MHz	44
	1930-1990 MHz	5 MHz	220 MHz	44
	2110-2170 MHz	5 MHz	220 MHz	44
802.11b	2400-2483.5 MHz	25/10,30/10 MHz	300MHz	$10 \sim 30$
802.11 a/g/h	$5.03 \sim 5.825$ GHz	g:25, a/h:20 MHz	300MHz	$10 \sim 15$

amplifier (DVGA) for wireless and ultra-sound applications or as the gain stage for high-frequency operational transconductance amplifier (OTA).

In this research work, a high-Q, high-frequency bandpass filter is developed for wireless receiver applications. It can also be used in any of the above mentioned applications. The receive band frequency and the bandwidth of different communication standards are listed in Table 1.1. The spectrum allocation of these applications ranges from 869 MHz to 5483.5 MHz and the channel bandwidth of the systems ranges from 200 kHz of GSM to 30 MHz of WLAN. In the transceiver signal-path design, a large intermediate frequency relaxes the requirement on the IR filter and the RF mixer. Therefore, an intermediate frequency of $10 \sim 300$ MHz is desired for many of the next-generation communication systems. Some plausible choices of center frequency of IF filters and corresponding quality factors are also listed in Table 1.1.

Presently, wireless communication devices use off-chip ceramic or SAW filters at the intermediate frequency stage, to select the channel from the entire signal band. The performance specifications of some of these SAW filters are listed in Table 1.2. Their performance

Table 1.2: Off-chip SAW filters and their specifications.

Technology	ω_0	**BW**	**Q**	**Stop-band**	**Insertion Loss**	**Size**
SAW	120	2.25	53.33	7.3MHz/40dB	6.2 dB	12.7 x 7.6 mm
SAW	140	4.1	34.15	6MHz/40dB	24.5 dB	
Ceramic	220	2	110	17.2MHz/52	13 dB	
SAW	110	1.15	95.49	5MHz/40dB	4.5 dB	
SAW	280	20	14	30MHz/37dB	11 dB	5.0 x 5.0 mm

is stable across environmental variations but they are off-chip, expensive, and bulky. Their physical size decreases with frequency, as it ranges from a few millimeters to a few tens of millimeters. SAW filters provide insertion loss in lieu of desired gain to the signal path. Their insertion loss also increase with their bandwidth, which becomes problem for large bandwidth 3G applications. Since the signal strength at the IF stage is not large, it is desirable to have gain from the IF filter, as it reduces the noise and the linearity requirements on the RF components and the VGA.

An on-chip filter can generate gain and can be integrated along with the VGA or the mixer. However, it suffers from instability in its quality factor with environmental and manufacturing process variations. The advantages and disadvantages of SAW filters and the on-chip IF filters are summarized in Table 1.3. The table also helps identify the key areas of improvement during the implementation of an on-chip IF filter. The italicized letters are used to show the performance advantage of one device over the other. On-chip filters have many advantages such as gain, size, re-configurability, and system integration, but instability in quality factor and poor dynamic range are not acceptable. Their dynamic range has to be improved and a reliable tuning algorithm has to be implemented to present the on-chip solution as a viable alternative to the off-chip SAW IF filters. Their variable center frequency (ω_0) and quality factor can be considered as an advantage in designing a reconfigurable signal path, if they are controlled reliably.

The reconfigurable system architecture is becoming more popular because it allows the service provider to use different standards in urban and rural areas, and it enables the end user to use the same device for different applications. The fixed center frequency and the

Table 1.3: Advantage and disadvantage of SAW and on-chip filters.

Metric	**SAW**	**On-chip**
Linearity	*Good*	Poor
Dynamic Range	*Good*	Poor
Center Frequency	Fixed	Variable
Stability	*Good*	Unstable
Quality factor	*Moderate to high*	low
Gain/Loss	Loss	*Gain*
Integration	No	*yes*
Re-configurability	No	*Yes*
Size	Huge	*on-chip(tiny)*
Cost	Expensive	*Sand*

Table 1.4: Key requirements and target filter specifications.

Parameters	**SAW**	**On-chip**
Center Frequency (MHz)	$10 \sim 300$	100
Quality factor	$30 \sim 100$	$40 \sim 50$
Gain (dB)	$-4 \sim -23$	$15 \sim 20$
Dynamic Range (dB)	$70 \sim 80$	$60 \sim 70$
Stop-band Attenuation (dB)	-50	-50

bandwidth of the SAW filters, along with the unavailability of tunable on-chip filters, are forcing the designer either to use the complicated direct-down converter architecture or to have several IR and IF filters for a reconfigurable signal path. Several SAW filters make the solution expensive and bulky [10]. An on-chip solution to the IF filter is essential to achieve a cost-effective, single-chip miniaturized solution. Much research have been performed on "how to tune the center frequency of an on-chip filter" [11, 12, 13]. This research focuses on solving the poor linearity and the quality factor instability problem of on-chip filters. In order to quantify the performance of the proposed theories, some performance metrics are generated, which are competitive with the SAW filter and encompass the need for an FM receiver, 802.11 b & g, Bluetooth, wide-band code division multiple-access (WCDMA) applications. The underlying requirements for an IF filter on these applications are summarized in Table 1.4.

A center frequency of 100 MHz has been chosen because it lies at the arithmetic mean of the required center frequency for different applications, and a quality factor of 50 has been chosen because it fulfills the bandwidth requirements for many next-generation applications. The dynamic range requirement has been relaxed because the on-chip solution is going to provide a gain of 20 dB in lieu of a loss of $3 \sim 23$ dB from the SAW filters [4, 5]. In this work a prototype second biquad filter is implemented, which has limited stop-band attenuation. The issue of stop-band attenuation can be addressed by using a similar high-order cascaded filter [14].

Thus, this research will focus on the technical issues of designing a *wide dynamic range high-Q, high-frequency*, IF filter with a reliable, automatic *quality factor tuning scheme*. This research goal will be measured and accomplished by designing an on-chip 100 MHz bandpass filter with dynamic range of 60 dB and quality factor of 50, along with an automatic quality factor tuning scheme in the complementary metal oxide semiconductor (CMOS) or bipolar complementary metal oxide semiconductor (BiCMOS) process.

CHAPTER II

FUNDAMENTALS OF ANALOG BANDPASS FILTERS

Filters have been a topic of interest to researchers for a long time. They have enabled the communication system to filter the desired band of frequencies from the entire frequency spectrum and condition them for further signal processing to extract useful information. Filters are either implemented in the analog or digital domain. Analog filters are built using a physical network of electrical components such as capacitors, inductors, and resistors. They are used in either low-cost or high frequency applications. Digital filters are synthesized using delay elements; they can virtually achieve any filtering effect that can be expressed as a mathematical algorithm. The two primary limitations of the digital filters are speed and cost. Therefore, they are primarily used for low-frequency and high-fidelity audio applications. This chapter discusses filter topologies, types, and ways to realize the analog filter. It also highlights some of the key challenges in designing high-Q, bandpass filters.

2.1 Analog Filters

A filter is defined by its corner frequency, quality factor, pass-band ripple, stop-band ripple, and stop-band attenuation. The frequency response of a lowpass filter is shown in Figure 2.1. The pass-band and the stop-band ripple determine the type of filter transfer function one can use; the stop-band attenuation and its slope determine the required order of filtering to achieve the desired characteristics. Several different types of filter transfer function tables have been developed over time, with varying characteristics, *e.g.*, Butterworth filter, Bessel filter, Elliptical filter (Cauer filter), Linkwitz-Riley filter, Chebyshev filter, etc.[14].

Once the transfer function of the filter is chosen, it can be implemented using one of the topologies listed below. The advantages and disadvantages of these topologies in monolithic implementation are also discussed.

In a modern IC process, monolithic active and passive components have 3σ tolerance

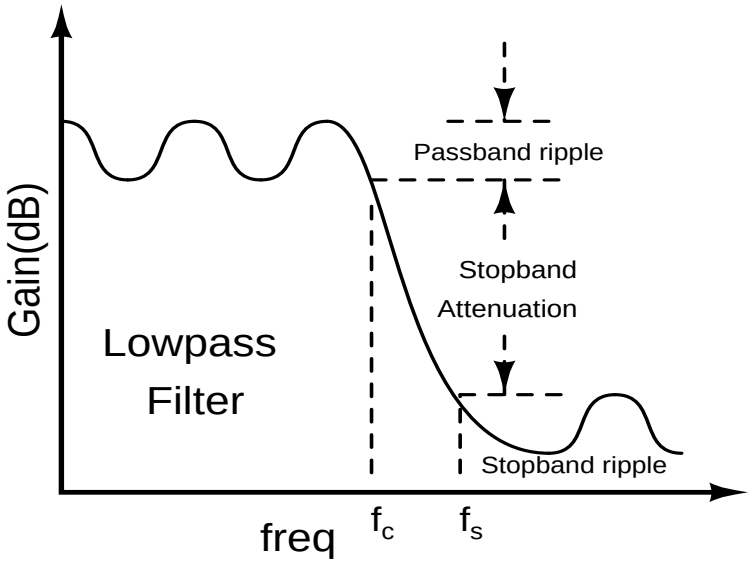

Figure 2.1: Design specification of a filter.

associated with their nominal value. Therefore, in monolithic implementation, the design parameters of the filter are made either as a ratio of like terms or they are made tunable. A ratio of like terms can be realized with 8-10 bits of accuracy, if their value and area are of the same order of magnitude. However, the pole frequency of the filter is determined by the value of the resistor and capacitor. Therefore, monolithic filters need an on-chip tuning algorithm to tune the filter parameters. The quality factor and the gain of the filter can be made as a ratio of like terms; however, when this ratio becomes too large, their accuracy can no longer be maintained. Thus, a high-Q, high-frequency filter needs a tuning algorithm for both center frequency and quality factor.

2.1.1 Cascade Approach

In cascade realizations, a higher-order filter (> 2) transfer function is factorized into several first-order and second-order transfer functions. An even-order (2n) filter is broken into n-bi-quadratic (biquad) filters, and an odd-order(2n+1) filter is broken into one first-order filter and n-biquads. The resulting first- and second-order transfer functions are implemented independently using active or passive RLC networks and are connected in cascade fashion to achieve the desired filter characteristics, as shown in Figure 2.2. This factorization

technique makes the design modular and easy to analyze and tune.

$$\frac{a_n s^n + a_{n-1} s^{n-1} + \cdots + a_1 s + a_0}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + b_0} = \prod_{i=1}^{m} \frac{a_{2i} s^2 + a_{1i} s + a_{0i}}{b_{2i} s^2 + b_{1i} s + b_{0i}} \tag{2.1}$$

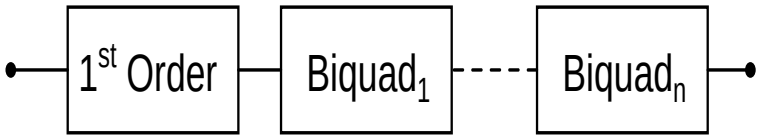

Figure 2.2: Cascade approach to realize a higher-order filter.

One of the key requirements for monolithic implementation is tunability against process and temperature variations (PVT). In the cascade design approach, each biquad controls only a pair of poles and zeroes; therefore they can be tuned individually. Ease of tuning makes this approach suitable for monolithic filters.

One disadvantage of the cascade design approach is its pass-band sensitivity to the component values. This limits the maximum attainable order of the filter to 10.

2.1.2 Multiple Feedback Loop Approach

The multiple-loop feedback design technique overcomes the component sensitivity problem of the cascade approach by connecting the individual biquads in a particular feedback configuration to minimize the transfer function sensitivity to their component values. This design technique retains the modularity of the cascade design approach by using biquads as a building block for the higher-order filters.

These biquads are connected in a complex feedback structure to realize a high-order filter, and they work together to control all poles and zeroes of the filter at once. Therefore, it is impossible to design a tuning algorithm to tune the center frequency and the quality factor of the filter by tuning the individual biquad.

The difficulty of tuning the filter parameters makes this design technique suitable only for discrete filters or non-tunable on-chip filters. One popular topology of this approach is the Leapfrog architecture [14, 15].

2.1.3 LC Ladder Structure

In this design approach, a doubly terminated passive LC ladder filter is converted into its active counterpart. Here, an inductor is realized using gyrators or general admittance converting circuits. The resulting active inductor circuit is inserted into the 'LC ladder' filter topology to realize the filter. A small component sensitivity of the ladder topology is retained during its active component transformation.

This topology has small component sensitivity, therefore, it is also hard to tune against process and temperature variations. Also at 100 MHz, inductors are realized using active gyrator circuits and they are noisy and dissipate power. These problems make this architecture unsuitable for on-chip implementation of continuous time filters, where accuracy is required.

Hence, for a high-frequency IF filter (IF=70 200MHz, Q=30 100) of 3G-GSM and WCDMA transceivers [14, 15, 16], the cascade approach looks more attractive than the other two. These high-Q filters can be realized using innovative feedback and feed-forward Q enhancement design techniques [17].

2.2 Biquad Filter Transfer Function

In cascade approach, a filter transfer function is broken into several first-order and second-order polynomials. First-order and second-order biquads are rational functions of first-order and second-order polynomials given by Equation 2.2 and Equation 2.3, respectively.

$$1^{st}\text{order}H(s) = H_0 \, \frac{a_1 s + a_0}{b_1 s + b_0} \tag{2.2}$$

$$2^{nd}\text{order}H(s) = H_0 \, \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{2.3}$$

where H_0 is the gain of the system. Lowpass, bandpass, highpass, and band-stop filter characteristics are realized by making the appropriate numerator coefficients of the above transfer function zero, *e.g.*, a highpass biquad is realized by choosing the numerator coefficients a_0 and a_1 of Equation 2.3 equal to zero.

2.2.1 Lowpass Filter

A lowpass filter passes the low frequencies up to a cut-off frequency (f_c) and attenuates all others. A first-order and second-order filter transfer function can be realized by leaving only the a_0 term in the numerator polynomial of Equation 2.2 and Equation 2.3. Thus, the first- and the second-order lowpass filter transfer functions are given by Equation 2.4 and Equation 2.5, respectively. A typical frequency response of a lowpass filter is shown in Figure 2.3, where H_0 is the gain, f_c is the cut-off frequency, and f_s is the stop-band frequency of the filter.

The slope of the frequency response form pass-band gain at cut-off frequency to attenuation at the stop-band frequency determines the required order of the filters.

$$1^{st}\text{order}H(s) = H_0 \frac{a_0}{b_1 s + b_0} \tag{2.4}$$

$$2^{nd}\text{order}H(s) = H_0 \frac{a_0}{b_2 s^2 + b_1 s + b_0} \tag{2.5}$$

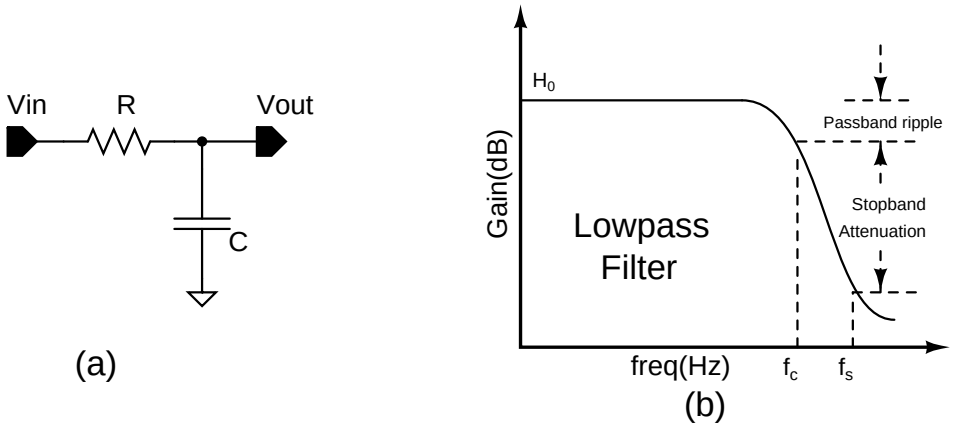

Figure 2.3: A typical frequency response of a lowpass filter.

An ideal filter can give a brick wall response, where f_c and f_s are the same frequency. However, in reality, each pole gives 20 dB per decade of attenuation, often known as 'roll-off', *e.g.*, first-order filter gives an attenuation of 20 dB/decade and second-order gives 40 dB/decade. There are several different ways to implement a lowpass filter; some give

sharper transition from pass-band to stop-band at the expense of ripples in the pass-band and the stop-band, *e.g.*, Chebyshev filter, Cauer filter. A Bessel filter gives flat gain and linear phase shift in its pass-band, but it has large component sensitivity.

A lowpass filter is used in many applications such as driving the sub-woofer of a music systems and filtering the voice signal from data in a DSL modem. It is also used as an integrator in proportional integrator and differentiator (PID) control systems.

2.2.2 Highpass Filter

A high-pass filter is the opposite to the lowpass filter; it allows a frequency higher than the cut-off frequency f_c with an amplification H_0 and attenuates the other. Similar to the lowpass filter, a highpass filter can be realized from the generic first-order and biquadratic function by dropping the a_0 and a_0, a_1 terms of the numerator polynomial of Equation 2.2 and Equation 2.3, respectively. First-order and biquad highpass transfer functions are given below.

$$1^{st}\text{order}H(s) = H_0 \frac{a_1 s}{b_1 s + b_0} \tag{2.6}$$

$$2^{nd}\text{order}H(s) = H_0 \frac{a_2 s^2}{b_2 s^2 + b_1 s + b_0} \tag{2.7}$$

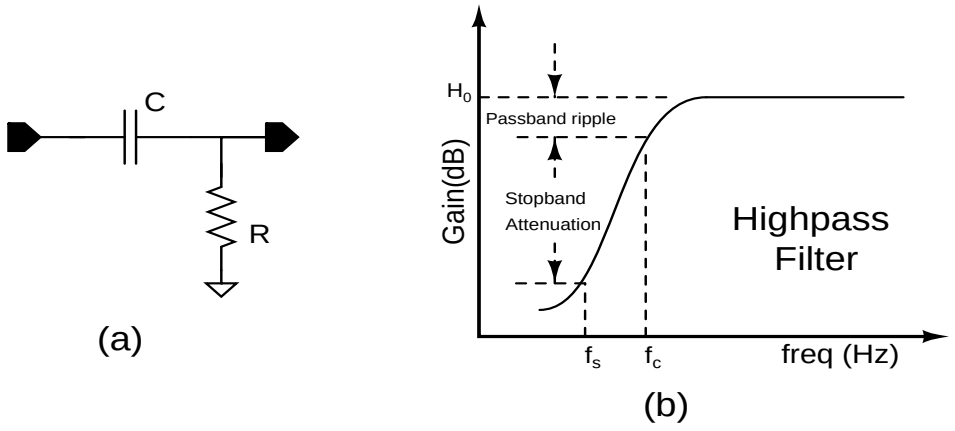

Figure 2.4: A typical frequency response of a highpass filter.

A simple first-order implementation of a highpass filter is shown in Figure 2.4.a; it is a

C-R circuit, often used as a differentiator in a control system. A typical frequency response of a highpass filter is shown in Figure 2.4.b, where H_0 is the pass-band gain, f_c is the cut-off frequency, and f_s is the stop-band frequency of the filter. The details of the pass-band gain, the stop-band attenuation, and the methods of implementations are similar to the lowpass filter. A highpass filter is used to drive the 'tweeter' of a music system. It is also used widely in communication systems, image processing applications, and as a differentiators in PID control systems.

2.2.3 Bandpass Filter

A bandpass filter passes the frequencies within a certain range and attenuates the other. A bandpass filter can be synthesized by cascading a lowpass and a highpass filter, where the cut-off frequency of the lowpass filter is higher than the lower cut-off frequency of the highpass filter. Thus, a bandpass filter requires at least two poles to shape its frequency response. A generic biquad transfer functions is transformed into a bandpass filter by leaving only the $a_1 s$ term in the numerator polynomial and is given in Equation 2.8.

$$2^{nd}\text{order}H(s) = H_0 \ \frac{a_1 s}{b_2 s^2 + b_1 s + b_0} \tag{2.8}$$

A simple passive structure of a second-order bandpass filter is shown in Figure 2.5.a. It is a series RLC network. This system contains two poles, one created by the R, L and the other created by R, C. Together, C and L determine the center frequency of the filter, which is also known as the resonance frequency of the network.

A typical frequency response of a bandpass filter is shown in Figure 2.5.b, where H_0 is the pass-band gain, f_{cl} and f_{ch} are the lower and higher cut-off frequencies, and, f_{sl} and f_{sh} are the lower and the higher stop-band frequencies. The difference $(f_{ch} - f_{cl})$ and the geometric mean $(\sqrt{f_{ch} f_{cl}})$ of the two cut-off frequencies are known as the *bandwidth* (Δf) and *center frequency* (f_0) of the filter.

The quality factor of an electrical network is defined in Equation 2.9. It is a ratio of the reactive energy to resistive energy or a ratio of energy stored in reactive component to energy dissipated in resistive components, which translates into the ratio of the bandwidth

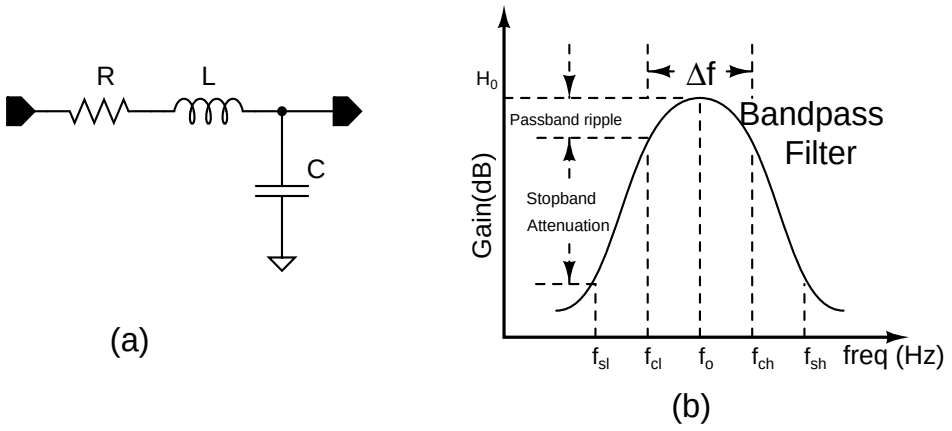

Figure 2.5: A typical frequency response of a bandpass filter.

over the center frequency for a bandpass filter.

$$Q = \frac{E_{stored}}{E_{dissipated}} = \frac{E_{reactive}}{E_{resistive}} = \frac{\Delta f}{f_0} \tag{2.9}$$

The polynomial coefficients of the bandpass filter defined by Equation 2.8 can be expressed in terms of filter parameters, and are given by Equation 2.10 and Equation 2.11. The center frequency, quality factor, and bandwidth of the bandpass filter are ω_0, Q, and $\frac{\omega_0}{Q}$, respectively. The numerator coefficients ω_0 and $\frac{\omega_0}{Q}$ of Equation 2.10 and Equation 2.11 corresponds to a_1 of the filter transfer function given by Equation 2.8. The denominator coefficients b_2, b_1, and b_0 of Equation 2.8 are 1, $\frac{\omega_0}{Q}$, and ω_0^2, respectively. These two transfer functions of the bandpass filter differ in terms of gain at the center frequency, which is often referred to as *mid-band gain*. The mid-band gains of the bandpass filter given by Equation 2.10 and Equation 2.11 are $H_0' \times Q$ and H_0, respectively.

$$H(s) = H_0' \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.10}$$

$$H(s) = H_0 \frac{\frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.11}$$

A bandpass filter is used in communication systems to select the desired channel from the entire frequency spectrum. It is also used to design tuned circuits for signal processing.

2.2.4 Bandstop Filter

A band-stop filter is an inverse of a bandpass filter, like the highpass to a lowpass. It passes all the frequencies except for the frequency within a certain range. A band-stop filter can also be realized by cascading a lowpass with a highpass filter, where the higher cut-off frequency of the lowpass filter is lower than the lower cut-off frequency of the highpass filter. Thus, a band-stop filter also requires a minimum of two poles to shape its frequency response. The transfer function of a biquadratic band-stop filter is given by Equation 2.12. A typical response of a band-stop filter is shown in Figure 2.6, where H_0 is the gain, f_{cl} and f_{ch} are the lower and the higher cut-off frequency, and f_{sl} and f_{sh} are the lower and the higher stop-band frequencies, respectively.

$$2^{nd}\text{order}H(s) = H_0 \ \frac{a_2 s^2 + a_0}{b_2 s^2 + b_1 s + b_0} \tag{2.12}$$

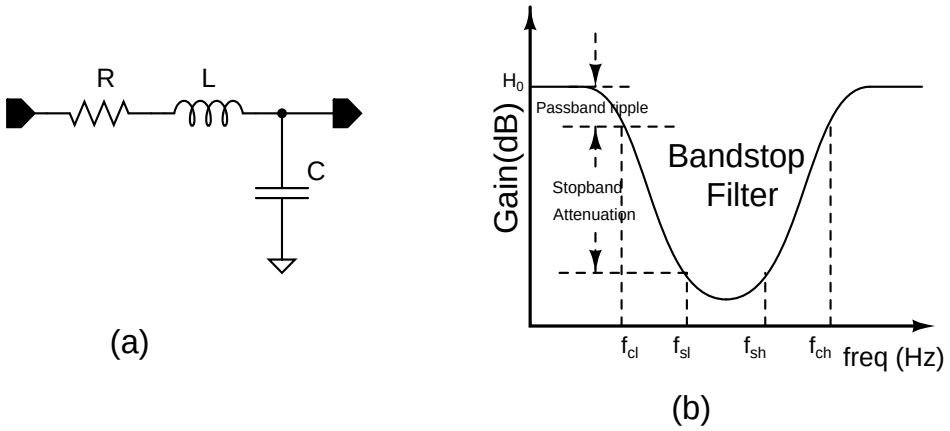

Figure 2.6: A typical frequency response of a band-stop filter.

A band-stop filter is commonly used in communication systems to block certain bands of signals, that could saturate the LNA and act as a blocker for a weak signal. A very narrow band-stop filter is also known as a notch filter. A notch filter is used as an image-reject filter in superheterodyne receivers.

Table 2.1: Monolithic filter topologies.

Topology	Dynamic Range	Operating Frequency
Switched Capacitor	Very high	f $\sim$ 100 kHz
Switched Current	Very High	f $\sim$ 1 MHz
Active RC	High	f $\sim$ 1 MHz
MOSFET-C	Low	f $\sim$ 10 MHz
Gm-C	Medium	f $\sim$ 100 MHz
Log Domain	High	f $\sim$ 100 MHz
Current Mode	High	f $\sim$ 100 MHz

2.3 Monolithic Filter Implementation

Several different topologies have been developed for monolithic implementation of filters since their introduction in the early 1980*s*. Some of these topologies are listed and compared in Table 2.1 based on their dynamic range and operating frequency. Each of these topologies is targeted towards different applications, *e.g.*, high-resolution *switched capacitor* (SC) and *switched current* filters are primarily used for audio applications [18, 19, 20, 21, 22]. They are also known as *sample-data filters*. The *active RC* filter, which goes to medium frequency range and provides high accuracy, is used in automotive and control system applications. A *Gm-C* filter is not limited by the internal pole of the operation transconductance amplifier (OTA); therefore it is used for high-frequency applications [23, 24].

Upon evaluating the frequency of operation of these filter topologies, it is evident that only *MOSFET-C*, *Gm-C*, *log-domain*, and *current-mode* topologies can be improved to meet the goals of this research. The simplest analog filter is an *integrator*. It is a single pole lowpass filter. Characteristics of integrators are discussed and compared with different topologies based on their low-voltage, power consumption, and noise.

2.3.1 Active RC Filters and MOSFET-C Filters

Filters were first created using passive components such as R, L, and C. They were giving 3dB insertion loss to the signal path. The active-RC filter is a variant of the classic RC filter structure, which was originated to overcome the '*loss*' from the passive RC filter. A typical first-order differential, active-RC filter, often known as an integrator, is shown in

Figure 2.7.a. It requires capacitors (C), resistors (R), and an operational amplifier (opamp). The transfer function of an ideal integrator is given by Equation 2.13. An ideal integrator provides an infinite gain at DC and has a single pole frequency response [25].

However, the finite gain (a_0) and the finite gain-bandwidth product (GBW) of an opamp moves the dominant pole of the integrator from DC to $\frac{\omega_0}{a_0} = \omega_\alpha$, assuming that the GBW of the opamp is higher than the pole frequency (ω_0) of the integrator. The modified magnitude and phase response of a non-ideal integrator are shown in Figure 2.8.a and Figure 2.8.b, respectively.

$$H_{int}(s) = \frac{1}{sRC} = -\frac{\omega_0}{s} \tag{2.13}$$

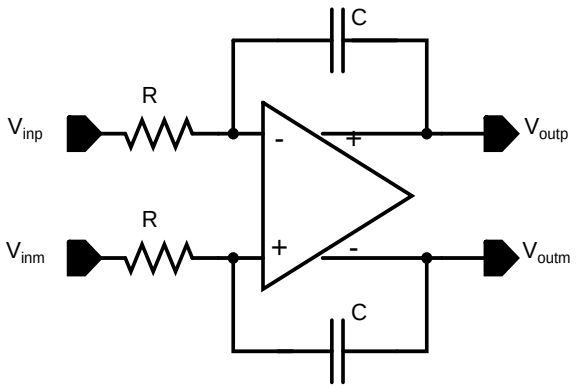

Figure 2.7: First-order active-RC filter.

A non-ideal integrator performs as an integrator for the frequency range between $10\times\omega_n$ and ω_0, where $\omega_0 < \frac{GBW}{10}$. If this inequality is not met, then the integrator response will be limited to $10\times\omega_\alpha$ and $\frac{GBW}{10}$. The non-zero finite pole (ω_α) of the non-ideal integrator causes a phase lead, whereas non-dominant high-frequency poles of the opamp causes an excess phase lag. They cancel each other in the middle; however, at high frequency, the excess phase lag dominates and can bring instability to the system. Thus, the maximum operating frequency of this topology is limited to ω_0 or $\frac{GBW}{10}$.

Opamps are compensated for a signal pole response up to GBW to simplify their use in different applications. However, the compensating capacitor also limits their slewrate,

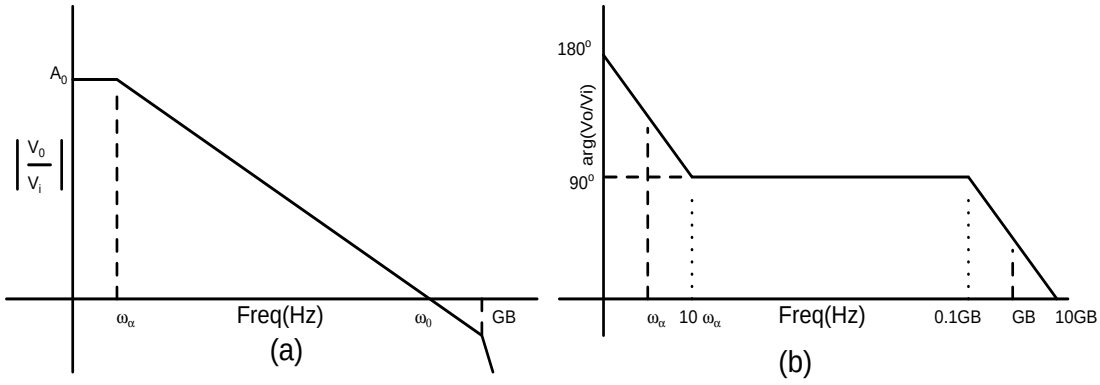

Figure 2.8: a: Frequency response of a non-deal integrator; b: Phase response of a non-ideal integrator.

which could potentially introduce distortion to the large signals. For example: A sinusoidal signal given by $v(t) = A_0 \sin(\omega t)$ will require a minimum slew rate of $A_0 \times \omega$. Thus, for a given slew-rate amplifier, the product of the maximum signal handling capacity and the maximum operating frequency is fixed. The maximum signal handling capacity can also be restricted by the power supply [26].

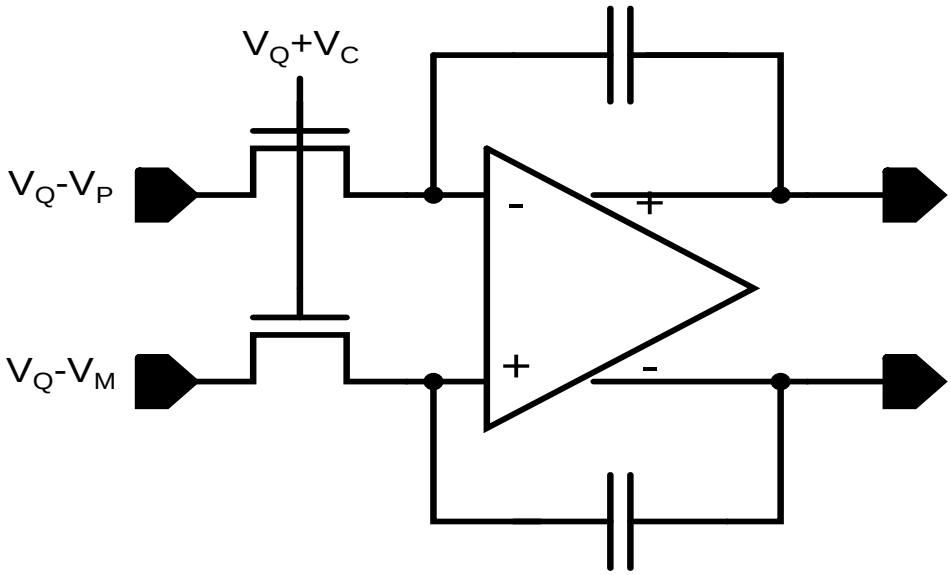

Figure 2.9: A differential MOSFET-C integrator.

An *active-RC* filter implementation is primarily used for discrete or low-frequency applications. A high-frequency monolithic version of this topology is *MOSFET-C* filters, where

resistors are emulated using metal oxide semiconductor field effect transistors (MOSFET) biased in the linear region, as shown in Figure 2.9. The gate voltage of a MOSFET resistor is V_T higher than the common mode voltage of the signal. The V_C component of the gate voltage is the tuned control voltage; V_P and V_M are differential input voltages. The voltage-current relationship of a MOSFET device biased in the linear region is given in Equation 2.14, where, I_d is the drain current, μ is the mobility of the minority carrier in the channel, $C_{ox}^{'}$ is the gate capacitance per unit area, W is the channel width, L is the channel length, V_{gs} is the gate to source voltage, V_T is the threshold voltage, and V_{ds} is the drain to source voltage of the device. The drain current, I_d, is proportional to the V_{ds} of the device for V_{ds} less than the gate overdrive voltage, $V_{gs} - V_T$.

$$\begin{aligned} I_d &= \frac{\mu C_{ox}^{'} W}{L} \times \left[(V_{gs} - V_T) - \frac{V_{ds}}{2} \right] V_{ds}; \quad \text{for } V_{ds} < (V_{gs} - V_T) \\ &\approx \frac{\mu C_{ox}^{'} W}{L} \times (V_{gs} - V_T)\, V_{ds}; \quad \text{for } V_{ds} << (V_{gs} - V_T) \end{aligned} \tag{2.14}$$

$$G_m = \frac{\mu C_{ox}^{'} W}{2L} \times (V_{gs} - V_T)\,; \quad \text{for } V_{ds} << (V_{gs} - V_T) \tag{2.15}$$

The transconductance of a MOSFET biased in the linear region is given by Equation 2.15. The pole frequency of the *MOSFET-C* integrator shown in Figure 2.9 is given by Equation 2.16, where G_m is the transconductance of the MOSFET device, and C is the capacitance [27, 28]. A MOSFET implementation of the resistor also makes the filter tunable by controlling the gate voltage (V_C) [29, 30, 31].

$$\omega_0 = \frac{G_m}{C} \tag{2.16}$$

The low device parasitic of MOSFET devices allows this topology to operate at higher frequencyies than *active-RC* filters. The maximum operating frequency of both these architectures is limited to one tenth of the gain bandwidth product of the opamp. This limitation comes from the excess phase shift caused by the higher-order non-dominant poles. The gain of the opamp is one at the GB and remains only 10 at frequency $\frac{GB}{10}$. This low gain from

the opamp also gives an offset near maximum operating frequency and introduces signal-dependent distortion to the signal.

In the *MOSFET-C* topology, the bias point of a MOSFET device is critical to the system performance. A strong input signal can push the MOSFET devices out of its linear region of operation, toward the saturation region, where it does not hold a linear voltage-current (V-I) relationship. The V-I relationship of a MOSFET operating in the saturation region is given by Equation 2.17, where λ is the channel length modulation parameter.

$$I_d = \frac{\mu C'_{ox} W}{2L} (V_Q - V_T)^2 (1 + \lambda V_{ds}) \tag{2.17}$$

The effective resistance of a MOSFET device operating in the saturation region is $1/\lambda$, which is independent of the device geometry and the control voltage. This change in effective resistance distorts the signal changes the pole frequencies of the filter. The second-order non-linearity resulting from overdrive of the MOSFET can be cancelled by employing a differential structure. However, higher-order non-linearity also appears if MOSFET resistors are over-driven [**?**].

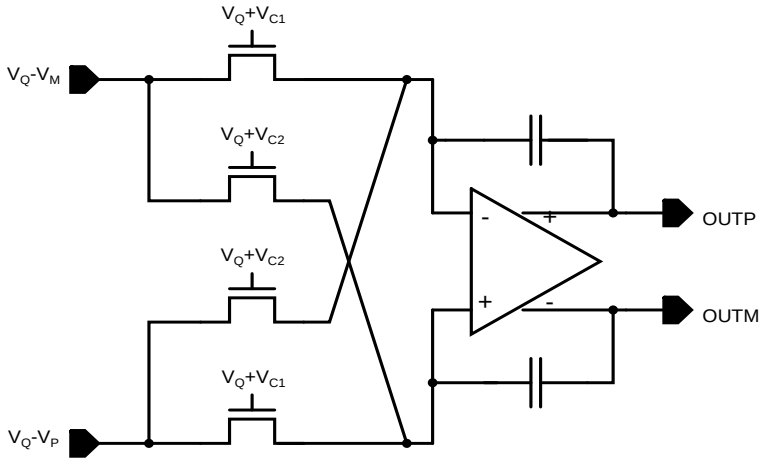

Figure 2.10: A wide-swing differential MOSFET-C integrator.

The effective resistance of a MOSFET resistor biased in the triode region remains linear for the input voltage smaller than the gate overdrive voltage ($V_{in} << V_{gs} - V_T$). The linearity of the MOSFET resistor is improved by either increasing the gate overdrive voltage

or canceling the second-order term of Equation 2.14. The gate overdrive voltage can be increased by reducing the aspect ratio of the device; however, the small devices will increase the $1/f$ noise, and the flat-band noise in the system. There are several other linearization techniques in [32, 28], that are successfully applied to achieve even higher-order linearization for audio-frequency application. One of these techniques is shown in Figure 2.10.

From the above research, it seemed evident that the operating frequency, and the linearity of the *MOSFET-C* architecture could not be improved simultaneously to achieve the goals of this research.

2.3.2 $G_m - C$ Filter

The *Gm-C* architecture is widely used to implement wide dynamic range, high-frequency, continuous-time filters. In this architecture, resistor and inductors are emulated using active transconductors. A transconductor operates at higher frequency than an opamp for a given current, as it does not require an internal capacitive compensation and a low-impedance output stage. Opamps have a high impedance stage to generate gain, followed by a low-impedance output stage, so they can drive voltage with sufficient current. In the G_m-*C* architecture, active transconductors replace the passive resistors and inductors of a filter. They are primarily used to convert an input voltage into an output current; therefore, they have a high-impedance output stage. Since these transconductors do not require an additional low-impedance output stage, they can use that extra current to bias their input stage for extra linearity or to save power [33, 34].

The dominant pole of a transconductor circuit comes from the high-impedance output node. The parasitic capacitance at the output node is lumped with the output capacitance, which makes this architecture less sensitive to any parasitic variation. It is less noisy than opamps, as it requires fewer active components. The value of transconductance is defined by a function of currents, voltages, and resistors, which makes this architecture tunable and suitable for monolithic applications.

2.3.2.1 G_m-C integrator

An integrator is an RC filter. In the G_mC implementation, resistors of the RC integrator are emulated using an active transconductor, as shown in Figure 2.11. Owing to the open-loop structure of the transconductor (no internal compensation), the integrator has a wide bandwidth therefore can be used for high-frequency applications. The transfer function of the integrator with an ideal transconductor is given by Equation 2.18. This ideal integrator has a single pole response for the entire spectrum, with a dominant pole at zero frequency. However, in reality, the frequency of operation is limited by parasitic poles and zeroes of the transconductors. [28, 35, 36].

$$H(s) = \frac{G_m}{sC} \tag{2.18}$$

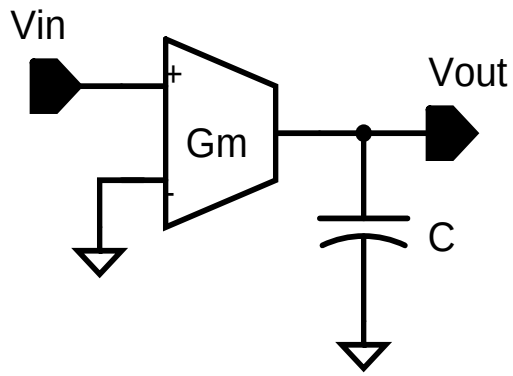

Figure 2.11: An G_mC implementation of an integrator.

A non-ideal transconductor has non-zero output conductance and finite parasitic zeroes. The transfer function of a real integrator is given in Equation 2.19, where G_m is the value of the transconductance, G_0 is the output transconductance, ω_z is the parasitic zero of the transconductor; ω_n and ω_0 are defined by $\frac{G_0}{C}$, and $\frac{G_m}{C}$, respectively. A non-zero output conductance limits the use of an integrator at lowfrequencies and parasitic zeros limit at highfrequencies.

$$H(s) = \frac{G_m\left(1-\frac{s}{\omega_z}\right)}{G_0+sC} = \frac{\omega_0}{s}\frac{s}{s+\omega_n}\left(1-\frac{s}{\omega_z}\right) \tag{2.19}$$

A typical phase and frequency response of a non-ideal $G_m - C$ integrator is shown in

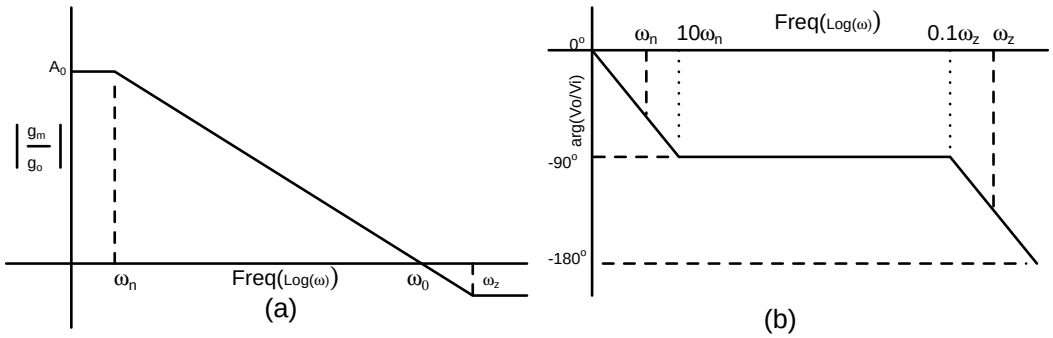

Figure 2.12: (a): Frequency response of a non-ideal G_mC integrator; (b): Phase response of a non-ideal G_mC integrator.

Figure 2.12.a and Figure 2.12.b. The effects of the non-zero output conductance and the parasitic zeroes of a non-ideal transconductor are similar to the finite gain and the high-order parasitic poles of a non-ideal opamp in the *active-RC* topology, except that here the left-half plane zero flattens the frequency response in lieu of rolling it faster. The non-zero output conductance causes a phase lead and parasitic zero causes an extra phase shift [26].

2.3.2.2 G_m-C inductor

A bandpass filter requires at least two poles to shape its frequency response. A series RLC or a parallel RLC circuits is the simplest circuit to achieve the two-pole response. In the $G_m - C$ implementation of a biquad, the inductors are emulated by a $G_m - C$ resonator structure, as shown in Figure 2.13. The value of inductance for this $G_m - C$ resonator is given by Equation 2.20. In this circuit, the input voltage is converted to a current by the transconductor (G_{m1}). This current flows into a capacitor (C), and the integrated voltage appears at the inverting input of the second transconductor (G_{m2}). Thus, this structure sources current proportional to the integral of an applied input voltage, which is identical to the behavior of an inductor.

$$L = \frac{C}{G_{m1}G_{m2}} \tag{2.20}$$

The non-idealities of the transconductor also degrades performance and quality factor of the emulated inductor. The non-zero output conductance of a transconductor increases

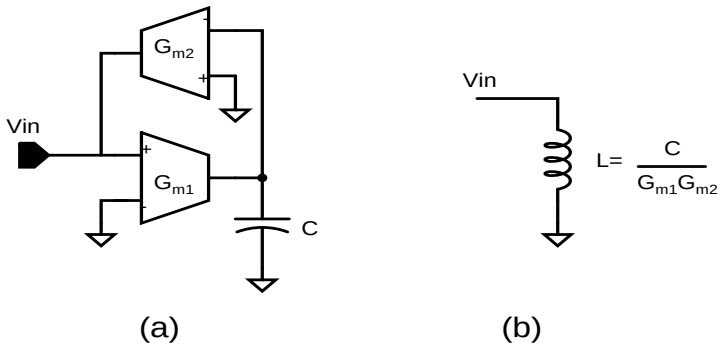

Figure 2.13: An G_mC implementation of an inductor and its value.

the resistive power dissipation in the emulated inductor, and hence it reduces the quality factor. A lumped model of the series resistance caused by the non-zero output conductance is shown in Figure 2.14.b.

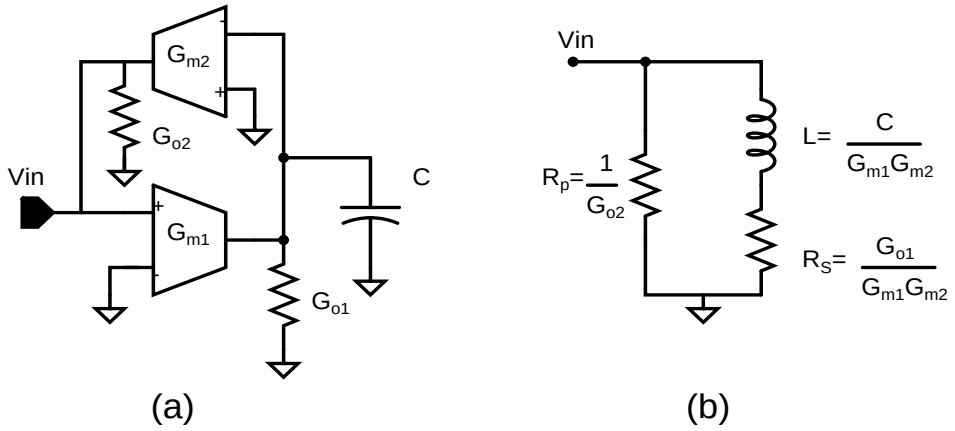

Figure 2.14: Effect of non-zero output conductance on $G_m - C$ inductor.

A parasitic zero causes an excess phase shift to a transconductor and adds a negative resistance to the $G_m - C$ inductor, which increases the quality factor and can bring instability to the system. In [37], it is shown that a parasitic pole at $4Q\omega_0$ in a transconductor, where Q is the quality factor and ω_0 is the center frequency of the resonator, causes a 6 dB increase in the pass-band gain, and a 50% increase in Q value. A non-zero output conductance of a transconductor leads the phase, and a parasitic zero lags it. Sometimes they are designed to counter balance each other [28, 37]; however, together they shift the center frequency of the filter. The effect of excess phase shift caused by zeroes is more dominant at high-frequency,

therefore, high frequency bandpass filters are vulnerable to oscillation.

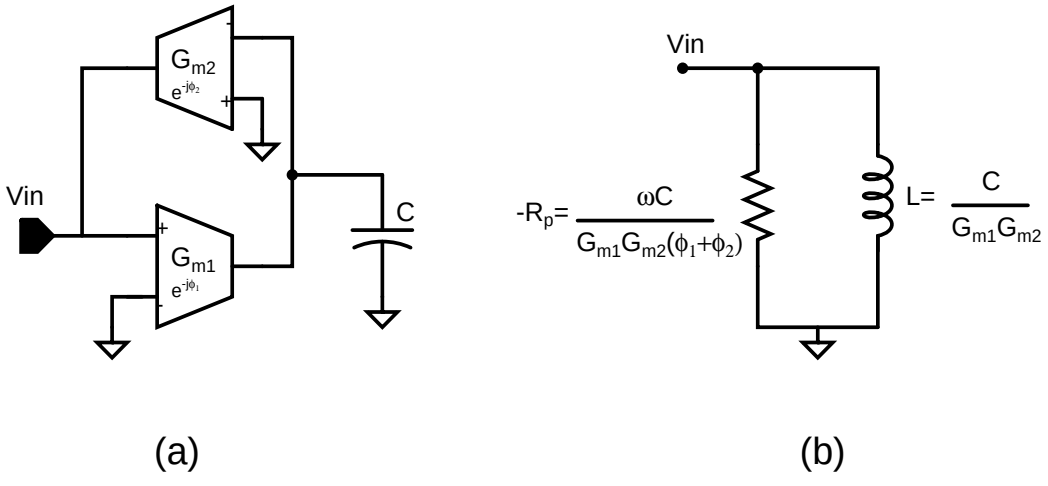

Figure 2.15: Effect of excess phase shift on $G_m - C$ inductor.

2.3.2.3 G_m-C Biquad Bandpass Filter

From the above discussion, it is evident that the $G_m - C$ inductor and integrator can only be used for frequency range between $10 \times \omega_n$ to $0.1 \times \omega_z$, because of the phase lead and lag caused by the non-zero output conductance and the parasitic pole/zero of the transconductor. In this section, the effect of these non-idealities will be observed on the performance of a biquad filter and a brief conclusion will be drawn on the basic design requirements for a transconductor.

A generic bandpass filter transfer function is given by Equation 2.10 and Equation 2.11. Once the polynomial coefficient of Equation 2.10 is replaced with the filter design parameter such as ω_0 and Q, the effective filter transfer function is given by Equation 2.21.

$$H_{BP}(s) = \frac{\frac{G_{mg}}{C_1}s}{s^2 + \frac{G_{mq}}{C_1}s + (\frac{G_{m1}G_{m2}}{C_1C_2})} = H_0 \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.21}$$

$$\text{where } H_0 = \frac{G_{mg}}{G_{mq}};\ \ \omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}};\ \ Q = \sqrt{\frac{C_1G_{m1}G_{m2}}{C_2G_{mq}^2}} \tag{2.22}$$

The schematic representation of this transfer function is shown in Figure 2.16. An equivalent lump RLC model of this filter is given by Figure 2.17. For an optimum dynamic

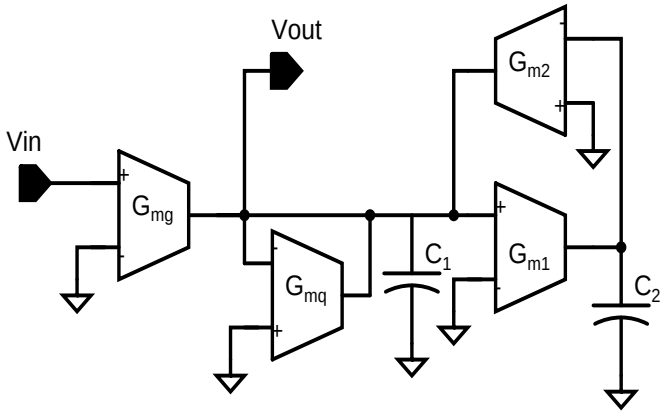

Figure 2.16: A G_mC implementation of a biquad bandpass filter.

range performance, G_{m1} and G_{m2} should be equal to G_{mf}, and C_1 should be equal to C_2 ($C_1 = C_2 = C$). Upon this optimization, the effective center frequency and the quality factor of the filter are given by Equation 2.23 and Equation 2.24 [26].

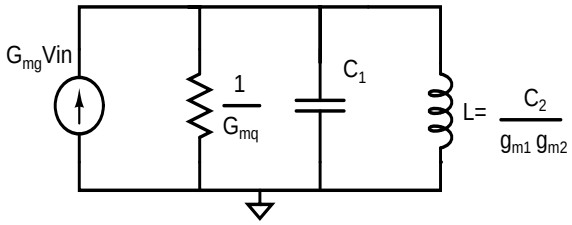

Figure 2.17: An equivalent lump RLC mode of the biquad bandpass filter.

The effect of non-dominant parasitic poles can be minimized by choosing an architecture that does not have any internal high impedance node or, if it does, it should be designed in such a way that the signal swing at the high-impedance node is small so that, the transconductor does not slew at the internal high-impedance node.

$$\omega_0 = \frac{G_{mf}}{C} \tag{2.23}$$

$$Q = \frac{G_m}{G_{mq}} \tag{2.24}$$

If the non-zero output transconductances of transconductors are taken into account, the equivalent lump model of a biquad filter is given by Figure 2.18, where G_{exph} is the

negative resistance caused by the excess phase shift and $G_{og},\ G_{oq},\ G_{o1},$ and G_{o2} are output transconductance of $G_{mg},\ G_{mq},\ G_{m1}$and G_{m2} respectively. The effective gain, center frequency, and quality factor of the filter are given by Equation 2.25, Equation 2.26, and Equation 2.27, respectively.

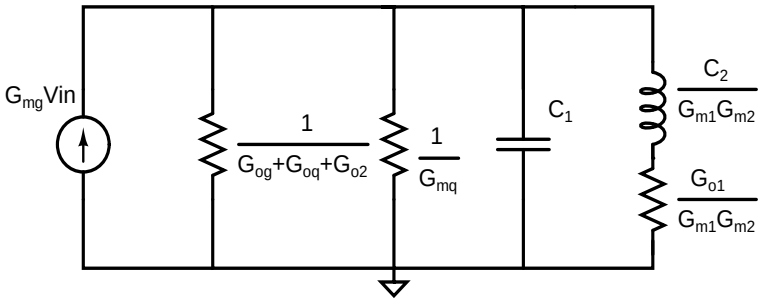

Figure 2.18: An equivalent lump RLC mode of a non-ideal biquad bandpass filter.

$$H_0 = \frac{G_{mg}}{G_{mq}} \left(\frac{1}{1 + \frac{G_{og}+G_{oq}+G_{o1}+G_{o2}-G_{exph}}{G_{mq}}} \right) \sqrt{1 + \frac{G_{o1}^2}{C^2\omega_0^2}}, \tag{2.25}$$

$$\omega_0 = \frac{G_{mf}}{C} \sqrt{1 + \frac{G_{o1}\left(G_{og} + G_{oq} + G_{o2} - G_{exph} + G_{mq}\right)}{G_{mf}^2}}, \tag{2.26}$$

$$Q = \frac{G_m}{G_{mq}} \left(\frac{1}{1 + \frac{G_{og}+G_{oq}+G_{o1}+G_{o2}-G_{exph}}{G_{mq}}} \right) \tag{2.27}$$

$$\text{where, } G_{exph} = \frac{G_{m1}G_{m2}}{\omega C}\left(\phi_1 + \phi_2\right)$$

From Equation 2.26 and Equation 2.27, the effect of non-zero output conductance can be cancelled with the effect of parasitic poles and zero; however, random variation in parasitic poles and zeroes makes this scheme unreliable. The effect of these non-idealities can also be mitigated by imposing the following inequalities during filter synthesis:

$$G_{og} + G_{oq} + G_{o1} + G_{o2} << G_{mq} \tag{2.28}$$

$$G_{exph} = \frac{G_{m1}G_{m2}}{\omega C}(\phi_1 + \phi_2) \; << \; G_{mq}$$

$$2\omega_0 Q << \omega_{p,z} \tag{2.29}$$

Thus, a transconductor should have a large output impedance, preferably larger than 40 (4×10) times the transconductance of the quality factor defining the transconductor and should have the parasitic pole and zero at frequencies higher than $2Q \times \omega_0$, as given by Equation 2.29.

2.3.2.4 Noise in a $G_m - C$ Biquad

Noise power in a passive LC resonator is independent of Q and ω_0 and is given by kT/C, where k is the Boltzmann's constant. The power spectral density (PSD) of the output current noise of a transconductor is given by Equation 2.30, where T is absolute temperature and ξ is the excess noise factor. Thus a noise equivalent model of a transconductor is given by Figure 2.19 [38, 26, 39].

$$\frac{i_n^2(f)}{\Delta f} = 4kT\xi G_m \tag{2.30}$$

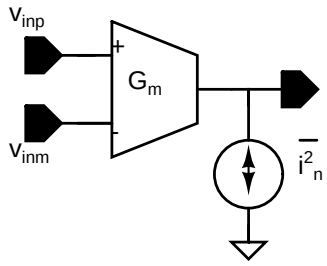

Figure 2.19: Noise equivalent model of transconductor.

Noise in a $G_m - C$ can be analyzed by replacing every transconductor of the biquad shown in Figure 2.16 by its noise equivalent model. The schematic diagram of the modified

biquad is shown in Figure 2.20, where PSDs of G_{mg}, G_{mq}, $G_{mf}(= G_{m1} = G_{m2} = G_m)$ are denoted by $i_{ng}^2(f)/\Delta F$, $i_{nq}^2(f)/\Delta F$, and $i_{nf}^2(f)/\Delta F$ and are given by $4kT\xi G_{mg}$, $4kT\xi G_{mq}$ and $4kT\xi G_{mf}$, respectively.

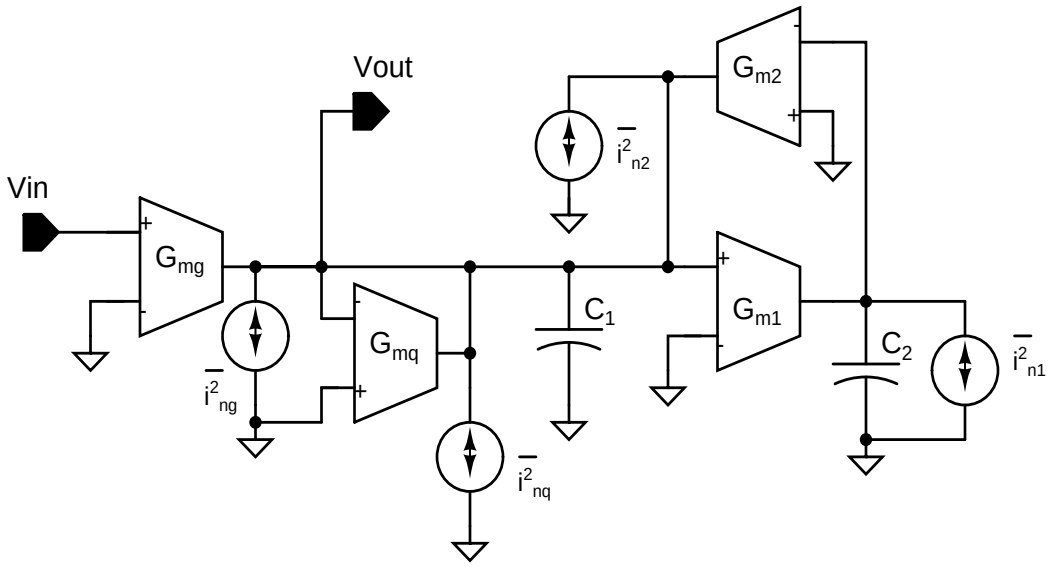

Figure 2.20: Noise equivalent model of $G_m - C$ bandpass biquad filter.

The PSD of total noise at the output and the noise equivalent bandwidth (NBW) of the bandpass biquad filter are given by Equation 2.31 and Equation 2.32, respectively.

$$v_{no} = \frac{1}{G_{mq}}\left(i_{ng} + i_{nq} + i_{n2} - \frac{G_{m1}}{j\omega_0 C_2} i_{n1}\right)$$

$$\frac{\overline{v}_{no}^2(f)}{\Delta f} = 4kT\xi\left(\frac{2}{G_{mq}} + \frac{\omega_0 C}{G_{mq}^2} + \frac{G_m^3}{G_{mq}^2\omega_0^2 C^2}\right) = \frac{8kT\xi Q}{\omega_0 C}(1+Q)$$

$$\frac{\overline{v}_{no}^2(f)}{\Delta f} \approx \frac{8kT\xi Q^2}{\omega_0 C} \tag{2.31}$$

$$NBW = \frac{\omega_0}{4Q} = \frac{\pi f_0}{2Q} \tag{2.32}$$

Thus, the total noise power at the output of a bandpass biquad filter is given by Equation 2.33. This results holds true only if the bias current of the transconductors scale with

the value of transconductance.

$$\overline{v}_{n0}^2 = \frac{2kT\xi Q}{C} = \frac{2kT\xi Q\omega_0}{G_m}. \tag{2.33}$$

2.3.3 Log-domain Filter

A log-domain filter exploits the exponential voltage-current relationship of a BJT device to do large-amplitude signal processing in a low-voltage environment. This architecture compresses the input signal with a logarithmic compressor at the input stage and expands the processed signal at the output stage using an exponential expander. This process of of compressing and expanding the signal is often known as *companding*. A transistor-level schematic of a first-order log-domain filter is shown in Figure 2.21 [40].

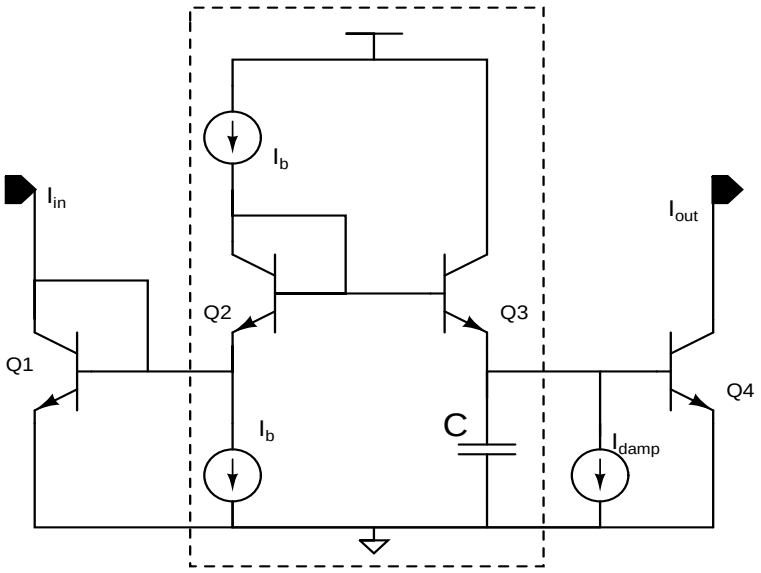

Figure 2.21: A first-order log-domain filter.

The transistors Q1 and Q4 work as a logarithmic compressor and an exponential expander, respectively. The base current of all transistors is assumed negligible or is neglected to simplify the analysis of this circuit. With this simplification the base voltage of the transistor Q3 is given by Equation 2.34, where V_T is the thermal voltage and I_s is the reverse saturation current of the bipolar transistors.

$$V_{B3} = V_T \ln\left(\frac{i_{in}}{I_s}\right) + V_T \ln\left(\frac{I_b}{I_s}\right) = V_T \ln\left(\frac{i_{in} I_b}{I_s^2}\right) \tag{2.34}$$

The current in the capacitor and the output current at the collector of transistor Q4 are given by Equation 2.35 and Equation 2.36, respectively.

$$i_C = C\,\frac{dV_C}{dt} = I_s e^{\frac{V_{B3}-V_C}{V_T}} - I_{damp} = \frac{i_{in} I_b}{i_{out}} - I_{damp}, \tag{2.35}$$

$$i_{out} = I_s e^{\frac{V_C}{V_T}} \tag{2.36}$$

$$\frac{i_{out}}{d_T} = \frac{i_{out}}{V_T}\frac{dV_C}{dT} \tag{2.37}$$

Upon some simplifications, and using the value of differentiation of the output current, Equation 2.35 and Equation 2.36 give the partial derivative of the input and output currents, as given in Equation 2.38. The Laplace transform of Equation 2.38 transforms the relationship between i_{out} and i_{in} into the s-domain, where I_{out} and I_{in} are the Laplace transforms of the current i_{out} and i_{in}, respectively. The gains of the filter and pole frequency are given by $H_0 = I_b/I_{damp}$ and $\omega_0 = I_{damp}/CV_T = \frac{g_{m3}}{C}$, respectively. The pole frequency of the filter is defined by the integrating capacitor (C) and the transconductance of the transistor Q3, which can be tuned by either trimming the value of capacitor (C) or changing the value of the bias current I_{damp}.

$$\frac{i_{out}}{d_T} + \frac{i_{damp}}{CV_T} i_{out} = \frac{I_b}{CV_T} i_{in} \tag{2.38}$$

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\frac{I_b}{CV_T}}{s + \frac{I_{damp}}{CV_T}} = H_0 \frac{\omega_0}{s + \omega_0} \tag{2.39}$$

The magnitude of the intermediate signals at internal nodes is kept small; therefore this architecture do not introduce any large signal distortion caused by the slew-rate limitation. However, small signal amplitude at internal nodes makes it susceptible to noise. Since the

expansion of the processed signal takes place at the output stage, the noise of the entire filter is amplified exponentially during this expansion process.

Despite its superior performance in large-signal environments, and high-frequency capabilities, the log-domain filter did not receive a widespread adaptation because of either poor BJT device or the unavailability of native BJT devices in a modern CMOS process. The integrated BJT devices in a digital CMOS processes have small current gain (β) and low early voltage (V_A), which degrade the quality factor and frequency of operation of the filter. An exponential behavior of the sub-threshold MOSFET devices can also be used for companding, However, their frequency of operation is limited because of low f_T of the sub-threshold devices.

2.3.4 Current Mode Filter

A current mode filter takes the good aspects from both the $G_m - C$ filter and log-domain filter. Here, signals are kept in the current domain without any compression. All internal nodes of this architecture are low-impedance nodes. Therefore there is no voltage swing or slew limitation. The poles frequency of these low-impedance nodes is also located at high frequency. These two advantages make this architecture suitable for high frequency application. A typical schematic diagram of a differential integrator is shown in Figure 2.22 [41]. In this architecture, only outputs are the high-impedance node. The transfer function of this integrator is given by Equation 2.40, where i_p and i_n are the positive and negative differential current, respectively, and C is the integrating capacitor.

$$i_{out} = K\frac{g_{m3}}{sC}(i_p - i_n) \tag{2.40}$$

The small signal swing at all the internal node also enables this architecture to use the high-density MOSFET gate capacitor as an integrating capacitor and makes it suitable for integration in digital CMOS processes. However, the poor transconductance and low output impedance of the CMOS devices in sub-micron CMOS processes limits the impedance at the internal nodes. The low output impedance of the mirror device is often improved by cascoding the output device.

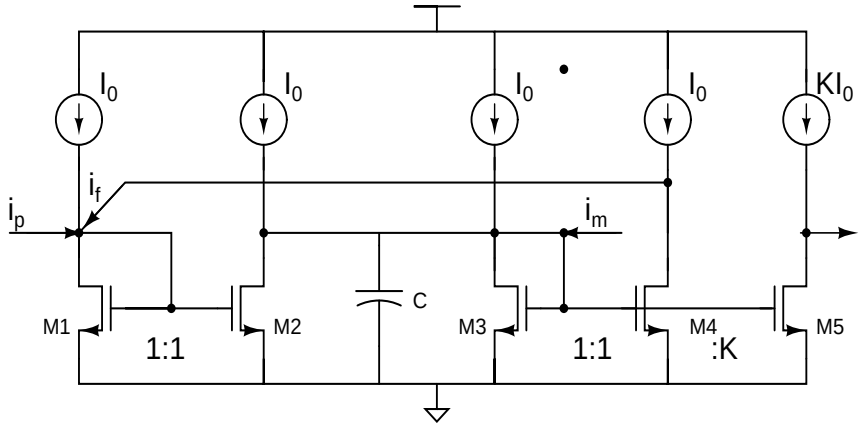

Figure 2.22: A first-order current mode filter.

This architecture uses current mirrors and current copies extensively; therefore, it has large current consumption. Also, the gain in this architecture comes from the output current mirror stage, which increases the output current noise and limits its dynamic range. Therefore despite its low voltage of operation, the current consumption and limited dynamic range do not make this architecture suitable for portable application.

2.4 Challenges to Realize a Bandpass Filter

Bandpass filters are commonly used as channel-select or band-select filters in communication systems; they are also used as front-end band limiters in band-limited applications or data converter systems (DCS). High-frequency and high-Q bandpass filters are of particular interest, as they are used as an IF filter in superheterodyne receivers and are implemented using off-chip SAW or BAW devices. SAW and BAW devices are passive components. They rely on mechanical and acoustic property of the material. A SAW device is a comb-like metal structure imprinted on a piezoelectric material, as shown in Figure 2.23. Once excited by an electrical signal, an acoustic wave, whose wavelength 'λ' is defined by the comb separation, propagates at the surface of the piezoelectric material and gets collected at the output. This piezoelectric wave travels along the surface of the material as it decays exponentially along the depth.

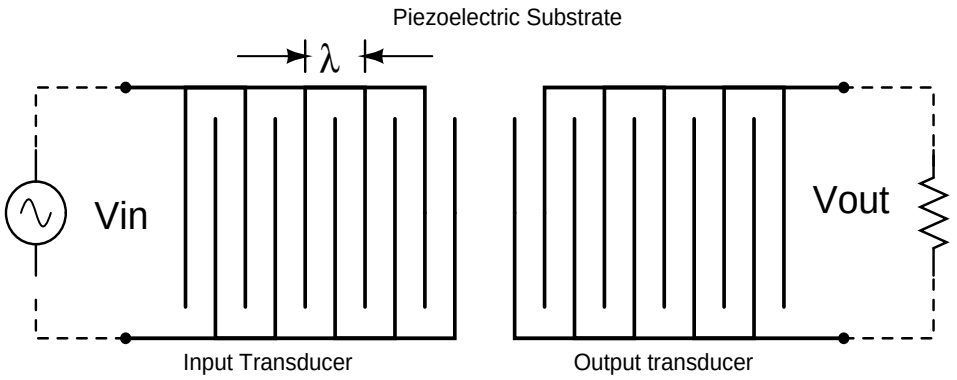

Figure 2.23: Foot prints of a typical SAW device.

The separation between the comb-fingers (λ) defines the center frequency and the bandwidth of the filter. Since the separation between the fingers is precisely defined and held constant, these SAW filters are primarily narrow-band filters and that gives high selectivity. The upper and lower cut-off frequencies are defined by the processing of the mechanical structure and by the material property such as loss. SAW filters have been used reliably for high-frequency (100 MHz to 10 GHz) and high-Q ($\sim$100) filter applications since their discovery in 1887 by Lord Rayleigh.

For wide-band application, where the frequency of interests encompasses large bandwidth, a SAW filter gives large loss, as its mechanical structure is tuned only for one or a set of frequencies, as indicated in Table 1.2. Therefore, for a wide-band applications, such as 3G communication or a generic ADC/DAC, on-chip bandpass filters are preferred. However, designing a high-Q, high-frequency bandpass filters has challenges of its own, some are discussed briefly in this section

2.4.1 Design Issues

2.4.1.1 Noise

The noise power of a bandpass filter is proportional to the bandwidth of the filter. Therefore, a good system-level analysis should be performed to determine the required bandwidth of the filter. If the bandwidth of a filter is large, then it degrades the signal-to-noise ratio (SNR) of the filter, and if it is small, the signal information is lost. Thus, the bandwidth of

a filter is critical to the system performance since it defines the selectivity and sensitivity of the system. Passive filters such as SAW and BAW filters have less noise than an on-chip filter; however, they introduce 6∼23 dB of loss, whereas on-chip filters can easily provide 6-20 dB of gain. Therefore, one can achieve a better system performance, even with higher noise, from an on-chip filter, by properly choosing a low-noise on-chip architecture and doing noise and maximum signal handling capacity analysis of the individual blocks at the system-level design. An IF filter is mostly followed by a DVGA in a communication systems. The coarse tuning of the DVGA can be combined with an on-chip programmable IF filter. Noise in a bandpass filter is also proportional to the quality factor of the filter [42].

2.4.1.2 Dynamic range

Dynamic range is an important indicator of system performance. It is a ratio of the maximum level of the signal, such as voltage, current, power, or frequency, to the minimum detectable signal, which is usually set by the noise, as defined in Equation 2.41. Thus, to achieve a large dynamic range, low-noise circuits, which can handle large input-output signals, should be used. In general these two design requirements give contradictory specifications, *e.g*, for a low-noise system, one will increase the transconductance of the input stage, but it reduces the maximum signal handling capacity of the system for a given current. Maximum signal handling capacity can be improved by increasing the supply voltage or by increasing the power dissipation, which is again a conflict with the prime goal of making a low-voltage and low-power circuits [26].

$$DR = \frac{S_{max}^2}{s_n^2} = \frac{P}{\eta k T f_B} \tag{2.41}$$

There is fundamental relationship between power dissipation and maximum the dynamic range achieved by an analog filters. For example, the fundamental limitation of dynamic range of a lowpass filter is given by Equation 2.41, where k is the Boltzmann constant, T is the absolute temperature, f_B is the noise equivalent bandwidth of the filter, and η is the dimensionless quantity, which depends on the implementation technique [26]. Noise in a bandpass filter is proportional to Q; thus dynamic range is inversely proportional to the

quality factor of the filter.

2.4.1.3 Sensitivity

As discussed in Section 2.1, multiple feedback loop approach has the least component sensitivity. It is resilient to process and temperature variation, so it is very hard to tune. The cascade approach is the most popular structure for the monolithic implementation of a high-Q, high-frequency, bandpass filter. It does have the highest component sensitivity, but it is also easy to tune. Therefore, most monolithic implementations of filters have an auxiliary tuning circuit to tune the filter parameters. These tuning schemes can be static or automatic.

In the static approach, filters are tuned using laser or diode trim links at the time of manufacturing. This tuning scheme tunes against process variation, but temperature variation remains a problem, as monolithic passive devices in CMOS processes tend to have large temperature coefficients. Thus, for an on-chip filter in an application where performance has to be met across temperature, an automatic tuning algorithm is required. An automatic tuning algorithm continuously senses the filter parameters and tunes them to the desired or the reference value [43].

2.4.1.4 Power Consumption

For portable applications, power consumption and supple voltage are a major concern, as they ensure long battery life. Low supply voltage means a lower maximum signal handling capacity; therefore, to achieve large dynamic range, one has to employ a lateral degenerative circuit design technique, which consumes more current but requires less headroom. A lateral structure also increases the number of active devices, which means more noise. Thus, for an analog circuit, low-voltage does not necessarily always means low power. One has to make a judicious decision based on the manufacturing process and application requirements to make power-optimized design [44].

2.4.2 Implementation Issues

Monolithic high-Q, high-frequency, bandpass filters are implemented using the cascade design approach, where higher-order filters are broken into first-order and second-order filter transfer functions. The poor temperature coefficient of monolithic passives, their process variation, change in end-user environment, and variation due to change in bias point cause a shift in filter parameters over time. Therefore, a monolithic implementation of bandpass filters needs a center frequency and a quality factor tuning scheme to ensure their performance over the above mentioned variations. There has been a significant amount of work done on center frequency tuning of a bandpass filter; however, work on quality factor tuning scheme is scarce. In this chapter, several quality factor tuning schemes are discussed and their limitations and possible improvements analyzed.

2.4.2.1 Monolithic Bandpass Filters

The transfer functions of a bandpass filter in terms of filter parameters are given by Equation 2.42 and Equation 2.43, where center frequency, quality factor, and bandwidth of the bandpass filter are ω_0, Q, and $\frac{\omega_0}{Q}$, respectively. The two filter transfer functions differ in terms of their mid-band gains at the center frequency. The mid-band gain of the bandpass filter given by Equation 2.42 and Equation 2.43 are $H_0' \times Q$ and H_0, respectively.

$$H(s) = H_0' \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.42}$$

$$H(s) = H_0 \frac{\frac{\omega_0}{Q} s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.43}$$

A $G_m - C$ representation of the above transfer function is given by Equation 2.44, and Equation 2.45, respectively. The mid-band gains of these filters are given by $\frac{G_{mg}}{G_{mq}}$, and $\frac{G_{mg1}}{G_{mg2}}$, respectively. The center frequency and the quality factor of these filters are given by $\frac{G_m}{C}$ and $\frac{G_{mf}}{G_{mq}}$, respectively. In this chapter, the transfer function given by Equation 2.44 is used for derivations and its $G_m - C$ implementation is shown in Figure 2.24.

$$H_{BP1}(s) = \frac{\frac{G_{mg}}{C}s}{s^2 + \frac{G_{mq}}{C}s + (\frac{G_{mf}}{C})^2} \tag{2.44}$$

$$H_{BP2}(s) = \frac{\frac{G_{mg1}}{G_{mg2}}\frac{G_{mq}}{C}s}{s^2 + \frac{G_{mq}}{C}s + (\frac{G_{mf}}{C})^2} \tag{2.45}$$

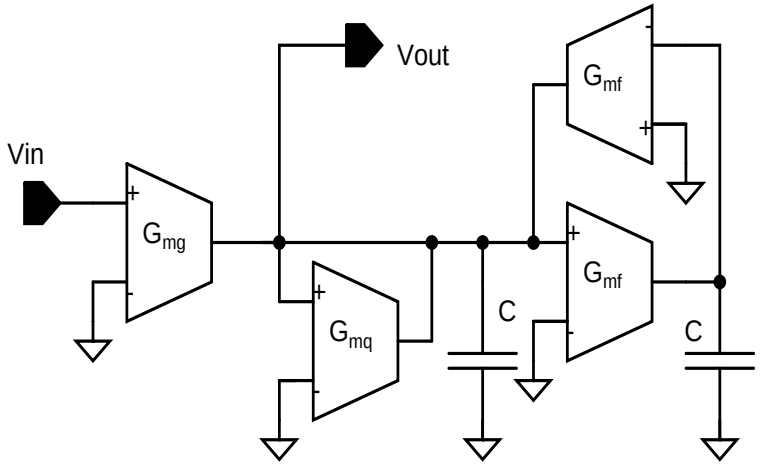

Figure 2.24: Single ended G_mC bandpass bi-quadratic filter.

In modern IC processes, poly-resistors and poly-to-poly capacitors are fabricated with $\pm 3\sigma$[1] variations of $\pm 15\%$, and $\pm 10\%$, respectively. The transconductance of an OTA is made a function of bias current, resistor value, or device size. The bias current in the monolithic circuit is generated by having a known voltage drop across a known value of resistor. Thus, the statistical variation of a bias current is the sum of these two independent statistical events (voltage variation and resistor variation). For calculation, we will assume that the bias current has a variation of $\pm 20\%$.

The transconductance of a transistor is given by $\sqrt{2\beta I_D}$; thus, a change of $\pm 20\%$ in bias current will cause a corresponing change of $\pm 10\%$ in transconductance value. If one takes both capacitor and transconductance variation into account, the center frequency of the above $G_m - C$ filter can have an offset of $\pm \%20$ with respect to its designed value. Therefore, a $G_m - C$ filter is always designed with an auxiliary tuning circuits to tune its

[1] $\pm 3\sigma$ is a statistical number, which includes 99.99% of Gaussian statistical event with standard deviation of σ.

center frequency. This auxiliary tuning circuit detects the current center frequency and adjusts the value of the transconductance of G_{mf} to tune the filter to its designed value [45].

In modern IC processes, the individual value of the components can have a variations of $\pm 20\%$, but their ratios (of alike terms), such as gain or quality factor of a $G_m - C$ filter, can be manufactured accurately, if their size and value are on the same order of magnitude. Process variation is a global event on-wafer; therefore, all like components tend to shift together in one direction in localized space. Thus, both numerator and denominator quantities of such ratios usually vary by a same relative amount to their original value, and their ratio remains unaffected, assuming the devices have the same area. However, this condition holds true only for a small to a moderate ratio (< 10) of terms. If this ratio becomes larger, such as is the case in a high-Q (~ 50) filter, then the area of two transconductors cannot be kept the same, and this analogy does not hold true. Thus, high-Q filters also need an auxiliary tuning mechanism to tune their quality factor.

The center frequency of the filter is tuned by changing the value of G_{mf}. Once G_{mf} is fixed by the center frequency of the filter, the value of Q is tuned by changing the value of G_{mq}. Hence, the center frequency of a filter needs to be tuned before the Q. The excess phase shift resulting from the higher-order parasitic poles and zeros also increases the quality factor of the filter, as given in Equation 2.29. This increases in quality factor can bring instability to the system.

2.5 Transconductors

There are primarily two ways to realize a transconductor in today's IC processes. One, the transconductance is defined by the *active* devices, such as transistors. Second, it is defined by the passive components, such as resistors.

2.5.1 Simple Differential Pair

A differential amplifier is often used as an input transconductor stage in many operational amplifiers. A schematic diagram of a differential amplifier is shown in Figure 2.25, where V_{cm} is the common mode signal to bias them, V_{id} is the input differential signals and I_{EE}

is the tail current.

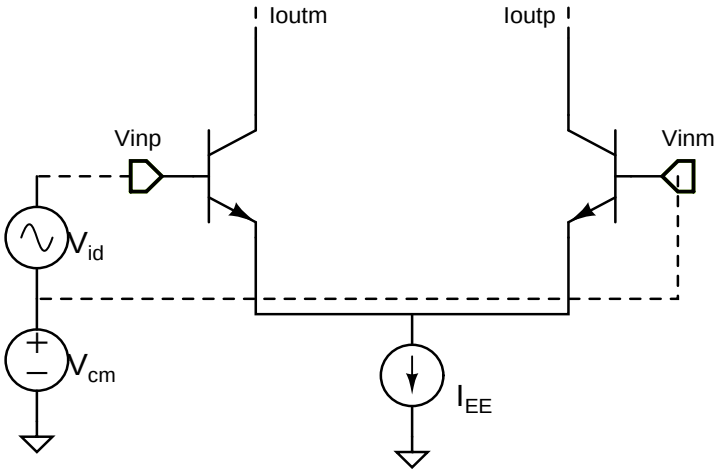

Figure 2.25: A simple differential pair transconductor.

The output current and the transconductance of this differential pair are given by Equation 2.46, where α_F is the device parameter given as $\beta/(1+\beta)$.

$$v_{id} - V_{Q1} + V_{Q2} = 0$$

$$\frac{I_{c1}}{I_{c2}} = e^{\frac{V_{Q1}-V_{Q2}}{V_T}} = e^{\frac{v_{id}}{V_T}}$$

$$\frac{I_{c1}-I_{c2}}{I_{c1}+I_{c2}} = \frac{i_{out}}{\alpha_F I_{EE}} = \frac{e^{\frac{v_{id}}{2V_T}} - e^{-\frac{v_{id}}{2V_T}}}{e^{\frac{v_{id}}{2V_T}} + e^{-\frac{v_{id}}{2V_T}}}$$

$$i_{out} = i_{outp} - i_{outm} = \alpha_F I_{EE} \ \tanh\left(\frac{v_{id}}{2V_T}\right) \tag{2.46}$$

The large-signal transconductance of the differential pair and its first-order component are given by Equation 2.47.

$$g_m = \frac{\alpha_F I_{EE}}{2V_T} \ \mathrm{sech}^2\left(\frac{v_{id}}{2V_T}\right) = G_{m0} \ \mathrm{sech}^2\left(\frac{G_{m0} v_{id}}{I_{IEE}}\right), \tag{2.47}$$

$$\text{where } G_{m0} = \frac{\alpha_F I_{EE}}{2V_T} = \frac{I_C}{V_T} \tag{2.48}$$

The Taylor series expansion of *sech* is given by Equation 2.49. The above transconductance expression is expanded using Taylor series expansion to get an expression for the third-order non-linearity term, given in Equation 2.50.

$$\text{sech}(x) = 1 - \frac{1}{2}x^2 + \frac{5}{24}x^4 - \cdots \tag{2.49}$$

$$\alpha_{3,G_m} = \frac{1}{2I_{EE}^2} \tag{2.50}$$

The -1 dB compression point of the differential pair transconductor is given by Equation 2.51. The linearity of a filter is also commonly rated for 40 dB linearity point, which corresponds to a 1% compression point. The 40 dB linearity point for the a differential transconductor is given by Equation 2.52.

$$V_{-1dB,G_m} = \sqrt{\frac{0.145}{|\alpha_{3,G_m}|}} \times \frac{1}{G_{m0}} = 0.533 \times \frac{I_{EE}}{G_{m0}} \tag{2.51}$$

$$V_{1\%,G_m} = \frac{0.1}{\sqrt{|\alpha_{3,G_m}|}} \times \frac{1}{G_{m0}} = 0.141 \times \frac{I_{EE}}{G_{m0}} \tag{2.52}$$

Thus, a differential amplifier gives 40 dB of linearity for a voltage amplitude of $\pm 0.282\ V_T$. The linearity of the differential pair transconductor can be improved by applying negative feedback to them; however, before going into the details of the linearization technique, noise in a differential pair is discussed here.

The output current noise of BJT and MOS transistors is given by Equation 2.53, and Equation 2.54, respectively.

$$\frac{\overline{i_n}^2}{\Delta f} = \frac{8kTG_{m0}}{3} \tag{2.53}$$

$$\frac{\overline{i_n}^2}{\Delta f} = 2qI_C \tag{2.54}$$

$$\overline{i_{no}}^2 = \overline{i_{nop}}^2 + \overline{i_{nom}}^2 = 2qI_{EE} \tag{2.55}$$

Table 2.2: Differential pair transconductor comparison in BJT and CMOS processes.

Process	G_m	α_3	V_{-1dB}	**Noise**(i_n^2)
BJT	$\frac{I_{EE}}{2V_T}$	$\frac{1}{2I_{EE}^2}$	$0.533\frac{I_{EE}}{G_{m0}}$	$2qI_{EE}$
CMOS	$\frac{1}{2}\sqrt{\beta_n I_{SS}}$	$\frac{3}{2I_{SS}^2}$	$0.31\frac{I_{SS}}{G_{m0}}$	$\frac{8kT\xi G_{m0}}{3}$

The total output current noise of a BJT differential pair is given by Equation 2.55. The above derivation is also performed for a MOS differential pair and their performances are compared in Table 2.5.1. It is obvious from this comparison that the BJT differential can provide higher linearity for the same amount of current at lower noise value. Also, the parasitic capacitance at the output of the transconductor is smaller in the BJT process, which results in high frequency of operation.

2.5.2 Degenerated Differential Pair

The linearity of a transconductor is improved by applying a local or global negative feedback loop around them. A feedback loop improves the linearity of the circuit by the $20\log(A_{fb})$ dB, where A_{fb} is the feedback loop gain. The simplest feedback to a differential pair is emitter degeneration, as shown in Figure 2.26. The voltage drop across the resistor increases the minimum power supply requirement or it reduces the output signal swing. Neither is desirable. This problem is solved using a lateral degeneration between the two emitters, as shown in Figure 2.27 [32, 46, 27].

The output current and the transconductance of the degenerated differential pair is given by Equation 2.56 and Equation 2.57, respectively. These equations hold true for both lateral and vertical degenerated differential pair.

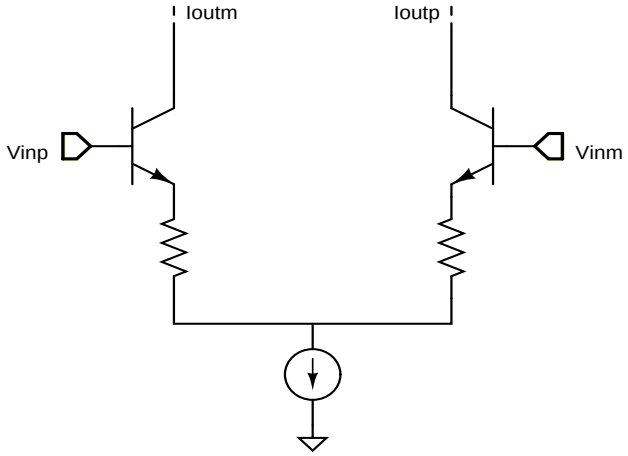

Figure 2.26: A vertical degenerated differential pair transconductor.

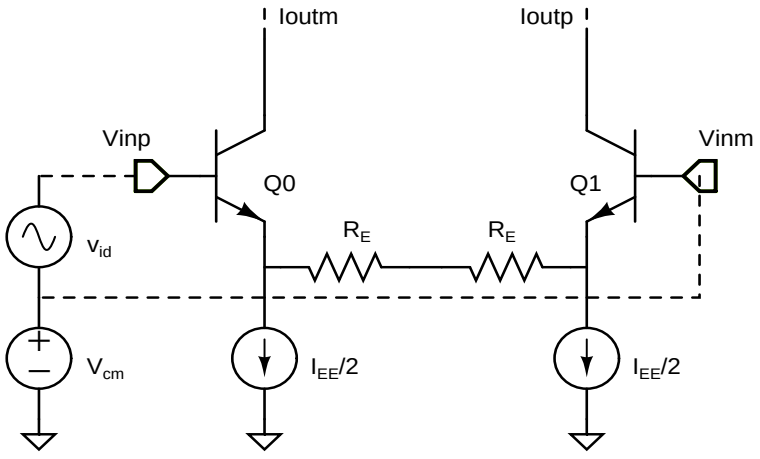

Figure 2.27: A horizontal degenerated differential pair transconductor.

$$i_{out} = \alpha_F I_{EE} \ \tanh\left(\frac{v_{id} - i_{out}2R_E}{2V_T}\right) \tag{2.56}$$

$$G_m = \frac{G}{1 + 2GR_E}, \tag{2.57}$$

$$\text{where } G = \frac{\alpha_F I_{EE}}{2V_T} \ \text{sech}^2\left(\frac{v_{id} - i_{out}2R_E}{2V_T}\right) \tag{2.58}$$

Once the term G in the above transconductance is expanded using Taylor series expansion given by Equation 2.49 and a first-order order approximation is made, the transconductance of an emitter degenerated differential pair is given by Equation 2.59, where g_m is the transconductance of the individual transistor of the differential pair and its value is given by Equation 2.60.

$$G_{m0} = \frac{g_m}{1 + g_m R_E} \tag{2.59}$$

$$g_m = \frac{\alpha_F I_{EE}}{2V_T} \tag{2.60}$$

The third-order non-linearity (α_3) of the emitter degenerated differential pair can be calculated using the secant hyperbolic series expansion in Equation 2.57, and with some approximation [2], can be simplified to

$$\alpha_{3,eG_m} = \frac{1}{2I_{EE}^2\left(1 + g_{m0}R_E\right)} \tag{2.61}$$

The above equation suggests that the linearity of the circuit has improved by the feedback loop gain ($1+g_m R_E$). It also improves the corresponding V_{-1dB} and $V_{1\%}$ compression point by the same amount.

The above analysis is independent of type of emitter degeneration used with the differential pair. Thus, the same analysis holds true for both circuits given by Figure 2.26

[2] Approximate the 'G' in denominator with G_{m0}

and Figure 2.27, with some obvious limitations such as the maximum output current being limited by the tail current I_{EE}. Minimum power supply requirement, and noise are other key parameters in choosing one structure over the another.

In the vertical degenerated differential pair shown in Figure 2.26, the noise generated by the tail current source is cancelled at the output, assuming the element of the differential pair are matched and have the same input impedance at the emitters. However, in a lateral degenerated differential pair, there are two independent current sources and the impedances looking into either side of the emitter are different ($1/g_m$ and $R_{EE} + 1/g_m$); therefore the tail current noise is not cancelled at the output [47]. Thus, the choice of topology is a trade-off between noise and the minimum power supply requirement [3].

2.5.3 Feedback Loop

Several different transconductor circuits with varying degree of linearity have been reported in the literature. Some of these circuits are shown in Figure 2.29. A set of performance metrics has been chosen to compare the performance of these circuits on the same process (0.25 μm BiCMOS), which includes DC linearity, small-signal bandwidth, and total harmonic distortion (THD). The performance comparison is complied in Table 2.3 for quick reference.

The *active* transconductors uses several active devices in parallel to improve its linearity; the doublet structure shown in Figure 2.29.b is a good example [32]. They are primarily open-loop structures and therefore have low linearity, and high cut-off frequency. The *passive* transconductors use operational amplifiers or differential pairs made by the active device to generate the input voltage across the inherently linear resistors, to generate the signal current. Sometimes, these structures also use the feedback loop to further improve their linearity by approximately $20\ln(A_v)$ dB, where A_v is the feedback loop gain. These feedback loops improve linearity, but they limit the frequency of operation to the loop bandwidth [29, 31, 30, 48, 49, 29, 50].

The linearity metric for the transconductors has been chosen as a 500 mV peak-to-peak

[3] it could be as high as twice the regular diff-pair, depending upon the implementation of current sources

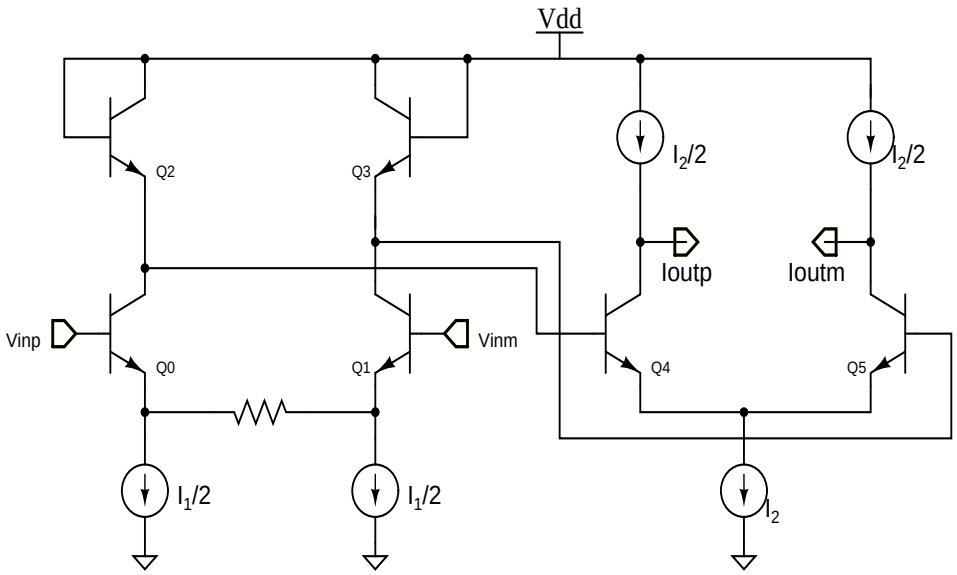

Figure 2.28: A doublet degenerated differential pair transconductor.

Table 2.3: Transconductors and their linearity.

Description	G_m	**Linearity**	f_{Cutoff}	**THD**
Degenerated differential pair	$\frac{g_m}{1+g_mR}$	Poor	High	Poor
Doublet differential pair	$K\frac{g_m}{1+g_mR}$	Low	High	Poor
Lateral degen. differential pair	$\frac{gm}{1+gmR}$	Low (40 dB)	High (2 GHz)	Medium
Lateral diff. pair with feedback	$\sim \frac{1}{R}$	High (90 dB)	Low (GBW)	Good

signal at the output of the IF filters. The cut-off frequency metric comes from the fact that the high-frequency bandpass filters suffer from instability. As discussed in Section 2.3.2.3, the minimum bandwidth of the OTA or the transconductor should be greater than $0.2Q\omega_0$. Thus, this research will require a transconductor circuit, whose bandwidth is at least 1.5 MHz, to implement a 100 MHz bandpass filter. Since the center frequency of the IF filter varies from 10 MHz to 300 MHz, it is definitely desirable to have a transconductor with a bandwidth greater than 1.5 GHz[37].

The results summarized in Table 2.3 suggests that the linearity of *lateral degenerated differential pair with feedback loop* is the best. However, it is not attractive on bandwidth metric. The *lateral degenerated differential pair* is the second best in terms of linearity and also has bandwidth over 2 GHz. There is no feedback loop in the second circuit, therefore

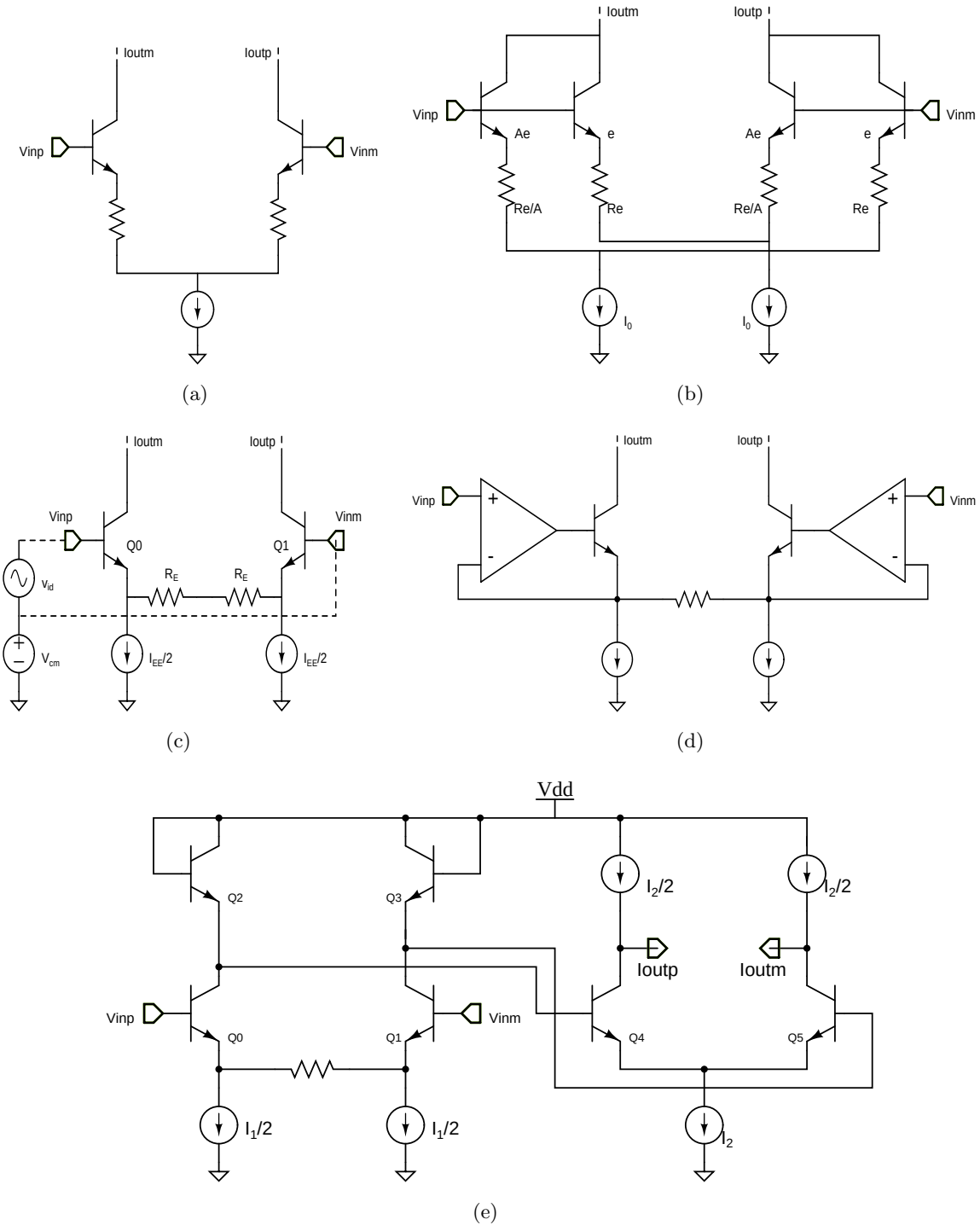

Figure 2.29: a: Degenerated differential pair. b: Doublet degenerated pair. c: Lateral degenerated differential pair d: Lateral degenerated differential pair with feedback loop e: Folded lateral degenerated differential pair.

its linearity is moderate and bandwidth is high [32]. The Gilbert transconductor circuit shown in Figure 2.29.e is a low-voltage derivative of the circuit shown in Figure 2.29.c.

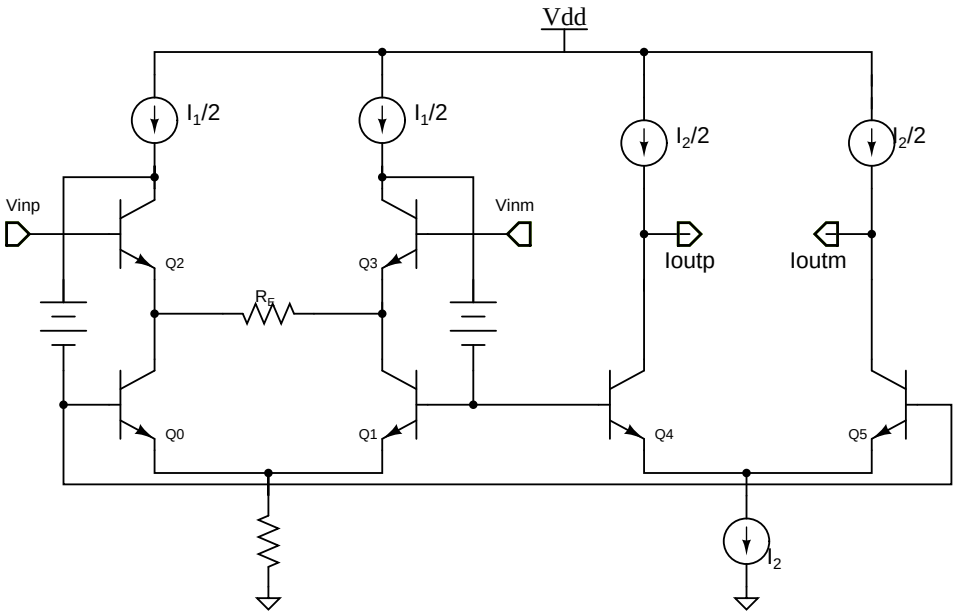

Figure 2.30: Enhanced Gilbert cell structure.

An enhanced version of this Gilbert cell structure is shown in Figure 2.30; it has a feedback around the input differential to improve its linearity. The feedback loop consists of high-frequency structures and it has local feedback loop around the input differential pair; therefore, it does not hurt the frequency response of the transconductor [51].

2.5.4 Manufacturing Process

The discussion of speed or bandwidth cannot be concluded without reviewing the manufacturing processes. Two state-of-the-art manufacturing processes are compared in Table 2.4 on the basis of f_T, transconductance, flat-band noise, and cost. The obvious choices of manufacturing processes are the sub-micron ($0.18\mu m$) CMOS technology and the sub-micron CMOS process with hetero-junction bipolar transistor (HBT). The CMOS process with native HBT devices is known as Bipolar CMOS (BiCMOS) technology.

The f_T of a CMOS process is an inverse function of $\frac{1}{L^2}$, and flat-band-noise is proportional to L, as given in Equation 2.62 and Equation 2.64. The output resistance of

Table 2.4: State-of-the-art monolithic IC manufacturing processes.

Process	f_T	G_m	Noise	Cost
CMOS($0.18\mu m$)	$\frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}}$	$\sqrt{\frac{2W\mu C_{OX}I_d}{L}}$	$\frac{8KTG_m}{3}$	150K
BiCMOS($0.25\mu m$	$\frac{1}{2\pi}\frac{G_m}{C_\pi+C_\mu}$	$\frac{I_C}{\phi_T}$	$4KTr_b$	150K

a MOSFET device is given by Equation 2.66, where λ is the channel length modulation parameter, which decreases with an increase in channel length; therefore, the r_{ds} is proportional to channel length (L). Thus, a long-channel device is desirable to get good linearity and high gain. However, it reduces the f_T and increases the noise. Noise can be compensated by increasing the width of the device, but this further reduces the f_T. Thus, there is a trade-off among linearity, speed, and noise.

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}+C_{gd}} \sim \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{3}{4\pi}\frac{\mu_0}{L^2}\left(V_{GS}-V_T\right) \tag{2.62}$$

$$C_{gs} = \frac{2}{3}C_{ox}WL \tag{2.63}$$

$$e_n^2 = \frac{8KT(1+\eta)}{3g_m} = \frac{8KTL(1+\eta)}{3\mu_0 C_{ox}W\left(V_{GS}-V_T\right)} \tag{2.64}$$

$$g_m = \mu_0 C_{ox}\frac{W}{L}\left(V_{GS}-V_T\right) \tag{2.65}$$

$$r_{ds} = \frac{1}{\lambda} = f(L) \tag{2.66}$$

The HBT devices behave and work the same way as a bipolar junction transistors (BJTs). They are built the same way except that Germanium (Ge) is implanted in the base of the device to reduce the base resistance(r_b), and to increase the β and the f_T of the device [52]. The small base resistance makes HBT devices less noisy compared to BJT devices. In the past few years, HBT devices have been added successfully to the standard CMOS flow with few additional mask steps. Thus, the BiCMOS manufacturing process is completely compatible with low-cost CMOS and provides the designer an advantage of

using the native superior BJT-like transistor.

The HBT devices are bulk devices and therefore can carry higher current density than their CMOS counterparts, which means smaller parasitic capacitance. The transconductance of an HBT device is higher than the MOSFET device for the same current. The base resistance of the HBT devices is on the order of $30 \sim 50\ \Omega$, so their voltage noise is also smaller than that of MOSFET devices. The transconductance and voltage noise of HBT devices is tabulated in Table 2.4. Lower parasitic, higher transconductance, and low voltage noise makes the BiCMOS process suitable for RF and high-frequency applications. Thus, this research plans to use the 0.25 μm BiCMOS process.

2.6 Bandpass Filter Tuning Techniques

2.6.1 Filter Tuning Methods

A tuning scheme of a filter is used in conjunction with either the *master-slave tuning* or *direct tuning* strategy. In the *master-slave* strategy, the designed filter parameters are extracted from a prototype *master* filter and are used by the tuning algorithm to tune the higher-order *slave* filter. In this strategy, an application filter can be tuned while it is operational. A pictorial representation of this tuning strategy is shown in Figure 2.31.

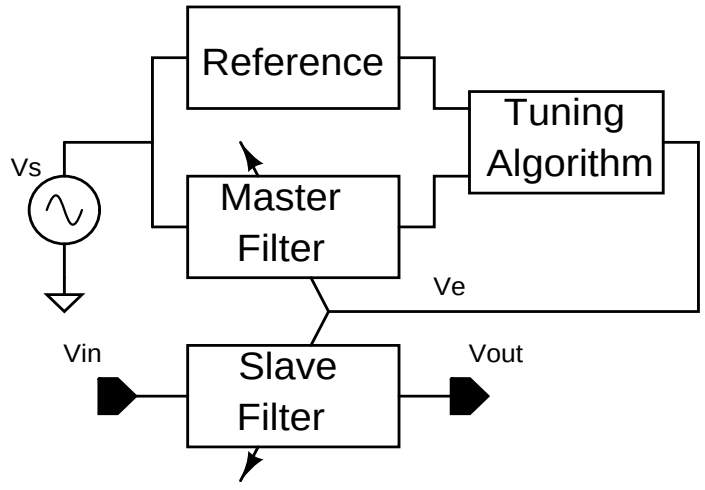

Figure 2.31: Block diagram of the master-slave tuning strategy.

The accuracy of this tuning scheme depends on the matching between the *master* and

the *slave* filter. The *master* should be an exact copy of the *slave* filter and should physically be placed right next to the slave filter for matching. Even with all the layout precautions, there will still be some difference in their performance, because the center of their layouts is located at two different locations.

The purpose of the master filter is only to gather information on the filter parameters of the slave filter; therefore, having a master filter of the same order as the salve filter, does not justify its area and power consumption. In a typical cascade approach implementation, the master filter is a biquad structure and the slave is a higher-order filter. The difference in the order of filter implementation limits the accuracy of the system. Thus, there is a trade-off between accuracy and power consumption. Another way to achieve higher accuracy without dissipating extra power would be to use time multiplexing, which is done in the *direct tuning* strategy.

In the *direct tuning* strategy, the application filter, itself is used to extract filter parameters on a time multiplexed basis. Therefore, it does not require a slave filter. However, with this approach, the filter is not available to the system, while it is being tuned. A pictorial representation of this scheme is shown in Figure 2.32.

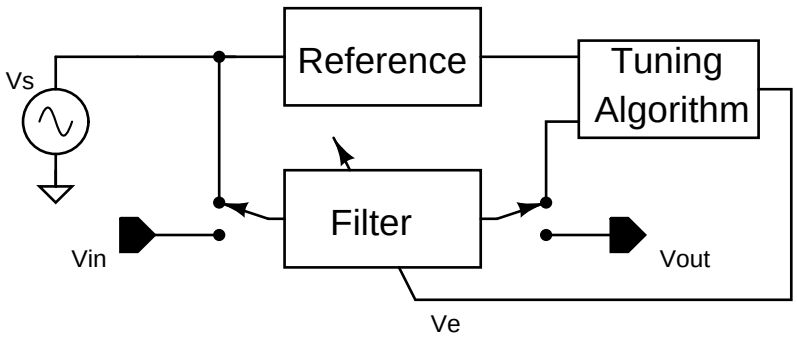

Figure 2.32: Block diagram of the direct tuning strategy

Thus, the direct tuning strategy is good for applications where, the filter is not being used all the time and high accuracy is required.

2.6.2 Q-tuning Algorithm for Bandpass Filter

As discussed in Section 2.4.2, the center frequency and the quality factor of the filter requires an automatic tuning scheme to ensure their performance over manufacturing process and end-use environment variations. Primarily, there are four quality factor tuning algorithms reported in the literature and are listed below. The *quality factor locked loop* is a new tuning method and it has not been implemented before.

- Envelope detection method (ED)
- Magnitude locked loop (MLL)
- Least-mean-square method (LMS)
- Quality-factor locked loop (QLL)

There are also some variants of the envelope detection method and the magnitude locked loop and some other relatively new unimplemented algorithms, which are discussed towards the end of this chapter.

2.6.3 Envelope Detection

In this method, a filter is excited by a step or a pulse waveform. The step (pulse) waveform has one (two) fast transition, which consists of the high-order harmonic components. The filter passes the frequency within its pass-band and attenuates the others. Thus, the output of a bandpass filter to a step waveform is a sinusoidal signal with an exponentially decaying envelope, as shown in Figure 2.33 [12, 53, 54, 55, 56].

Before going into details about the ED method, let us first look into the spectral content of a step function and step response of a bandpass filter. The Fourier transform (reference) of an ideal step function, which goes from '0' to '1' transition in no time, is given by Equation 2.67. This equation suggests the following:

- Step function constitutes an entire frequency spectrum (except DC).
- Signal strength of any frequency is inversely proportional to the frequency.

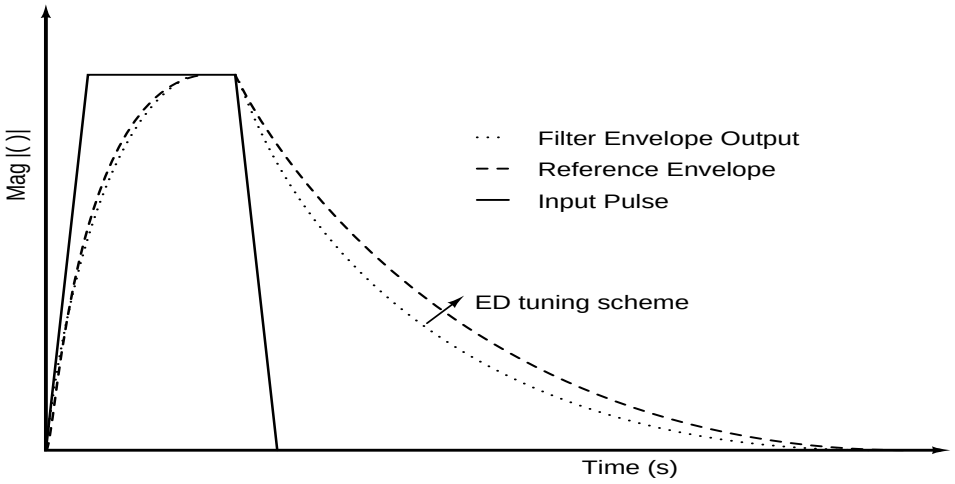

Figure 2.33: Pictorial representation of the envelope detection method.

$$U(j\omega) = \frac{1}{j\omega} \tag{2.67}$$

However, the real step signal takes a finite amount of time t_0 to go from '0' to '1'. The Fourier analysis of a real step signal is given by Equation 2.68, where m is the slope of the ramp, and t_0 is the transit time from '0' to '1'. As expected, the spectral signal strength of the real step is also an inverse function of frequency.

$$U(j\omega) = m\left(\frac{e^{-j\omega t_0} - 1}{\omega^2}\right) + \frac{e^{-}j\omega t_0}{j\omega}[mt_0 - 1] \tag{2.68}$$

For mathematical simplicity, an ideal step waveform, given by Equation 2.67, is used to understand the limitation of this tuning method. The transient response of a bandpass filter to an ideal step input is given by

$$y(t) = \frac{H_0}{\omega_0} \times e^{\frac{\omega_0}{2Q}t} \times \left[e^{\sqrt{1-4Q^2}\ t} + e^{-\sqrt{1-4Q^2}\ t}\right] \tag{2.69}$$

The first term of Equation 2.69 is the amplified input signal. The second term represents the exponential decay of the output with a time constant of $2Q/\omega_0$. The third term can be expressed in the form of Equation 2.70, where $\Omega = \sqrt{1-4Q^2}$. It is a sinusoidal signal component within the pass-band of the filter for $Q > \frac{1}{2}$.

$$e^{j\Omega t} + e^{-j\Omega t} = 2\cos(\Omega t) \tag{2.70}$$

The envelope detection method tunes the time constant of the decaying sinusoidal exponential, which is proportional to Q, to the desired value $2Q_0/\omega_0$. It detects the envelope of the filter output signal using an envelope detection circuit and compares it with an accurate reference envelope using two envelope detectors followed by a comparator. The comparator generates an error signal, which is integrated over time, and the integrated signal is used to tune the quality factor of the filter. A pictorial view of this mechanism is shown in Figure 2.33 and a block diagram is shown in Figure 2.34.

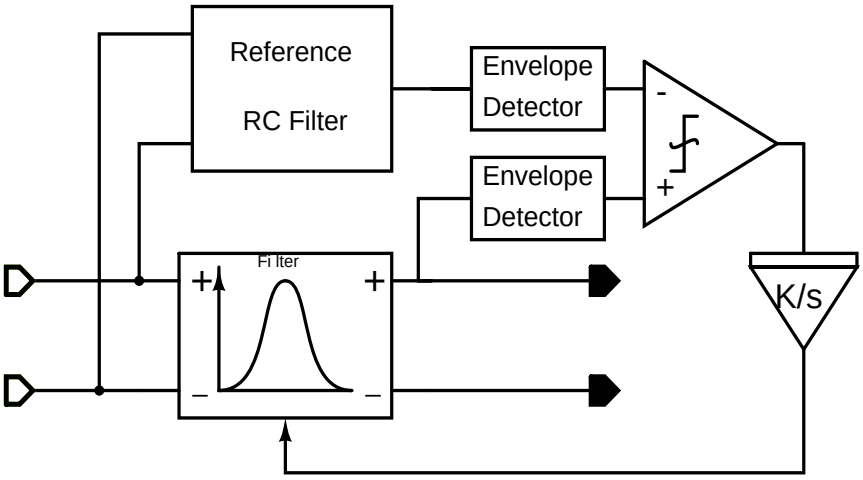

Figure 2.34: Block diagram of the envelope detection method.

An accurate reference envelope can be generated using a first-order resistor-capacitor (RC) switched capacitor (SC) or switched current (SI) circuit. SC and SI are accurate because their time constants are ratios of like terms (capacitor or current), which can be realized accurately in modern CMOS IC technology, even when their absolute value may have a $\pm 3\sigma$ variation of $\pm 20\%$.

2.6.3.1 Limitation of Envelope Detection Method

Some of the problems and limitation of the envelope detection method are listed below.

- The strength of the center frequency signal component in a step waveform.

- It has to tune the filter within four time constants ($2Q/\omega_0 = 1\mu$sec.).
- The offset from the comparator and envelop detector.

2.6.3.2 Possible improvements to Envelope Detection Method

One possible improvement of the envelope detection method would be to use a sinusoidal burst input in place of the step input. This improves the output signal strength from H_0/ω_0 to $H_0 \times A$. The mathematical expression for the sinusoidal burst output is given by Equation 2.71, where A is the applied signal strength.

$$h(t) = H_0.A.\omega_0 \times e^{\frac{\omega_0}{2Q}t} \times \left[e^{\sqrt{1-4Q^2}\ t} + e^{-\sqrt{1-4Q^2}\ t}\right] + H_0 \times A \times Sin(\omega_0 t) \tag{2.71}$$

The duration of the sinusoidal signal should be long enough so that the output of the filter reaches its amplitude $H_0 \times A$. Now, the strength of the output signal is large enough to be detected by the envelope detector. However, even with this amplitude increase the output will decay down to 2% in four time constant and ED has to the filter in this window.

The above mentioned reasons limits the use of this tuning scheme to low-frequency filters, whose center frequency or pole frequency is less than 1 MHz. The close-loop feedback technique of the envelope detection method is also applied to the magnitude locked-loop(MLL) technique.

2.6.4 Magnitude Locked Loop

The magnitude locked-loop (MLL) tuning scheme uses the filter transfer function given by Equation 2.72, which has a mid-band gain ($H_0 \times Q$) proportional to the quality factor of the filter, as shown in Figure 2.35. This scheme requires a reference amplifier, which has an accurate gain of $H_0 \times Q_0$, at the center frequency of the filter. It compares the mid-band gain of the filter with that of the reference amplifier using a peak detector circuits, and generates an error signal. The error signal is integrated over time to tune the quality factor of the filter, as shown in Figure 2.36 [11, 57, 58, 59, 60, 61].

$$H(s) = H_0 \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.72}$$

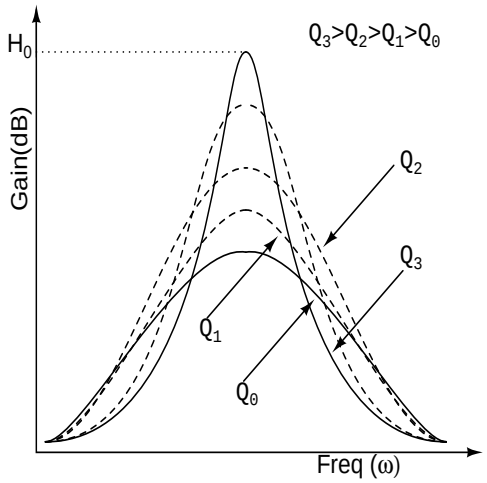

Figure 2.35: Frequency response of the filter with gain proportional to Q.

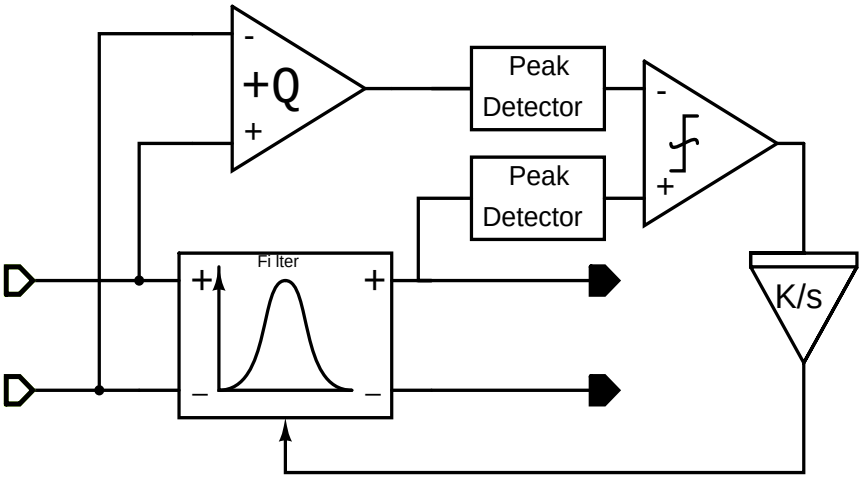

Figure 2.36: Block diagram of the MLL tuning scheme.

2.6.4.1 Limitations of MLL Tuning Technique

Some of the problems and limitation of the MLL method are listed below.

- It requires a peak detector circuit working at the center frequency of the filter.
- The gain-bandwidth product of the reference amplifier should be at least $H_0 \times Q \times \omega_0$, so that it can provide a gain of $H_0 \times Q$ at center frequency ω_0 *e.g.* for a filter with center frequency of 100 MHz, quality factor of 50, and gain of 20 dB, the reference amplifier should have a gain-bandwidth (GBW) product of more than 2 GHz .
- Offsets of the amplifier and the comparator give a Q-error, assuming that V_{os}^{ref}, V_{os}^{fil}, and V_{os}^{pd} are input-referred offsets of the reference amplifier, the filter, and the peak-detector, respectively. Then, the error in the quality factor resulting from offsets is given by

$$\Delta Q = \frac{H_0 \times Q_0 \left(V_{os}^{ref} + V_{os}^{fil} \right) + 2V_{os}^{pd}}{H_0 \times Q_0 \times v_{ref}} \times Q_0 \tag{2.73}$$

  This puts a contradictory requirement on the reference amplifier input stage. The input differential pair of the reference amplifier should be made small to minimize the input capacitance and to achieve high frequency of operation. However, a small input device gives large offset and thus a large Q-error[62].
- The feedback loop tunes the value of $H_0 \times Q$; therefore any error in H_0 will appear in Q.
- The gain and the noise of the filter put a minimum limit on the start-up quality factor. For a high-Q filter, this can cause instability in the filter because of the process variation.

2.6.4.2 Possible Improvements to MLL tuning scheme

The GBW requirement from the reference amplifier can be reduced by having another peak detector circuit before it. The output of the peak detector circuit is a DC voltage. Thus the reference amplifier has to only amplify the DC signal. However, it introduces another

offset parameter into the Q-error equation and the matching between the two peak detector circuits becomes important.

The MLL scheme is the most commonly used technique to tune high-frequency filters. However, the above mentioned limitations of the reference amplifier and peak detector limit the use of this scheme to $10 \sim 20$ MHz applications. There are some improvements to the MLL tuning scheme, such as least-mean-square method, which have been reported to tune a 100 MHz filter [62]. The LMS tuning scheme is discussed in details in the next section.

2.6.5 Least-Mean-Square Method

The least-mean-square method also uses the bandpass filter transfer function given by Equation 2.72. It also extracts the quality factor information of the filter from its gain. The operating principle of this tuning scheme can be understood from the following analysis.

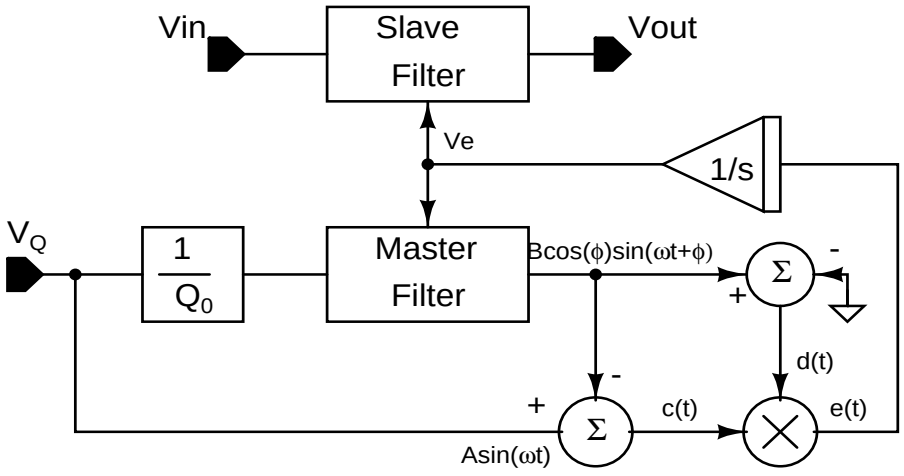

Figure 2.37: Block diagram of the least-mean-square tuning scheme.

The quality factor tuning signal (V_Q) is first attenuated by a value equals to the desired quality factor (Q_0) of the filter. Assuming that the current quality factor of the filter is Q_c, the output signal strength (B) of the filter is $A\frac{Q_c}{Q_0}$. The output of the first summer ($c(t)$), which sums the input signal with the output of the filter, is given by Equation 2.74. The second summer circuit is used as a dummy block to equate the group delay (ϕ_g) through the two paths of the system. The analog mixer is used as a multiplier that gives an error signal along with high-frequency noise given by Equation 2.76. The noise in the error signal *e(t)*

is filtered using an integrator. The integrator accumulates the error signal and generates a tuning voltage, v_e, given by Equation 2.77.

$$c(t) = A\sin(\omega t) - B\sin(\omega t + \phi_g) \tag{2.74}$$

$$d(t) = B\cos(\phi_g)\sin(\omega t + \phi_g) \tag{2.75}$$

$$e(t) = [A\sin(\omega t) - B\sin(\omega t + \phi_g)] \times B\cos(\phi_g)\sin(\omega t + \phi_g) \tag{2.76}$$

Now, if filter is tuned to its correct Q value, then Q_c will be equal to Q_0, which means the error signal, v_e, will be zero. Since, this tuning algorithm looks for a minimum error of the squared output signal, it is known as *least-mean-square* (LMS) tuning algorithm.

$$\begin{aligned} v_e &= AB\cos\left(\frac{\phi_g}{2}\right) - B^2\cos^2(\phi_g) \\ &\approx AB - B^2 = A^2\frac{Q_c}{Q_0}\left(1 - \frac{Q_c}{Q_0}\right) \end{aligned} \tag{2.77}$$

The LMS tuning algorithm requires two summers and an analog mixer operating at the center frequency of the filter, which should not be difficult to design. Thus, this tuning scheme can be used to tune a high-Q high-frequency bandpass filter.

2.6.5.1 Problems associated with LMS tuning scheme

Some of the problems associated with this tuning scheme are listed below.

- The input offset of the attenuator and the summer block causes an error in the final quality factor value. The effect of this error can be derived similar to the MLL tuning scheme [62]. The input offset of the attenuator has a severe effect, as it is amplified by the gain of the filter. This again incurs a similar trade-off in speed or power consumption of the summer and the attenuator block with their offsets.
- This scheme requires several analog blocks such as attenuator, summer, mixer, and integrator. Therefore, the power consumption of this scheme is large.

- Any error (δ) in the attenuator will be amplified by the gain of the filter. The amplified error will appear as the final Q value error ($H_0 \times Q_0 \times \delta$). Thus, the design and layout of the attenuator are critical to the performance of this scheme.

2.6.5.2 Possible Improvements to LMS Tuning Scheme

The offset problem resulting from the summer and multiplier blocks of the LMS tuning scheme is solved by swapping the place of the multiplier and the summer block [62]. However, the offset problem of the attenuator still persists.

2.6.6 Q-Locked Loop

The Q-locked loop (QLL) tuning scheme uses the phase characteristics of the filter to extract the quality factor information and modulates the transconductance of the Q-tuning transconductor to tune the quality factor of the filter. The magnitude and phase characteristics of a filter for any applications are known prior to its implementation. This scheme uses the phase information of the filter to tune the phase shift at the output at a known reference frequency to a known reference value, *e.g.*, a biquad filter gives a phase shift of 45^o at its 3 dB cut-off frequencies with respect to the center frequency. If the phase shift is more than the desired value, it implies that the quality factor of the filter is more than the desired value Q_0 and vice-versa. The above argument can be seen graphically in Figure 2.38 [63, 64, 65, 66].

2.6.6.1 Problems associated with QLL tuning scheme

Some of the problems associated with QLL tuning scheme are listed below.

- Any delay mismatch between ϕ_{fil} and ϕ_{ref} will appear as a tuning error in quality factor. For example, a delay mismatch of $\tau/360$ will generate a phase error of 1^o, which will appear as Q-error. Since, it is a difference between two similar quantities, it can be matched and realized with good agreement in modern IC processes.

- The accuracy of the QLL scheme depends on the deadzone of the PFD. Thus, it requires a very fast and no-deadzone PFD circuit.

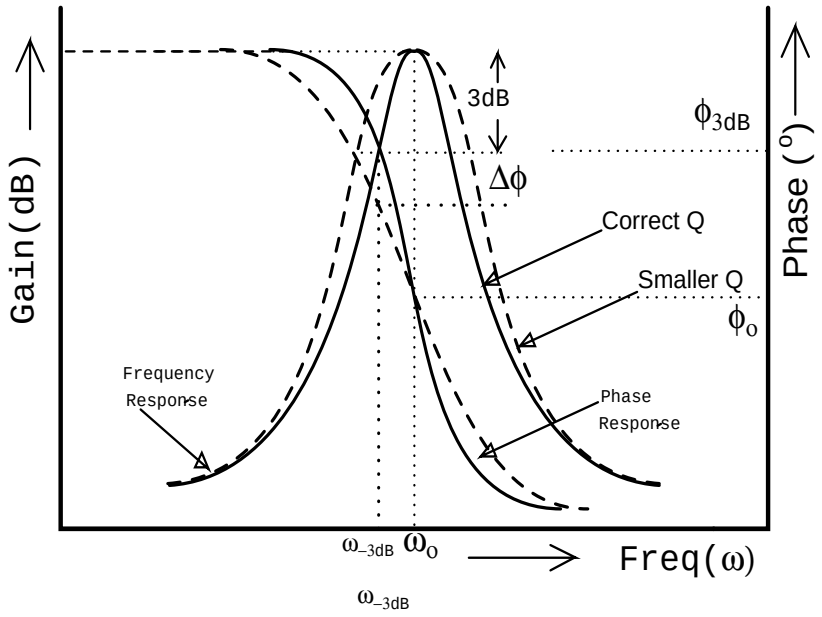

Figure 2.38: A pictorial representation of the QLL tuning algorithm.

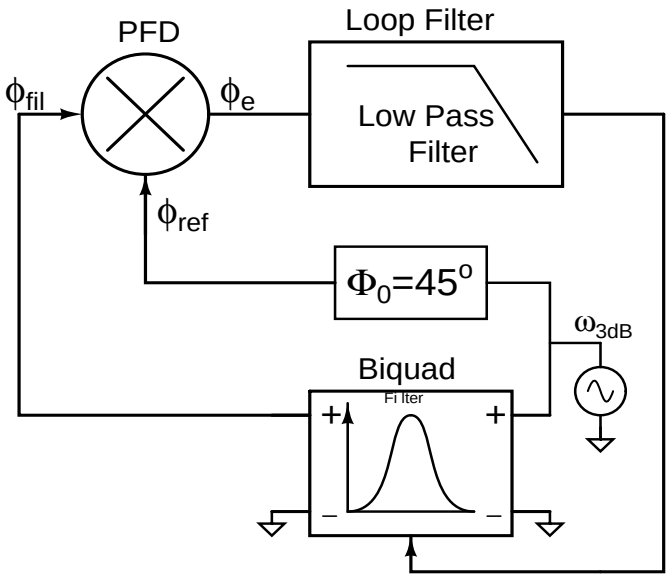

Figure 2.39: Block diagram of the Q-lock-loop tuning scheme.

2.6.7 Other Reported Techniques and their Limitations

A few other tuning techniques, which have been reported in the literature that are capable of tuning small to moderate quality factor value filters at lower frequencies.

- *Cosine peak comparison with the non-zero DC reference*

  This tuning scheme encodes the quality factor information of the filter into the pulse width of a pulse-width modulated (PWM) wave by comparing the *cosine* wave output to a non-zero DC reference. It tunes the quality factor of the filter by comparing the duty cycle of the PWM signal with a reference signal. It is also a variant of the MLL tuning technique. It uses the filter gain ($H_0 \times Q$) property to tune the Q. If the Q of the filter is less, i.e., the gain is small and resulting output *cosine* signal strength will be small as well [67].

- *Programmable capacitor array implementation*

  This is another variant of the MLL tuning scheme. It extracts the filter Q information from the filter mid-band gain and, then tunes the filter by appropriately choosing the correct combination in programmable capacitor array (PCA) [68].

- *Bandpass filter output phase extraction from inherent lowpass filter*

  This tuning algorithm is different from the traditional ED and MLL methods. It uses a filter topology where lowpass and bandpass can be realized in the same circuit. The center frequency of the bandpass filter and the 3 dB roll-off frequency of the lowpass filter are the same. Thus, when the bandpass filter reaches its peak, the lowpass filter reaches the 3 dB roll-off point where the lowpass output gets a 90^o phase change. This tuning scheme uses lowpass filter phase slope information to tune the bandpass filter Q [69, 70, 71].

- *Derivatives of MLL and ED*

  There are few schemes that use a fast analog-to-digital converter to sample the filter response and then process the digital words using a DSP processor. The DSP processor generates an an error control signal based on tuning algorithm to tune the quality

factor. These schemes are expensive in terms of area and power dissipation; therefore, they have very little practical use. Another tuning scheme uses sigma-delta ($\Sigma\Delta$) circuit inside the loop to tune the quality factor, so its speed and power consumption are defined by the sample-and-hold circuit [55, 72, 73, 74, 75, 76, 77, 78, 79].

2.7 Summary

The monolithic solution of a high-Q high-frequency bandpass filter tends to have poor noise performance in comparison to SAW or BAW filters. However, an on-chip filter provides gain that can still improve the overall system performance with an appropriate architectural redesign. The on-chip filters are implemented using the cascode approach and have large component sensitivity. Therefore, they are accompanied by an auxiliary tuning circuit, which ensures their performance over all environmental variations. For a low-voltage application, the $G_m - C$ filters are implemented using folding and lateral degenerated structures.

The resistive degenerated transconductor is more linear because the transconductance is defined by inherently linear passive components. Its linearity is further improved by employing the feedback loop around the degenerating resistor; however, the linearity comes at the expense of poor bandwidth and inferior noise performance.

The finite bandwidth of the individual transconductors causes the *Q enhancement effect* in the bandpass filter, which may eventually lead to instability. The MLL and LMS tuning schemes look promising for tuning a high-Q, high-frequency bandpass filters. However the offsets in the individual components makes them susceptible to large error for a high-Q filters.

The quality factor locked loop tuning is promising candidate but it has not been implemented before and its mathematics needs to be driven and behaviour needs to be understood. Hence, the QLL tuning scheme needs to be further developed to be useful for this work.

CHAPTER III

AUTO-Q TUNED HIGH-Q BANDPASS FILTER

High-frequency continuous time filters are used as front-ends for high-speed analog to digital converters (ADC), reconstruction filters in DACs, front-ends of disk drive applications, intermediate frequency stages in superheterodyne transceivers, and front-ends of FM and HD audio receivers. At present, many of these applications use passive, off-chip SAW or BAW filters (DR ∼70 dB). A SAW filter is 20 dB more linear than an on-chip continuous time filters of the same frequency (DR = 40∼50 dB). However, an on-chip filter generates gain, whereas a SAW filter introduces 3∼20 dB of loss to the signal path Table 1.2. The loss from the SAW filter also increases with bandwidth, and makes it unsuitable for 3G applications. A superheterodyne receiver can achieve better signal-to-noise ratio with a redesign using an on-chip continuous-time filter in large bandwidth applications. However, an on-chip continuous-time filters are vulnerable to oscillation because of the excess phase shift from the transconductor. Therefore, an on-chip filter is always built with an automatic tuning scheme. A high-frequency bandpass filters also filters the out of band noise for high-performance, high-speed ADC.

3.1 Outline of the Proposed Research

The goal of this research is to address the poor dynamic range and the quality factor instability problem of an on-chip continuous-times filter, and take a step further toward a single-chip solution. To quantify the contribution and the improvements in performance, a 100 MHz biquad bandpass filter has been designed with DR > 60 dB and gain ∼20 dB, using an ultra-linear transconductor circuit in the BiCMOS process. To achieve this DR from filter, the linearity of the transconductor should be more than 80 dB and the 3 dB cut-off frequency close to 1.5 GHz.

The proposed transconductor circuit employ a local negative feedback loop to achieve high linearity while maintaining high cut-off frequency. It has achieved a linearity of 80

dB by optimizing the design to reduce systematic and random process mismatch. The biquad bandpass filter is designed using a noise-optimized structure, where large gain and quality factor are achieved by defining them as a ratio of transconductance to a difference in transconductances. This has enabled the filter to achieve a quality factor of 50 without using a large conductance ratio ($\sim$50) in design. The design of the filter is optimized for overall dynamic range performance where noise is limited by the first stage and the maximum signal handling capacity limitation comes from the output stage.

The instability in quality factor (Q) of a filter is solved by employing the QLL tuning loop. This new tuning scheme overcomes the limitations of the ED, MLL, and LMS methods and reliably tunes the high-Q, high-frequency continuous-time filter. It extracts the Q information from the phase response of the filter, which makes it immune to the offset and gain-mismatch problem of monolithic solutions. It tunes the quality factor of the filter by modulating its phase characteristics inside a phase-locked-loop system. The loop stability analysis is performed using an approximated phase response of a filter, as the Laplace transform of the phase of the filter is a non-integrable function. Therefore, it is approximated to an exponential function using series expansion within the band of interest.

The loop stability condition loop performance parameters ($\omega_n,\ \zeta$) are derived and its response is analyzed for expected input signal. The proposed Q-tuning scheme is a unique case of a generic PLL system designed only to tune the quality factor of the filter. Therefore, its input is confined to a limited sub-space. The circuit performance metrics such as power consumption, stability, and steady-state error are optimized for the problems at hand. The input to the QLL tuning scheme is always a step change in phase; it represents a finite error in the quality factor of the filter. Hence, a stable second QLL system is necessary and sufficient to reach zero steady-state error.

The finite mid-band gain and left half plane poles of the phase response of the filter makes the proposed second-order Q-tuning scheme unconditionally stable under all extreme corners. The loop bandwidth of the QLL tuning scheme controls the settling time and deadzone of the DPFD determines the hysteresis in the final Q-value. The loop bandwidth is reduced by reducing the loop gain or cutting the integrator gain. The gain from the

integrator is reduced by decimating its clock frequency. A large loop gain gives fast settling time, but it increases the hysteresis in Q. If a fast loop transient response is required, then a third-order loop can be employed.

The delay mismatch between the reference and the filter output signal determines the static Q-error. Therefore, a similar delay network is used for both signal paths of the loop to minimize mismatch and static Q-error [80, 64].

Upon completion, this research work will provide a wide dynamic range, high-Q, high-frequency bandpass filter circuit with a reliable automatic Q-tuning scheme.

3.2 Excess Phase Shift Effect

A high-Q, high-frequency filter suffers from an *excess phase shift effect,* as described in Section 2.3.2. This effect can also be explained using a delay model of an integrator and some simple mathematics using a series expansion and approximations. A bandpass filter is described by a transfer function given by Equation 3.1, where ω_0 is the center frequency, and Q is the quality factor, and H_0 is the gain of the filter.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = H_0 \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} = \frac{\frac{H_0\omega_0}{Qs}}{1 + \frac{\omega_0}{Q}\frac{1}{s} + \frac{\omega_0^2}{s^2}} \tag{3.1}$$

The Laplace transform [1] of a normalized ideal integrator is $1/s$. A block-level implementation of a second-order bandpass filter using ideal integrators is shown in Figure 3.1. An ideal integrator has infinite gain at DC and has its pole at zero frequency. Hence, it does not introduce delay to the signal. However, a real integrator has finite gain at DC and a non-zero dominant pole, which provides non-zero delay to the integrated signal. The effect of the integrator non-zero dominant pole and its higher-order parasitic poles can be modelled using a delay model, where together they introduce a delay 'τ' to the signal. The Laplace transform of this integrator model is given by Equation 3.2.

[1] Appendix A.1

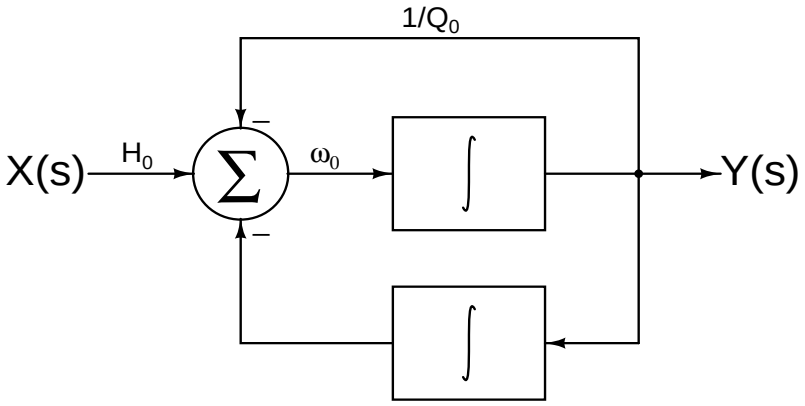

Figure 3.1: Integrator equivalent block diagram of bandpass filter.

$$U(s) = \frac{e^{-s\tau_p}}{s} \approx \frac{G_m}{sC\left(1 + \frac{s}{\omega_p}\right)} \tag{3.2}$$

In other words, the above model approximates the integrator with a single high-order non-dominant pole/zero response ($e^{-s\tau}$ is approximated to $\approx 1 - s\tau$ using the Taylor series expansion[2]. This approximation is valid only when the $\omega_0 \ll 1/\tau_p = \omega_p$; which is true in case of parasitic poles of the integrator.

Upon substituting the real integrator transfer function into the bandpass filter shown in Figure 3.1, the effective transfer function of the bandpass filter is given in Equation 3.4, where the quality factor of the filter is given by Equation 3.5.

$$H_{eff}(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{H\omega_0 e^{-s\tau_p}}{s}}{1 + \frac{\omega_0}{Q_0}\frac{e^{-s\tau_p}}{s} + \frac{\omega_0^2 e^{-2s\tau_p}}{s^2}} \tag{3.3}$$

$$\approx \frac{\frac{H_0\omega_0}{Q_0 s} - \frac{H_0\omega_0\tau_p}{Q_0}}{\left(1 - \frac{\omega_0\tau_p}{Q} + \omega_0^2\tau_p^2\right) + \frac{\omega_0}{s}\left(\frac{1-2\omega_0\tau_p Q_0}{Q_0}\right) + \frac{\omega_0^2}{s^2}} \tag{3.4}$$

$$Q_{eff} = \frac{Q_0}{1 - 2\omega_0 Q_0 \tau_p} \tag{3.5}$$

The denominator of the effective quality factor (Q_{eff}) of the filter is always less than one. Thus, the effective quality factor of the filter is always greater than the designed value

[2]Appendix A.2

Q_0. This phenomenon of increase in quality factor of the bandpass filter is also known as the *Q-enhancement effect* [37]. The Q-enhancement effect is minimized by reducing the delay ($\omega_p = \frac{1}{\tau_p} >> 2Q_0\omega_0$) through the integrator, in other words by increasing the DC-gain and minimizing the parasitic capacitance. The quality factor of an IF filter is already large, therefore any further unaccounted for increase in Q can bring instability to the system. The Q-enhancement effect becomes critical for Gm-C filters because of the additional variation from temperature and manufacturing processes.

3.3 Continuous-time Bandpass Filter

As discussed in Section 2.2, the biquad bandpass filters are defined by Equation 3.6 and Equation 3.7. The filters defined by these two transfer functions differs in their mid-band gain at the center frequency (ω_0) of the filter. In this research work, a bandpass filter described by the transfer functions of Equation 3.6 is implemented using a fully differential $G_m - C$ biquad structure, where the inductor is emulated using a Gyrator structure as described in Section 2.3.2.2. Filter parameters such as gain, center frequency, and quality factor are given in Equation 3.8. The center frequency and the quality factor of the biquad are chosen to be 100 MHz and 16∼48 for this research work, as per the conclusion drawn in Table 1.4 of Chapter 1.

$$H(s) = H_0' \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} = \frac{\frac{G_{mg}}{C}s}{s^2 + \frac{G_{mq}}{C}s + (\frac{G_{mf}}{C})^2} \tag{3.6}$$

$$H(s) = H_0 \frac{\frac{\omega_0}{Q}s}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} = \frac{\frac{G_{mq}}{C}s}{s^2 + \frac{G_{mq}}{C}s + (\frac{G_{mf}}{C})^2} \tag{3.7}$$

$$\text{where} \quad H_0' = \frac{G_{mg}}{G_{mf}};\ H_0 = \frac{G_{mg}}{G_{mq}};\ \omega_0 = \frac{G_{mf}}{C};\ Q = \frac{G_{mf}}{G_{mq}} \tag{3.8}$$

The gain and the quality factor of the filter are a ratio of two transconductances. A large gain and quality factor requires a large transconductances ratio ($16 \sim 48$). The transconductance of a transconductor is mostly defined by the current in the active components or by the size of the passive resistors. A large transconductance ratios requires either large area or large current ratio, which is not a low-power solution. Large resistors gives large thermal noise and large current generates large shot noise [81].

In this work, a noise-optimized biquad structure, given in Equation 3.9, is used, where a large quality factor and gain are achieved by taking ratios of transconductance to the difference in transconductances, as given in Equation 3.10. This keeps the value of individual transconductances on the same order of magnitude and still allows a large ratio. This method gives an optimal noise and area for a given high-Q filter. The transconductance of the transconductors is defined by the passive resistor but its noise is dominated by the active components.

$$H(s) = \frac{\frac{G_{mg}}{C}s}{s^2 + \frac{G_{mh}-G_{mq}}{C}s + (\frac{G_{mf}}{C})^2} \tag{3.9}$$

$$\text{where} \quad H_0 = \frac{G_{mg}}{G_{mh} - G_{mq}};\ \omega_0 = \frac{G_{mf}}{C};\ Q = \frac{G_{mf}}{G_{mh} - G_{mq}} \tag{3.10}$$

The center frequency of the filter defines the value of the transconductor G_{mf}. The quality factor of the filter is tuned by changing the value of G_{mq} inside an automatic Q-tuning scheme, where the transconductance G_{mf} and G_{mh} are held constant. The gain of the filter increases with the quality factor of the filter, which is not desirable. The gain is held constant during the tuning process by tuning the value of G_{mg} in opposite direction to G_{mq} while holding the G_{mf} and G_{mh} constant.

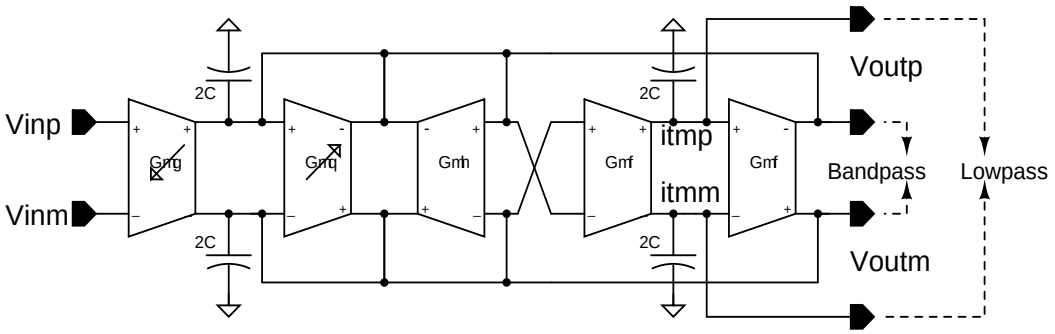

Figure 3.2: The block level representation of the biquad filter.

The block-level schematic diagram of the above transfer function is shown in Figure 3.15. It is a differential architecture, where the value of capacitors is chosen to be equal for area optimization and layout simplicity. The linearity of the G_{mh}, G_{mq}, andG_{mf} is kept higher, as

they have an amplified output signal as their input. Thus, the maximum handling capacity is determined by these transconductors.

There is an overall gain of 20 dB from the filter; therefore the noise from g_{mg} becomes critical, as the input-referred noise from $G_{mq}, G_{mf}, \text{and} G_{mh}$ is divided by the gain from the system. Also, from Section 2.4.1.1, the noise in a filter is inversely proportional to the value of capacitor. Thus, for a given center frequency (ω_0), G_{mf} should be kept large to have the large dynamic range. Now, a large G_{mf} means either smaller IIP3 or large power consumption. Hence, the value of G_{mf} is designed from P_{-1dB} and the supply current specification. The integrating capacitor 'C' is chosen based on the center frequency of the filter. The distortion introduced by G_{mh} and G_{mq} is minimized by designing them 12 dB more linear than G_{mf}. Thus, the transconductor G_{mg} determines the input-referred noise and the transconductor G_{mf} determines the linearity parameter such as P_{-1dB} and IIP3.

3.4 High-Frequency Linear Transconductor

A transconductor generates an output current proportional to an applied input voltage. A voltage input stage requires a large input impedance and the current output stage requires a large output impedance. From the discussion on integrators, inductors and bandpass filters in Section 2.3.2, it is evident that the transconductors should have a large output resistance to minimize the phase lead. They should also have small parasitic capacitance to push out the parasitic poles and zeroes (at least fives times the center frequency of the filter) and minimize the excess phase shift effect [6, 37]. For a high-Q, high-frequency bandpass filter, excess phase shift is of greater concern because it can push the filter into instability. Noise, maximum signal strength, the power consumption are also areas of concern in designing a bandpass filter [6, 33, 82, 83]. Thus, a desired transconductor should have the following:

- Large output impedance
- Parasitic poles and zeroes pushed out to high frequency (∼1.5 GHz)
- Large dynamic range or high linearity
- Low voltage capability and low power consumption

A differential transconductor circuit is commonly used to eliminate the even-order nonlinearity and to gain common mode noise immunity.

The proposed transconductor circuit is an improved version of the folded Gilbert structure with a local feedback loop around the input stage. The feedback loop consists of a high-speed common base stage, and an emitter follower stage. The loop bandwidth is determined by the common emitter amplifier stage. A schematic diagram of the proposed circuit is shown in Figure 3.3.

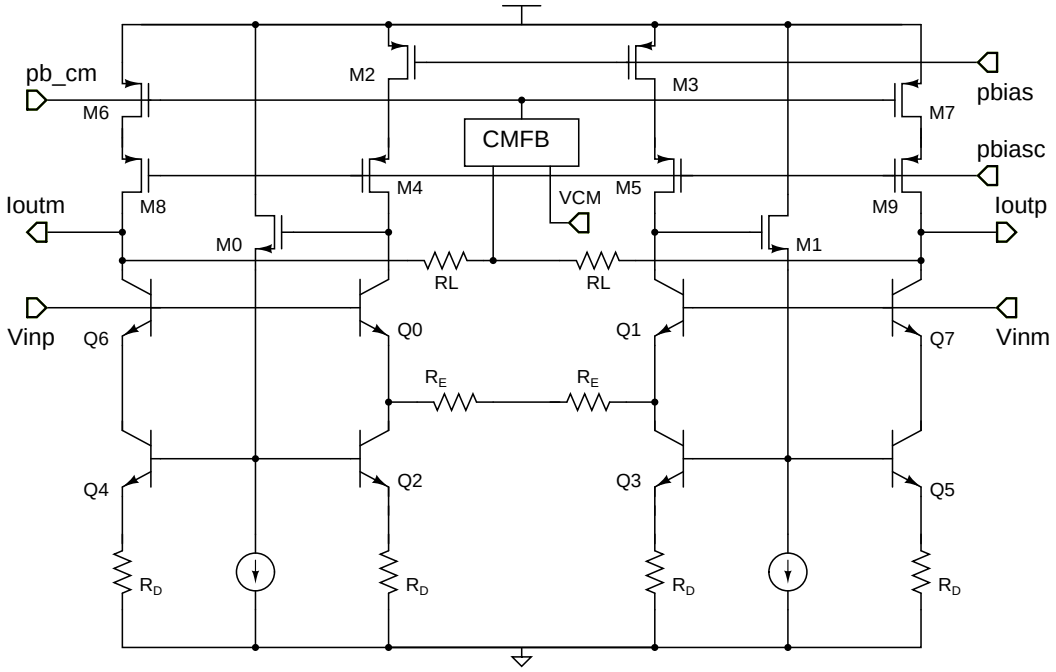

Figure 3.3: An enhanced Gilbert cell transconductor circuit.

The operating principle of the proposed circuit is as follows: The input differential amplifier transistors Q0 and Q1 produce the input voltage across the resistor ($2R_E$), which generates a signal current (i_{sig}). The common base amplifier Q0, level shifter transistor M0, and a common emitter amplifier Q2 form the negative feedback loop around the input stage. An error signal current (i_e) flows into the emitter of the input differential pair transistors, Q0 and Q1. The common base amplifier formed by the input differential pair amplifies the error signal (i_e), at the collector, and converts the error current signal into a voltage. Transistors M0 and M1 are level shifters. The amplified error voltage signal appears and

modulates the base of transistors Q2, and Q3, such that the signal current (i_{sig}) could be absorbed at the collectors. The transistor pairs Q2-Q4 and Q3-Q5 form current mirrors, as their bases are tied together and the emitters are held at the same potential. Thus, the differential signal current, (i_{sig}), is reproduced at the collector of transistors Q4 and Q5, respectively. The linearity of the proposed circuit depends on the matching between the transistor pairs Q2-Q4 and Q3-Q5. Transistors Q6 and Q7 are driven by the same input signal as differential pair Q0 and Q1. The purpose of transistors Q6 and Q7 is to cancel the *early voltage effect* on the mirror transistors Q4 and Q5 by modulating the collector of these transistors with the same voltage as the input mirror transistors Q2 and Q3. Transistors Q6 and Q7 also act as common base amplifiers, which reproduce the input current from their emitters to their collectors. Hence, the differential output current of the transconductor is collected at the collectors of transistors Q6 and Q7. The MOS transistor pairs M2-M4, M3-M5, M6-M8, and M7-M9 are current sources. The gates of transistors M6 and M7 are driven by the common mode feedback circuit to regulate the DC output common mode voltage at the output of the transconductor.

3.4.1 Small-Signal Model

The above transconductor circuit is broken into two symmetrical halves to analyze the small-signal circuit model. A half-circuit is shown in Figure 3.4 and its small-signal model is given in Figure 3.5. The transconductance of the above transconductor circuit is derived and given in Equation 3.11, where g_{mx} is the transconductance of the transistor Q_x, $g_{\pi x}$ is the π model parameter of the transistor Q_x, g_{inx} is the input impedance of the transistor Q_x, g_{out} is the conductance at the internal high impedance node, and g_D is inverse of resistance R_D . The impedance (R_{out}) at the internal high-impedance node is the output resistance(r_o) of transistor Q0-Q1 in parallel with the output impedance of the current source (M2-M4), which is ($g_{m_{M4}} r_{ds_{M4}} r_{ds_{M2}}$). Since the output impedance of the current source is much higher than the output resistance of the transistor Q0 and Q1, the impudence R_{out} can be approximated to r_o, as given in Equation 3.12. The source follower amplifier M0 and M1 act only as a DC level shifter. Therefore, they do not affect the AC performance and are

neglected in this small signal analysis for simplicity. A small-signal analysis that includes M0 and M1 is given in Appendix B.

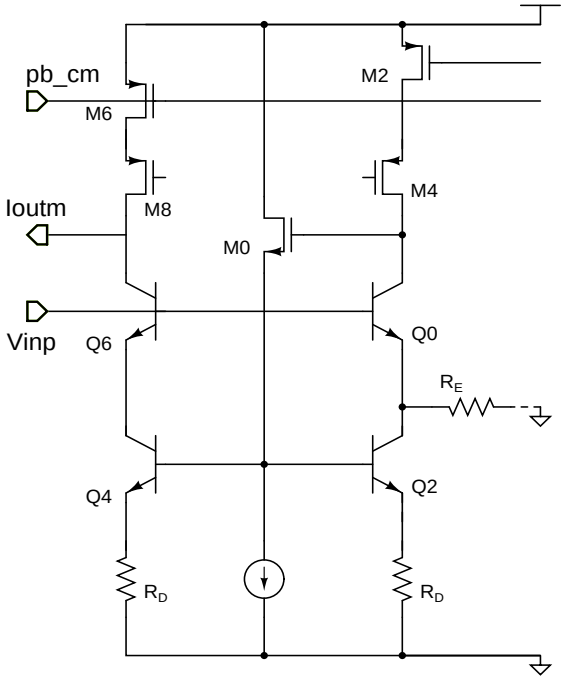

Figure 3.4: One half of the transconductor circuit.

$$G_m = \frac{g_{m6}}{g_{m6}+g_{\pi 6}} \times \frac{g_{m4}g_D}{g_D+g_{\pi 4}+g_{m4}} \times$$
$$\times \frac{g_E g_{m0}}{(g_{out}+g_{in2}+g_{in4})(g_E+g_{\pi 0}+g_{m0})+g_{in2}g_{m2}r_{\pi 2}g_{m0}}; \quad (3.11)$$

where $g_{in2} = \frac{g_D g_{\pi 2}}{g_D+g_{\pi 2}+g_{m2}}$

$$g_{in4} = \frac{g_D g_{\pi 4}}{g_D+g_{\pi 4}+g_{m4}}$$

$$R_{out} = r_o||(g_{m_{M4}} r_{ds_{M4}} r_{ds_{M2}}) \approx r_o \quad (3.12)$$

The above transconductance equation is simplified and approximated by Equation 3.13. The value of the transconductance of the above circuit can be approximated to $1/R_E$, as long as the inequality $g_{m0}R_E A_v \gg 1$ holds true, where A_v is the feedback loop gain and r_{out} is the AC-impedance at the internal high impedance node. The term A_v in this inequality, comes from the local feedback loop, which improves the linearity by $20\log A_v$ dB. The

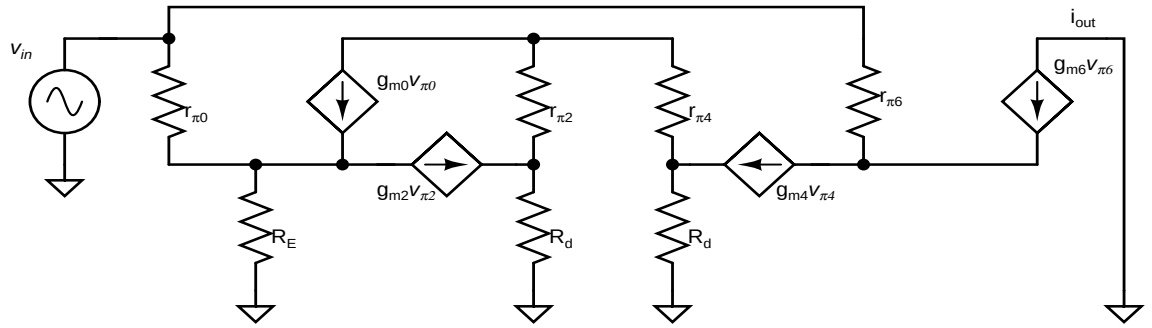

Figure 3.5: The small signal model of one half of the transconductor circuit.

magnitude of loop gain is given by Equation 3.17.

The output resistance of an HBT transistor is given by V_A/I_{CC}, where V_A is the early voltage of the device (Q0-Q8) and I_{CC} is the collector current of the particular device. The V_A and I_{CC} are 100 V and 0.8 mA in this design, which gives an output resistance of 125 Kohms. In this 0.25 μm BiCMOS process, the β of the device is 150, which gives an approximates input impedance r_{in} of 23 Kohms for 0.8 mA of bias current and 120 Ω of degeneration. Thus, the AC impedance (r_{out}) of the loop can be approximated to $r_{in}/2$. Hence, the theoretical improvement in linearity from the local feedback loop is 20 $\times$ $\log\left(\frac{\beta+1}{2}\right) = 37.5$ dB at direct current (DC), as given in Equation 3.17.

$$G_m = \frac{\beta_6}{\beta_6+1} \times \frac{g_E g_{m0} \frac{\beta_4}{r_{in4}} R_{out}}{g_E + g_{\pi 0} + g_{m0} + g_{m0}\frac{\beta_2}{r_{in2}} r_{out}}$$

$$\approx \frac{g_{m0} \times \frac{r_{out}}{R_D}}{1 + g_{m0} R_E \frac{r_{out}}{R_D}} = \frac{g_{m0} A_v}{1 + g_{m0} R_E A_v}; \tag{3.13}$$

$$\approx \frac{1}{R_E}; \quad \text{for} \quad g_{m0} R_E A_v >> 1 \tag{3.14}$$

$$\text{where} \quad r_{out} = \frac{1}{g_0 + g_{in2} + g_{in4}} \approx \frac{2}{g_{in}} \tag{3.15}$$

$$r_{in_x} = r_{\pi_x} + (\beta_x + 1) R_D \tag{3.16}$$

$$\frac{\beta}{r_{in}} = \frac{\beta}{r_\pi + (\beta+1) R_D} \approx \frac{\beta}{(\beta+1) R_D} \approx \frac{1}{R_D}$$

$$A_v = \frac{r_{out}}{R_D} = \frac{\beta+1}{2} \tag{3.17}$$

The emitter degeneration resistors R_D of transistors Q2-Q5 reduce the loop gain; however, their presence is necessary to counter the processing mismatch effect on mirror devices Q2-Q4 and Q3-Q5. The process mismatch analysis of the above transconductor is done later in this chapter.

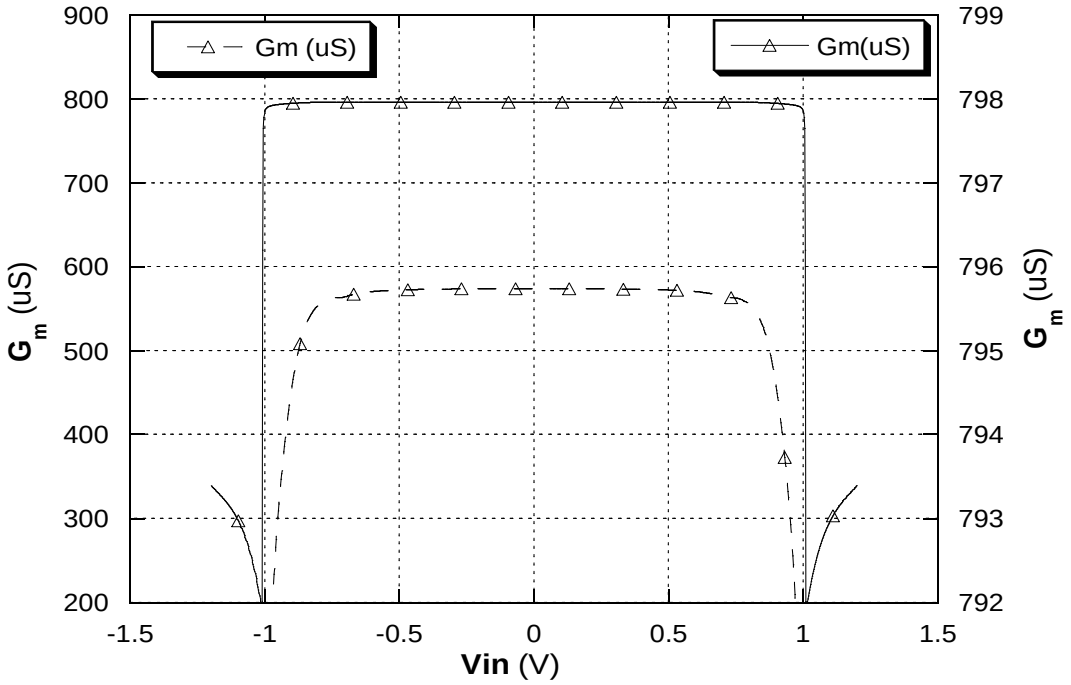

Figure 3.6: Value of transconductor verses input signal.

The simulation results of the transconductance with respect to input signal strength, and the frequency response are shown in Figure 3.6 and Figure 3.7, respectively. The simulated linearity of the above transconductance is 90.3 dB for an 800 mV peak peak signal and the -3 dB cut-off frequency is 1.7 GHz.

3.4.2 Noise

Noise in a high-frequency bandpass filter is dominated by the flat band thermal noise and the shot noise of the active devices. The flicker noise of the transistors is rolled off or blocked by the filter frequency response. A small-signal model of the transconductor is shown in Figure 3.8. Now upon solving the KCL and KVL nodal equations and using the super-position theorem for output noise current, a simplified total output noise current of the transconductor is given by Equation 3.18, where i_{nx} is the shot noise of device Qx. The

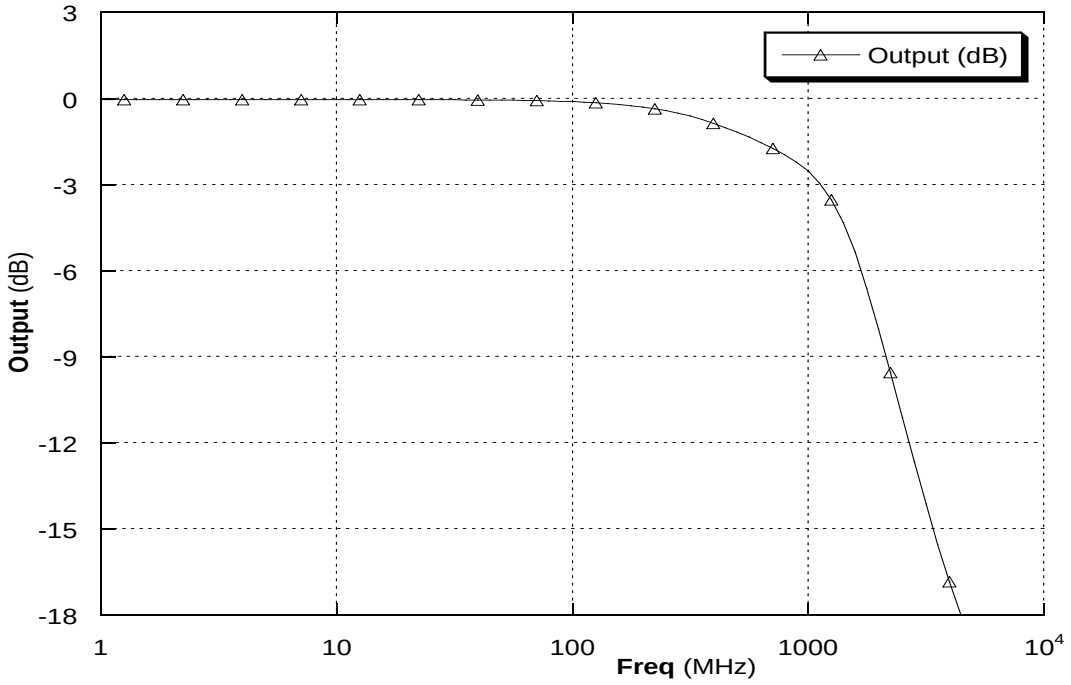

Figure 3.7: Unity gain frequency response of the transconductor.

detailed derivation of this results is shown in Appendix B.

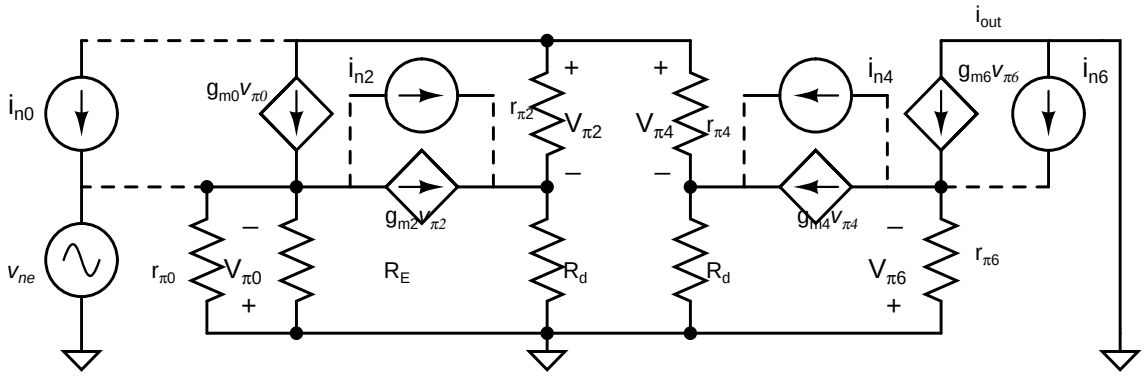

Figure 3.8: Noise equivalent small-signal model of the transconductor.

$$\begin{aligned}
\overline{i_{n_{out}}}^2 &= 2\left[\frac{4KT}{R_E}\left(1+\frac{r_b}{R_E}\right)+\frac{\overline{i_{n0}}^2}{{g_{m0}}^2 R_E^2}+\overline{i_{n2}}^2+\frac{\overline{i_{n6}}^2}{\beta_6^2}+\left(\frac{\beta_6}{\beta_6+1}\right)^2\overline{i_{n4}}^2\right] \\
&\approx 2\left[\frac{4KT}{R_E}\left(1+\frac{r_b}{R_E}\right)+\overline{i_{n2}}^2+\overline{i_{n4}}^2\right] \\
&\approx \overline{i_{n2}}^2+\overline{i_{n4}}^2+\overline{i_{n3}}^2+\overline{i_{n5}}^2 = 8qI_C
\end{aligned} \tag{3.18}$$

As can be seen from the above equation, the major noise contributors of the transconductor shown in Figure 3.3 are RE and transistors Q2-Q5. Since the noise contributed by active devices is larger than that of the degeneration resistor R_E, its noise contribution along with Q0, Q1, Q6, and Q7 is neglected, as it has little contribution. In this design, all transistors Q0-Q8 carry the same amount of current (IC = 800 μA); therefore, the total output current noise power can be approximated to $8qI_C$, as given in Equation 3.18.

3.4.3 ICMR

The input common mode range of this transconductor circuit is from $V_{BE} + V_{CE}^{sat}$ to $VDD - V_{BE} + V_{ce}^{sat} + 2V_{ds}^{sat}$, which approximates to 1.2 V and 3 V, respectively, as shown in Figure 3.9. Thus, the above transconductor can take a differential input of $\pm$1.8 V in a 3.3 V supply. The minimum supply requirement for this circuit to be functional is close to 1.2 V, but at this point the circuit does not have any input common mode range.

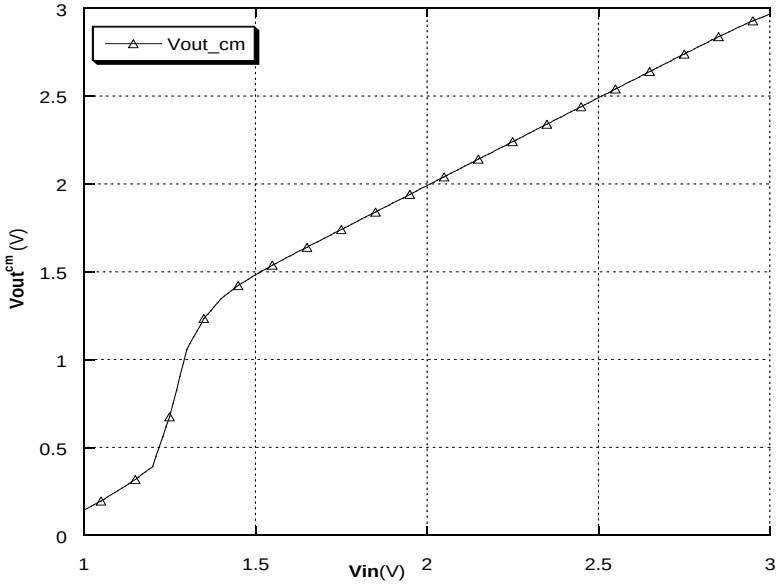

Figure 3.9: Input common mode range of the transconductor.

3.4.4 Common Mode Feedback

An inherent advantage of differential signaling is its immunity to the common mode perturbation; however, it requires a common mode feedback (CMFB) circuit to stabilize the common mode voltage at the output. A CMFB circuit has a large gain at DC to minimize

any common mode drift along the signal path and its dominant pole is higher than the pole frequencies of the system so that it can suppress the common mode signal from the band of interest. For example, in this case, it is the center frequency of the filter. The schematic diagram of the CMFB circuit used in this research is shown in Figure 3.10. It is a simple degenerated differential amplifier, as the expected signal swing at the inputs is small and it gives the largest bandwidth for a given current. The vertical emitter degeneration also helps minimize any process mismatch effect on the differential pair of the CMFB amplifier.

The CMFB circuit is a Miller-compensated, single-stage amplifier, where input voltage is converted into current using the differential input transconductance stage; the current is mirrored at the output using MOS current mirrors (M0-M6) and is finally amplified at the high-impedance output. The dominant pole of this amplifier comes from the Miller multiplication of the capacitor '*C0*' at node 'pb_cm' and is given by Equation 3.19. The Miller multiplication factor is the gain from the output leg of the current mirror (M5-M6) and is given by Equation 3.20. The overall gain of the CMFB amplifier is given by Equation 3.21, where g_{mc} is the transconductance of transistors Q0-Q4, R_{cm} is the degeneration resistor of the differential pairs Q0-Q4, $g_{m_{Mx}}$ is the transconductance of the MOS transistor Mx, and r_{dsx} is the output resistance of the MOS transistor Mx. C_0 is the Miller-compensation capacitor.

$$\omega_{pCM} = \frac{g_{m1}}{g_{m6} r_{ds6} r_{ds8} g_{m8} C_0} \tag{3.19}$$

$$A_M = g_{m6} r_{ds6} r_{ds8} g_{m8} \tag{3.20}$$

$$A_{vCM} = \frac{g_{mc}}{1 + g_{mc} R_{cm}} \times \frac{g_{m_{M6}}}{g_{m1}} \times g_{m6} r_{ds6} r_{ds8} \tag{3.21}$$

Inputs to the CMFB circuit are taken from the mid-point of a resistive divider connected across the output of the respective transconductor, as shown in Figure 3.3. This diminishes any differential swing from being fed into the CMFB circuit and minimizes any capacitive coupling through the parasitic capacitance from the input to the output of the CMFB amplifier. Only a common mode signal appears at the gate of the input differential pair and it is small in amplitude. This eases the design, linearity, and power requirements from

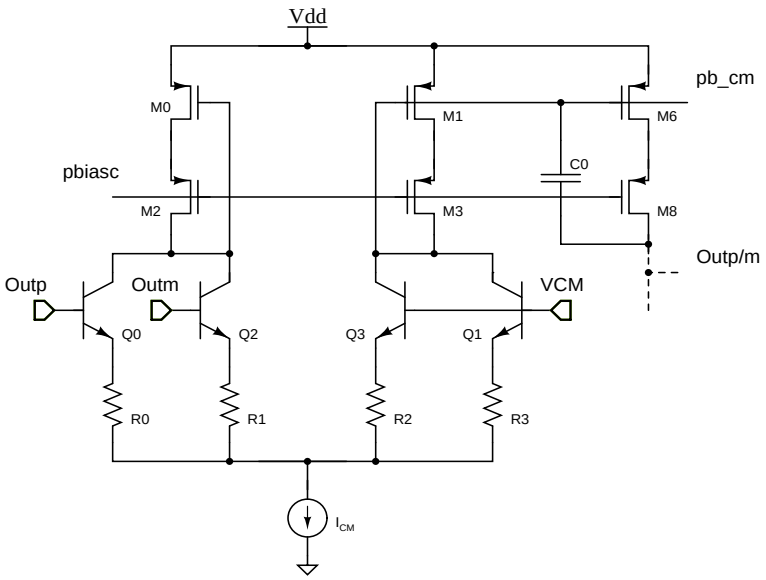

Figure 3.10: A schematic diagram of the common mode feedback circuit.

the CMFB amplifier. A CMFB amplifier is always connected in a unity gain feedback configuration to the differential circuit. Thus, the unity gain bandwidth product (GBW) of the CMFB amplifier should be kept larger than the center frequency of the filter. In simulation, the GBW of the CMFB amplifier is $\approx 180MHz$, as shown in Figure 3.11. Some margin is kept into the design to account for the parasitic capacitance and the manufacturing process variations.

Any mismatch between the dividing resistor will generate a common mode output signal from the differential signal and HD2, which could limit the THD of the system. Therefore, the dividing resistor is laid out in 4x4 matrix common centroid structure, to achieve a matching of in excess 10 bit (62 dB) of accuracy.

3.4.5 Common Mode Rejection Ratio

The common mode gain of the proposed transconductor circuit is found by applying a common input signal to both the inputs of the transconductor. A simplified small-signal equivalent circuit diagram of a transconductor with a common input signal is shown in Figure 3.12. From the symmetry of the small circuit model, one half of the g_{m0} $v_{\pi 0}$ current

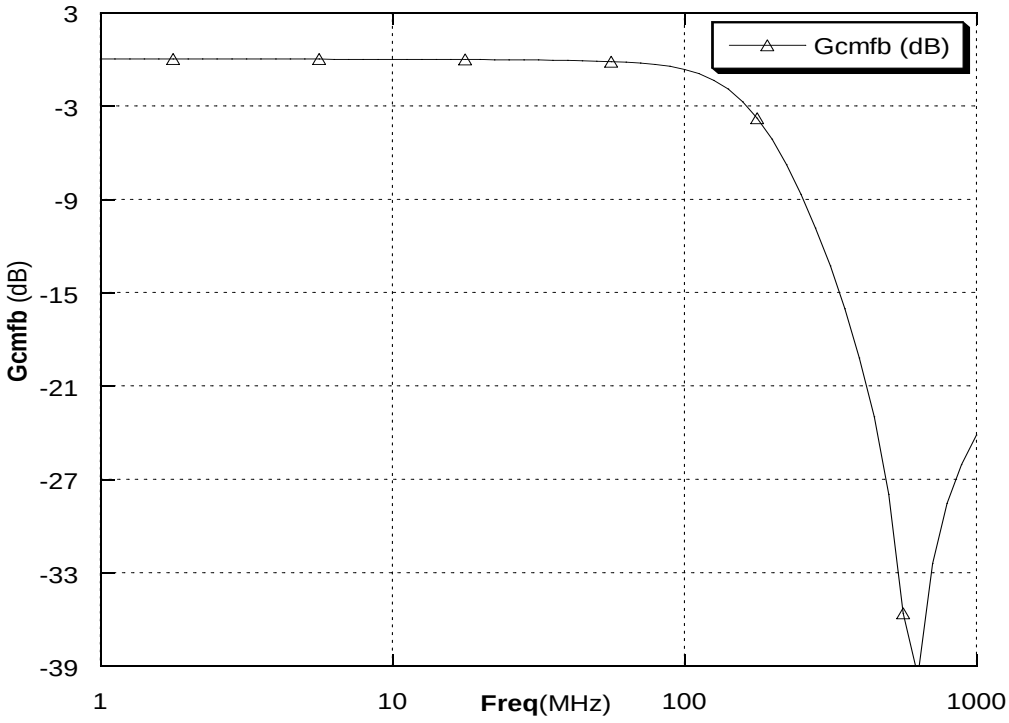

Figure 3.11: Frequency response of the CMFB amplifier.

comes from Q2 and the other half comes from Q4. With this assumption and some simplification to the KCL and KVL nodal equations, the common mode gain of the circuit is simplified to Equation 3.22, where r_o is the output of the BJT transistor. Since all transistors of the transconductor carry the same current, their output resistances are the same. A detailed derivation of the following result is given in Appendix B.

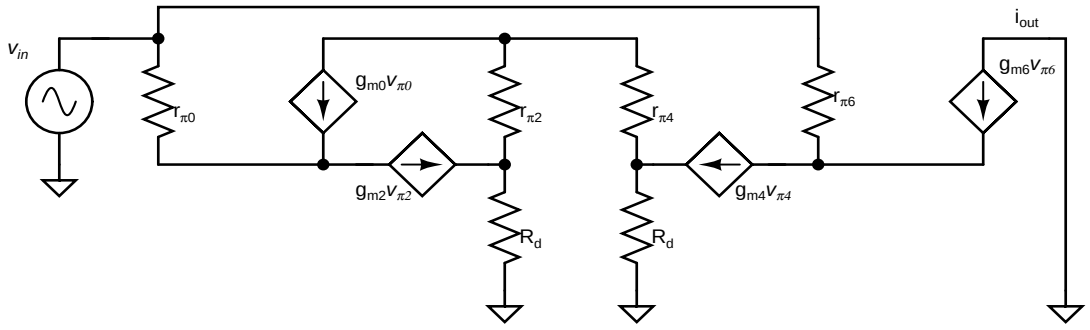

Figure 3.12: A small-signal circuit equivalent of the transconductor.

$$i_{cm} = \frac{\frac{\beta_2 g_{m0}}{2}\frac{v_{in}}{r_0}}{\left(1+\frac{\beta_2}{2}\right)g_{m0} + g_{\pi 0} + \frac{g_{m0}R_D}{2r_0}}$$

$$i_{cm} = \frac{\beta_2 g_{m0} v_{in}}{\beta_2 g_{m0} r_0 + 2g_{\pi 0} r_0 + g_{m0} R_D}$$

$$g_{cm} = \frac{i_{cm}}{v_{in}} = \frac{\beta_6}{\beta_6 + 1}\frac{1}{r_0 + \frac{2r_0}{\beta_2\beta_0} + \frac{R_D}{\beta_2}} \approx \frac{1}{r_o} \tag{3.22}$$

The CMRR of a differential circuit is given by Equation 3.23, where A_d is the differential gain, A_{CM} is the common mode gain, and A_{vCM} is the CMFB loop gain. From simulation, the CMRR at the DC is -146 dB, but has its pole at 10 KHz. Thus, the CMRR at the center frequency of the filter is about -76 dB, which is more than the target linearity.

$$CMRR = \frac{A_d A_{vCM}}{A_{CM}} = \frac{g_{m6} r_{ds6} r_{ds8} r_o}{R_{CM} R_E} \tag{3.23}$$

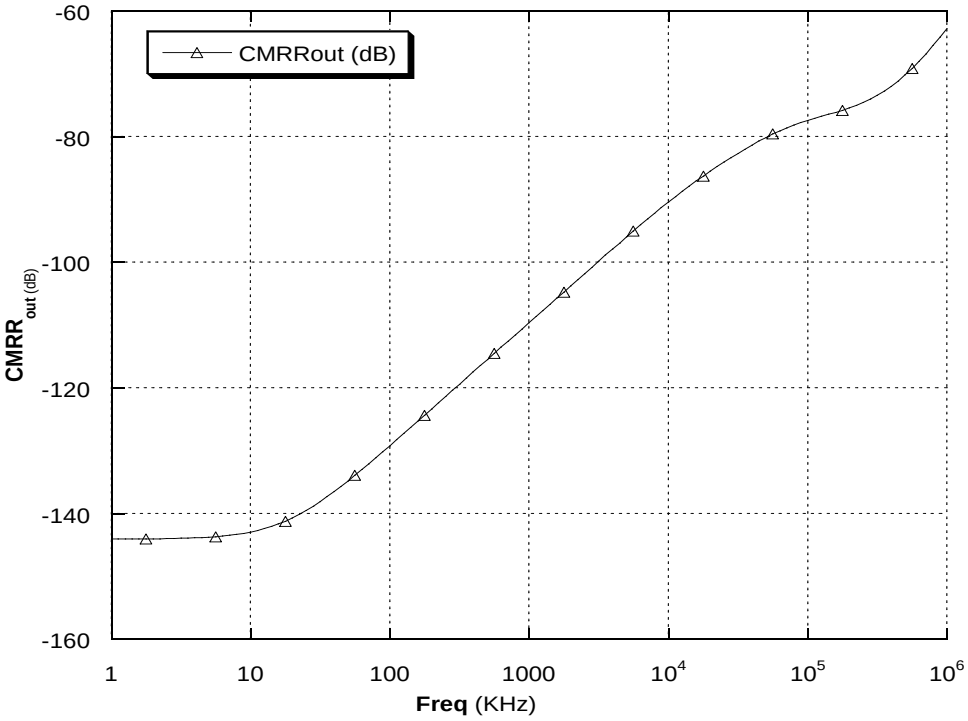

Figure 3.13: Common mode rejection ratio of the proposed transconductor.

3.4.6 Tunable Transconductor

The value of the transconductance is tuned by changing the value of the lateral degeneration resistor. In this implementation, it is tuned using a 5-bit control word; C0 is the least significant bit and C4 is the most significant bit. The control bit either shorts the resistors or plugs them into the transconductance element. The value of an individual resistor of the Q-tuning transconductor is chosen such that it gives an uniform unity steps to the quality factor of the filter. Since the value of the quality factor is a ratio of transconductance to the difference in transconductance, therefore an uniform steps in the quality factor does not results in an uniform steps in transconductance.

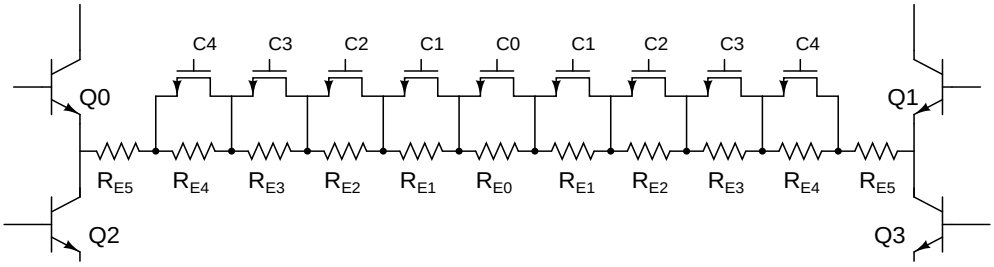

Figure 3.14: A schematic diagram of the tunable transconductor.

With an increase in the quality factor of the filter, the gain of the filter is held constant by reducing the value of the gain controlling transconductor simultaneously. The value of the gain controlling transconductor is also chosen such that with an increment increase in quality factor, the gain of the filter is held between 20-24 dB. Thus, the stand-alone transconductance steps are also non-uniform but maintains a constant gain.

3.4.7 Process Mismatch Analysis to Signal Distortion

The performance of the continuous-time filters have already been pushed beyond a moderate level; for any further increase in performance, in terms of linearity, distortion or center frequency depends on the subtle aspects of circuit design, in which device mismatch and parasitic become important. In SPICE simulation, which does not account for process mismatch, one can be deceived by the simulation result, as it shows 90+ dB of linearity without emitter degeneration [51, 4]. Since the emitter degeneration resistor reduces the loop gain,

as given in Equation 3.17, it is counter-intuitive to degenerate the mirrors. However, the above analysis holds true of the mirror, and diff-pair devices have an exact match.

The V_{BE} mismatch of the HBT device degrades the linearity of the transconductor, *e.g.*, a V_{BE} mismatch of 1 mV gives 4% error in the current or gm of a transistor, which limits the performance of the work published by Koyoma. But for the transconductor shown in Figure 3.3, the emitters of all mirror devices are degenerated with ηV_T where $\eta = 3$. This degrades the loop gain but improves the DC linearity with mismatch in the transconductor by $20 \times \log(1+\eta)$ dB. In simulation, this degeneration improves the overall linearity of the circuit from 65 dB to 80+ dB, as shown in Figure 3.6. Thus, the effect of mismatch is mitigated by emitter degeneration in the design and by using a common centroid structure in the layout. The HBT is a bulk device and it has smaller process mismatch than MOS transistors.

3.5 Design of Biquad Bandpass Filter

3.5.1 Biquad Bandpass Filter

A prototype biquad filter is implemented using the above transconductor with dynamic range of 62 dB. This filter is also used to verify the proposed quality factor tuning scheme. The transfer function of the filter is given by Equation 3.24. The quality factor of the filter is made from the ratio of G_{mf} to the difference of two transconductance, a large quality factor($\sim$50) is achieved without having a large transconductance ratio. A small transconductance means large resistance, and large voltage noise. The gain of the filter is held constant with Q by reducing the value of G_{mg} while increasing the G_{mq} and vice-versa. A block-level implementation of the biquad circuit, is shown in Figure 3.15.

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_{mg}}{sC}}{1 + \frac{G_{mh}-G_{mq}}{sC} + \left(\frac{G_{mf}}{sC}\right)^2}; \tag{3.24}$$

$$\text{where } \omega_0 = \frac{G_{mf}}{sC} \tag{3.25}$$

$$Q = \frac{G_{mf}}{G_{mh} - G_{mq}} \tag{3.26}$$

$$Gain = \frac{G_{mg}}{G_{mh} - G_{mq}} \tag{3.27}$$

Table 3.1: Component values of the biquad filter.

Components	*Value (Q=16 ⇒ Q=48)*
G_{mf}	760 μS
G_{mh}	138 μS
G_{mg}	$629 \Rightarrow 385 \mu S$
G_{mq}	$209 \Rightarrow 243 \mu S$
$2C$	1.56 pF

The values of the transconductors are tuned using a 5-bit controller, which switches the resistors in and out from the resistors (REs). The REs are implemented using a low-temperature coefficient poly resistor that has a sheet resistance of 35 Ω and process variation of ±10%. The smallest value used for the tuning resistors is 20 Ω, which is laid out 3 square long to minimize any etching effect. The size of the switches is chosen judicially so that their on-resistances are small compared to the REs, and they do not add parasitic capacitance to cause an excess phase shift.

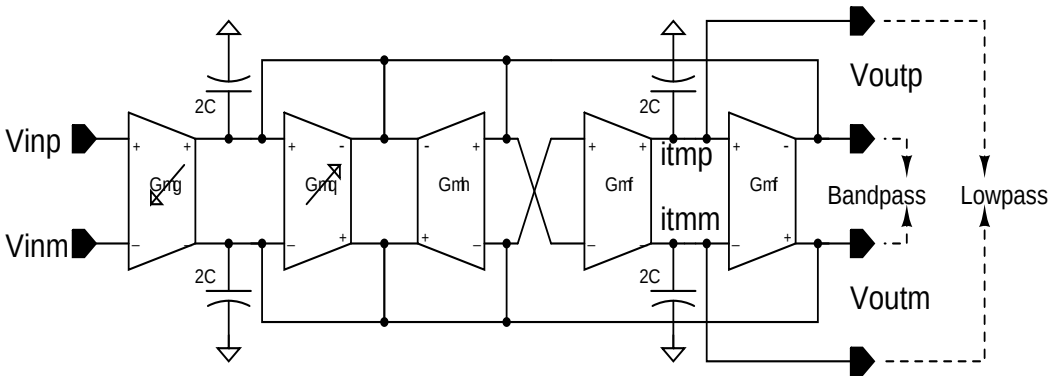

Figure 3.15: The block-level representation of the biquad filter.

The values of the transconductances and the capacitance of the biquad filter are listed in Table 3.1. The quality factor of the filter can be tuned from 16 to 48 with an incremental step of 1, while the gain and the center frequency are held constant at 20 dB and 100 MHz, respectively. The frequency and phase response of the biquad filter are shown in Figure 3.16. The second and third harmonic distortion numbers for different signal levels are listed in Table 3.2. The magnitude and phase response of the filter with all 32 values of the quality

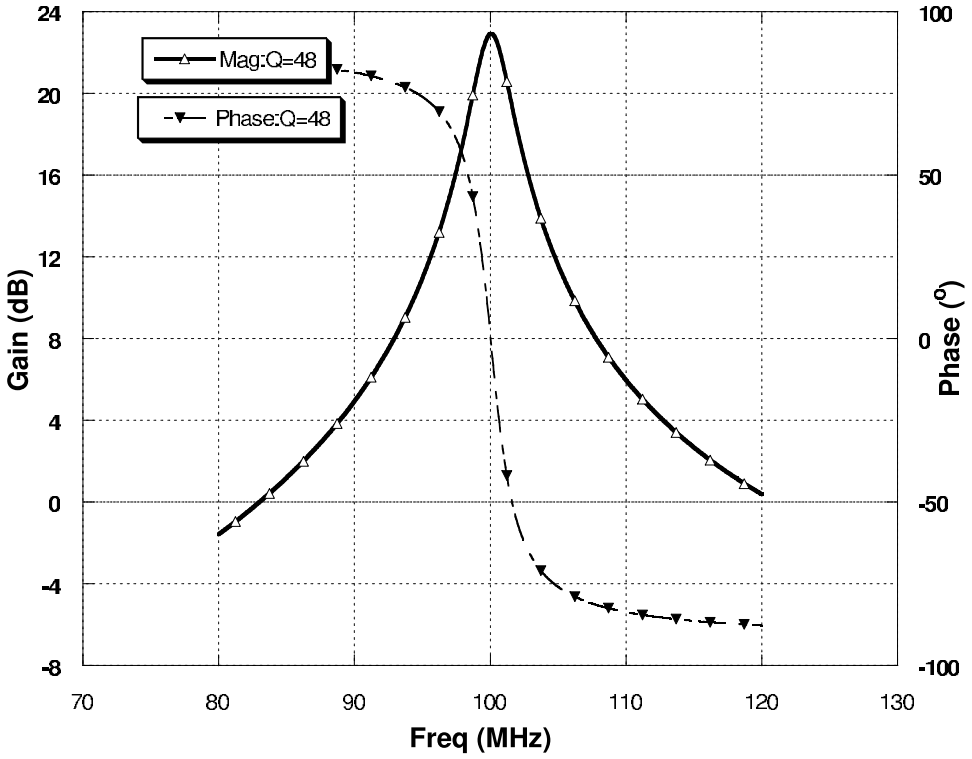

Figure 3.16: The magnitude and the phase response of the biquad filter.

factor from 16 to 48 is shown in Figure 3.17 and Figure 3.18, respecitvely. The phase lags with frequency which confirms that the biquad filter is stable and is a causal system.

3.5.2 Noise

The noise equivalent model of the proposed biquad filter is shown in Figure 3.19. From Section 2.3.2.4, the noise power spectral density of the filter is given by Equation 3.28. At the output of the filter, the Q-defining transconductor is connected in a diode configuration and it converts the total output current into voltage. Here, the noise in the biquad is dominated by the active devices.

$$
\begin{aligned}
v_{no}(f) &= \frac{1}{G_{mh} - G_{mq}} \left(i_{ng} + i_{nq} + i_{nh} + i_{nf2} - \frac{G_{mf1}}{j\omega_0 C_2} i_{nf1} \right) \\
\frac{\overline{v}_{no}^2(f)}{\Delta f} &= \frac{1}{G_{mq_1}^2} \left(i_{ng}^2 + i_{nq}^2 + i_{nh}^2 + i_{nf2}^2 + i_{nf1}^2 \right) \approx \frac{40 q I_C}{G_{mq_1}^2} \qquad (3.28) \\
&\text{where } G_{mq_1} = G_{mh} - G_{mq}
\end{aligned}
$$

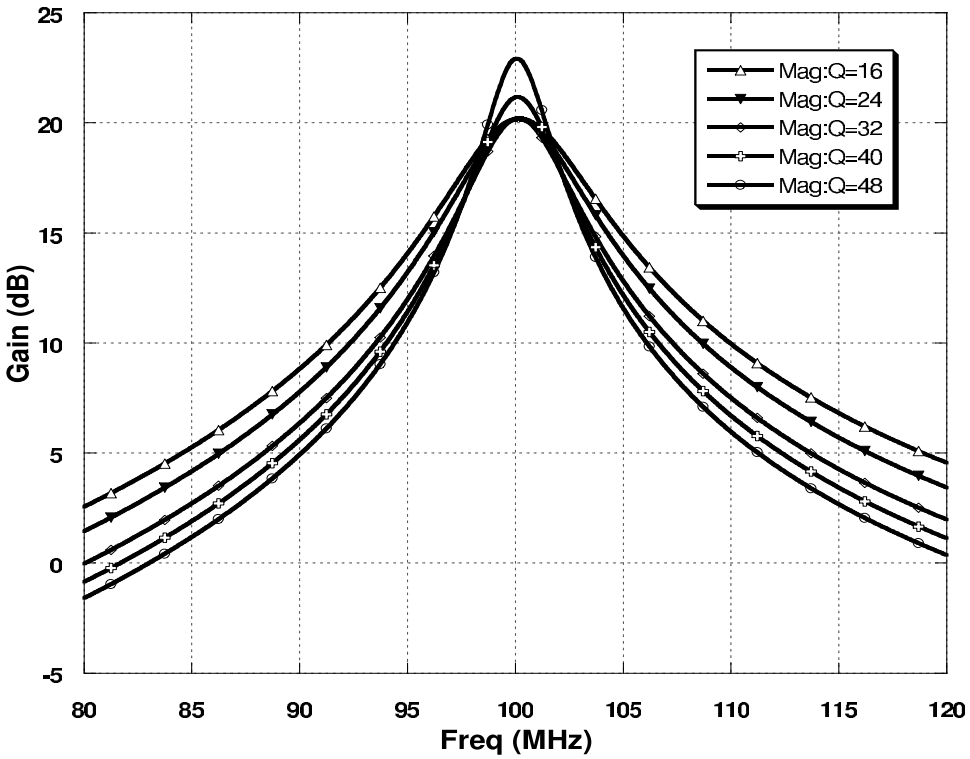

Figure 3.17: The magnitude response of the biquad filter at few quality factor values.

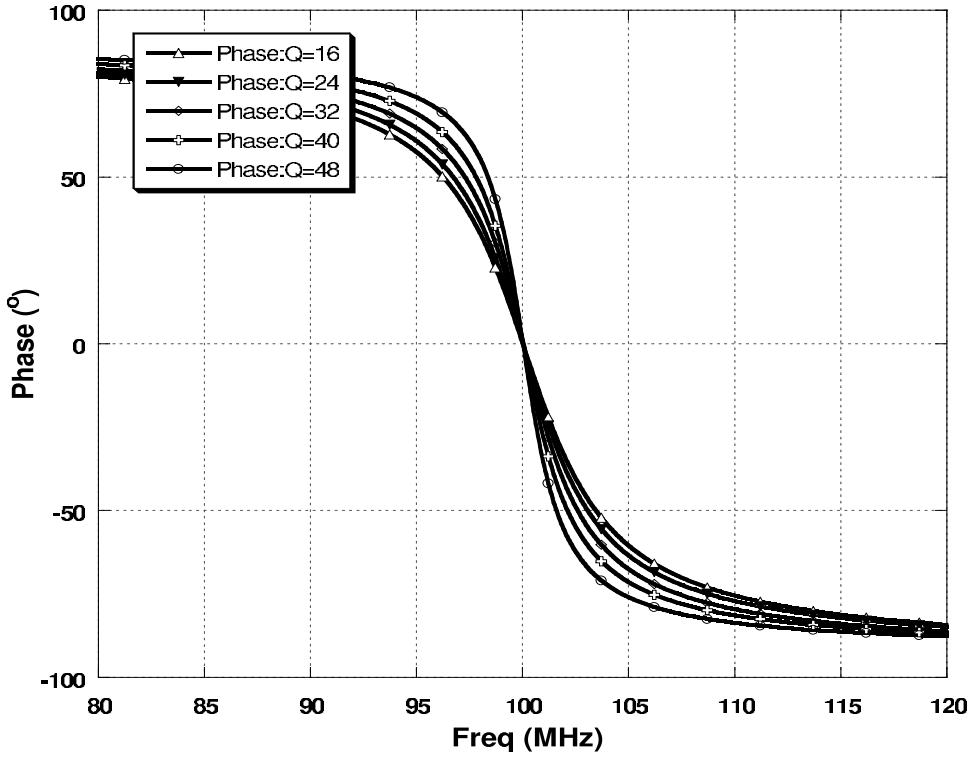

Figure 3.18: The phase response of the biquad filter at few quality factor values.

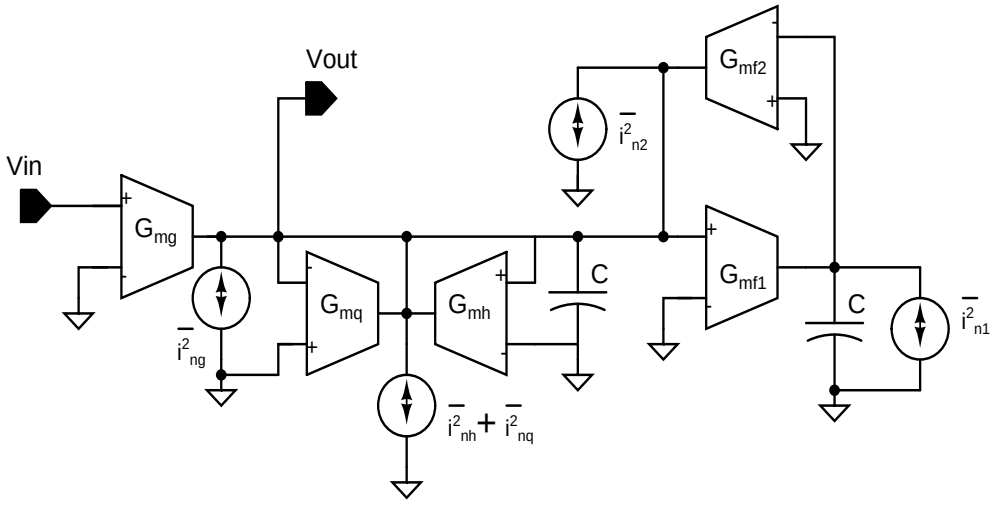

Figure 3.19: The noise model of the proposed biquad filter.

3.5.3 Dynamic Range

The amplified output signal of the filter is fed as input to transconductors g_{mh}, G_{mq}, and G_{mf}. All of them have equal contribution in the output signal distortion. In order to keep the step size of transconductor G_{mq} within practical limits, the values of G_{mh} and G_{mq} have to be kept five to six times smaller than the value of G_{mf}. Thus, the maximum signal handling capacity and distortion are limited by transconductor G_{mf}. Hence, the peak-to-peak signal handling capacity of the filter is $4 \times I_{CC}/G_{mf}$.

The noise power spectral density of the filter is given by Equation 3.28 and the noise equivalent bandwidth of a bandpass filter is given by Equation 2.32. Hence, the total output noise power of the filter is given in Equation 3.29, which is a multiplication of the two. The dynamic range (DR) of the biquad is given in Equation 3.30. For this 100 MHz filter, the dynamic range of the filter is 65 dB.

$$\overline{v}_{no}^2(f) = \frac{40qI_C}{G_{mq_1}^2} \times \frac{\pi f_0}{2Q} \tag{3.29}$$

$$DR = \frac{V_{-1dB}^2}{\sum \overline{v_{no}}^2} \approx \frac{I_c}{\pi q f_0 Q} = 65.2dB \tag{3.30}$$

The total harmonic distortion of the biquad filter for various output signal amplitudes

Table 3.2: Harmonic distortion of the biquad filter.

$V_{in}pp$	$V_{out}pp$	*HD2 (dB)*	*HD3 (dB)*	*THD (dB)*
14 mV	0.1 V	79	85	77.8
36 mV	0.5 V	75.1	78.2	72.7
71 mV	1 V	68.3	79.4	67
111 mV	1.6 V	66	66.5	63

is listed in Table 3.2. These simulation results suggest that the proposed biquad filter has a total harmonic distortion of 67 dB for a 1V peak-to-peak signal and 63 dB for 1.6 V peak-to-peak signal. At a 1.6 Vpp output signal, the HD2 and and HD3 of the signal are well above the noise floor of the filter.

3.6 Q-Locked-Loop Tuning Scheme

As discussed in Section 2.6, an on-chip continuous-time filter requires an automatic center frequency and quality factor tuning scheme to counter the process variation ($\pm 20\%$) of monolithic active and passive components, and end-user enveromental temperature variation. The inability of the existing tuning schemes to tune a high-Q, high-frequency filter has provided the motivation for this work.

The Q-locked-loop (QLL) tuning scheme uses the phase characteristics of the filter to extract the quality factor information and it uses the filter as a VCO inside a PLL system where it modulates the transconductance of the Q-tuning transconductor using loop control voltage to tune the quality factor of the filter. The magnitude and phase characteristics of the filter are known prior to its implementation. This prior knowledge of frequency response is used to tunes the output phase shift at a known reference frequency to a known reference value. For example, a biquad filter gives a phase shift of 45^o at its 3 dB cut-off frequencies with respect to its center frequency. If the phase shift at 3 dB frequency is more than the desired value (45^o), it implies that the quality factor of the filter is also more than the desired value (Q_0) and vice-versa. The above argument can be seen graphically in Figure 3.20.

This scheme compares the output phase shift (ϕ_{fil}) of the filter at a reference frequency

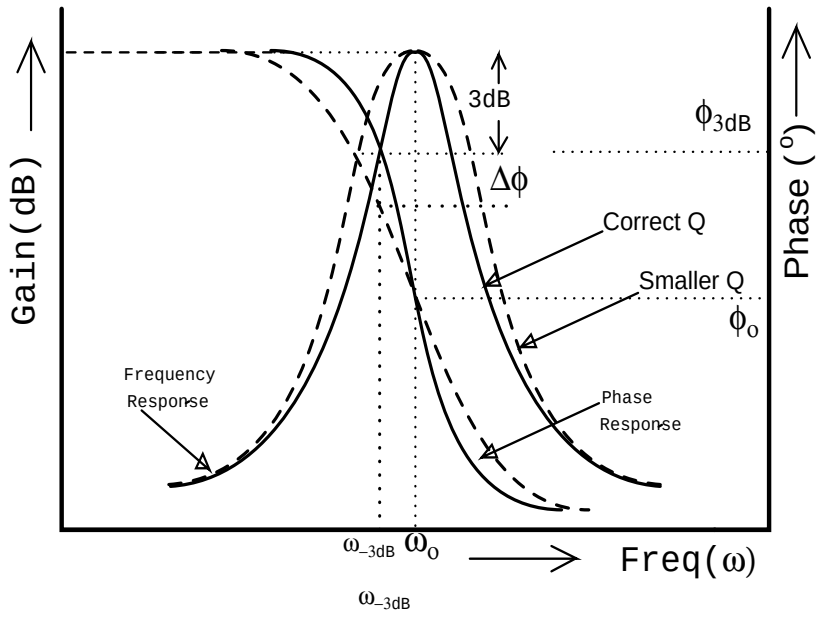

Figure 3.20: A pictorial representation of the Q lock loop tuning algorithm.

ω_{ref} to a desired reference value (ϕ_{ref}) using a phase frequency detector (PFD). This PFD generates an error signal (ϕ_e) based on the phase difference between the ϕ_{ref} and ϕ_{fil}. The phase error signal ϕ_e of the PFD is filtered and integrated using a lowpass loop filter. The integrated voltage, V_e, is used to tune the quality factor of the filter. The block diagram of this scheme is shown in Figure 3.21, where it tunes the biquad filter using one of its 3 dB cut-off frequencies. The concept and the operation of the QLL is similar to a phase-locked-loop (PLL) system, except it uses the phase characteristics of the filter in lieu of voltage controlled oscillator (VCO) to convert the loop control a voltage into the phase information [84]. Therefore, it has been referred to as a quality factor locked-loop (QLL) scheme. This scheme uses elicited knowledge of the PLL system; therefore, even though it is a new scheme, it benefits from the work and research published on DPFD and PLL systems [63, 64].

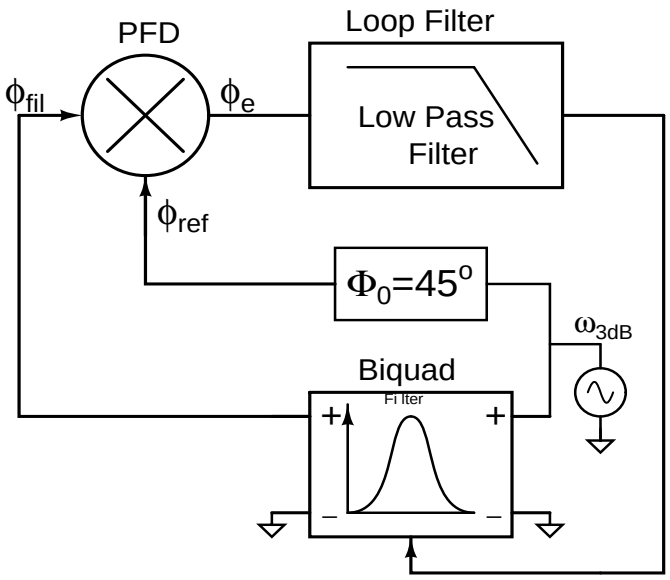

Figure 3.21: Block diagram of Q-lock-loop tuning scheme.

3.6.1 Loop Dynamics

The loop behavior of a control system is easily understood in the s-domain using a Laplace transform. Therefore, the phase characteristics of the filter are transformed into the s-domain to understand the loop dynamics of the proposed QLL system. The transformed expression of the filter phase response is used along with the phase frequency detector, charge-pump, and loop filter transfer function to solve for the loop parameters ($\omega_n$and ζ) and draw an analogy to a PLL system [85, 86, 87].

3.6.1.1 Filter Phase Characteristics

The phase characteristics of a bandpass filter defined by Equation 3.6 are given in Equation 3.31, where $\omega_0 = G_{mf}/C$ is the center frequency, $Q = G_{mf}/G_{mq}$ is the quality factor of the filter, and ω is an arbitrary input frequency.

$$\phi\left(H(s)\right) = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega.\omega_0}{Q.(\omega_0^2 - \omega^2)}\right) \tag{3.31}$$

The Laplace transform of the phase characteristics of the filter is given by Equation 3.32 [88]. This transformation equation is a non-integrable function. Therefore, the arctan(t) is

approximated to an exponential function to understand the loop behavior within the band of interest [88].

$$\Phi(s) = \int_0^\infty \left(\frac{\pi}{2} - tan^{-1}(v)\ e^{-sv}\right) dv; \text{ where } v = \frac{\omega_0\omega_1}{Q\left(\omega_0^2 - \omega_1^2\right)} \tag{3.32}$$

The band of interest is defined by evaluating the output phase shift from the biquad filter at extreme values of Q. The two extreme values of Q are 1/2 and ∞. Let us assume that the ω_1 and ω_2 are the lower and upper 3dB cut-off frequencies of the filter. We also know that the $\omega_2 - \omega_1 = \Delta\omega$ is the bandwidth of the filter and $\sqrt{\omega_1\omega_2} = \omega_0$ gives center frequency of the filter.

Upon using the above formulas and some simplification of Equation 3.31, it is found that a biquad bandpass filter with a quality factor of 1/2, Q_0, and ∞ gives a phase change of $0^o, 45^o$, and 90^o, respectively, at its one of the cut-off frequencies. In the QLL tuning scheme, the output phase shift of the filter is compared with a reference (ϕ_{ref}), which is 45^o. Thus, the maximum phase error in the QLL scheme is 45^o. Hence, the the value of 'v' is bounded to ± 1. Hence, without looking at any generality, the function $tan^{-1}(v)$ is approximated to Equation 3.33 within the band of this band of interest.

$$\tan^{-1}(v) \approx \begin{cases} \frac{\pi}{2}\left(1 - e^{-nv}\right); \text{ where } 0 \leq\ v\ \leq 1 \text{ and } n = 0.7 \\ -\frac{\pi}{2}\left(1 + e^{-nv}\right); \text{ where } -1 \leq\ v\ < 0 \text{ and } n = 0.7 \end{cases} \tag{3.33}$$

The numerical simulation of the above approximation is shown in Figure 3.22. The Laplace transform of the approximated filter phase transfer characteristic is given by Equation 3.34.

$$\mathcal{L}\left(\frac{\pi}{2} - \frac{\pi}{2}\ (1 - e^{-nv})\right) = \frac{\pi}{2}\frac{1}{s+n}\ \sim K.\frac{1}{s+0.7} \tag{3.34}$$

The s-domain representation of the filter phase characteristics is very similar to an ideal voltage controlled oscillator, which is $\frac{1}{s}$. A normalized VCO has its pole at $\omega = 0$ and provides infinite gain at zero frequency, whereas the phase characteristics of the filter have

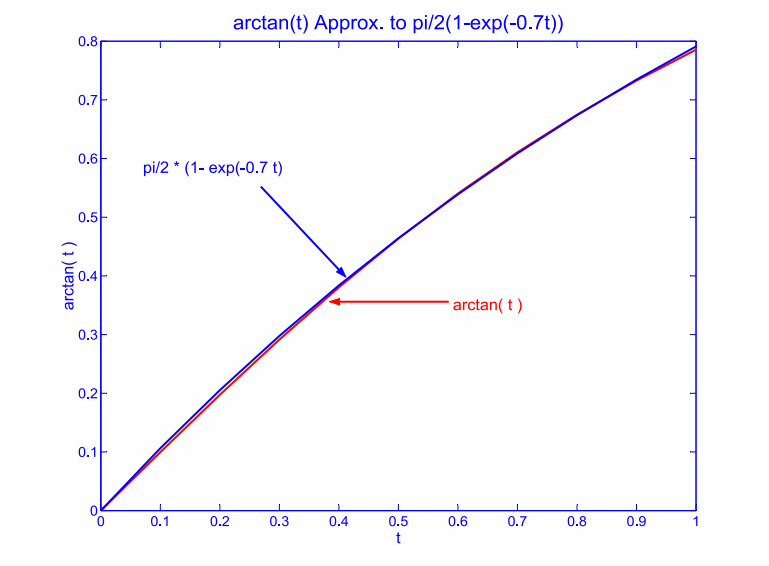

Figure 3.22: Comparison of $tan^{-1}(t)$ to $\frac{\pi}{2}(1 - e^{-0.7t})$.

their pole on the negative real axis of the s-plane and have only a finite gain at DC. This difference in gain and pole location determines the stability of the second-order PLL and QLL system.

3.6.1.2 Digital Phase Frequency Detector and Charge-pump

A digital phase frequency detector (DPFD) in a PLL system detects phase and frequency differences between a reference and a clock signal. In the proposed QLL system, it detects the phase difference between the reference signal (ϕ_{ref}) and the filter output signal (ϕ_{fil}). It generates an *up* or *down* signal, depending up on whether the phase error (ϕ_{err}) is positive or negative. These outputs of the DPFD drive a charge-pump circuit like any PLL system; together they perform the function of analog mixer and loop filter of an analog PLL system. An analog mixer can only detect phase error between the two input signals whereas a DPFD can detect both phase and frequency error; this gives a large *lock range*, and an infinite *pull-in range* to a PLL system [64]. A typical digital PFD circuit is made from flip-flops therefore it does not consumes any quiescent current. It is smaller in area compared to an analog mixer. Therefore, in the QLL system, even though it does not require a frequency-error detector, a DPFD is used as a phase detector.

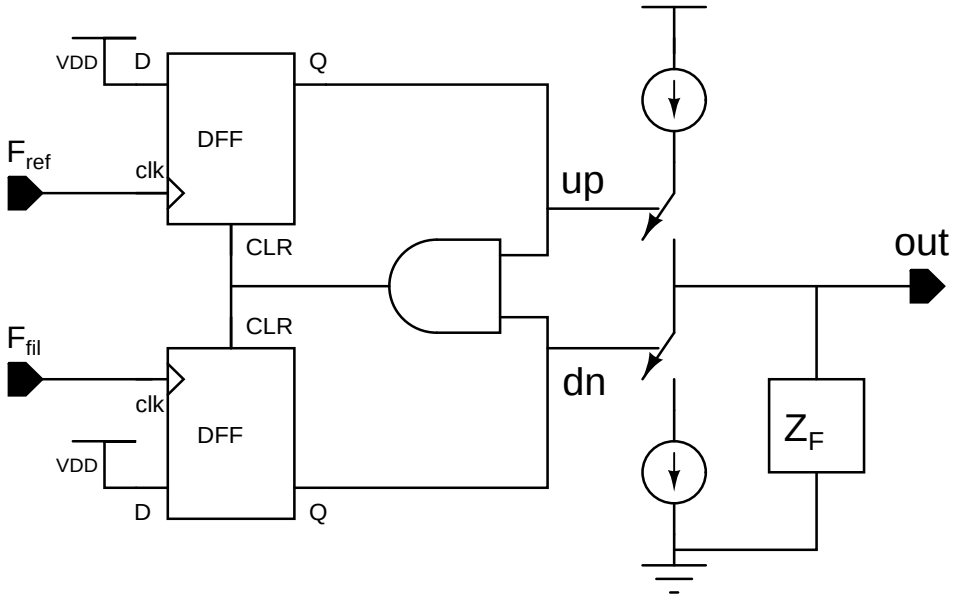

Figure 3.23: Basic principle of a charge-pump circuit.

A charge-pump circuits receives the *up* and *down* signals as input from the DPFD. It sources or sinks a current proportional to the difference in pulse width of the input signals, as shown in Figure 3.23. A charge-pump sources (sinks) a difference current, given by Equation 3.35, to (from) the loop filter for $\frac{\phi_e}{2\pi} \times T$ time, where $1/T$ is the tuning frequency (in this case it is $\omega{-}3dB$ frequency) and ϕ_e is the phase error between the two inputs. The combined transfer function of the DPFD and the loop filter (K_D) is given by Equation 3.36. [64, 80].

$$I_d = I_0 \times \frac{\phi_e}{2\pi} \tag{3.35}$$

$$V_c(s) = \frac{I_0(s) Z_F(s) \phi_e(s)}{2\pi}; \text{ where } Z_F(s) = \text{Loop filter transfer function.} \tag{3.36}$$

where I_0 is the the charge-pump current. The loop filter (Z_F) integrates the difference current (I_d) and generates a loop control voltage (V_c). Thus, the over all transfer function of the loop control voltage (V_c) is given by Equation 3.36.

3.6.1.3 QLL Close-Loop Transfer Function

A block diagram of the second-order quality factor locked-loop system is shown in Figure 3.24. Upon substituting the transfer function of the individual blocks of the QLL system, the closed loop transfer function of the proposed tuning scheme is given by Equation 3.37 [64].

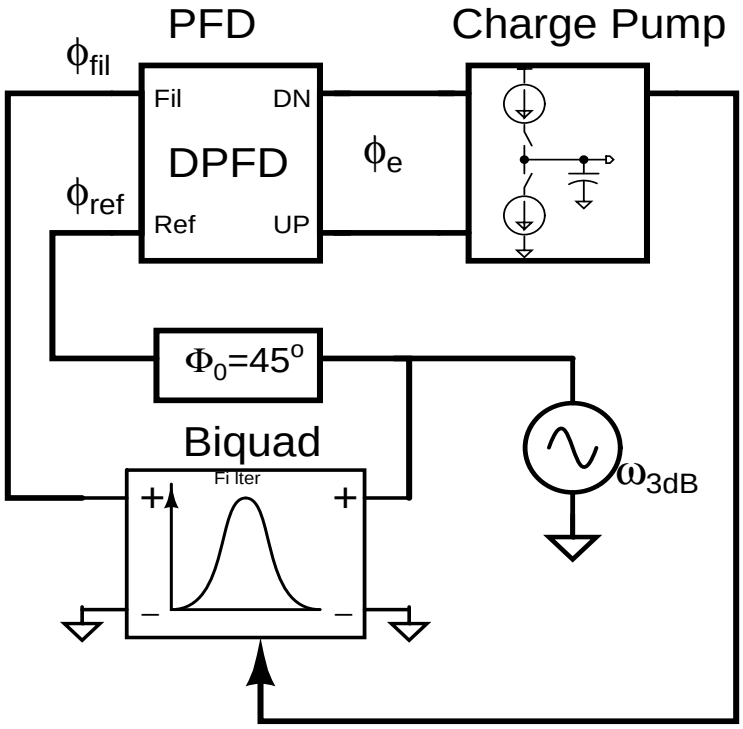

Figure 3.24: A second-order quality factor locked-loop system.

$$\frac{\phi_o}{\phi_{ref}} = \frac{K_0 K_D I_0 Z_F(s)}{2\pi(s+n) + I_P K_0 K_D Z_F(s)} \tag{3.37}$$

$$Z_F(s) = \frac{1}{sC} \tag{3.38}$$

where K_0 is the VCO gain, K_D is gain of the DPFD, Z_F is the loop filter transfer function, and I_0 is the charge-pump current. For a second-order QLL tuning scheme, the loop filter is a first-order capacitive filter, and its transfer function is given by Equation 3.38. Upon substituting the value of Z_F in Equation 3.37, and with some simplifications, the phase

transfer function ($H(s)$) and phase-error transfer function($H_e(s)$) of the loop are given by Equation 3.39 and Equation 3.40, respectively.

$$H(s) = \frac{\phi_o}{\phi_{ref}} = \frac{\frac{I_0 K_0 K_D}{2\pi C}}{s^2 + ns + \frac{I_0 K_0 K_D}{2\pi C}} \tag{3.39}$$

$$H_e(s) = 1 - H(s) = \frac{\phi_e}{\phi_{ref}} = \frac{s^2 + ns}{s^2 + ns + \frac{I_0 K_0 K_D}{2\pi C}} \tag{3.40}$$

From the above equation, it is evident that a second-order implementation of the proposed QLL tuning scheme has both its poles in the left half of the s-plane. Hence it is unconditionally stable. The QLL tuning scheme benefits from the fact that a bandpass filter has gentle phase roll-off in its pass-band and has finite gain at its center frequency.

The natural frequency (ω_n) and the damping factor (ζ) of the closed loop QLL tuning scheme are given in Equation 3.41 and Equation 3.42, respectively. These equations are used to design the value of the current (I_0) of the charge pump and the capacitance of the loop filter. For the second-order QLL system to be critically damped, the ζ of the loop should be greater than 0.707.

$$\omega_n = \sqrt{\frac{I_0 K_0 K_D}{2\pi C}} \tag{3.41}$$

$$\zeta = \frac{n}{2}\sqrt{\frac{I_0 K_0 K_D}{2\pi C}} \tag{3.42}$$

$$\tau_s = \frac{4.5 \times \zeta}{\omega_n}; \quad \text{for } \zeta > 0.69 \tag{3.43}$$

The settling time for such a second-order control system is given by Equation 3.43, which is inversely proportional to the natural frequency of the loop. Therefore, a fast settling time is achieved by choosing a large natural frequency and large loop bandwidth. However, the loop bandwidth for a phase-locked-loop system is limited by one tenth of the input frequency of the DPFD. The DPFD inside a PLL system performs a sample-and-hold function in the phase domain. Therefore, from sampling theorem, the signal frequency has to be less than half the sampling frequency. For better and accurate performance, it is recommended to keep the loop bandwidth (LBW) below one eighth of the DPFD frequency (f_{dpfd}) in a PLL system.

In the above derivation of natural frequency and damping factor, the sampling effect of the DPFD is not taken into consideration. The sampling effect decreases the phase margin of the filter by $LBW/f_{DPFD} \times \pi$ degrees. If the loop bandwidth is kept more than half the sampling frequency, the loop goes into oscillation [64]. Thus, the gain from the first-order capacitive filter is chosen such that the loop bandwidth remains on the order of one tenth the sampling frequency.

The above result of the second-order QLL system is contrary to the stability of a conventional second order PLL system. The transfer function of a second-order PLL system is given by Equation 3.44. Both its poles are on the $j\omega$ axis; given by Equation 3.45, therefore it is only conditionally stable.

$$\frac{\phi_f}{\phi_{ref}} = \frac{\frac{I_0 K_0 K_D}{2\pi C}}{s^2 + \frac{I_0 K_0 K_D}{2\pi C}} \tag{3.44}$$

$$s = \pm j\sqrt{\frac{I_0 K_0 K_D}{2\pi C}} \tag{3.45}$$

A typical VCO has its pole at the origin and a first-order capacitive filter also has its pole at the origin. Thus, when they are connected in a closed-loop system, they give a pair of complex conjugate poles on the $j\omega$ axis, making the system only conditionally stable. However, in the proposed QLL tuning loop, the approximated s-domain transfer function of the filter phase response has its pole on the negative real axis. This negative real axis pole, when combined with the pole at the origin of the loop filter in a closed-loop system, gives a pair of complex conjugate poles in the left half of the s-plane. Hence, the proposed second-order QLL tuning loop is unconditionally stable even with a first-order capacitive loop filter.

3.6.2 Loop Dynamics to Q-error Input

The input to the tuning scheme is the error in quality factor of the filter, which is equivalent to a step phase change input to a QLL system. As discussed in Section 3.6, the largest Q-error (45^o) occurs when quality factor of the filter is either 0.5 or ∞. This phase error is equivalent to a step phase input of magnitude $\Delta\phi$ to the QLL system, as given in

Equation 3.46, where *u(t)* is a unit step function.

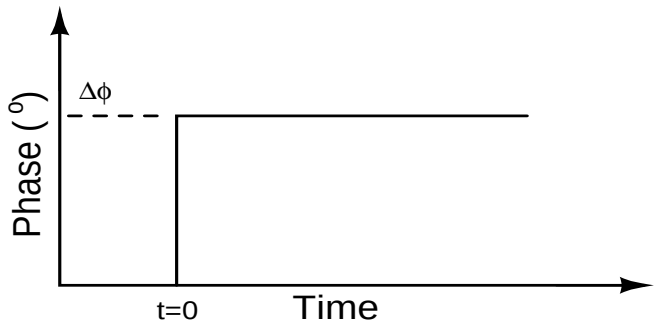

Figure 3.25: ΔQ-error equivalent step input phase change.

The error in the final Q-value of the filter (after tuning) can be found by looking at the steady state-error of the QLL to a step input. A Laplace of the step phase change is given by Equation 3.47.

$$\theta_{in}(t) = \Delta\Phi u(t) \tag{3.46}$$

$$\Theta_{in}(s) = \frac{\Delta\Phi}{s} \tag{3.47}$$

The steady state error from the proposed second-order system to a step phase change in the s-domain is given by Equation 3.48. From the final value theorem of the Laplace transform, the steady-state error in Q is zero [88] and is given in Equation 3.49. Thus, a second-order Q-tuning loop is necessary and sufficient to achieve zero Q-tuning error.

$$\Theta_e(s) = \Theta_{in}(s)H_e(s) = \frac{\Delta\Phi}{s}\frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3.48}$$

$$\theta_e(\infty) = \lim_{s\to 0} s\Theta_e(s) = 0 \tag{3.49}$$

This time-domain step response of a critically damped second-order QLL system is also shown in Figure 3.26. A second-order control system gives a constant error to a ramp input but, no such input appears to the proposed QLL scheme [89].

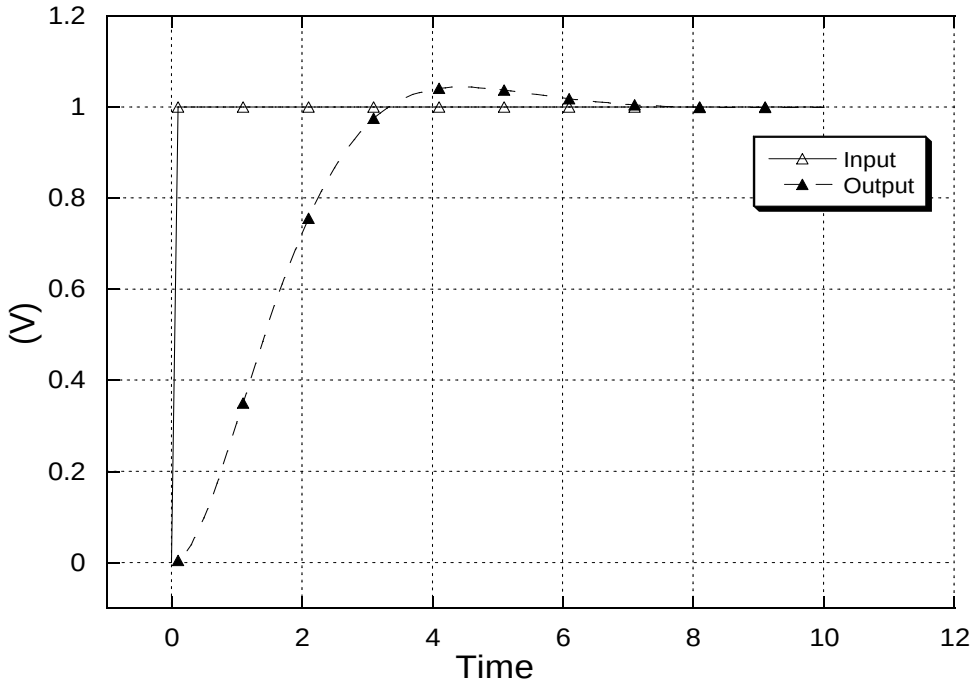

Figure 3.26: Second order QLL response to step change in input.

3.6.3 Non-idealities and Mismatch Analysis

The proposed tuning scheme extracts the quality factor information of the filter from its phase response; therefore is immune to any magnitude and offset variations. However, it is susceptible to any phase/delay mismatch, as it relies on the phase shift through the system. From Laplace theorem, a constant delay in the time domain in an electrical system is equivalent to the linear phase shift in the frequency domain, as given in Equation 3.50 [88].

$$\mathcal{L}\left(u(t-\tau)\right) = e^{-s\tau} \tag{3.50}$$

The proposed QLL tuning scheme requires a constant phase shift of ϕ_{ref} signal to f_{ref} signal, which can be generated either by using a multi-phase oscillator of frequency f_{3dB} or by delaying the input signal by a constant time $\tau_{ref} = T/8$, where *'T'* is the time period of the f_{3db} signal. In this implementation, the latter scheme is used because it has less circuit complexity. It does have a sensitivity to process variation, but it is low enough to prove

the concept. For higher accuracy, a multi-phase oscillator should be used to generate an accurate phase shift.

The above theorem also suggests that any delay mismatch τ_{mis} between the filter output signal and the reference signal will also appear as a phase mismatch error ϕ_{mis} at the output of the DPFD and it will result in an error to the final quality factor of the filter. The effect of delay mismatch on loop dynamics is better understood by incorporating the mismatch as a non-ideality to the ϕ_{fil} signal.

Assuming that there is an extra delay of τ_{mis} in the ϕ_{fil} signal compare to ϕ_{ref} signal. Since the phase response of the filter is a phase information, the delay mismatch is first converted into the phase domain by using the Laplace transform given in Equation 3.50. From the convolution theorem of the Laplace transform, a convolution in the time domain is equivalent to a multiplication in the frequency domain [88]. Thus, the equivalent delayed phase response of the filter is a multiplication of the phase response of the filter given by Equation 3.34 with the s-domain transform of the delay as given in Equation 3.51.

$$\Phi_{delay_{fil}}(s) = \mathcal{L}\left(e^{-nv}e^{-s\tau_{mis}}\right) = \frac{1}{s+n+\tau_{mis}} = \frac{1}{s+n'} \tag{3.51}$$

Now upon using the above delayed phase response of the filter in the closed-loop transfer function of the proposed QLL tuning scheme, the new modified phase transfer function of the loop is given by Equation 3.52. The new natural frequency and the damping factor of the loop are given by Equation 3.53 and Equation 3.54.

$$H(s) = \frac{\phi_o}{\phi_{ref}} = \frac{\frac{I_0K_0K_D}{2\pi C}}{s^2 + n's + \frac{I_0K_0K_D}{2\pi C}} \tag{3.52}$$

$$\omega_n = \sqrt{\frac{I_0K_0K_D}{2\pi C}} \tag{3.53}$$

$$\zeta = \frac{n'}{2}\sqrt{\frac{I_0K_0K_D}{2\pi C}} \tag{3.54}$$

From the above results, it is evident that the natural frequency of the loop is independent of the delay mismatch between the ϕ_{ref} and ϕ_{fil}. The damping factor of the loop is function of delay mismatch and its sensitivity to delay is given by Equation 3.55. The quantity in the

square root of Equation 3.55 is the total loop gain of the system. Thus, the zeta sensitivity to delay mismatch can be reduced by choosing a small loop gain and large integrating capacitor.

$$\mathcal{S}_\zeta = \frac{\partial \zeta}{\partial n} = \frac{1}{2}\sqrt{\frac{I_0 K_0 K_D}{2\pi C}} \tag{3.55}$$

This mismatch is between two similar quantities; therefore they can be matched to a great extent in the modern IC process using good layout techniques [90]. Since mismatch in a system is a relatively small quantity, it will not alter system performance, but it does change the settling time and the peaking in the loop.

3.6.4 Effect of Deadzone on Accuracy

The deadzone of the DPFD desensitizes the phase-locked loop. If a phase error is small enough to fall within the deadzone of the DPFD, the loop will not be able to resolve that error, as if the loop has reached its numerical limitation. This means that a small change in quality factor or phase of the filter will not change the control voltage of the loop. Thus the loop sensitivity to the deadzone of the DPFD is found by taking a partial derivative of the phase error (ϕ_e) to phase, as given in Equation 3.56. Hence, for the QLL tuning loop, sensitivity to deadzone is directly proportional to the error in the quality factor.

$$\begin{aligned} \frac{\partial \Phi_e}{\partial \phi} &= \frac{\partial \Phi_{fil} - \Phi ref}{\partial \phi} = \frac{\partial \Phi_{fil}}{\partial \phi} \\ &\approx \frac{\partial\ tan^{-1}\left(\frac{1}{Q}\right)}{\partial \phi} = \frac{1}{1+\frac{1}{Q^2}} \times \frac{\partial Q}{\partial \phi} \end{aligned} \tag{3.56}$$

$$\frac{\partial \Phi_e}{\partial \phi} \approx \frac{\partial Q}{\partial \phi};\ \text{for } Q >> 1 \tag{3.57}$$

Thus, from Equation 3.57, the error in the final Q-tuning value is also proportional to the phase error caused by the deadzone of the DPFD. This phase-error resolving limitation defines the minimum Q-error of the QLL tuning scheme.

3.7 Implementation of the QLL Tuning Scheme

The final implementation of the proposed QLL tuning scheme is shown in Figure 3.27. In this implementation, a second-order biquad is used as a prototype filter, and a constant phase shift of 45^o is achieved using a delay network. The propagation delay of the filter output signal (ϕ_{fil}) and reference signal (ϕ_{ref}) are matched by using a similar delay network to both signal paths. It is an RC delay network, where R is the *on* resistance of an inverter and C is the sum of the gate capacitor and poly-poly capacitor. The phase frequency detector is a precharge based dynamic DPFD, and first-order loop filter is implemented as a 5-bit digital integrator. The digital integrator allows the loop to digitally store the final control voltage in a 5-bit digital word. The gain of the digital integrator is reduced by reducing the clock frequency of the integrator.

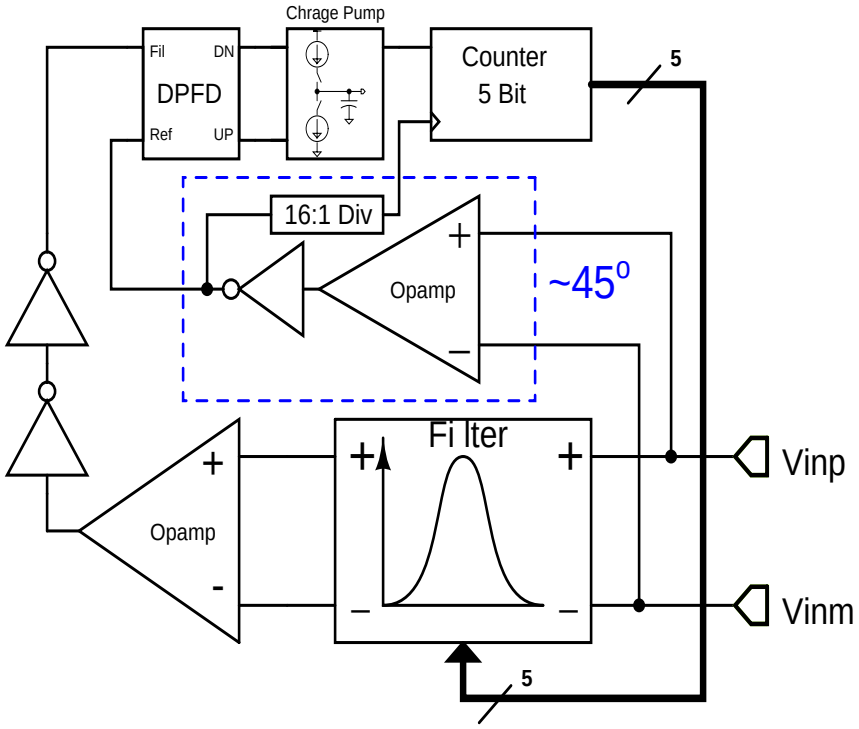

Figure 3.27: Block diagram of the implemented second-order QLL tuning scheme.

3.7.1 Digital Phase Frequency Detector

In a PLL systems, tracking range, acquisition range, loop gain, and transient response depend on the performance of the phase frequency detector. A Gilbert cell is often used as a phase detector in a PLL systems. It is an analog multiplier circuit. For $\omega_{ref} \neq \omega_{fil}$, the average output of this circuit is zero; therefore it cannot be used as a frequency detector [64]. An EXOR gate gives a similar response with digital input and output. An analog mixer or EXOR gate has periodic constant gain for $0 < |\Delta\phi| < \pi$.

A phase detector using two DFFs is commonly used in modern PLL or frequency synthesizer systems, as it has constant gain for phase error between $\pm 2\pi$. Therefore, it can also be used as the frequency detector. A schematic diagram of a PFD using a DFF is shown in Figure 3.28. It is referred to as a digital phase frequency detector, and can be implemented using either static logic or dynamic logic [85, 86, 87, 91, 92, 93, 94].

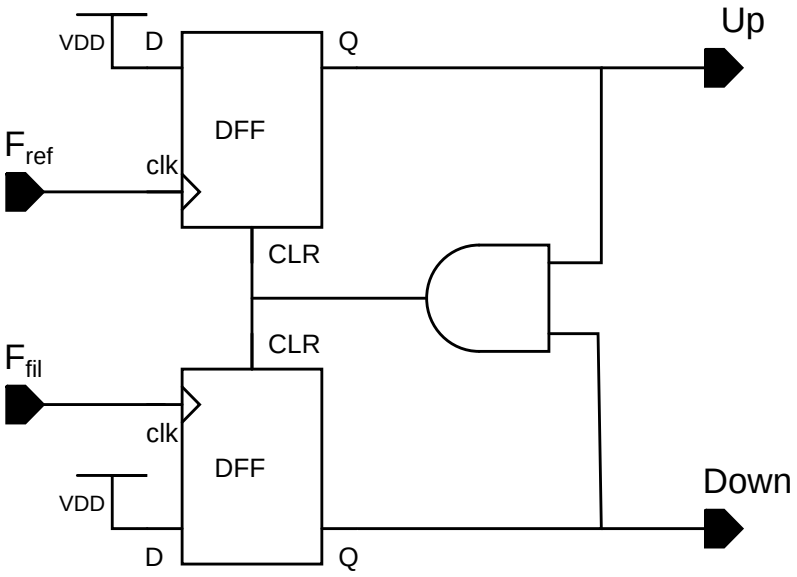

Figure 3.28: A DFF based digital phase frequency detector.

As discussed in Section 3.6, the Q-error of the proposed tuning scheme is directly proportional to the deadzone of the DPFD. Hence, the QLL tuning scheme requires a low-deadzone or no-deadzone DPFD circuit that can operate at f_{3dB} frequency [95].

3.7.1.1 Dynamic DPFD

The precharge-based no-deadzone DPFD circuit commonly is used for high-frequency PLL systems. A typical-latch based DPFD circuit is shown in Figure 3.29. There are three limitations to this DPFD circuit [96, 97, 98].

First, it is a latch based, level-sensitive architecture (not an edge-sensitive circuit); therefore input phase range depends on the duty cycle of the signal. Second, the transistors M4 and M11 of the second stage are driven directly from input, which causes redistribution of the precharge at the high-impedance *itm* to *shr* node. This redistribution can result in an incorrect output from the DPFD. This effect can be quantified as follows:

During the pre-charge event, the *itm* node is precharged to the VDD and holds charge $Q = C_{itm}VDD$, where C_{itm} is the total capacitance at the *itm* node. The total capacitance at the *itm* and *shr* nodes is given by Equation 3.58 and Equation 3.59. The transistors M4 (M11) is driven directly from the input, that comes before the signal driving the gate of the transistors M1 and M6. Therefore, the precharge (Q_{itm}) at the *itm* node gets shared with node *shr* and the final voltage at the *itm* node is given by Equation 3.60.

$$C_{itm} = C_{GI4} + C_{gd1} + C_{gd4} \tag{3.58}$$

$$C_{shr} = C_{gd6} + C_{gs4} \tag{3.59}$$

$$V_{itm} = \frac{C_{GI4} + C_{gd1} + C_{gd4}}{C_{GI4} + C_{gd1} + C_{gd4} + C_{gd6} + C_{gs4}} \times VDD \tag{3.60}$$

$$V_I = \frac{VDD - |V_{TP}| + \sqrt{\frac{\beta_n}{\beta_p}} V_{TN}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{3.61}$$

Now, if the gate capacitance of the following inverter I4 is small, the final voltage (V_{item}) at node *itm* can fall below the the threshold voltage of the inverter V_I, is given in Equation 3.61, and the DPFD will give a false result. This problem can become severe if the threshold voltage of the inverter moves higher as a result of process and temperature variation. This problem holds true for both internal high impedance nodes of the DPFD, given by Figure 3.29.

The proposed new DPFD circuit, shown in Figure 3.30, alleviates these limitations of the

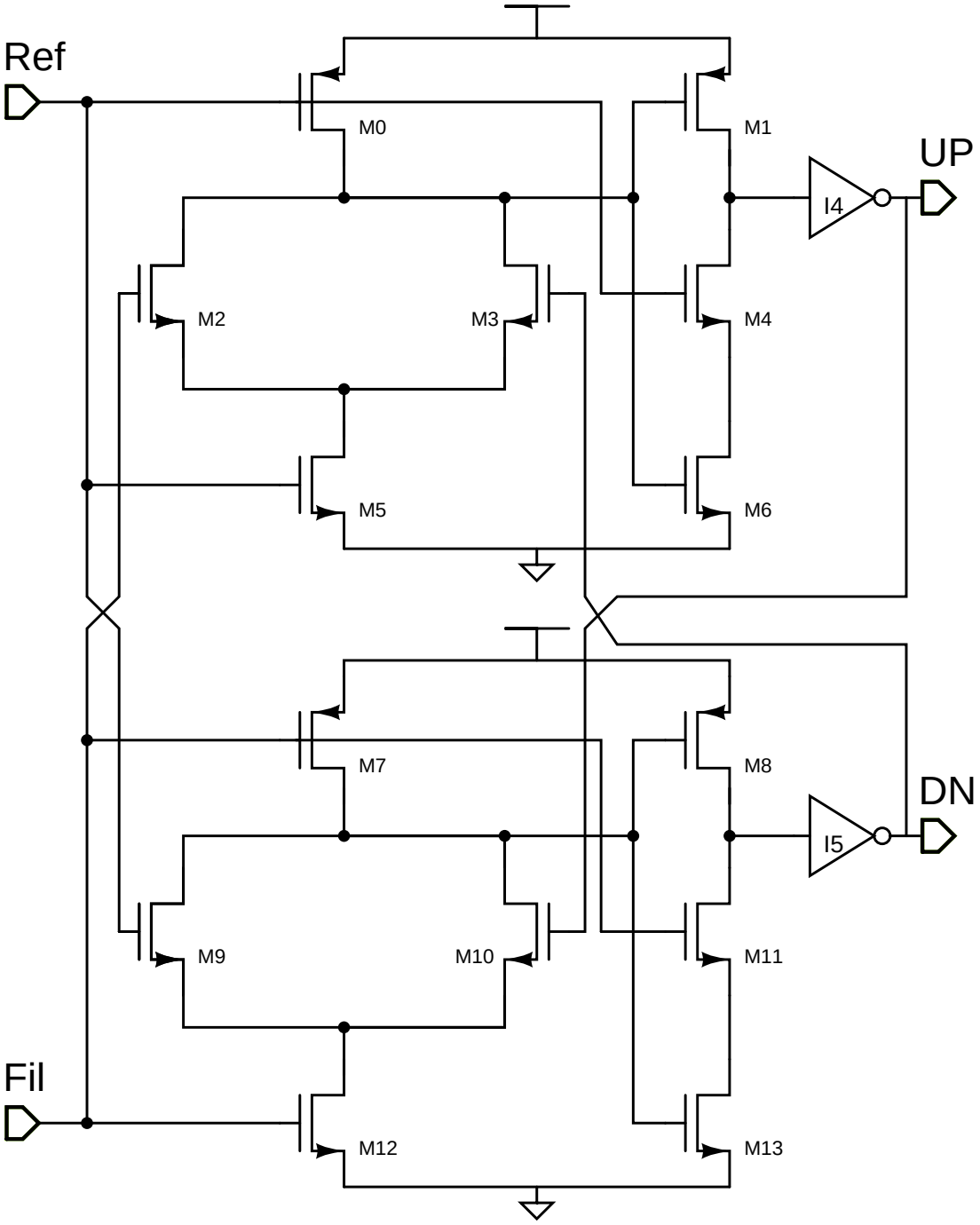

Figure 3.29: A digital phase frequency detector based on dynamic DFF.

above DPFD circuit. First, it divides the clock frequency of the input signal by half,making both input signal, have a 50% duty cycle. The phase information of the signal is kept only in the zero crossing.

Second, the transistors M4, and M11 are driven by two inverter-delay delayed input signal. The delayed input *ref(fil)* signal reaches the gate of transistor M4 (M11), at the same time or after the signal that drives the gates of transistors M1 (M8) and M6 (M13). This synchronization in signal timing helps preserve the precharged charge at the gates of the output inverters, *I4* and *I5*, and increases the sensitivity of the DPFD by fourfold.

The sensitivity plot of the DPFD circuit is shown in Figure 3.31. The proposed circuit has a deadzone of only $\pm 0.3^o \approx \pm 10$ pS in simulation and $\pm 1^o \approx \pm 40$ pS in post-layout simulation. From Equation 3.57. This will give rise to an error of ± 1 in the final Q-value of the filter.

3.7.2 Digital Integrator

The output of the charge-pump circuit controls the counting direction of the digital integrator. The output of the charge-pump (V_c) goes to the positive (negative) rail for negative (positive) phase error. This flip in sign of the phase error to the output of the charge-pump circuit creates the negative feedback in the loop. The digital integrator is a 5-bit up-down counter. It counts forward if the control signal is *high* ot backward otherwise. A block diagram of the digital integrator is shown in Figure 3.27.

A schematic diagram of the digital integrator and the signal bit charge-pump circuit is given in Appendix C. A digital integrator allows the loop to store the final control voltage in registers. In this implementation, the digital integrator limits the accuracy of the loop. The LSB of the the integrator corresponds to a $\pm$ 1 change in quality factor of the filter. Thus, a bit digital integrator can tune the quality factor of the filter by ± 16.

A higher-order digital integrator or an analog integrator can be used to achieve higher accuracy. An analog integrator uses the capacitor to store the tuned controlled voltage of the loop. An integrated capacitor in modern IC processes has a large leakage current beacuse of oxide imperfection and impurities. Therefore, in the case of the analog integrator,

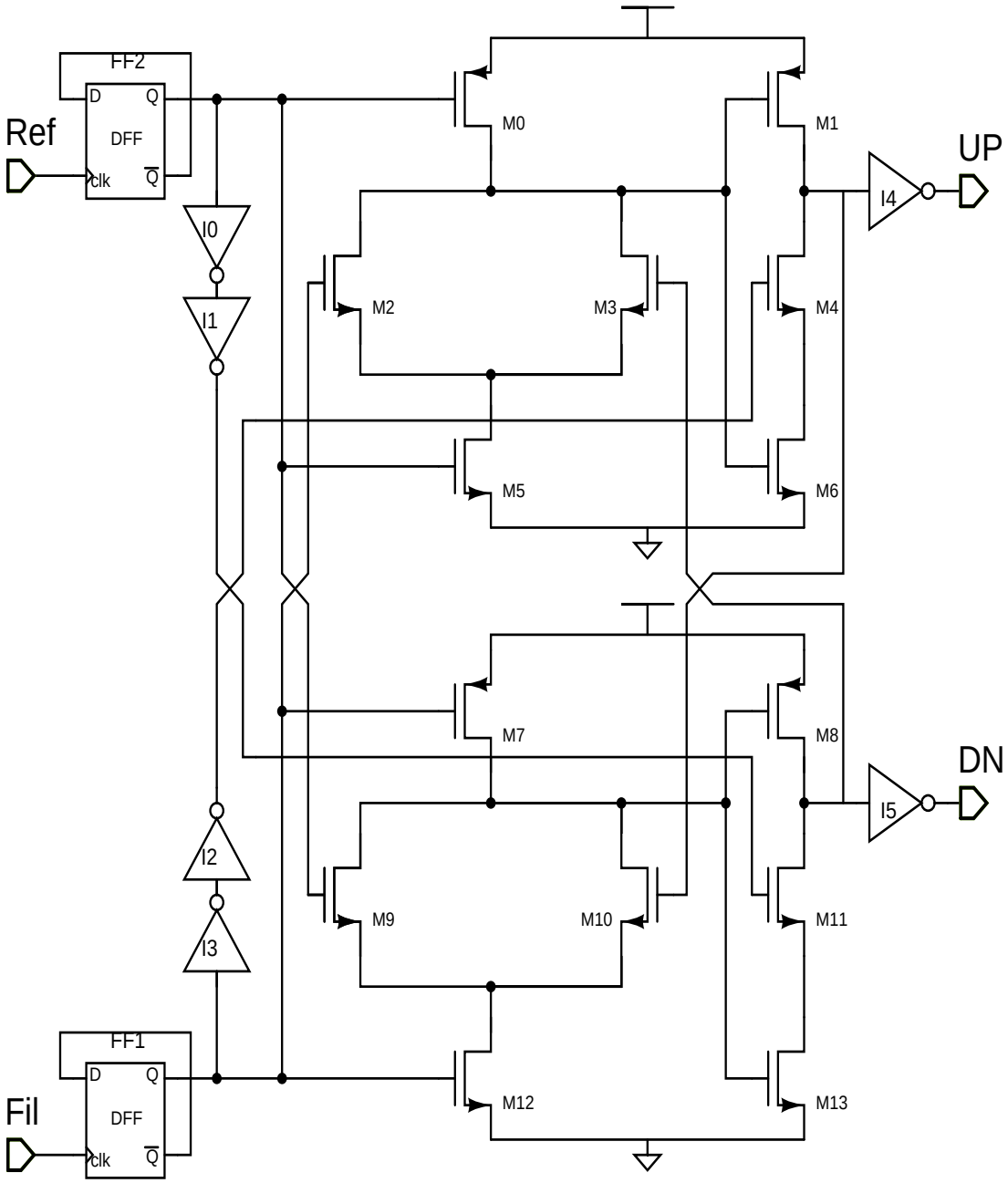

Figure 3.30: An improved DPFD based on dynamic DFF.

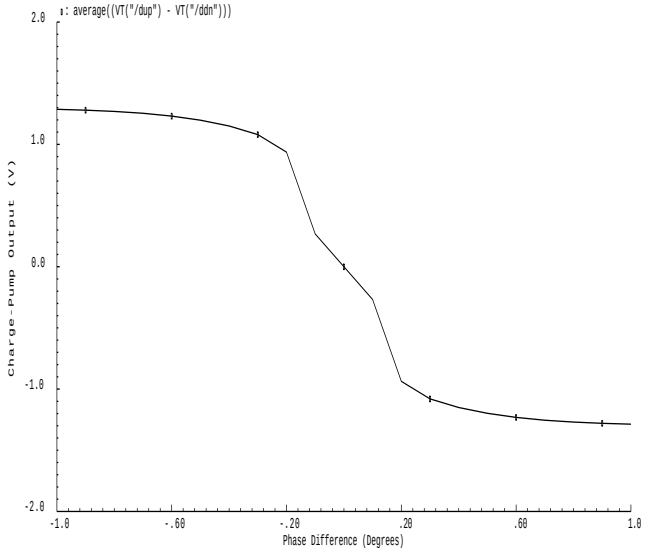

Figure 3.31: The deadzone simulation results of the improved DPFD.

the filter needs to be tuned continuously or periodically to avoid any large quality factor drift. Another solution could be to use a high-Q external components.

3.7.3 Delay Network

The prototype biquad filter is implemented using a differential architecture to gain common mode noise immunity, to improve its linearity, and to achieve a large dynamic range, whereas the rest of the QLL tuning scheme is implemented single-endedly to reduce the power consumption. Therefore, the first-stage delay network is a differential to a single ended amplifier shown in Figure 3.32.

As given in Section 3.6.3, delay mismatch between the reference and the filter output signal causes a constant Q-error in the quality factor of the filter. Therefore, a similar delay network, shown by Figure 3.32, is added to both the reference signal and filter output. From Section 3.6, the reference signal (ϕ_{ref}) requires an extra delay of 45^o; therefore the delay network has twice the capacitors shown in Figure 3.32.b. These capacitors are placed in close proximity in a common centroid structure.

The first stage of the delay network amplifies the differential output signal and converts

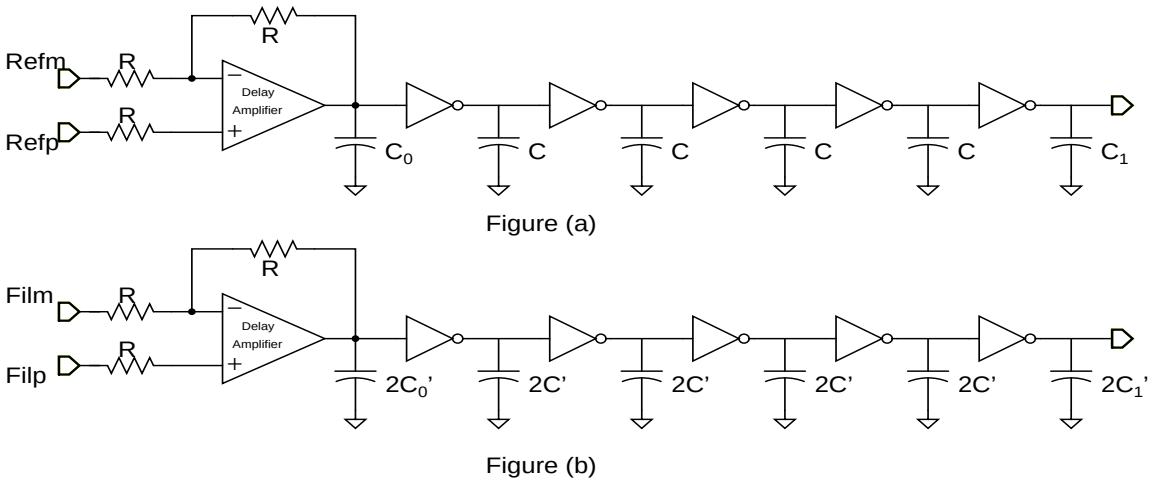

Figure 3.32: a: Delay network for the ϕ_{fil} signal; b: Delay network for ϕ_{ref} signal.

it into a single-ended signal. The amplification also helps convert the sinusoidal output signal to a digital signal, so that a digital DPFD can be used. The amplified signal feds through several inverters and capacitors, which act as an RC delay. The *on* resistor of the inverter acts as R of this delay network. The first-stage amplification is critical for low power consumption, as a slow moving input will keep both device of the inverter on for longer period of time. Another advantage of using a differential amplifier as the first stage is that it makes the delay network insensitive to the common mode voltage of the filter.

A schematic of the first-stage amplifier is shown in Figure 3.33. It is a single-stage differential amplifier with an HBT input stage and MOS output stage. An HBT differential pair gives large input transconductance and a MOS output stage gives wider swing and large output resistance; together they result in a large gain-bandwidth product. The necessary delay is achieved by feeding the signal through several inverters loaded with poly-poly capacitors. The *on* resistance of the inverter defines the R of the delay cells. Poly-poly capacitors are added at the intermediate stage to minimize the effect of parasitic capacitance on the total delay.

3.7.4 Tuning Response

As discussed in Section 3.2, an on-chip continuous-time high-Q bandpass filter is vulnerable to oscillation. Therefore, in this implementation the biquad filter is powered on at low

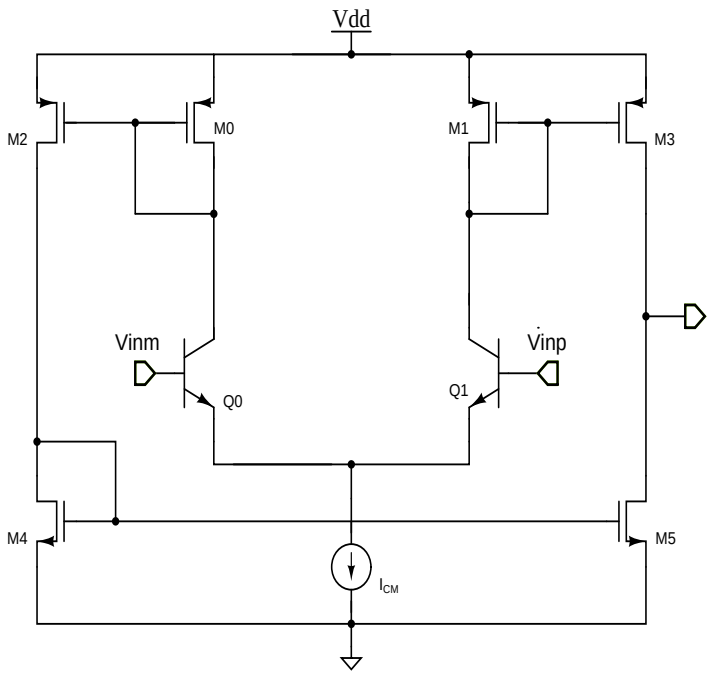

Figure 3.33: Differential input to single-ended output delay-amplifier.

quality factor, so that even with process and environmental variation, it never behaves like an oscillator. The biquad starts at a quality factor of 16, which is represented by the counting sequence *'00000'* of the digital integrator. The tunable part of the G_{mq} transconductance of the biquad filter is designed such that an increment in counter sequence causes an equal increment in the quality factor of the filter. Thus, the sequence *'11111'* represents a quality factor of 48 for the biquad filter.

Once the QLL scheme changes the value of G_{mq}, it has to give the biquad filter sufficient time to respond to its new G_{mq} value. The *16:1 divider* in the QLL system divides the amplified 3 dB frequency by 16 times and generates the clock signal for an up-down counter. The divided clock signal gives ∼160 nS to the filter to respond to its new Q value. It seems to work well in simulation. A faster counter clock does not give enough time for the filter to respond to the changes and increases hysteresis in Q. In other words, it increases the the gain from integrator, so in turn the loop bandwidth gives small lock time and large hysteresis.

The overall response of the QLL tuning scheme is shown in Figure 3.34. The figure

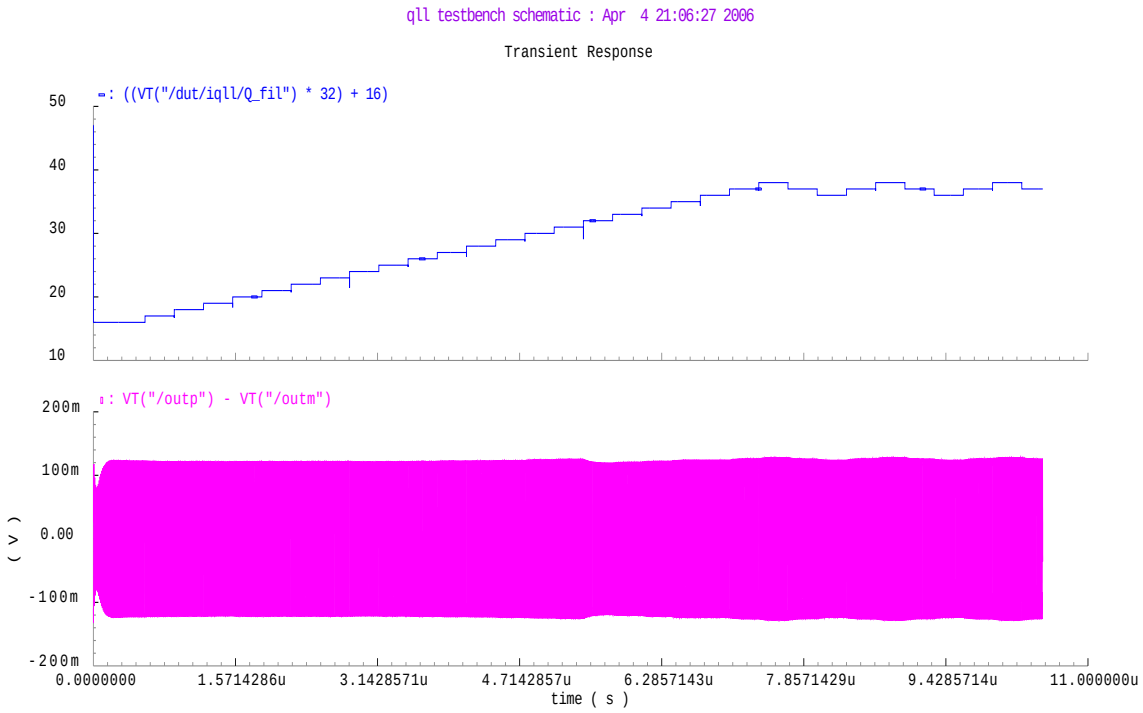

Figure 3.34: Transient response of the QLL tuning scheme.

shows the value of Q and the output transient response. The output envelope of the filter is varing because the gain of the filter varies between 19dB to 23dB for different quality factor values of the filter. The quality factor of the filter has a hysteresis of $\pm$ 1 around the desired Q value, which is 37 in this simulation.

3.8 Design for Testability

The prototype biquad filter, shown in Figure 3.15, has an integrating capacitor at its output node. Therefore, an on-chip driver amplifier is used to isolate the bond wire inductance and load capacitor from the integrating capacitors. Also, the prototype filter is constructed using OTA stages, which cannot drive a voltage output to a low resistive load. This strengthens the need for an on-chip driver. It is difficult to make a differential driver with low output impedance in CMOS processes; therefore two single-ended drivers are used to drive the differential signal.

In order to measure the linearity performance of the prototype filter, the linearity and the gain-bandwidth product of the driver amplifier are kept larger than the filter (DR =

66dB, $\omega_0 = 100$MHz) for a given fixed-light differential load (R_L= 300 Ω and $C_L = 2$ pF). It is easier to achieve a higher linearity from an amplifier with a light load and smaller signal. The on-chip driver has a linearity of 80 dB for 0.5 Vpp signal, which is a differential 2 Vpp signal. A schematic diagram of the on-chip driver is shown in Figure 3.35.

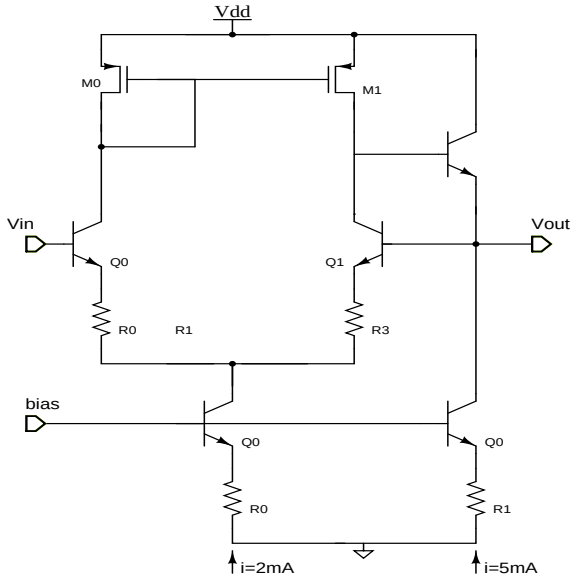

Figure 3.35: On-chip resistive driver.

The maximum differential output signal from the filter is 3.6 Vpp, therefore an on-chip resistive divider with a total resistance of 5K Ω is used to cut the signal strength in half. This on-chip load resistance also emulates an input impedance of a typical ADC in a receiver signal path. A differential load resistance of driver 300 Ω means a single-enged load of 150 Ω, which is 100 Ω in series with a measurement instruments. Hence, there is a total loss of 6 dB of signal from the filter output to the output pin of the prototype chip.

The driver amplifier consumes 5m A each. To quantify the performance of the filter, a separate power supply pin is used to drive the driver amplifiers.

3.9 Floor Plan and Layout of Biquad Filter

3.9.1 Identification of Matched devices

From the schematic of the improved transconductor circuit shown in Figure 3.3, the transistor pairs Q0-Q1, Q2-Q3, Q4-Q5 and Q6-Q7 needs critical matching; therefore these pairs

are laid out in a cross-coupled common centroid structure, as shown in Figure 3.36. All these devices are laid out in close proximity, as devices Q2-Q5 and Q0-Q1 with Q6-Q7 also need to match to a good extent.

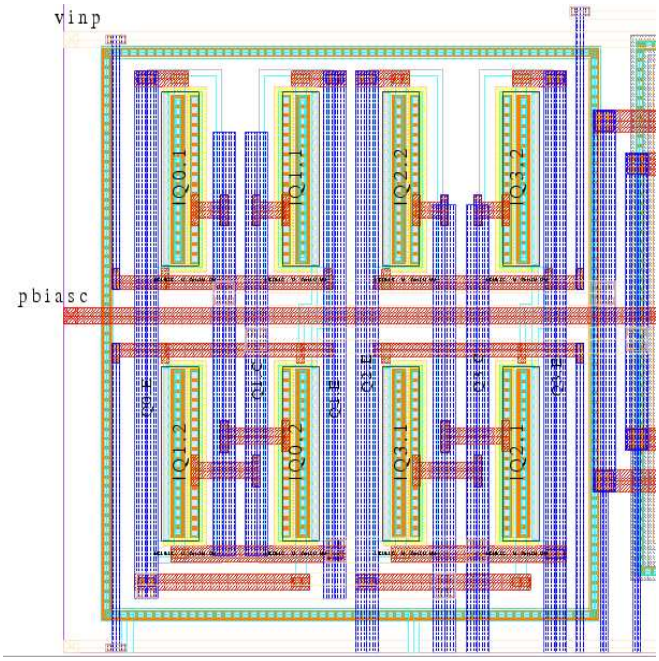

Figure 3.36: Common centroid layout for the input differential pair.

The current sources M2-M4, M3-M5, M4-M6, and M7-M9 are only laid out in close proximity using an inter-digitated structure, as they are big and inter-digitated gives a first-order of matching. Two large device laid out in close proximity match better in a modern IC process [99]. Devices M0 and M1 are small; therefore cross-coupling will only make the device further smaller, so they are also laid out using an inter-digitated structure.

3.9.2 Parasitic Sensitive Nodes

The connections to the high-impedance node inside the transconductor are made with care to minimize any parasitic capacitance at that node. Further, the any parasitic at the output of the transconductors, at nodes *itmp* and *itmm*, and at the outputs of the filter will move the pole frequency of the filter and will cause a shift in filter parameters. Therefore, these connections are made with top metal lines (metal 5) and there are no metal lines or devices beneath them or on either side of them. These output lines are placed in the center of the

chip, as shown in Figure 3.38. The metal line running parallel to these lines are power buses and bias signal, as they are the quietest signal of the circuit.

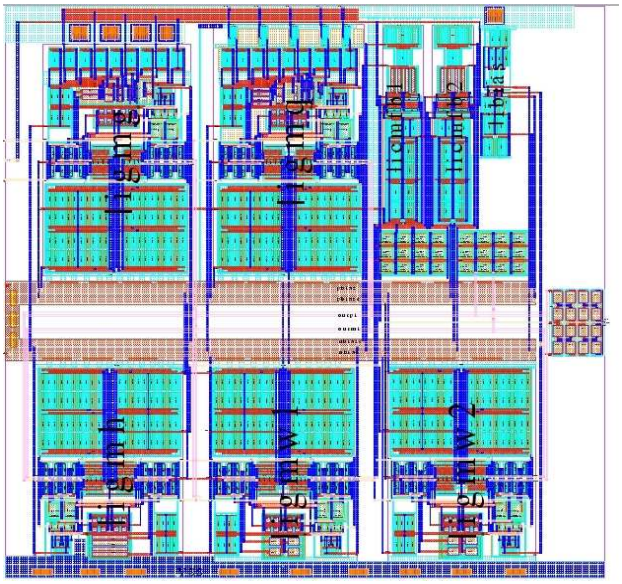

Figure 3.37: Layout of the outputs of filter.

3.9.3 Transconductor and Biquad Layout

The layout of an individual transconductor is shown in Figure 3.38. Here, the PMOS current sources isplaced on the top and no metal is routed over the gate devices. The cascode devices sit in the center of the layout. Since mismatch in cascode devices does affect the amount of the current in the current sources, few DC signals are routed over these devices to reduce the size of the layout.

The layout of the biquad filter is shown in Figure 3.39. The parasitic sensitive node, such as the output of the filter, is laid out in M5 with 8 μm clearance on either side and no metal beneath them. They are also in the middle of the chip for symmetry. The transconductors of the biquad are placed such that their interconnect lengths are small.

The integrating capacitors C0 and C1 and the 5K of the load resistance are laid out in a matrix structure for matching. The capacitors are laid out with six fingers each, in a 4x3 matrix, and resistors are laid out in a 4x4 matrix, as shown in Figure 3.40 and Figure 3.41, respectively.

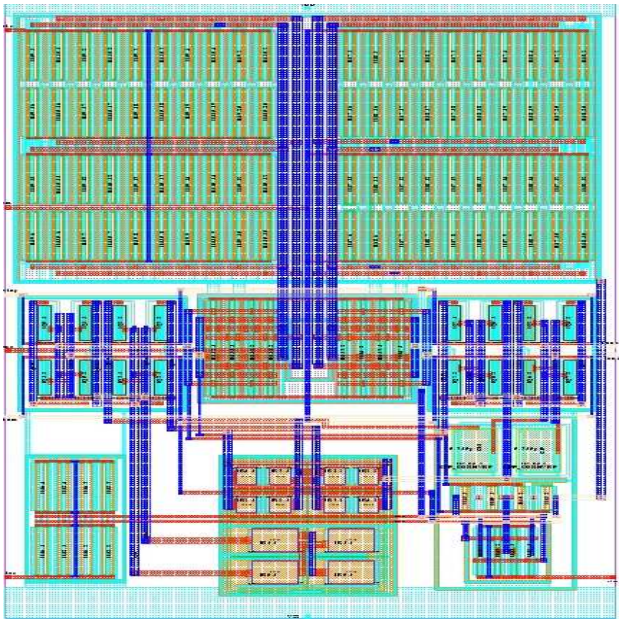

Figure 3.38: Layout of the individual transconductor.

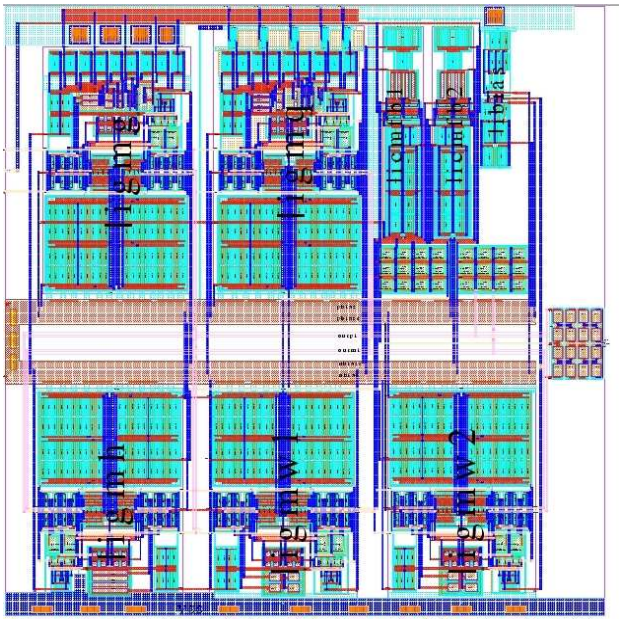

Figure 3.39: Layout of the biquad filter.

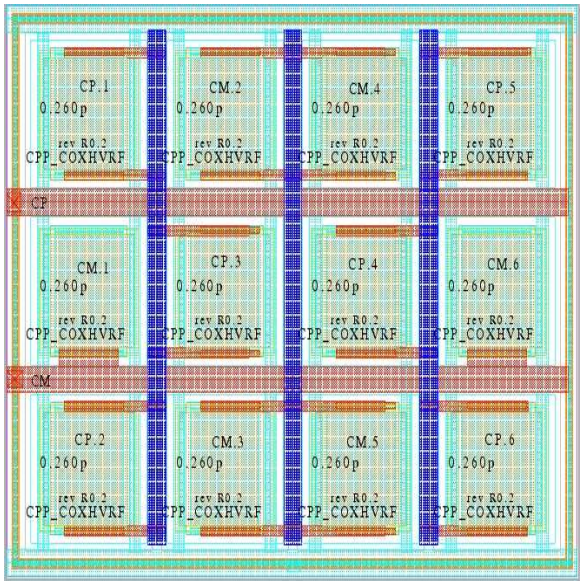

Figure 3.40: Layout of the integrating capacitors of the biquad filter.

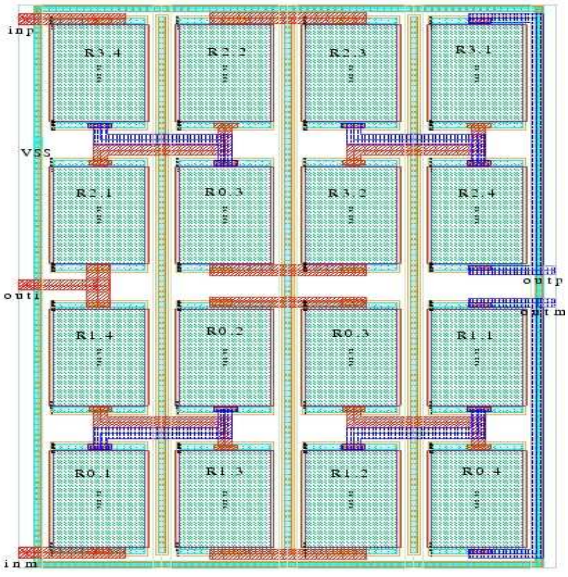

Figure 3.41: Layout of the load resistor of the biquad filter.

This test-chip has two on-chip drivers to isolate the filter output from pin capacitance and to drive an external load (150 Ohms). The maximum output signal signal ended is $\sim$ 500 mV, which corresponds to a maximum output current of 33 mA for 150 Ohms of load. The device placement and metal connections of the driver output are done in diamond shaped structure as to minimize capacitance and at the same time have a large drive capability, as shown in Figure 3.35. These output nets contains metal-3, metal-4, and metal-5 in parallel.

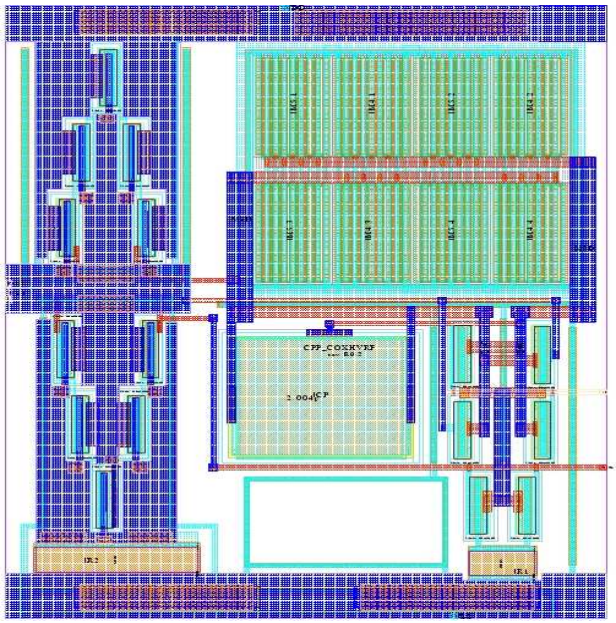

Figure 3.42: Layout of the on-chip driver.

The layout of the overall filter is shown in Figure 3.43. It includes the biquad filter, on-chip drivers, and ESD structure. The ESD structures are embedded in the perimeter as a ring with pads.

3.9.4 QLL tuning scheme and Tunable Transconductor

The layout of the tunable resistors is shown in Figure 3.44. A switch is connected in parallel to each tunable part of the resistor. These switches are controlled by the digital integrator output and are placed beneath the gm block of an inverter driving their gates.

Since the DPFD and digital integrator are digital blocks running at a clock speed 100 MHz, which is well below the *ft* of the devices in this process, a standard CMOS cells are

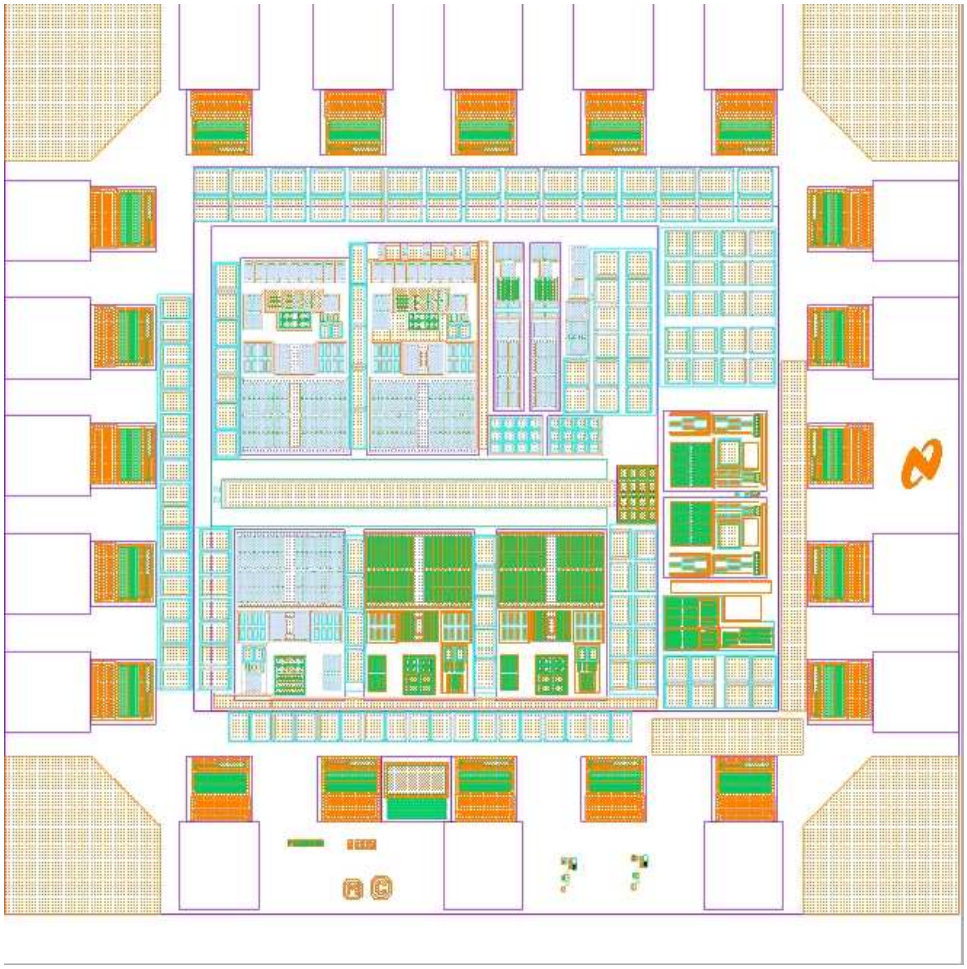

Figure 3.43: Layout of the test-chip.

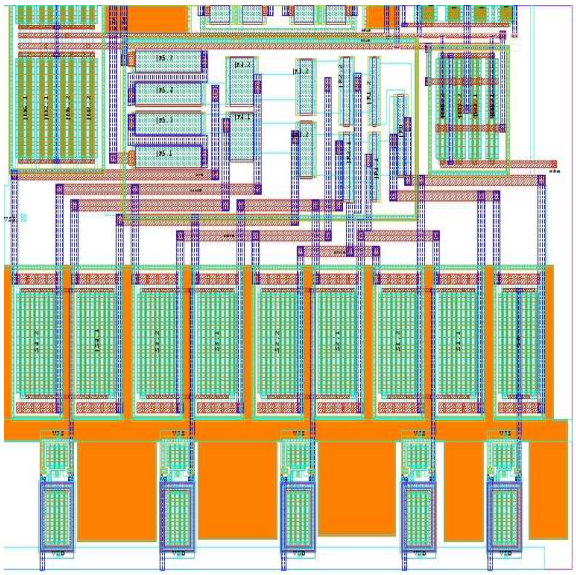

Figure 3.44: Layout of switches of the tunable transconductor.

used. The overall layout of the test-chip and die photograph are shown in Figure 3.45 and Figure 3.46.

There is a 120 pF of decoupling added on the die in the open space around the circuit. The decoupling capacitors are also sprinkled on the die at any empty space so that the transient current of an individual current can be supplied.

3.9.5 Pin Diagram

The pin diagram of both test-chips, biquad filter, and QLL-tuning scheme, are kept the same to reuse the PCB, and it is shown in Table 3.3. The inputs are kept on the left and quiet power supply signal is placed next to them. The outputs are kept on the right and the remaining pins are distributed for the control bits of the QLL tuning scheme.

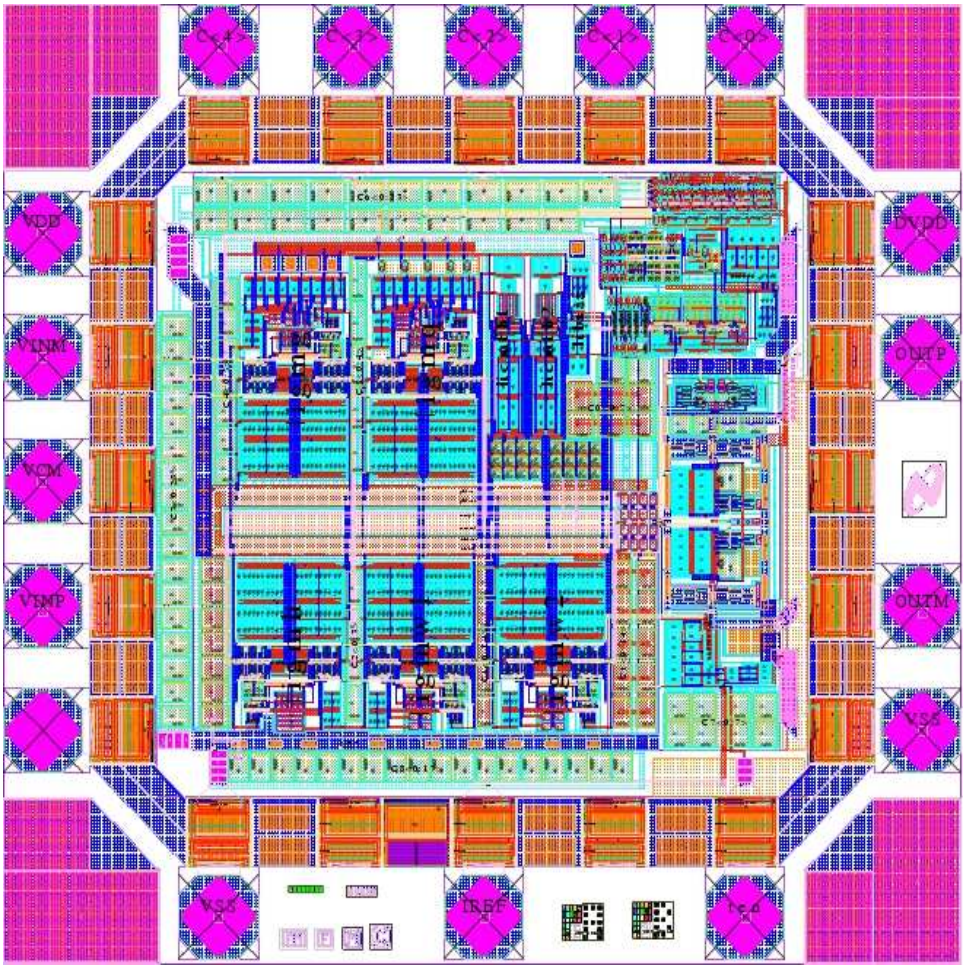

Figure 3.45: Layout of the QLL tuning scheme.

Table 3.3: Pin names and numbers for the test chips.

Pin Number	Pin Name	Pin Number	Pin Name
1	C2	9	Iref
2	C3	10	VSS
3	C4	11	VSS
4	AVDD	12	OUTM
5	VINM	13	OUTP
6	VCM	14	DVDD
7	VINP	15	C0
8	VSS	16	C1

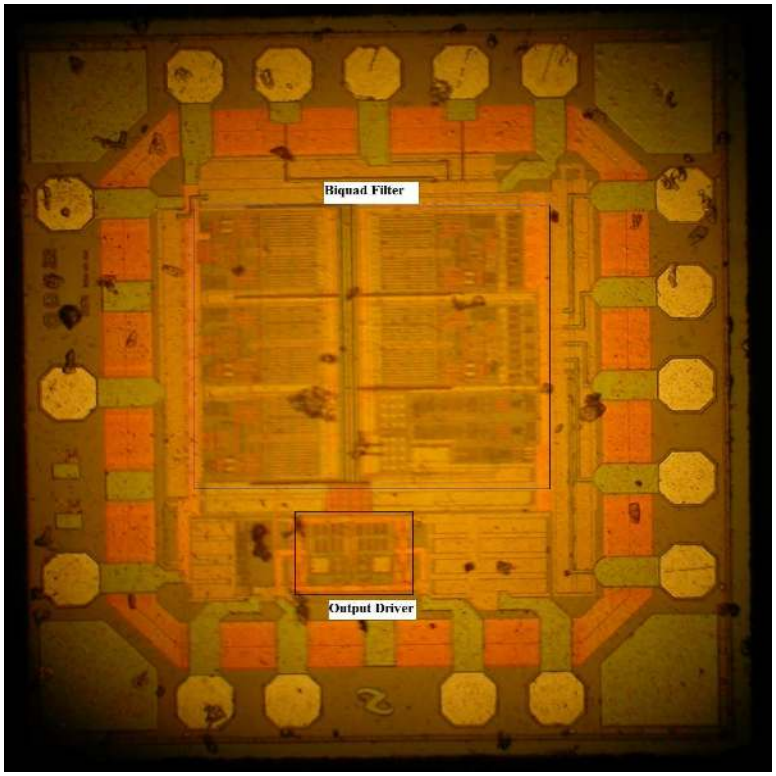

Figure 3.46: Micro-photograph of the die

CHAPTER IV

TEST SETUP AND MEASUREMENT RESULTS

4.1 PCB Design

A schematic diagram of the PCB is shown in Figure 4.1. All power supply lines and the common mode signal have a DC decoupling capacitor to ground to provide a low-resistance path to the disturbance. These decoupling capacitors are built using 0.1μF and 0.01μF in parallel. The 0.1μF capacitor provides a low-resistance path for low frequency signal, and the 0.01 μF provides a low-resistance path a decade higher-frequency. Frequencies above these are decoupled using 400 pF on-chip decoupling capacitor. All external passive components are 0402 surface mount devices.

The input traces are terminated with 50-Ohm impedance for matching. This matching is achieved by terminating the differential signal with a 100-Ohm resistor. The differential signals are generated using a center-tapped external transformer (balun). It is a 1:2 transformer. Hence, it provides 6 dB gain to the signal.

There is need for two transformers. The first one converts the single-ended input signal to the differential and the second converts the differential output signal to single-ended signal, so the output signal can be measured using a single ended 50-Ohm matched instrument, as shown in Figure 4.1. Hence, the balun at the input amplifies the input signal by 6 dB, whereas the balun at output attenuates the output signal by the equal amount.

The on-chip driver can only drive a differential load of 300 Ohms. This differential load is emulated by terminating the the output balun with a 150-Ohm single-ended load. The measurement instrument input impedance is 50 Ohms. Thus this load is emulated such that the impedance looking from the device under test (DUT) is 150 Ohms, but the impedance looking from the load is 50 Ohms. This is achieve by implementing this load as a series resistance of 118 Ohms and a parallel resistor of 86 with the instrument, as shown in Figure 4.1. This ensures impedance matching from the source as well as load and gives

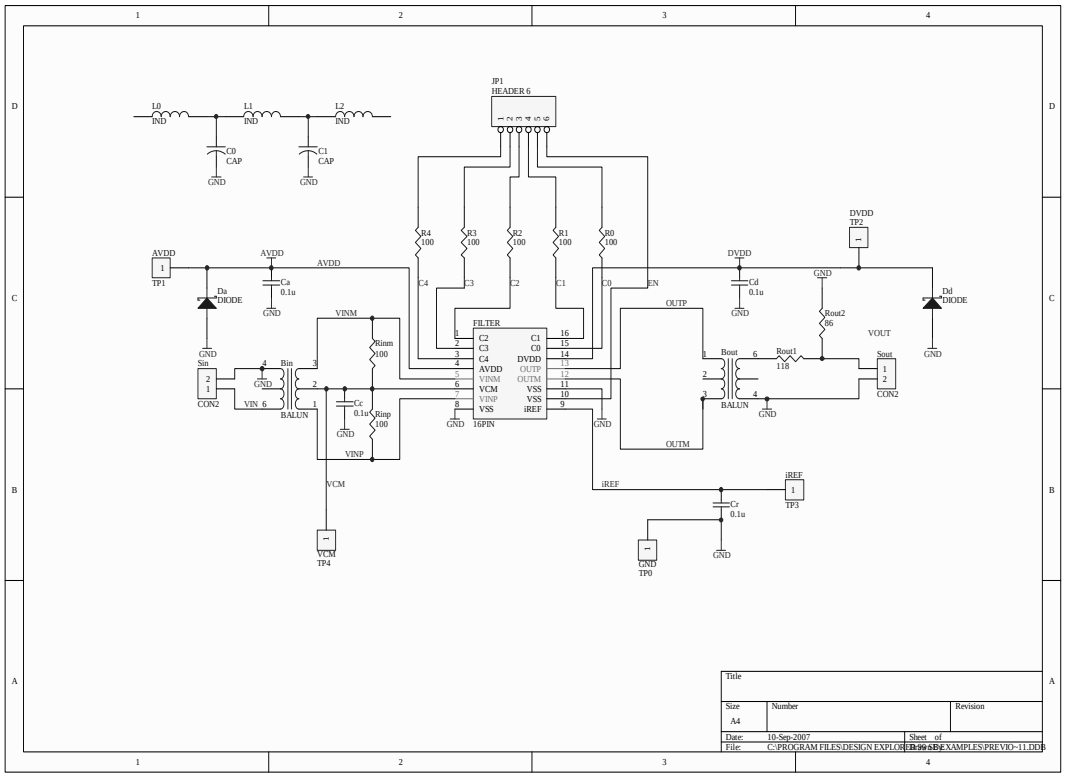

Figure 4.1: Schematic diagram of the PCB to measure the filter.

minimum reflection.

The control bit has a series resistance of 100 Ohms to avoid any accidental damage to the DUT from short . There is separate power supply for the filter and the driver inside the DUT, their individual power consumption can be measured. The input and the output signals are interfaced using SMA connectors for better signal integrity.

4.1.1 Test Board Layout

The layout of the PCB is shown in Figure 4.2. A two-layer PCB is used for cost reasons. The bottom layer of the PCB is used as a ground plane for noise immunity and strong ground connection. The traces between SMA connectors and pins of the test-chip are micro-strip lines with 50 Ohms of characteristics impedance. They are terminated with a 50-Ohm resistor right next to the pin to minimize any refection. The differential input traces are symmetrical and are of equal length.

The common mode signal is connected to the center tap of the balun. Its decoupling

cap is placed right next to the supply hook to minimize the signal disturbance coupling to the PCB. The common mode signal trace is placed such that it has minimum coupling with the input balun and its signals.

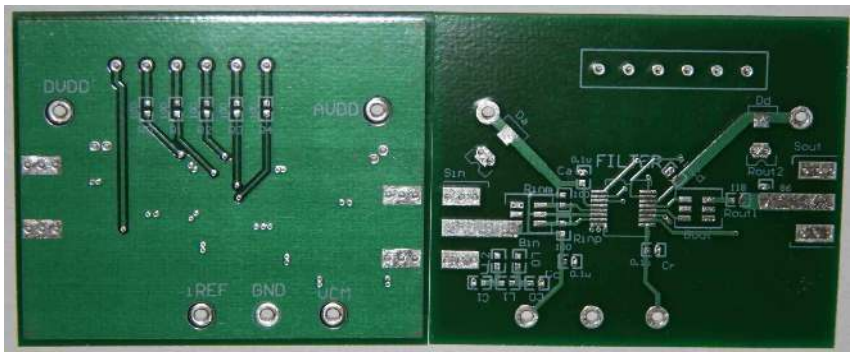

Figure 4.2: The top and bottom plate layout of the PCB.

The output traces from the pin of the test-chip to balun are also micro-striplines with 50 Ohms of characteristics impedance. The center tap of the output balun is left floating as the common voltage of the output is determined by the CMFB circuit. The traces between the output balun to the SMA connector is 50 Ohms of impedance and is kept small to minimize the capacitance.

The control-bit traces are kept at the perimeter with minimum trace width to reduce the coupling capacitor from the control bit to the signal. The power supply traces are kept wide and their decoupling capacitor is placed right next to the hook to minimize any disturbance coupling to the ground plane. All 0402 surface mount passive devices (SMD) are used for self-resonant frequency small parasitic capacitance. The PCB dimension is 1.8" x 2.2".

4.2 Measurement Results

The measurements are made at room temperature in a single-ended environment, where, wire loss and instrument-artifacts are calibrated to cancel their effects.

4.2.1 Balun Response

The frequency response of the balun is measured by replacing the DUT with a pair of parallel metal wires, thus by creating a short between the input and output of the DUT, as

shown in Figure 4.3. The resistive divider at the output (118+86——50) introduces a loss of 13.55 dB. The loss from the balun is measured at various signal amplitude is shown in Figure 4.4. The average loss from the balun because of its non-ideality is 0.64 dB.

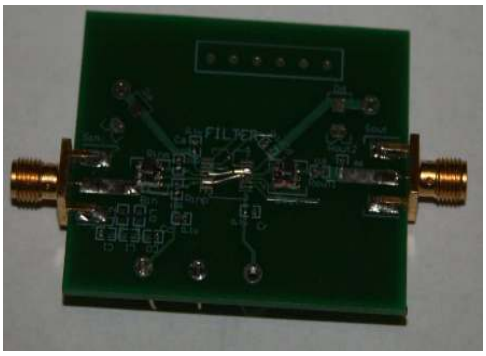

Figure 4.3: The modified PCB to measure the response of the balun.

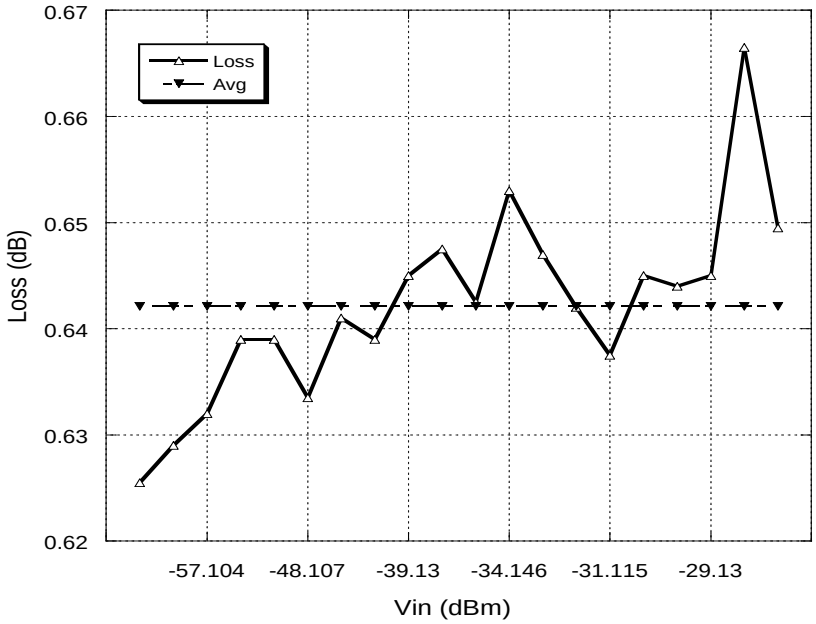

Figure 4.4: Measured loss from the balun.

At input, the balun introduces a total gain of 5.36 dB (= 6 - 0.64) and at output it introduces a total loss of 6.64 dB. Hence, there is total loss of 20.83 dB (= +6-0.64-6-6.64-13.55) in the measurement setup.

Since these external resistors are built only with ± 1% precision, the attenuating pad of 14.55 dB loss and 50-Ohm characteristics impedance are used at the input and output

of the PCB to achieve better impedance matching and minimize the signal refection. This increases the accuracy of the measurements.

4.2.2 DC Setup and Power Dissipation

The power supply voltage is 3.3 V and common mode voltage is set to 2 V. The DC current source is set to 200 μA as design in simulation. As simulated, the approximated total supply current is 20 mA. The supply current is close to very close to simulation because input is a bias current, which is mirrored using a cascoded structure to generate the necessary internal current. Since a cascoded current mirror (with ratio of no more than 1:5) can mirror the current with high accuracy, the total current consumption came close to the simulation.

4.2.3 Frequency and Phase Response

The PCB setup for this measurement is shown in Figure 4.5. The input signal is applied through the SMA connector, and the power supply and common mode voltage are held constant using a DC source.

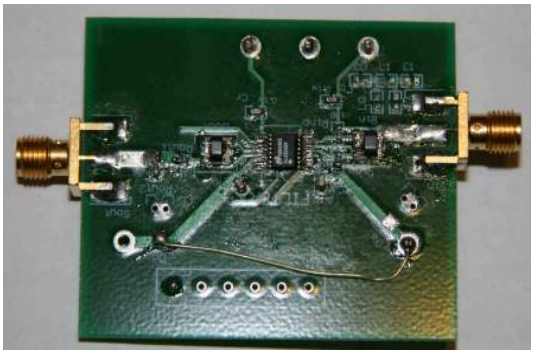

Figure 4.5: The PCB measurement setup for phase and frequency response.

The measured phase and frequency responses of the filter are shown in Figure 4.6. The center frequency of the filter is at 80 MHz. The above plot includes the above loss (20.83 dB) in the measurements. It was designed for 100 MHz but because of unaccounted parasitic of the devices, the center frequency has moved to 80 MHz. The quality factor of the filter is tuned from 20 to 40. It was designed for 16 to 48.

The center frequency of the filter is independent of any variation in the bias current of

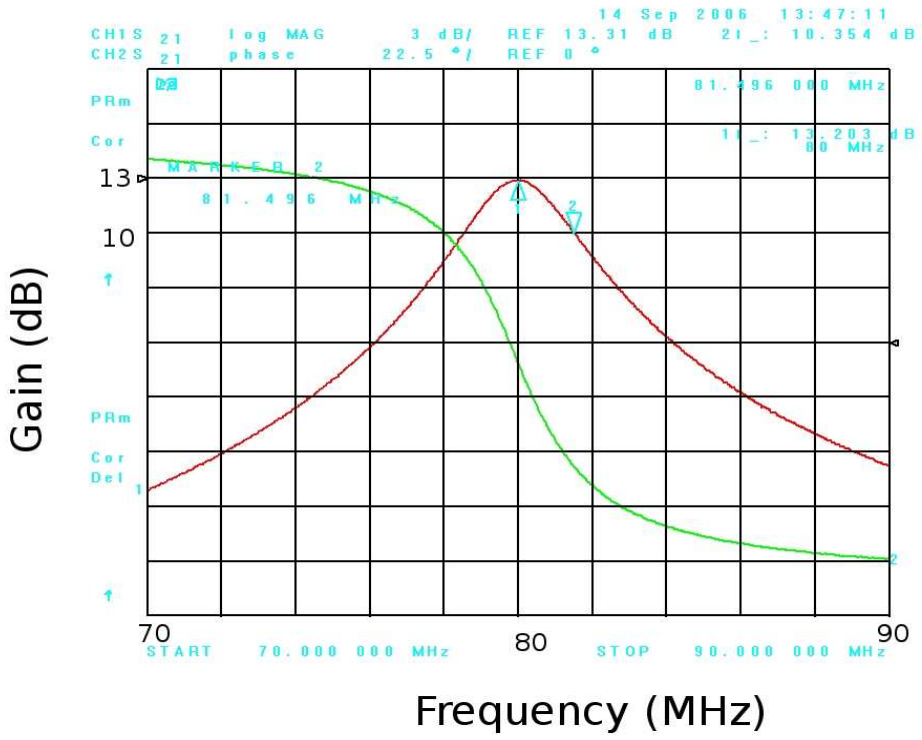

Figure 4.6: Frequency and phase response of the test-chip.

the filter, but it does have sensitivity to the common mode voltage. It has the largest signal handling capacity for common mode voltage between 1.9 V-2.1 V.

4.2.4 Common Mode Rejection

The PCB setup for the CMRR measurement is shown in Figure 4.8. Because of unavailability of a DC-RF coupler, the AC-input signal is added to the common mode voltage using 1 mH series inductor with the DC source and 10 μF series coupling cap in the AC path, as shown in the Figure 4.7.

The coupling cap blocks the DC and provides a low-resistance path for AC signal. The series inductor is a short for DC, but it provides large impedance (open) for the AC signal. Thus, together they ensure that the AC source and DC source do not load each other while still seeing a very low resistance path to the DUT.

The coupled common mode signal is used to drive both input of the filter. The power supply and DC common mode voltage are held constant using a DC source.

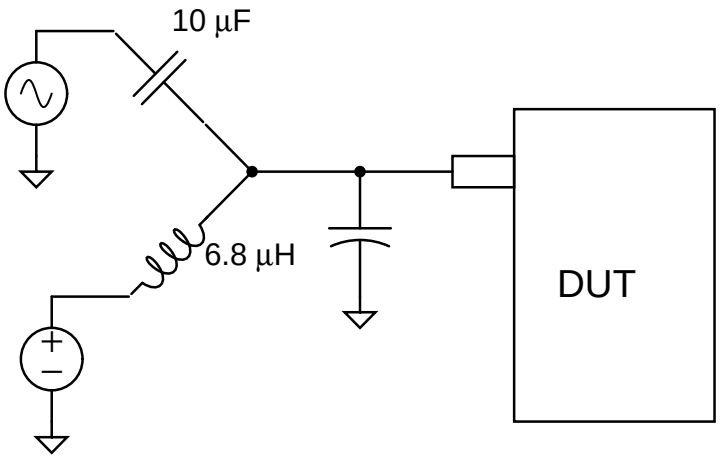

Figure 4.7: A discrete coupler used to add an AC signal over a constant DC voltage.

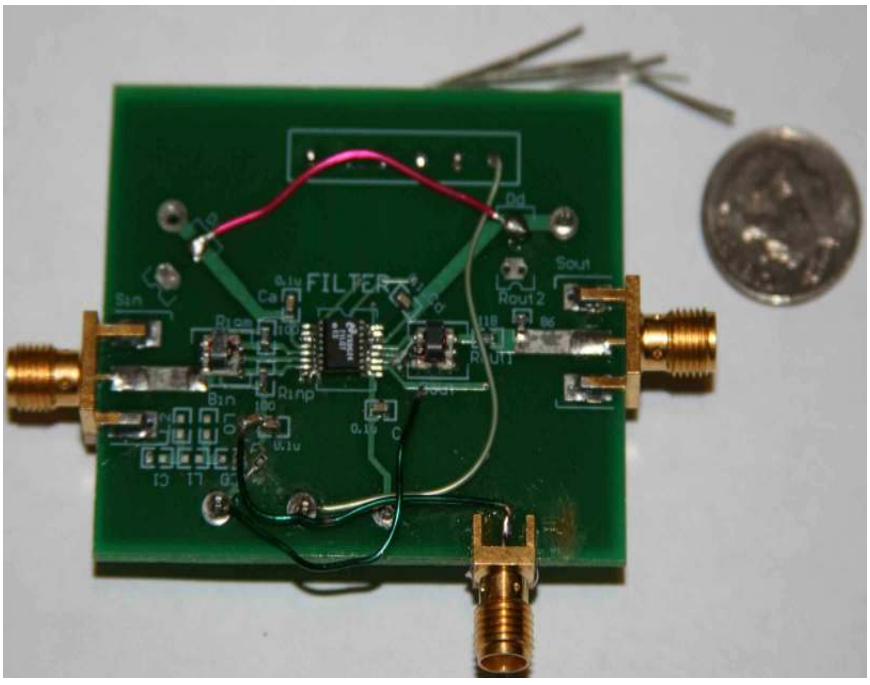

Figure 4.8: The PCB measurement setup for phase and frequency response.

The common mode rejection ratio (CMRR) of the biquad filter is given in Figure 4.9. It is measured with -15 dBm common mode input signal level. At the center frequency of the filter, the CMRR of the filter is -60dB. The above plot is generated by dividing the common mode rejection plot by the magnitude response of the filter.

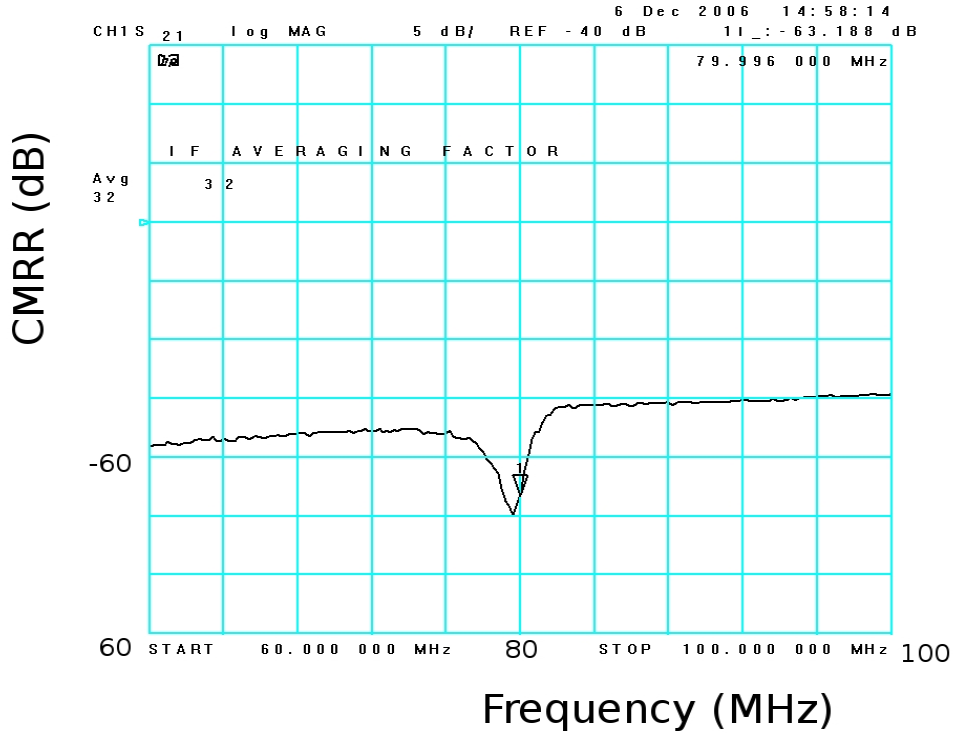

Figure 4.9: Common mode rejection ratio frequency response of the biquad filter.

There is a dip in the CMR plot near the center frequency of the filter, which is due to CMFB circuit having maximum gain near the center frequency.

4.2.5 Power Supply Rejection Ratio

The PCB setup for the PSRR measurement is shown in Figure 4.10. The same coupling method (0.01 mF series capacitor + 6.8 μH series inductor) is used to add the AC signal with the DC power supply. Here, both inputs and the common mode input of the DUT are held constant or connected to the AC ground. The power supply has a DC-common mode and an overriding coupled AC signal.

The power supply rejection ratio (PSR) of the filter is shown in Figure 4.11. This

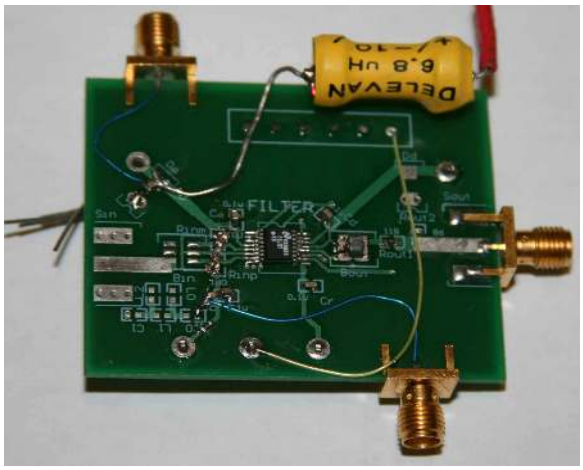

Figure 4.10: The PCB measurement setup for phase and frequency response.

measurement is also made using a -15 dBm sinusoidal signal coupled to the DC power supply voltage. The PSRR of the filter at the center frequency is -42dB. Again, this plot is generated by dividing the power supply rejection plot with the magnitude response of the filter.

The PSRR plot has a peak at the center frequency of the filter. As the power supply signal gets coupled through different gate-to-source capacitance of the MOS current mirrors and they get shaped by the frequency response of the filter, a peaking at the center frequency results.

4.2.6 P-1dB Compression Point

The P_{-1dB} plot of the filter is shown in Figure 4.12. The P_{-1dB} compression point and average gain of the filter are -9 dBm and 19.55 dB. Thus, the total dynamic range of the filter is 65dB. The simulation of P-1dB compression could not be performed because the design filter is a narrow-band system and the simulation crashed because of lack of sufficient memory on the computer.

4.2.7 Intermodulation Distortion

The intermodulation product of the filter is measured with -29 dBm input signal strength. Since intermodulation is a small-signal measurement, therefore the input signal amplitude

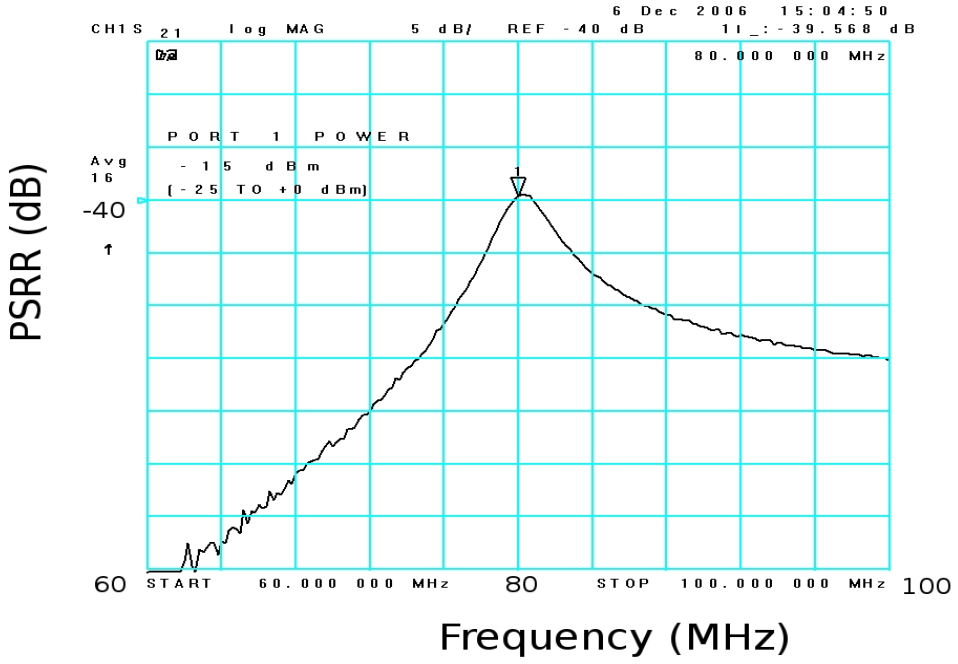

Figure 4.11: Power supply rejection ratio frequency response of the filter.

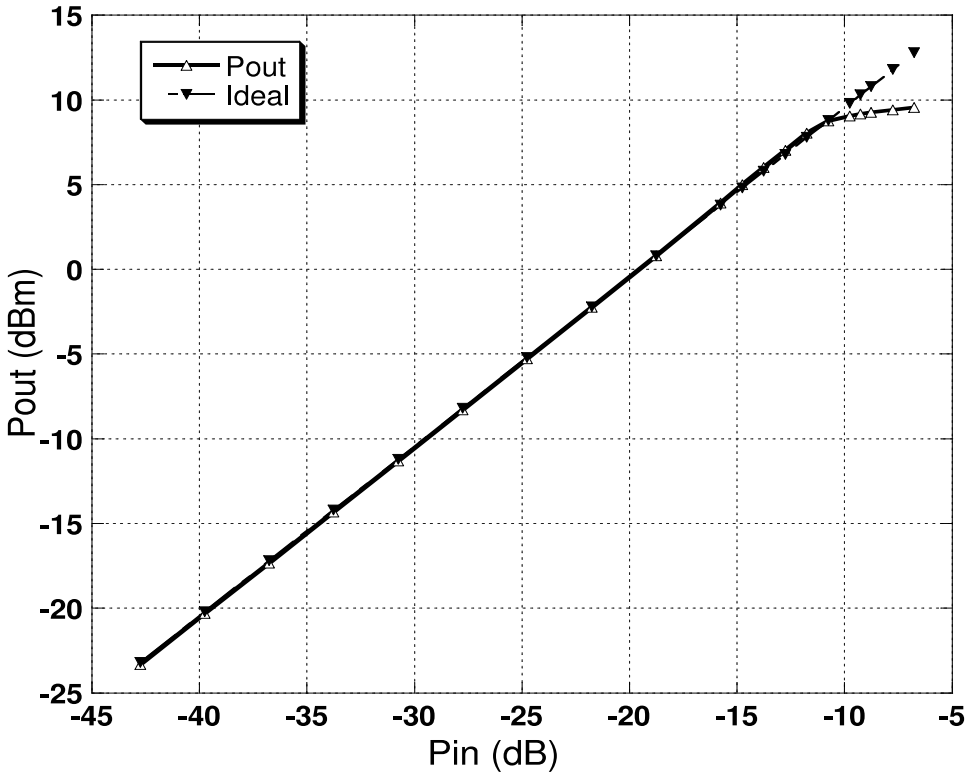

Figure 4.12: The P-1dB compression point of the filter.

is chosen to be 20 dB below the P-1dB point. The measured IMD of the filter is -52.8 dB. Thus, the IIP3 of the filter is -27dB + (-52.8)/2= -2.8 dBm.

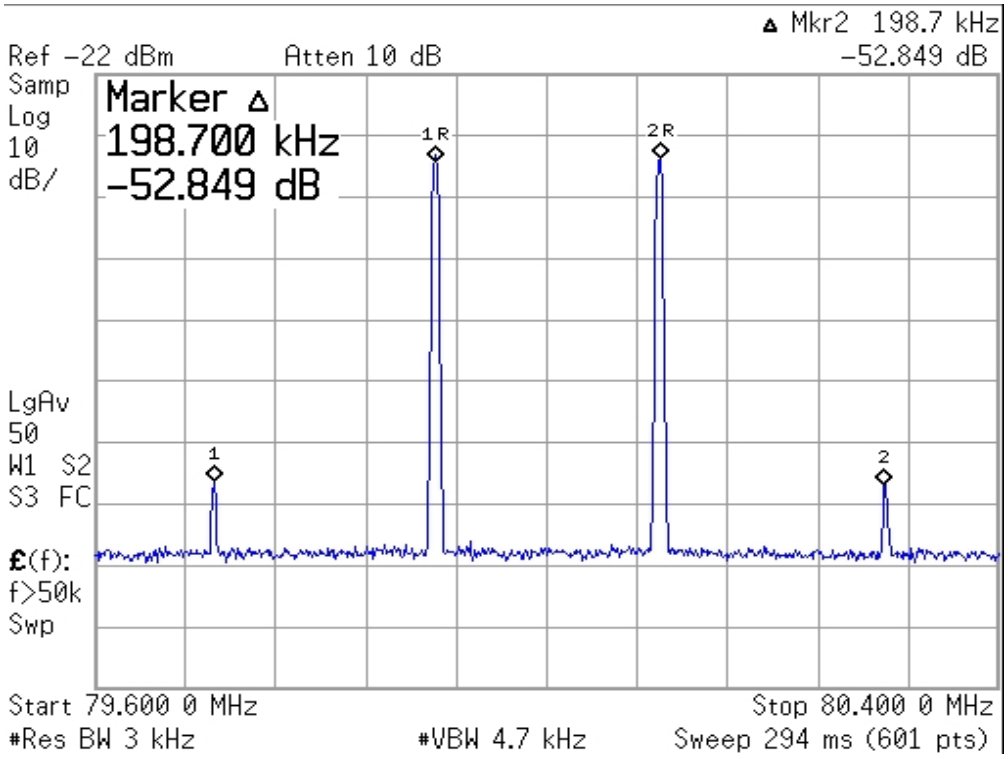

Figure 4.13: Inter modulation production of the filter.

The shown view-graph is generated after a 16-point moving average in the instrument.

4.2.8 QLL Tuning Scheme

Figure 4.14 shows the same filter tuned at two quality factor values. The first quality factor is 20 and the second one is 32. It is tuned by using a combination '00000' to '10100' in the control word. The filter was designed for a tunable quality factor of 16 to 48. The measured quality factor of the filter varies from 20 to 40. The difference from the simulation to the measured values are due to the process variations in the small-step of the Q-tuning transconductor.

4.3 Conclusion

From the two test-chips, this work has verified the linearity performance of the proposed transconductor circuit, an stable 80 MHz filter with 62 dB dynamic range and first time

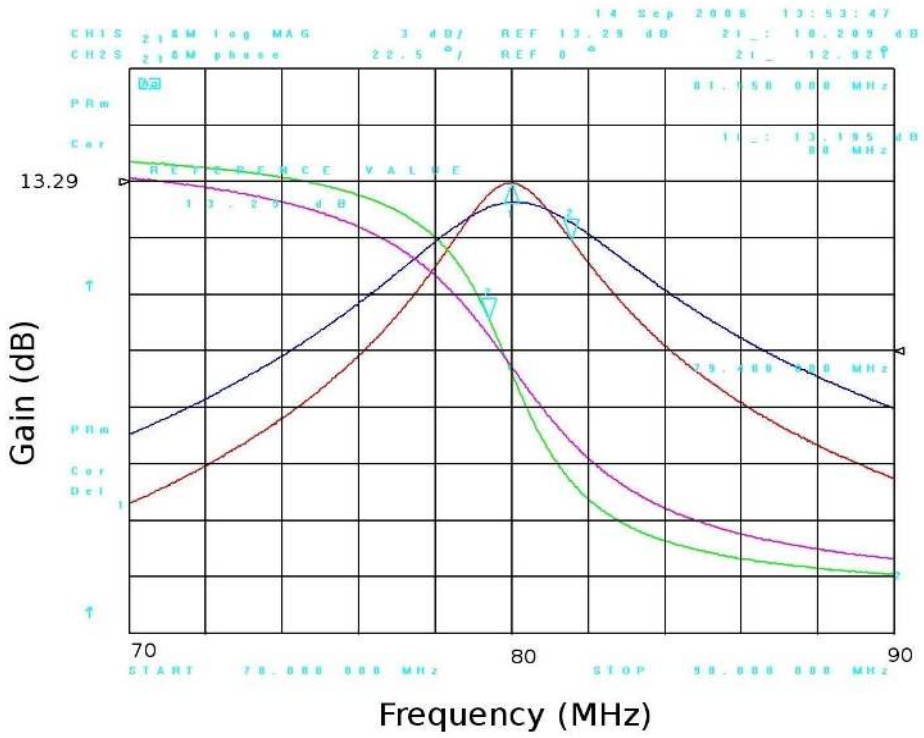

Figure 4.14: Inter-modulation production of the filter.

successful implementation of the new QLL- tuning scheme.

The first test-chip had an 80 MHz bandpass filter with an external tunable quality factor of 16∼44 using an ultra-linear transconductor circuit is developed. The proposed transconductor achieves this high linearity by using local high-feedback loops around the matched diff-pair and current mirrors. The noise optimized biquad structure using the proposed transconductor gives SNR of 45 dB and a DR of 65 dB, which meet the linearity requirements from next generation communication and data converter systems. This filter is designed in a 0.25μm BiCMOS process, and it takes only 0.3 mm^2 of die area.

The second test-chip has an on-chip automatic QLL tuning scheme to tune the quality factor of the filter anywhere from 16 to 44. The power consumption of the QLL tuning is very small as it is all digital block. The die are of the QLL is about 0.04 mm^2 which is close to 15% of the biquad filter area. This meets bothe our objective as to have no-quisceient current and area much smaller than the filter itself. The filter performance of the second test-chip is same as the the first-silicon and filter was tuned automatically from

20 to 32. The measurement results of both test-chips are summarized and given to full fill the objectives of this research.

CHAPTER V

CONTRIBUTION

The prime contributions of this research is to propose, analyze, and implement a reliable quality factor tuning scheme for high-Q, high-frequency, continuous time bandpass filters, while analyzing the limitation of other existing techniques. The mathematical loop analysis of the Q-locked-loop tuning scheme is derived and the loop-behaviour for a typical step input is analyzed. It is proved that a second-order loop is required to tune the quality factor of the filter with zero steady-state error.

The effect of process mismatch on the performance of the QLL tuning-loop is performed, and few preventive steps are proposed to mitigate the affect. It is found that the proposed QLL tuning scheme is nor affected by gain and offset mismatch however a delay-mismatch results in a finite Q-error. The proposed QLL tuning scheme prototype is designed to tune a biquad bandpass filter, and the same operating principal of QLL-algorithm can be applied to tune any kind of monolithic filters.

The accuracy of the QLL scheme is dependent on the dead-zone of the DPFD circuit. Therefore, this research has made a valuable contribution by developing an ultra-low dead-zone, pre -charge based DPFD circuit, which could also be used to design a PLL, delay locked loop (DLL) or frequency synthesizer.

This research has also made a significant contribution by developing a stable, wide dynamic range, high-Q, high frequency bandpass filter to meet the requirements of the several next generation wireless applications. For which, it has further extend the operating-frequency and linearity of the on-chip transconductor circuit. The proposed improved linear transconductor circuit can also be used to design a front-end for FM receiver, high-frequency variable gain amplifier, lowpass and highpass filters.

The summary of all the contributions are listed below.

- Analyzed and developed an ultra wide dynamic range, high-frequency transconductor

circuit.

- Developed and implement a noise optimized, stable, high-Q, high-frequency continuous time bandpass filter circuit using the above transconductor.
- Analyzed and develop an ultra-low dead-zone, pre-charge based digital phase frequency circuit.
- Analyzed the loop-dynamics and accuracy of the QLL tuning scheme. Derive the sensitivity of the over all loop with all the controlling parameters.
- Proposed a mathematical derivation to quantify the effect of process-match on the steady state Q-error.
- Implemented the new and reliable QLL tuning scheme to tune a high-Q high-frequency bandpass filter.

Together, these contributions will provide the integrated on-chip solution to replace the bulky, expensive, and off-chip SAW IF filters of the superheterodyne transceiver or FM receivers.

APPENDIX A

SERIES APPROXIMATION AND EXPANSION

A.1 Laplace transform

The Laplace transform is an integral transform perhaps second only to the Fourier transform in its utility in solving physical problems. The Laplace transform is particularly useful in solving linear ordinary differential equations such as those arising in the analysis of electronic circuits.

The (unilateral) Laplace transform L (not to be confused with the Lie derivative, also commonly denoted L) is defined by

$$\mathcal{L}\left[f(t)\right](s) = \int_0^\infty f(t)e^{-st}dt$$

where f(t) is defined for t≥0 (Abramowitz and Stegun 1972). The unilateral Laplace transform is almost always what is meant by "the" Laplace transform, although a bilateral Laplace transform is sometimes also defined as

$$\mathcal{L}^{(2)}\left[f(t)\right](s) == \int_{-\infty}^\infty f(t)e^{-st}dt$$

A.2 Taylor series expansion

A Taylor series is a series expansion of a function about a point. A one-dimensional Taylor series is an expansion of a real function *f(x)* about a point $x=a$ is given by

$$\begin{aligned} f(x) &= f(a) + f^{'}(a)(x-a) + \frac{f^{''}(a)}{2!}(x-a)^2 + \frac{f^{(3)}(a)}{3!}(x-a)^3 + \\ &\quad \cdots + \frac{f^{(n)}(a)}{n!}(x-a)^n + \cdots \\ e^x &= e^a\left[1 + (x-a) + 1/2(x-a)^2 + 1/6(x-a)^3 + \cdots\right] \end{aligned}$$

APPENDIX B

SMALL SIGNAL ANALYSIS

Small Signal Analysis with R_V

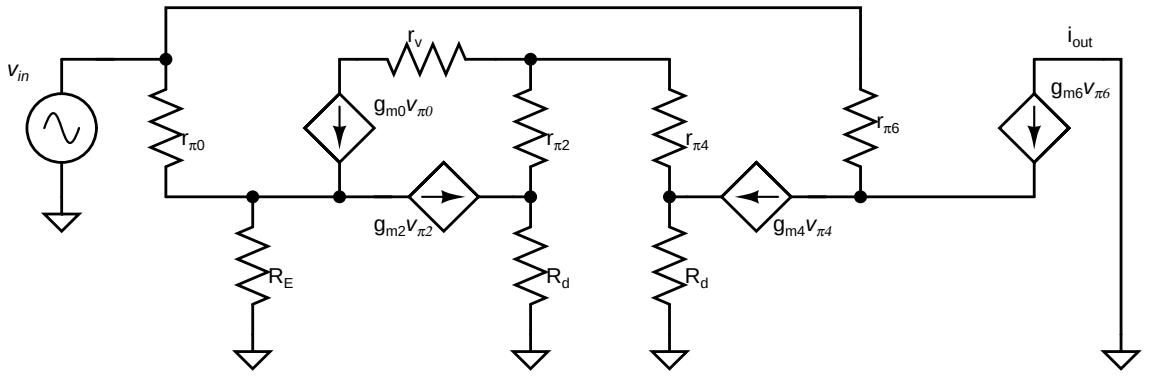

Figure 2.1: Small signal circuit equivalent of transconducto

Node equation at v_{eo}

$$(V_{in} - V_{e0})(g_{\pi 0} + g_{m0}) - V_{e0}g_e + g_{m2}(v_d - v_t) = 0 \tag{2.1}$$

Node equation at v_d

$$-(v_d - v_t)(g_{m2} + g_{\pi 2}) - v_d g_d = 0 \tag{2.2}$$

$$v_d(g_{m2} + g_{\pi 2} + g_d) = v_t(g_{m2} + g_{\pi 2}) \tag{2.3}$$

$$v_d = \frac{g_{m2} + g_{\pi 2}}{G} v_t; \text{where} G = g_{m2} + g_{\pi 2} + g_d \tag{2.4}$$

Node equation at v_t

$$(v_d - v_t)(g_{\pi 2} + g_{\pi 4}) - (v_t - v_{c0})g_v = 0 \tag{2.5}$$

$$(v_d - v_t)(g_{\pi 2} + g_{\pi 4}) = g_{m0}(v_{in} - v_{e0}) \tag{2.6}$$

$$v_{e0} = \frac{g_{m0}v_{in} - (v_d - v_t)(g_{\pi 2} + g_{\pi 4})}{g_{m0}} \tag{2.7}$$

From Equation 2.1, Equation 2.6 and Equation 2.7

$$\frac{g_{\pi 0}(g_{\pi 2}+g_{\pi 4})}{g_{m0}}(v_d-v_t)-\frac{g_{e0}\left\{g_{m0}v_{in}-(v_d-v_t)(g_{\pi 2}+g_{\pi 4})\right\}}{g_{m0}}$$
$$+(v_d-v_t)(g_{\pi 2}+g_{\pi 4})+g_{m2}(v_d-v_t)=0 \tag{2.8}$$
$$(v_d-v_t)\left[\frac{(g_{\pi 0}+g_e)(g_{\pi 2}+g_{\pi 4})}{g_{m0}}+g_{\pi 2}+g_{\pi 4}+g_{m2}\right]=g_eV_{in} \tag{2.9}$$

Node equation at v_{c4}

$$(g_{m6}+g_{\pi 6})(v_{in}-v_{c4})=-gm4(v_d-v_t) \tag{2.10}$$

from Equation 2.9 and Equation 2.10

$$G_m=\frac{i_{out}}{v_{in}} = \frac{g_{m6}}{g_{m6}+g_{\pi 6}}\frac{g_{m4}g_{e0}}{\frac{(g_{\pi 0}+g_e)(g_{\pi 2}+g_{\pi 4})}{g_{m0}}+g_{\pi 2}+g_{\pi 4}+g_{m2}} \tag{2.11}$$
$$= \frac{\beta_6}{\beta_6+1}\frac{\beta_0\beta_4}{(r_{\pi 4}g_{\pi 2}+1)(\beta_0+1+g_er_{\pi 0})+\beta_0g_{m2}r_{\pi 4}} \tag{2.12}$$
$$\tag{2.13}$$

Assuming that $r_{\pi 2}\approx r_{\pi 4}$, above equation becomes:

$$G_m=\frac{\beta_6}{\beta_6+1}\frac{\beta_0\beta_4}{2\left(\beta_0+1+\frac{\beta_0}{g_{m0}R_E}\right)+\beta_0\beta_4}\frac{1}{R_E} \tag{2.14}$$

Hence, the on resistance r_v of the source follower sircuit does not affect the transconductance value.

Simaple Small signal Model

Node equation at$\mathbf{V}_{e0}$

$$(v_{in}-v_{eo})g_{\pi_0}-v_{e0}g_e+g_{m0}(v_{in}-v_{e0})+g_{m2}(v_d-v_t)+(v_d-v_{e0})g_0-(v_{e0}-v_{c0})g_0=0 \tag{2.15}$$

Node equation at $\mathbf{v}_{c0}$

$$(v_t-v_{c0})g_v+(v_{e0}-v_{c0})g_0-(v_{in}-v_{e0})g_{m0}=0 \tag{2.16}$$
$$v_{c0}(g_v+g_0)=v_tg_v+V_{e0}(g_0+g_{m0})-v_{in}g_{m0} \tag{2.17}$$
$$v_{c0}=\frac{v_tg_v+V_{e0}(g_0+g_{m0})-v_{in}g_{m0}}{g_v+g_0} \tag{2.18}$$

Node equation at $\mathbf{v}_t$

$$2(v_d-v_t)g_{\pi 2}-(v_t-v_{c0})g_v=0 \tag{2.19}$$

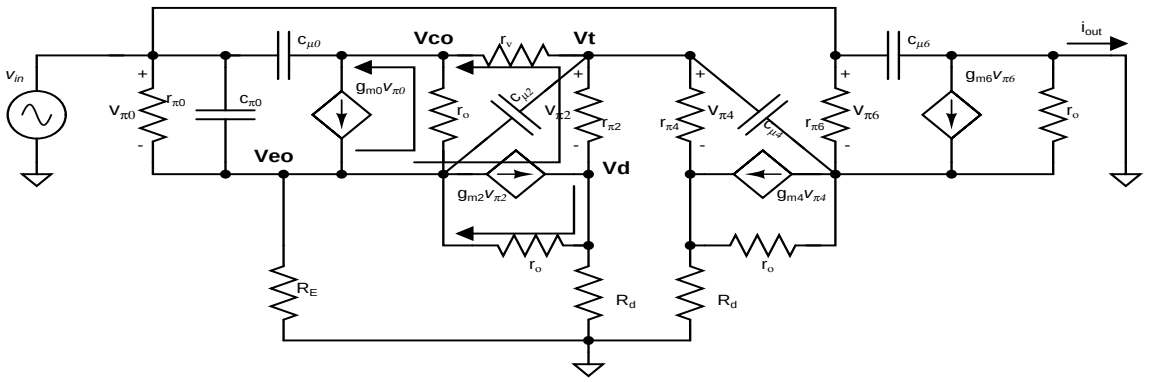

Figure 2.2: Small signal circuit equivalent of transconducto

Node equation at $\mathbf{v}_d$

$$-(v_d - v_t)g_{m2} - (v_d - v_{e0})g_0 - (v_d - v_t)g_{\pi 2} - v_d g_d = 0 \tag{2.20}$$

$$(v_d - v_{e0})g_0 = -(v_d - v_t)(g_{m2} + g_{\pi 2}) - v_d g_d \tag{2.21}$$

$$v_d(g_0 + g_{m2} + g_{\pi 2} + g_d) = v_t(g_{m2} + g_{\pi 2}) + v_{e0}g_0 \tag{2.22}$$

$$v_d = \frac{v_t(g_{m2} + g_{\pi 2}) + v_{e0}g_0}{g_0 + g_{m2} + g_{\pi 2} + g_d} \tag{2.23}$$

$$v_d - v_t = \frac{-v_t(g_0 + g_d) + v_{e0}g_0}{g_0 + g_{m2} + g_{\pi 2} + g_d} \tag{2.24}$$

$$v_d - V_{e0} = \frac{v_t(g_{m2} + g_{\pi 2}) - v_{e0}(g_{m2} + g_{\pi 2} + g_d)}{g_0 + g_{m2} + g_{\pi 2} + g_d} \tag{2.25}$$

Now Substituting the value of v_d in Equation 2.19:

$$2\frac{-v_t(g_0 + g_d) + v_{e0}g_0}{g_0 + g_{m2} + g_{\pi 2} + g_d}g_{\pi 2} - (v_t - v_{c0})g_v = 0 \tag{2.26}$$

$$v_t\left(\frac{2g_{\pi 2}(g_0 + g_d)}{g_0 + g_{m2} + g_{\pi 2} + g_d} - g_v\right) + v_{e0}\frac{g_0 g_{\pi 2}}{g_0 + g_{m2} + g_{\pi 2} + g_d} + v_{c0}g_v = 0 \tag{2.27}$$

$$v \tag{2.28}$$

from Nodal Equation 2.16 and Equation 2.19

$$2(v_d - v_t)g_{\pi 2} + (v_{e0} - v_{c0})g_0 - (v_{in} - v_{e0})g_{m0} = 0 \tag{2.29}$$

$$(v_{e0} - v_{c0})g_0 = (v_{in} - v_{e0})g_{m0} - 2(v_d - v_t)g_{\pi 2} \tag{2.30}$$

from Equation 2.15, Equation 2.25 and Equation 2.30

$$(v_{in} - v_{e0})(g_{\pi 0} + g_{m0} - g_{m0}) + (v_d - v_t)(g_{m2} - g_{m2} - g_{\pi 2} + 2g_{\pi 2}) - v_{e0}g_e - v_d g_d = 0 \quad (2.31)$$

$$(v_{in} - v_{e0})g_{\pi 0} + (v_d - v_t)g_{\pi 2} - v_{e0}g_e - v_D g_d = 0 \quad (2.32)$$

Small Signal Analysis for CMRR From Symmetry of the cicuit, one half

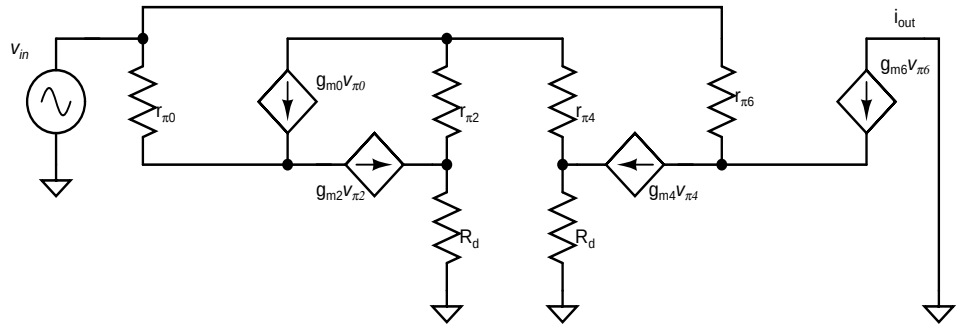

Figure 2.3: Small signal circuit equivalent of transconducto

of the g_{m0} $v_{\pi 0}$ current will come from Q2 and other half will come from Q4. With this assumption the analysis is as follows

$$V_D = \frac{g_{m0} v_{\pi 0}}{2} \times R_D \tag{2.33}$$

$$v_{\pi 0}(g_{m0} + g_{\pi 0}) + \frac{g_{m2} g_{m0} v_{\pi 0} r_{\pi 2}}{2} = \frac{v_{in} - v_{\pi 0} - V_D}{r_0} \tag{2.34}$$

$$v_{\pi 0}(g_{m0} + g_{\pi 0}) + \frac{g_{m2} g_{m0} v_{\pi 0} r_{\pi 2}}{2} = \frac{v_{in}}{r_0} - \frac{1}{r_0}(1 + \frac{g_{m0} R_D}{2}) v_{\pi 0} \tag{2.35}$$

$$\frac{v_{in}}{r_0} = v_{\pi 0} \left[g_{m0} + g_{\pi 0} + \frac{\beta_2 g_{m0}}{2} + \frac{1}{r_0} \left(1 + \frac{g_{m0} R_D}{2} \right) \right]$$

$$\frac{v_{in}}{r_0} \approx v_{\pi 0} \left[\left(1 + \frac{\beta_2}{2} \right) g_{m0} + g_{\pi 0} + \frac{g_{m0} R_D}{2 r_0} \right] \tag{2.36}$$

$$i_{cm} = \frac{g_{m2} g_{m0} r_{\pi 2} v_{\pi 0}}{2} = \frac{\beta_2 g_{m0}}{2} v_{\pi 0}$$

$$i_{cm} = \frac{\frac{\beta_2 g_{m0}}{2} \frac{v_{in}}{r_0}}{\left(1 + \frac{\beta_2}{2} \right) g_{m0} + g_{\pi 0} + \frac{g_{m0} R_D}{2 r_0}}$$

$$i_{cm} = \frac{\beta_2 g_{m0} v_{in}}{\beta_2 g_{m0} r_0 + 2 g_{\pi 0} r_0 + g_{m0} R_D} i_{cm} = \frac{\beta_6}{\beta_6 + 1} \frac{1}{r_0 + \frac{2 r_0}{\beta_2 \beta_0} + \frac{R_D}{\beta_2}} \tag{2.37}$$

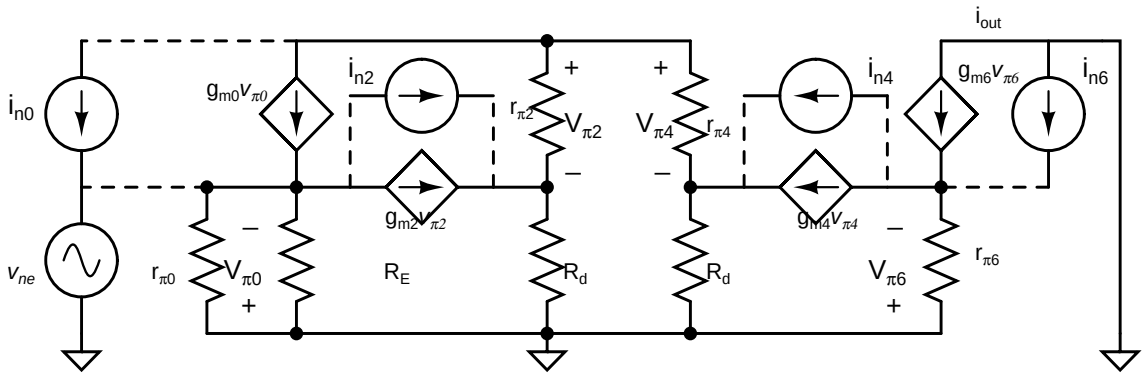

Figure 2.4: Noise small signal circuit equivalent of transconducto

Noise due to input transistor Q0,$(i_{n0} = 2qI_C)$

$$i_{out} = \frac{\beta_4}{2}\left(g_{m0}v_{\pi 0} - i_{n0}\right) = \frac{\beta_2}{2}\left(g_{m0}v_{\pi 0} - i_{n0}\right)$$
$$v_{\pi 0} = \frac{1}{g_{m0}}\left(i_{n0} + \frac{2i_{out}}{\beta_2}\right) \tag{2.38}$$

KCL at the Emitter of Q0

$$\left(g_{m0}v_{\pi 0} - i_{n0}\right) + g_{m2}\left(\frac{g_{m0}v_{\pi 0} - i_{n0}}{2}\right)r_{\pi 2} = -v_{\pi 0}\left(g_{\pi 0} + g_E\right)$$
$$i_{out} = i_{n0} - v_{\pi 0}\left(g_{m0} + g_{\pi 0} + g_E\right)$$
$$i_{out} = i_{n0} - \left(i_{n0} + \frac{2i_{out}}{\beta_2}\right)\left[\frac{g_{m0} + g_{\pi 0} + g_E}{g_{m0}}\right]$$
$$i_{out} = \frac{i_{n0}\left(1 - \frac{g_{m0}+g_{\pi 0}+g_E}{g_{m0}}\right)}{1 + \frac{2}{\beta_2}\left(\frac{g_{m0}+g_{\pi 0}+g_E}{g_{m0}}\right)}$$
$$i_{out} \approx i_{n0}\left(1 - \frac{g_{m0} + g_{\pi 0} + g_E}{g_{m0}}\right) = i_{n0}\left(\frac{g_{\pi 0} + g_E}{g_{m0}}\right)$$
$$i_{out} \approx \frac{g_E}{g_{m0}}i_{n0} \tag{2.39}$$

Noise due to input transistor Q2($i_{n2} = 2qI_C$)

$$i_{out} = \frac{\beta_4}{2}\left(g_{m0}v_{\pi 0}\right) = \frac{\beta_2}{2}\left(g_{m0}v_{\pi 0}\right)$$
$$v_{\pi 0} = \frac{1}{g_{m0}}\left(\frac{2i_{out}}{\beta_2}\right) \tag{2.40}$$

KCL at the Emitter of Q0

$$g_{m0}v_{\pi 0} + \frac{g_{m2}g_{m0}v_{\pi 0}r_{\pi 2}}{2} + i_{n2} = -v_{\pi 0}\left(g_{\pi 0} + g_E\right)$$
$$i_{out} = -i_{n2} - v_{\pi 0}\left(g_{m0} + g_{\pi 0} + g_E\right)$$
$$i_{out} = -i_{n2} - \left(\frac{2i_{out}}{\beta_2}\right)\left[\frac{g_{m0} + g_{\pi 0} + g_E}{g_{m0}}\right]$$
$$i_{out} = \frac{-i_{n2}}{1 + \frac{2}{\beta_2}\left(\frac{g_{m0}+g_{\pi 0}+g_E}{g_{m0}}\right)}$$
$$i_{out} \approx i_{n2} \tag{2.41}$$

Noise due to input transistor Q6($i_{n6} = 2qI_C$)

KCL equation at the emitter of Q0

$$g_{m0}v_{\pi 0} + \frac{g_{m2}r_{\pi 2}g_{m0}r_{\pi 0}}{2} = -v_{\pi 0}\left(g_{\pi 0} + g_E\right)$$
$$v_{\pi 0}\left(...\right) = 0$$
$$\text{thus} V_{\pi 0} = 0$$

KCL nodal equation at the emitter of Q6

$$i_{n6} - g_{m6}v_{\pi 6} = v_{\pi 6}g_{\pi 6}$$
$$v_{\pi 6} = \frac{i_{n6}}{g_{\pi 6} + g_{m6}} \tag{2.42}$$
$$i_{out} = i_{n6} - g_{m6}v_{\pi 6} = i_{n6} - g_{m6}\frac{i_{n6}}{g_{\pi 6} + g_{m6}}$$
$$i_{out} = \frac{i_{n6}}{\beta_6} \tag{2.43}$$

Noise due to input transistor Q4($i_n 4 = 2qI_C$)

$$v_{\pi 6}\left(g_{\pi 6} + g_{m6}\right) = i_{n4}$$
$$i_{out} = g_{m6}v\pi 6 = \frac{\beta_6}{\beta_6 + 1}i_{n4} \tag{2.44}$$

Thus from Equation 2.39,Equation **??**,Equation 2.44,and Equation 2.43, total noise at the output is

$$\begin{aligned} i_{out} &= 2\left(\frac{g_E}{g_{m0}}i_{n0} + i_{n2} + \frac{i_{n6}}{\beta_6} + \frac{\beta_6}{\beta_6+1}i_{n4}\right) \\ &\approx i_{n2} + i_{n4} + i_{n3} + i_{n5} = 8qI_C \end{aligned} \tag{2.45}$$

Thus total noise in noise optimized biquad filter will be

$$v_{nO}^2 = \frac{1}{G_{mq}^2}\left(8qI_c|_{gmf} + 8qI_c|_{gmg} + \left(\frac{g_{mh}}{g_{mf}}\right)^2 \times 8qI_c|_{gmh} + \left(\frac{g_{mq}}{g_{mf}}\right)^2 \times 8qI_c|_{gmq} + 8qI_c|_{gmf}\right) \tag{2.46}$$

APPENDIX C

SCHEMATIC DIAGRAM

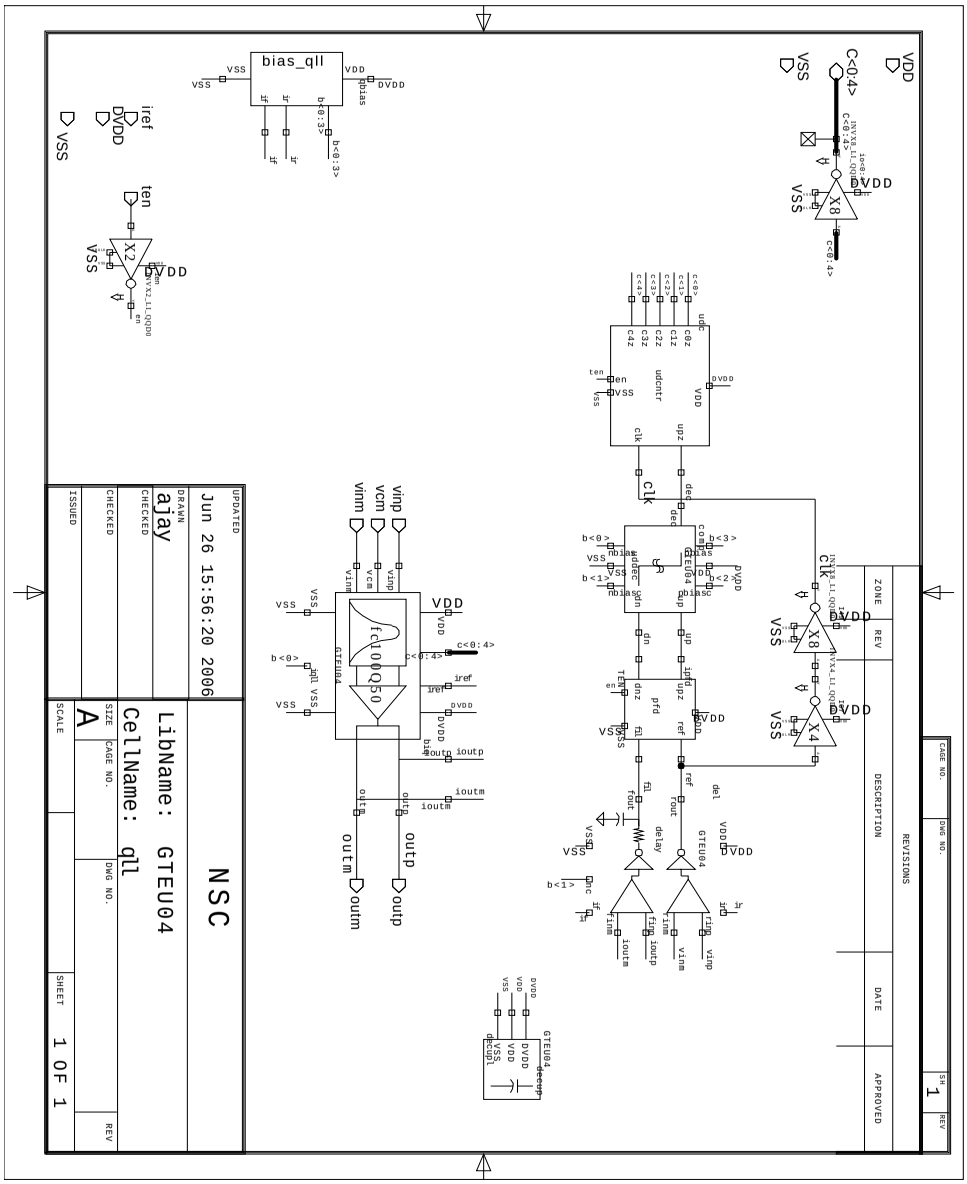

Figure 3.5: The cadence schematic diagram of the QLL tuning scheme.

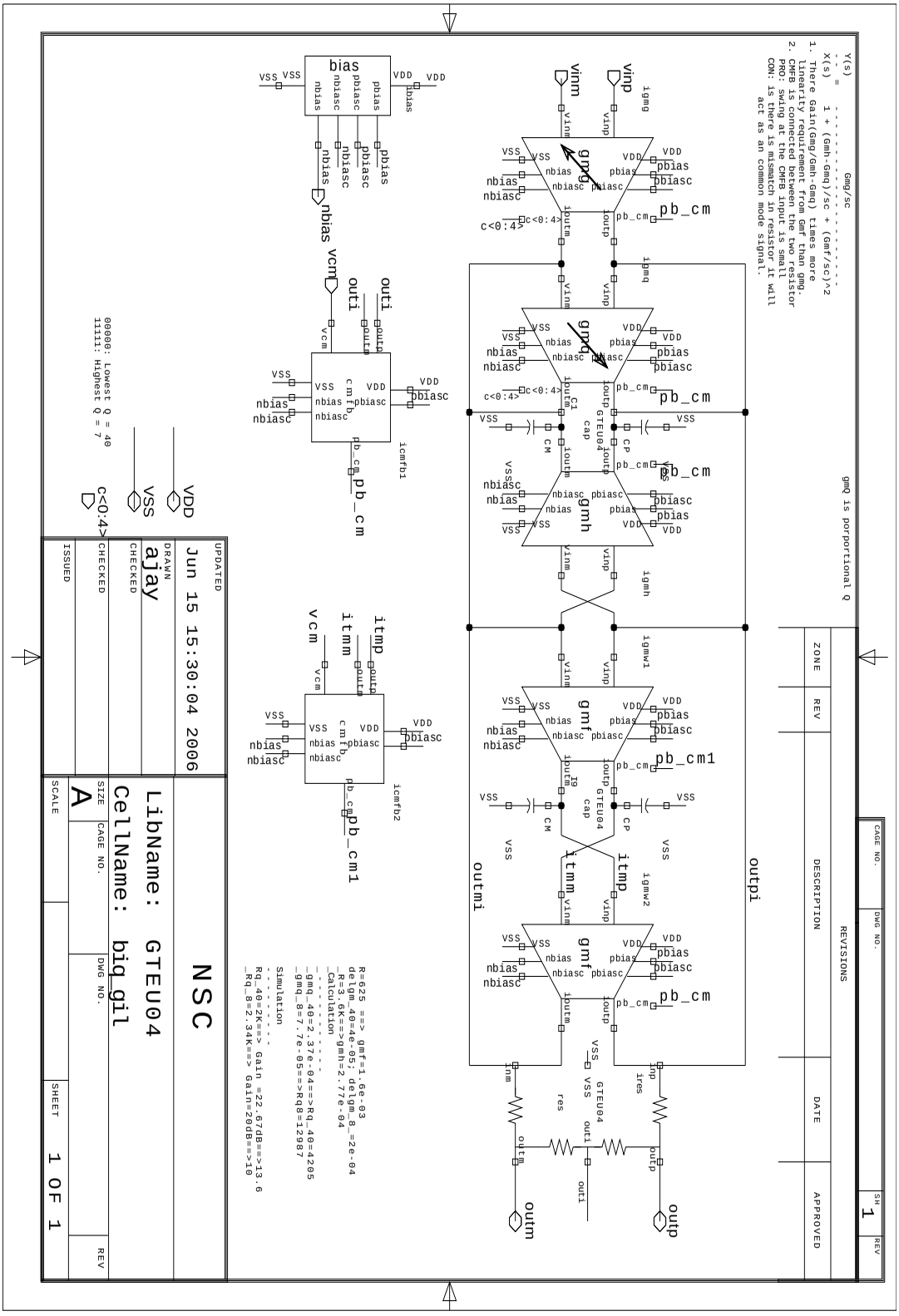

Figure 3.6: The cadence schematic diagram of the biquad filter.

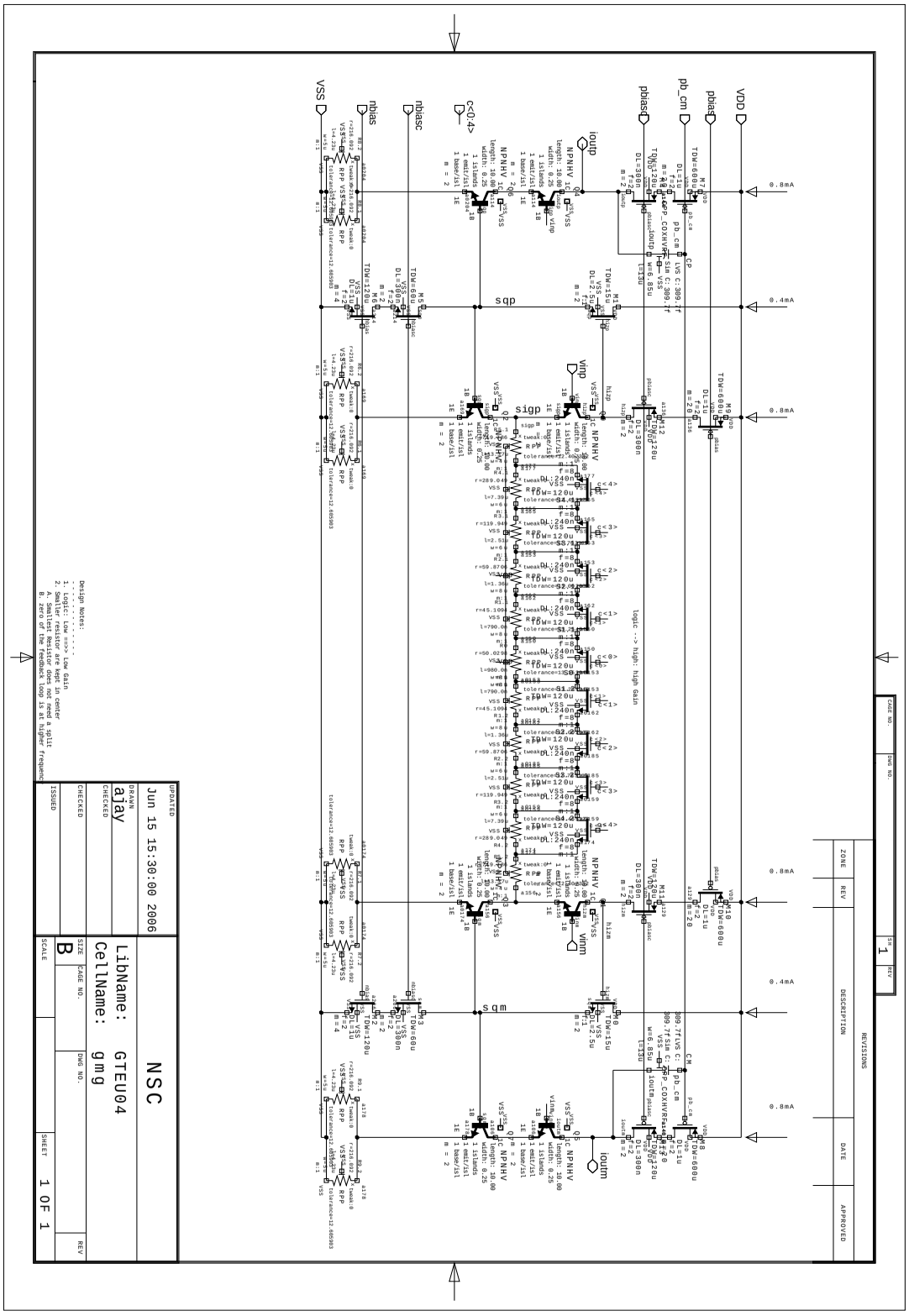

Figure 3.7: The cadence schematic diagram of the gain tuning transconductor.

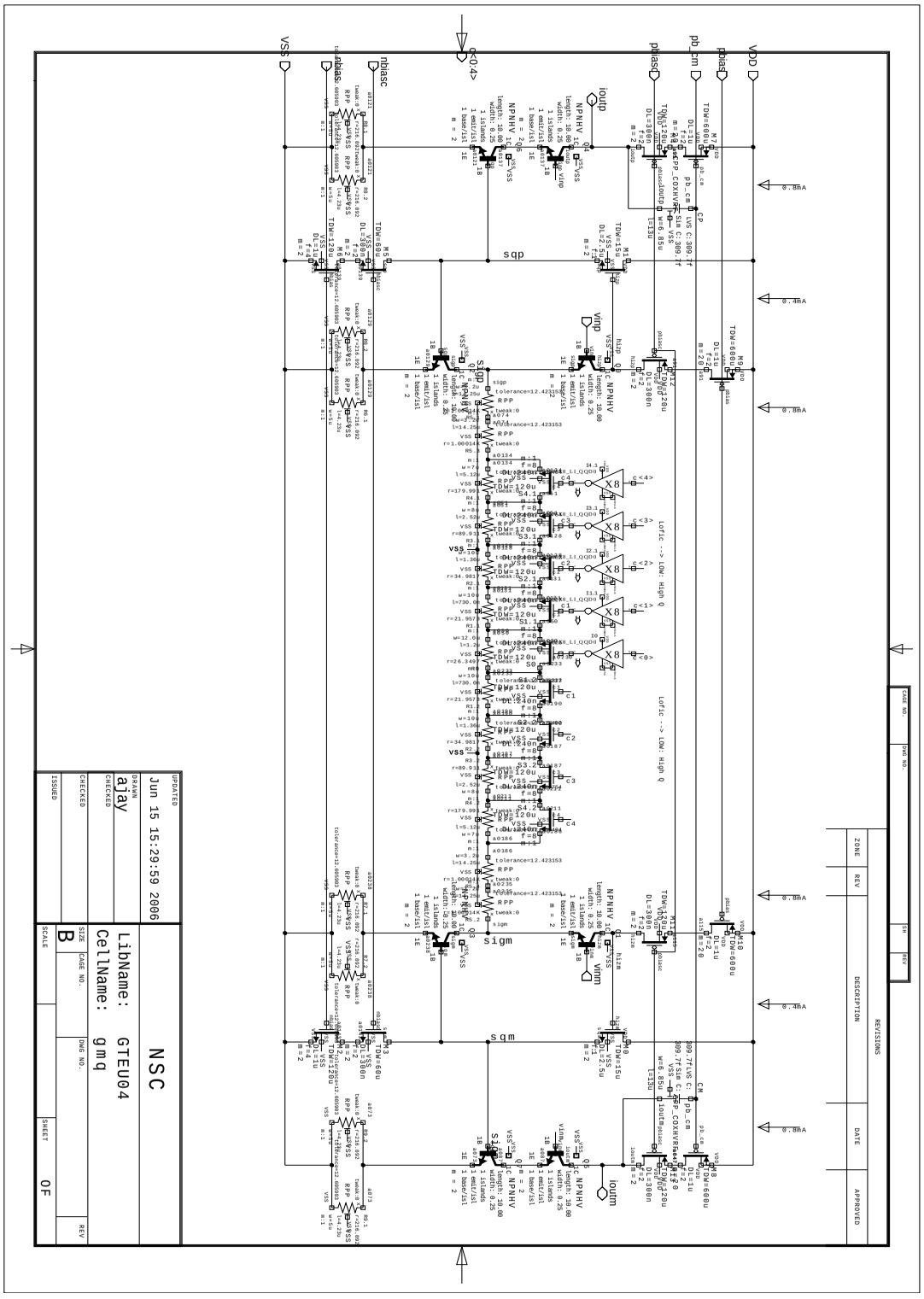

Figure 3.8: The cadence schematic diagram of the Q-tuning transconductor.

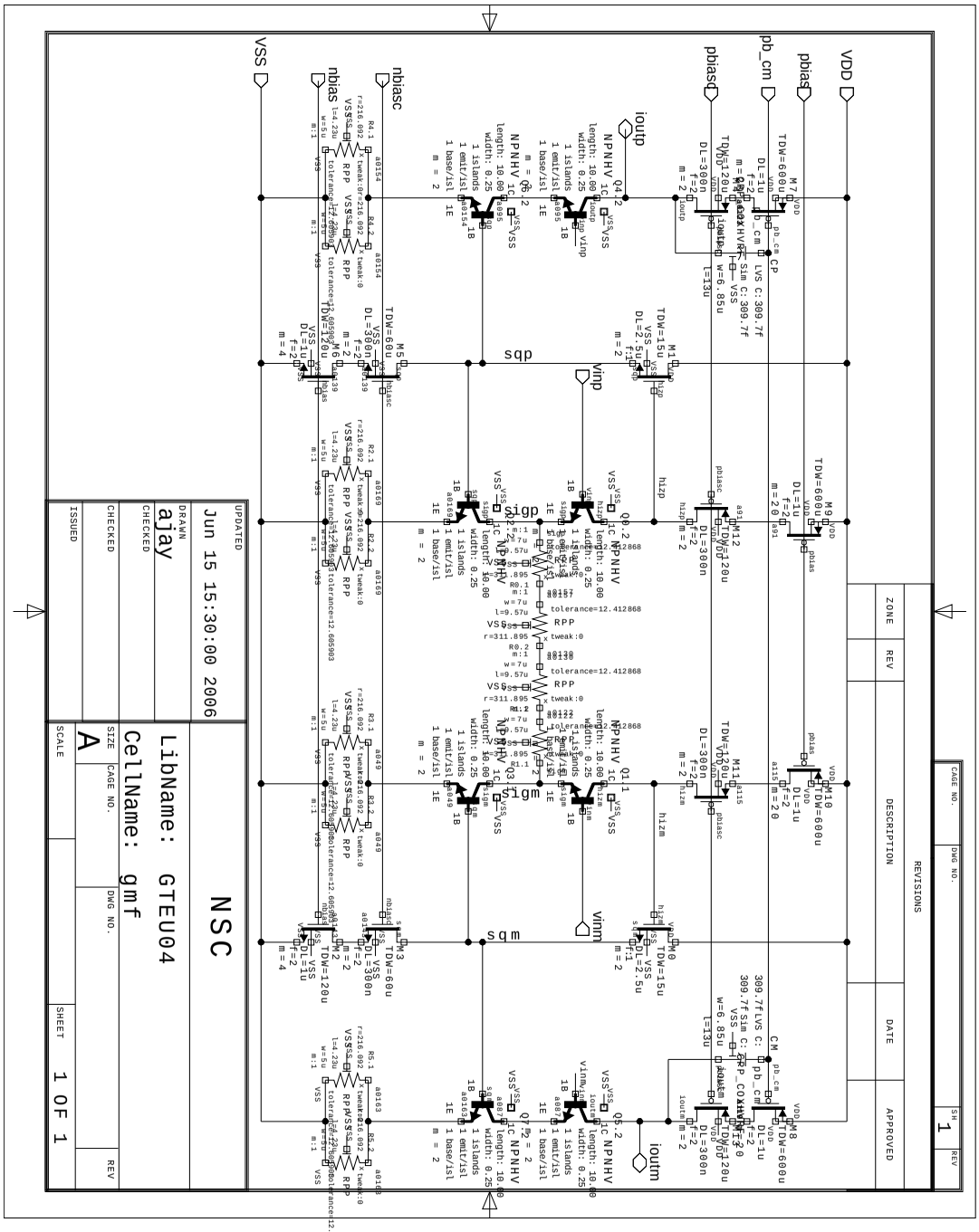

Figure 3.9: The cadence schematic diagram of the resonant transconductor.

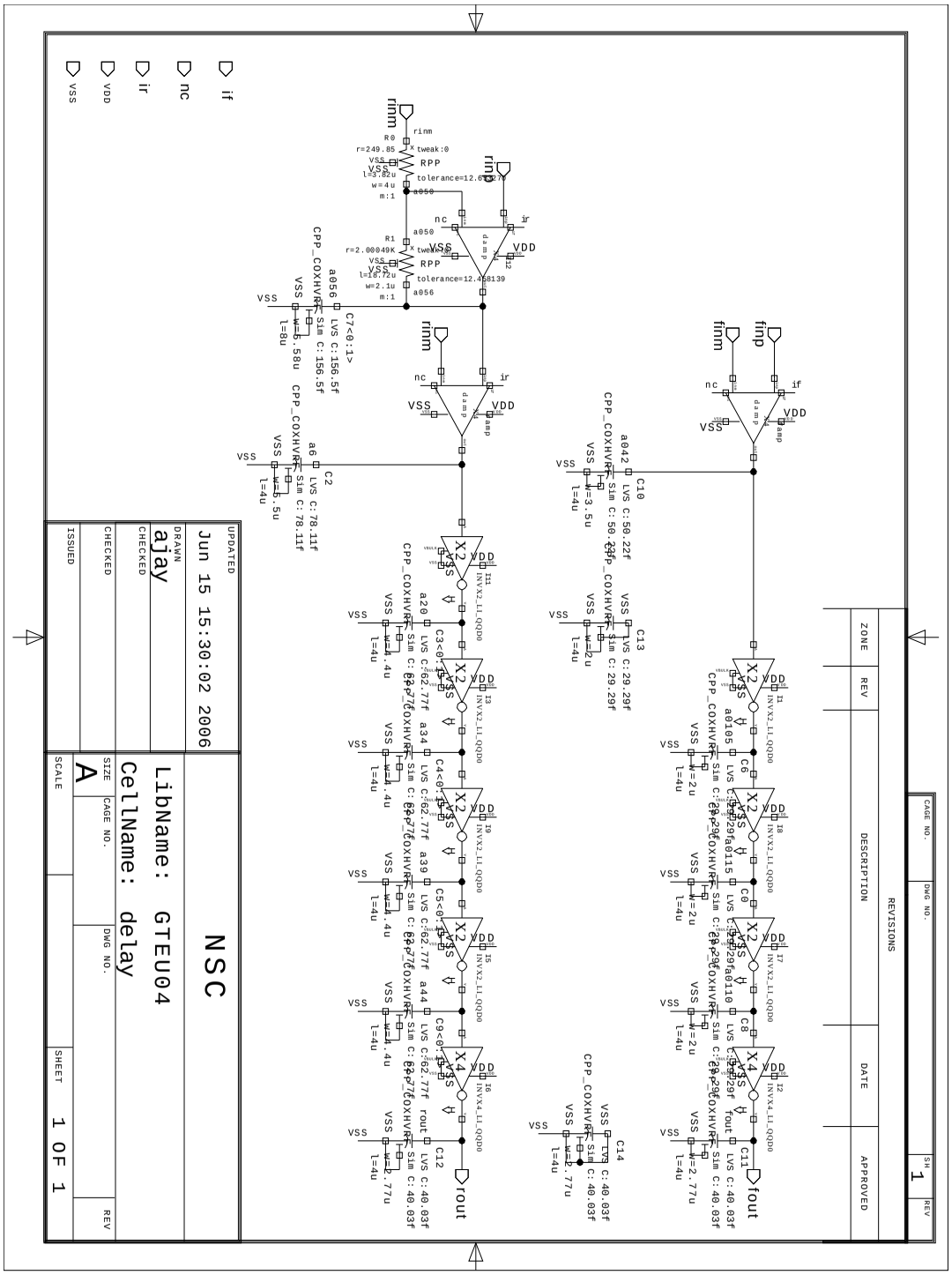

Figure 3.10: The cadence schematic diagram of the delay network.

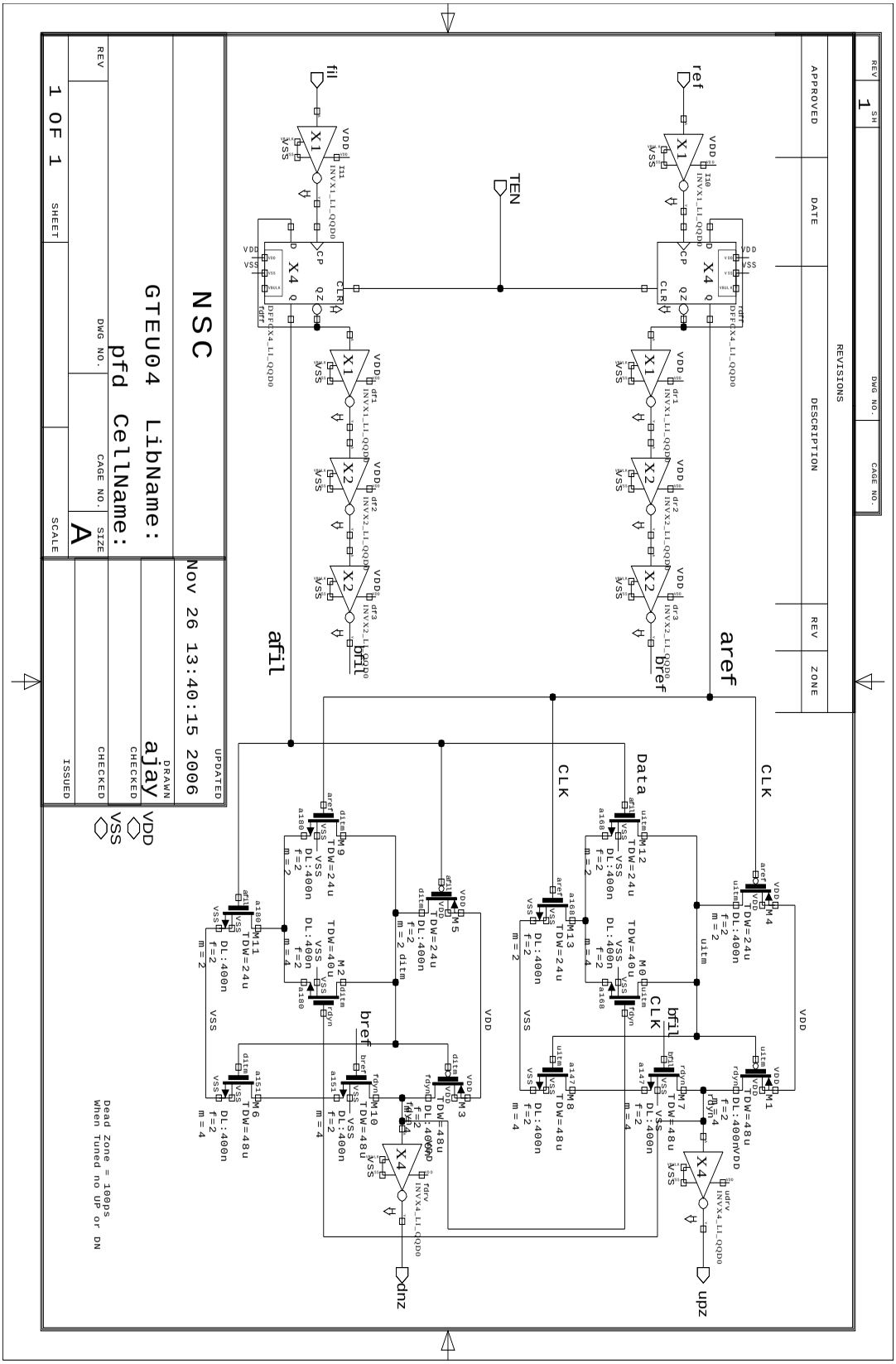

Figure 3.11: The cadence schematic diagram of the phase frequency detector.

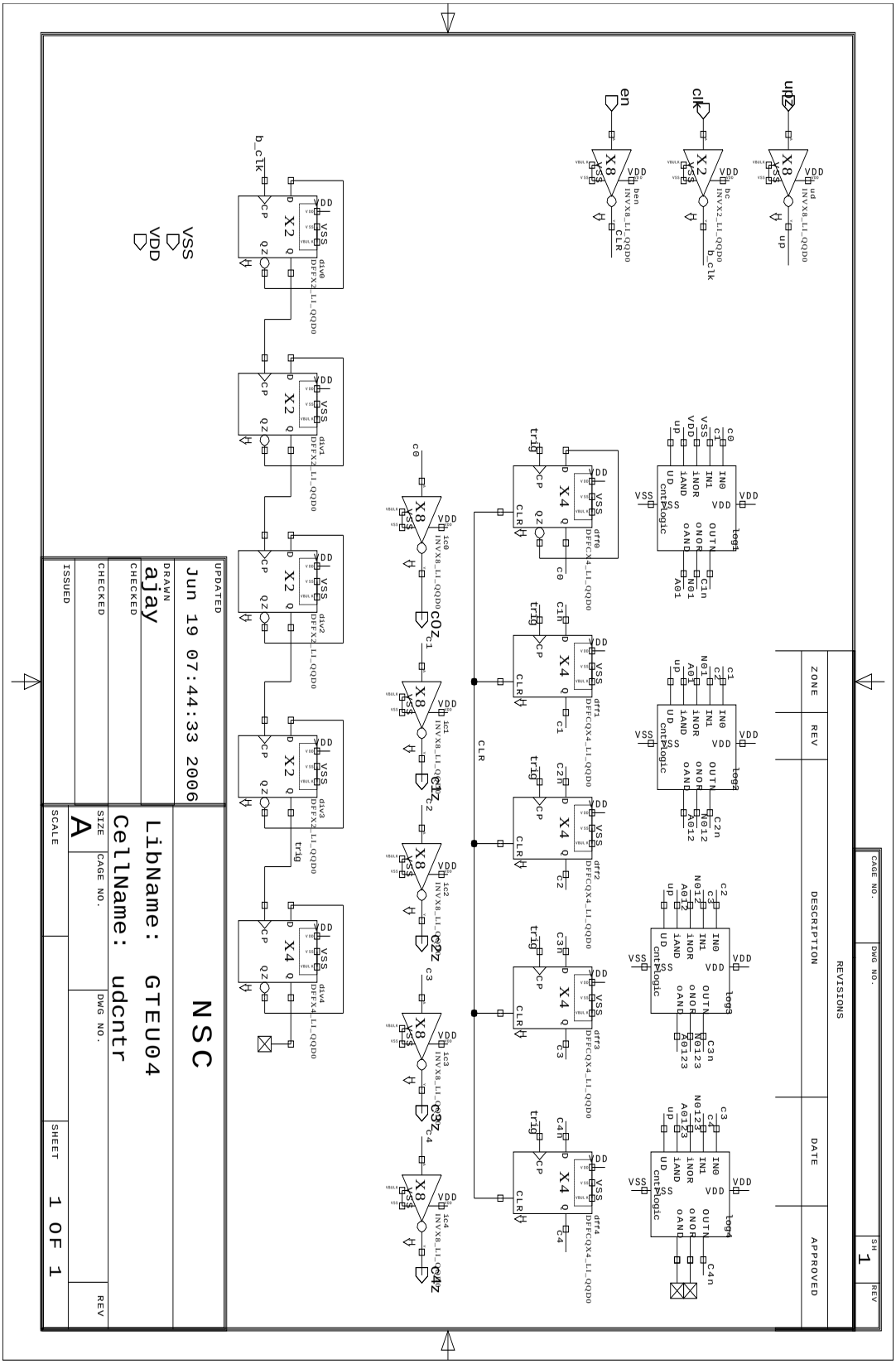

Figure 3.12: The cadence schematic diagram of the 5-bit counter.

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