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A Wide Tuning Range Gated Varactor

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Abstract— **A wide tuning range gated varactor for radio frequency (RF) applications is described in this paper. The gated varactor is a three terminal device. The third terminal helps achieve an improved tuning range. The measured tuning range of the varactor exceeds ± 50%. The new device can be implemented with standard CMOS process without any post-processing. A 2 G Hz prototype VCO is implemented using the new varactor in a 0.35 μm CMOS process. The VCO achieved a sensitivity of 220 M Hz/V.**

I. Introduction

The remarkable growth of modern wireless communication systems calls for lower cost and more integrated wireless transceivers. Voltage-controlled oscillator (VCO), widely used as a part of the frequency synthesizer to generate the local oscillator (LO) signal for both up conversion and down conversion of baseband signal, is one of the key elements of modern wireless transceivers. In achieving a monolithic VCO, a LC-tank CMOS oscillator is commonly used since they exhibit better phase noise performance than ring oscillators.

Monolithic LC-tank CMOS oscillators with on-chip spiral inductors have been intensively studied to improve the phase-noise performance [1][2]. Challenges, however, still lie ahead in achieving reliable monolithic VCOs. For one thing, the process variation makes it rather difficult to accurately produce a VCO with the right center frequency and tuning range. One possibility is to enhance the tuning range of the LC-tank so as to offer some compensation over process variation. In a LC-tank VCO, a varactor is primarily used as the tuning element. Thus, the tuning range of the VCO is strongly related to the tuning range of the varactors. The traditional PN junction varactor is quite limited in the tuning range. One way to overcome the problem is to employ a switched tuning VCO[3]. Such an approach increases the circuit complexity and may not be preferred. Alternatively, innovation can be made with the varactor itself. Accumulation-mode varactors with a tuning range of ±30% and nominal capacitance of 1pF and 3.1pF have been reported[4][5].

This study describes a new varactor structure with a further improved tuning range. The new structure can be fabricated with a standard CMOS process without any post-processing. When implemented in a 0.35 μm standard CMOS process, the varactor achieved a tuning range of ± 53% with a center capacitance of 1.5pF. Without any intention of optimizing the Q-factor of the varactor, we achieve a maximum measured Q-factor greater than 20.

The proposed varactor is a three terminal device. The third terminal enables the device to have a wider tuning range. A prototype VCO is fabricated to demonstrate the use of the third terminal.

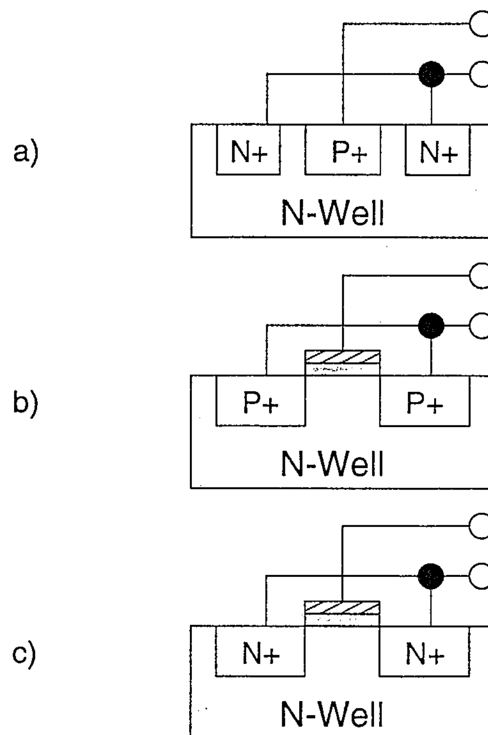

Fig. 1. a) an PN junction varactor, b) an PMOS capacitor varactor and c) an accumulation-mode varactor

Including this introductory section, this paper is divided into six subsections. The varactor structure along with some commonly used varactor structures are described in Section II. In Section III, the operation of the varactor, is described. The measured performance of a fabricated varactor is shown in Section IV. In Section V, a prototype VCO using the proposed varactor is described. How the VCO uses the third terminal of teh device to achieve a wider tuning range is also discussed. The conclusion is drawn in Section VI.

II. The Varactor Structure

Commonly used varactors include the PN junction varactors, the PMOS varactors and the accumulation-mode varactors. The structures of these varactors are shown in Figure 1. One of the implementations of the PN junction varactors in the standard CMOS process is shown in Figure 1a. The structure consists of a P+ and an N+ region residing in an N-Well. The depletion region is formed between the P+ region and the N-Well. The tuning range provided by a PN junction varactor varies with the doping

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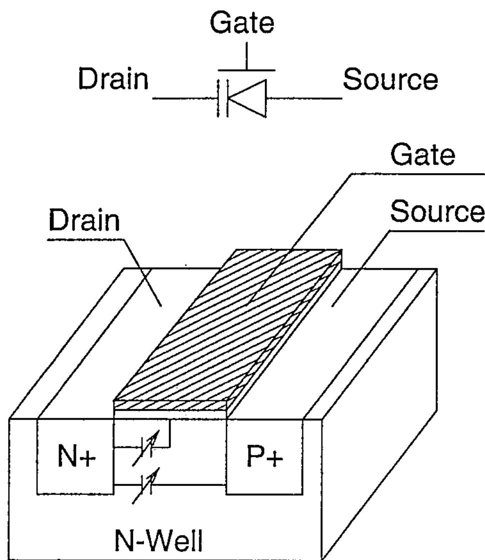

Fig. 2. Cross-sectional view of the gated varactor

profile. Typical PN junction varactors provide a ± 10% tuning range. The PMOS varactor utilizes the gate capacitance of a PMOS transistor. While providing a wider tuning range than the PN junction varactors, the tuning range of the PMOS varactors is limited by the source and drain parasitic capacitance. In an accumulation-mode varactor, the N+ contacts replace the source and drain of an PMOS varactor. Accumulation-mode varactors achieve a tuning range of ±30% after the removal of the parasitic source/drain capacitance.

The gated varactor structure is shown in Figure 2. The structure is similar to a PMOS transistor except that the drain node is replaced by an N+ contact. The gated varactor can be considered to be a combination of the three varactor structures mentioned above. Replacing only the drain node by an N+ region while keeping the source node as P+, the gated varactor provides a wider tuning range by varying the source capacitance.

The new structure is a three terminal device. The first terminal connected to the N+ contact is defined as the drain node. The gate node is connected to the poly-silicon gate. The P+ node is defined as the source node. In this study, the capacitance of the device is defined as the capacitance looking into the drain node. These notations are shown in Figure 2.

The capacitance can be varied by changing the potential difference between either the drain node and the gated node, or the drain node and the source node. The characteristics and the physics behind the gated varactor are discussed in later sections of this paper. The capacitance consists of several capacitances — the gate capacitance, the junction capacitance, and some parasitic. Due to the presence of these capacitances, the gated varactor is able to offer a higher capacitance per unit area than the other implementations. The implemented varactor records a capacitance per unit area of 2.875 fF/μm^2 .

The new structure is fully compatible with the standard

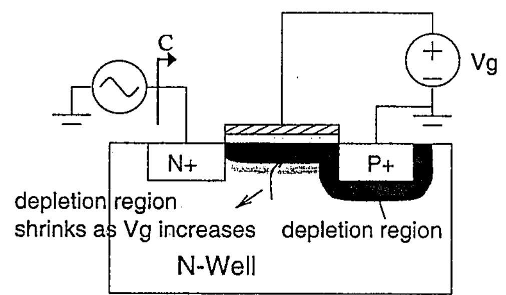

Fig. 3. Simplified MEDICI simulation showing the carrier concentration under different gate bias

CMOS process, and does not require any post-processing.

III. Operation and Characteristics of The Gated Varactor

In order to understand the operation of the varactor, a device simulation tool, MEDICI, is used to simulate the carrier concentration of the device with a standard bulk CMOS process. N-Well doping concentration of $1.2 \times 10^{17} cm^{-3}$ is set. The structure is simulated under different biasing condition. The simulation is used to develop a set of theories that explain the operation of the device.

The experiment was divided into two parts. In the first part, we examined the impact of varying the voltage at the gate node. In the second part, we examined the effect of varying the voltage at the drain node. In both cases, the source node was connected to ground.

The simplified MEDICI simulation results are shown in Figure 3. In order to improve the readability of the simulation results, we redrew the diagrams and showed only the important information of the simulation. Figure 3 shows the carrier concentration under different gate biasing. The drain and the source node are grounded. The darkened region represents the depletion region. The depletion region shrinks as the voltage at the gate increases.

The operation of the gated varactor is similar to the operation of the accumulation-mode varactor. Increasing the gate voltage moves the varactor towards the accumulation mode and the capacitance increases.

In Figure 4, a similar diagram with the drain biased at different voltage is shown. The gate node and the source node are grounded while the drain voltage is varied. Varying the drain voltage has two impacts on the device. Despite the finite resistance of the N-Well structure, the drain node and the N-Well should have roughly the same potential. Increasing the drain voltage increases the potential of the N-Well. And, as the potential difference between the gate and the N-Well reduces, the device moves into inversion mode. This is shown by arrow 1 in Figure 4. The depletion region extends as the device moves towards inversion mode and reduces the capacitance that looks into the drain node. As the drain voltage increases, the potential across the PN junction also increases. The depletion region across the PN junction widens, and the capacitance further reduces. One may notice that the depletion region

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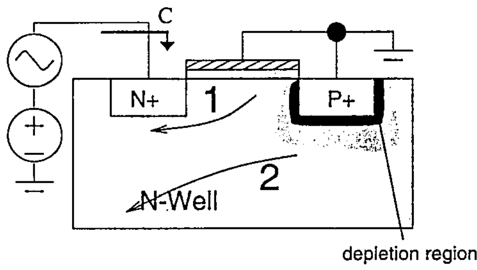


Fig. 4. Simplified MEDICI simulation showing the carrier concentration under different drain bias

extends at the subsurface region of the N-Well at which the gate loses control of the carrier concentration. This phenomena is similar to the sub-surface DIBL effect and occurs at the lower doping region at the subsurface. When the drain voltage increases to a certain point, a depletion region which formed underneath the gate merges with the depletion region which formed at the subsurface. The capacitance looking into the drain reaches its minimum at the point.

As discussed in the previous sections, the total capacitance of the gate primarily consists of three components: the gate capacitance, the junction capacitance and some parasitic. While the first two components offer the varactor the ability to tune its capacitance, the last component limits the capacitance at some finite value. The maximum capacitance can be estimated by

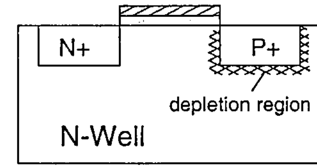
$$C_{total} = C_{ox} + C_j + C_{min} \tag{1}$$

C_{total} is the total capacitance that looks into the drain. C_{ox} is the oxide capacitance. C_j is the junction capacitance and C_{min} includes the overlapping capacitance, the interconnection capacitance and other parasitic capacitance that may appear at the drain node. When reaching its minimum capacitance, due to the subsurface depletion phenomena described, the C_{ox} and C_j offer little capacitance to the total capacitance. The minimum capacitance of the varactor is roughly equal to the quality C_{min}.

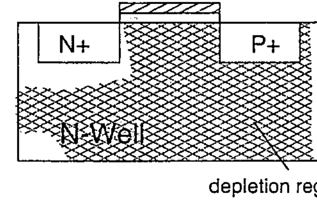
Compared with the accumulation-mode varactor, which has a maximum capacitance of C_{ox}, the gated varactor offers a higher total capacitance. When the varactor reaches its minimum capacitance, the depletion region under the gate merges with the depletion region at the subsurface. This depletion enables the subsurface region, which cannot be depleted by controlling the gate voltages, to be depleted, and leads to a lower minimum capacitance. Figure 5 shows the carrier concentration of these cases. Essentially, with a higher maximum capacitance and lower minimum capacitance, the gated varactor allows a wider tuning range.

IV. Measurement Results

A testing varactor was fabricated using a 0.35μm digital CMOS process. The measured varactor consists of 100 segments with a total gate dimension of 500μm by 0.4μm. The size of each segment including the gate , source and drain is $5\mu m \times 1.6\mu m$. Fingering reduces the gate resistance. The



a) Maximum Capacitance



b) Minimum Capacitance

Fig. 5. The carrier concentration of the varactor when reaching its a) maximum capacitance and b) minimum capacitance

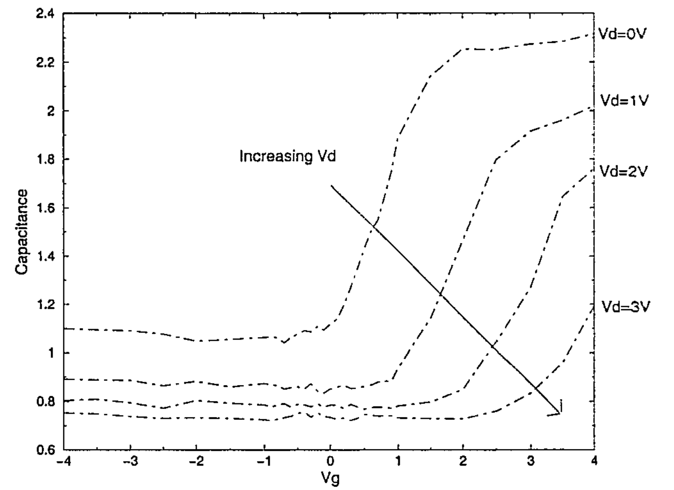


Fig. 6. Measured capacitance under different bias

measurement was done by a network analyzer. The 2-port S-parameters were measured with the drain node and the gate node as the ports. The source node was connected to the ground port. The capacitance and the resistance values were finally extracted from the 2-port S-parameters. The admittance looking from the drain was calculated from equation (2), while the equivalent R_p and capacitance C_{eq} was calculated as in equation (3) and (4).

$$Y = Y_o \frac{1 - S_{11}}{1 + S_{11}} \tag{2}$$

$$R_p = Re(y)^{-1} \tag{3}$$

$$C_{eq} = \frac{Im(y)}{2\pi f} \tag{4}$$

The extracted capacitance is shown in Figure 6 with the x-axis showing the gate voltage and the family of curves

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representing the capacitance measured with the drain biasing voltage varying from 0V to 4V with a 1V step. With an oxide thickness, t_{ox}, of 7.5nm, junction bottom capacitance , C_{jo}, of $9.3\times10^{-4}F/m^2$, and junction sidewall capacitance, C_{jsw}, of $2.1\times10^{-10}F/m$ and gate-to-drain parasitic capacitance, C_{gdo}, of $4.7\times10^{-10}F/m$, the capacitances are calculated as in equation (5) to equation (7).

$$\begin{aligned} C_{ox} &= \frac{\varepsilon A}{t_{ox}} \\ &\approx 0.94pF \\ where\ A &= 500\mu m \times 0.4\mu m \end{aligned} \tag{5}$$

$$\begin{aligned} C_j &= C_{jo} \times A_{source} + C_{jsw} \times w \\ &\approx 0.66pF \\ where\ A_{source} &= 500\mu m \times 1.2\mu m \\ w &= 500\mu m \end{aligned} \tag{6}$$

$$\begin{aligned} C_{min} &= C_{gdo} \times w + C_{pad} + C_{inter} \\ &\approx 0.55pF \\ where\ C_{pad} + C_{inter} &\approx 0.3pF \end{aligned} \tag{7}$$

The A_{source} is the area of the source node, w, the gate width is 500 μm in our varactor. C_{pad} and C_{inter} is estimated by multiplying the metal area with the capacitance per unit area measured. Substituting the values in equation (1), we get C_{max} =2.15pF and C_{min}=0.55pF. 0.66pF of the total capacitance is provided by the PN junction which is roughly about 30% of the total tuning range. Compared with the measured values, the equation is correct within ±10%. If one of the curves in Figure 6 is looked at, the behavior of the varactor is similar to an accumulation-mode varactor. When the drain voltage is varied, the curves shift to the right and experience a reduction in the minimum capacitance. This corresponds to the effect of driving the device to inversion mode with subsurface depletion. The tuning range is calculated with equation (8). With a center capacitance of 1.5pF, the fabricated varactor achieves a tuning range of ±53%, from 0.7pF to 2.3pF.

$$tuning\ range = \pm\frac{1}{2}\frac{C_{max} - C_{min}}{\frac{C_{max}+C_{min}}{2}} \tag{8}$$

The Q factor of the varactor is shown in Figure 7. In the graph, both axes are shown in log scale. The measured Q value, when measured, exceeded 20 at 2G Hz A capacitor C_{eq} with a parallel resistor R_p and a series resistor R_s represent a simplified model for the varactor. The series resistance includes the contact resistance, gate resistance and the N-Well resistance. The parallel resistance is an equivalent resistance related to the generation-recombination current, diffusion current and surface leakage current. For a given bias, Q varies as $\omega C_{eq} R_p$ at low frequency and as $1/\omega C_{eq} R_p$ at a high frequency.

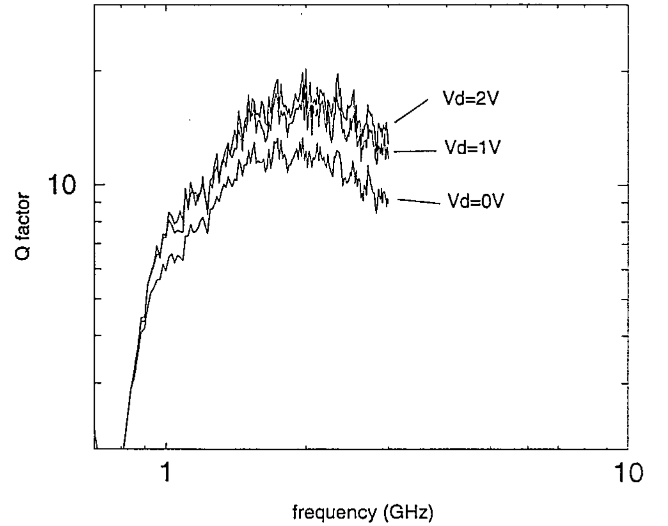

Fig. 7. Measured Q-factor of the varactor

V. Circuit Design with The Gated Varactor

The gated varactor, unlike conventional varactors, has an extra, third, terminal. A circuit topology is developed to exploit the third terminal. The objective here is to force the varactor to traverse across a family of curves in Figure 6, while not needing an extra control voltage. Figure 8 shows the schematic of a differential cross-couple LC-tank VCO with the gated varactors. The LC-tank consists of an integrated single layer metal spiral inductor of 2nH. The drain nodes of the varactors are biased at 1V. The sources of the varactors are connected to the output of a source follower to provide a level shifting from the tuning voltage. The tuning voltage also directly controls the voltage bias of the gate nodes. The level shifting of 1.5V provided by the source follower prevents the PN junctions of the varactors from forward biasing. The source follower should be carefully designed to prevent excessive noise being injected into the VCO. A long channel transistor, rather than minimum gate length transistor, is used for the source follower. The noise current injected by the NMOS transistor can be described by equation (9). K is a constant for a particular device and a and b are constants. With the short channel device, the value of γ in equation (9) can be as high as 3, while γ is around 2/3 for the long channel transistor. Using a long channel device for the source follower reduces the noise injected into the VCO.

$$\overline{i_{noise}}^2 = 4kT\gamma g_{d0} + K\frac{I^a}{f^b}\Delta f \tag{9}$$

When V_{tune} is set to 0V, the PN junctions are reverse biased at 1V and the potential of the N-Wells (drain node voltage) is lower than the gate by 0.5V. When the tuning voltage V_{tune} increases, the voltage across the drain and source nodes drops. As discussed in previous sections this action increases the capacitance of the varactor. At the same time, as V_{tune} increases, the gate voltage also goes up. This drives the device from inversion mode to accumulation mode and the capacitance further increases. With

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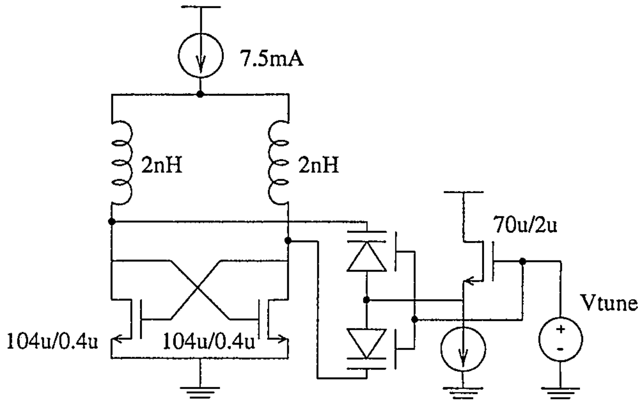

Fig. 8. Schematic of VCO using the third terminal of the varactor to achieve high tuning range

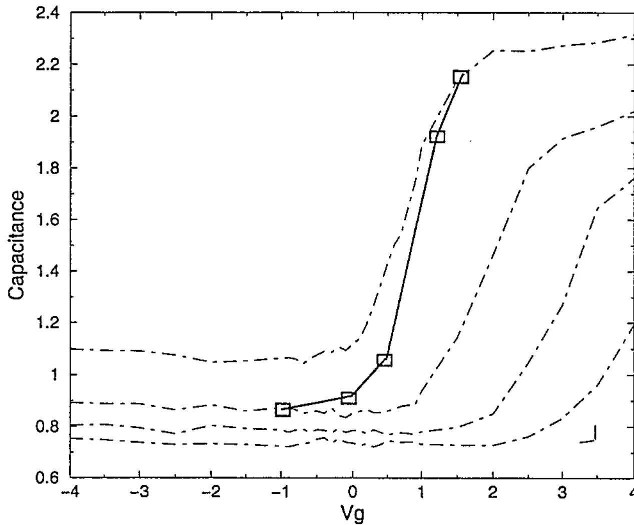

Fig. 9. Capacitance tuning characteristic

both actions moving the capacitance to the higher capacitance region, this circuit topology provides maximum VCO gain and tuning range. The capacitance tuning characteristic is shown by a solid line in Figure 9. The capacitance of the varactor is now varied by one tuning voltage as in conventional varactors.

The tuning characteristic of the VCO is shown in Figure 10. The frequency of oscillation varies by 320M Hz with a 1.4V variation in the tuning voltage. The high sensitivity of this VCO is ideal for low voltage designs in which the tuning voltage is limited by the supply.

The VCO, excluding the output buffers, draws 7.5mA from a 3V supply. When used to drive a 50 ohm loading, the measurement of the output power which including the buffers with again of -3.8dB, is -6dBm. When used to drive a capacitive load, the output voltage swing is 900m Vpp when oscillating at 2G Hz. The single-side band phase noise, when driving a 50 ohm loading, is measured to be -87 dBc/Hz at 100k Hz offset and -105 dBc/Hz at 1M Hz offset. The phase noise performance is mostly limited by the Q factor of the inductors. The Q factor of the inductors are simulated to be 2.

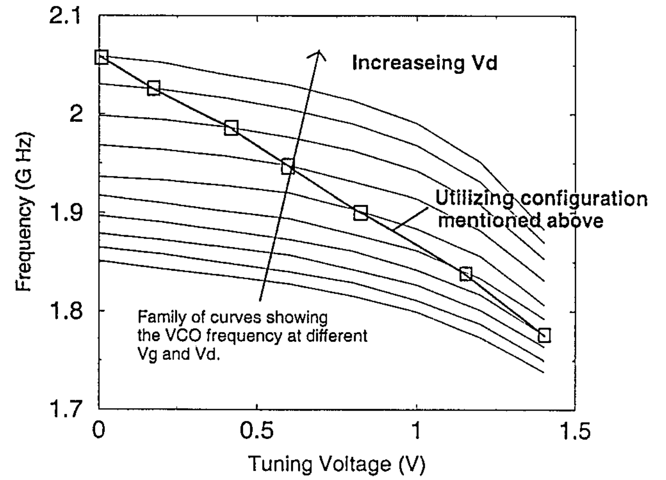

Fig. 10. VCO tuning characteristic

The reader may notice that the tuning characteristic of the VCO is highly linear. This is because the nonlinearity of the tuning source follower compensated for the nonlinearity in the frequency-capacitance relationship of the VCO.

While the aim of our circuit implementation is to provide a simple way to achieve large tuning range, the drain and gate node voltage do not necessarily need to related as in our example. One alternative is to allow the drain node to be used as an externally tuning node independent of the gate voltage. The drain node can thus be used as a coarse tuning node while the gate node can be be part of the intrinsic phase locked loop tuning. As discussed in the introductory section, the motivation for having a wide tuning range is to compensate for variations in the fabrication process. Lacking good theory to predict the Q-factor of the inductor, designers may find predicting the oscillating frequency of the VCO difficult. Process variation and process parameters variation may further exacerbate the problem. A coarse tuning node can be used as a safety valve in post fabrication adjustment. This would be better than relying solely on a highly sensitive varactor based on a single node. In a highly sensitive varactor based on a single node, the high sensitivity increases the loop gain and thus worsens its noise performance. The coarse tuning node can be well protected from noise sources and hence will reduce the VCO's sensitivity to noise while allowing the various variations to be compensated by external adjustment.

VI. Conclusion

A new varactor structure providing a wide tuning range is implemented with 0.35 μm CMOS process. When applied in a LC-tank VCO, the varactor allows the VCO to have a wide tuning range, and mitigated the problems due to process variation. The implemented varactor provides a tuning range of $\pm$ 53% with a nominal capacitance of 1.5pF. A VCO with the proposed varactors is fabricated. The VCO consumes 7.5mA from a 3V supply and achieves a phase noise of -87dBc/Hz at 100k Hz offset and -105dBc/Hz

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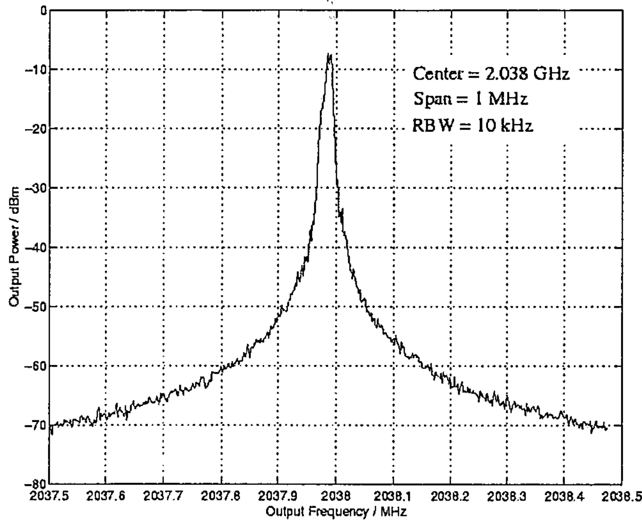

Fig. 11. Measured output spectrum of the VCO

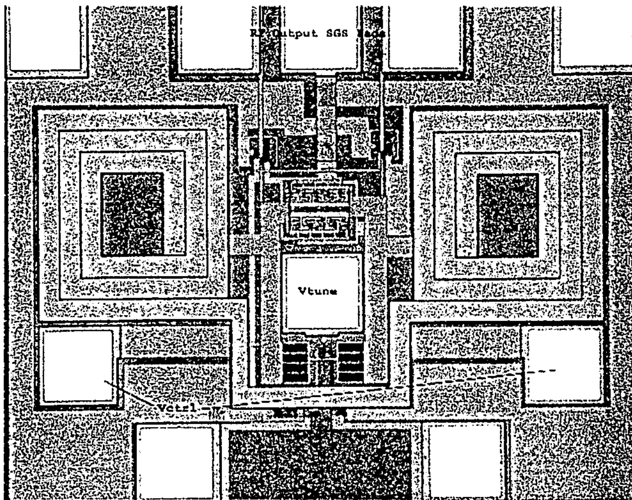

Fig. 12. Die photo of the VCO

at 1M Hz offset.

REFERENCES

[1] J. Craninckx and M. Steyart, "1.8G Hz low-phase noise CMOS VCO using optimized hollow spiral inductors", *IEEE J. Solid-State Circuits*, vol.32, pp. 736-744, May 1997.

[2] A. Hajimiri and T.H. Lee, "Phase Noise in CMOS Differential LC Oscillators", *1998 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 48-51, June 1998.

[3] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS Oscillators with Switched Tuning", *Proceedings of the IEEE 1998 Custom Integrated Circuit Conference*, pp. 555-558, May 1998.

[4] R. Castello, P. Erratico, S. Manzini and F. Svelto, "A 30% Tuning Range Varactor Compatible with Future Scaled Technologies", *1998 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 34-35, June 1998.

[5] T. Soorapanth, C. P. Yue, D. K. Shaeffer, T. H. Lee and S. S. Wong, "Analysis and Optimization of Accumulation-mode Varactor for RF ICs", *1998 Symposium on VLSI Circuits Digest of Technical Papers*, pp. 32-33, June 1998.

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