A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon

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***Abstract*—A 77-GHz, +17.5 dBm power amplifier (PA) with fully integrated 50-Ω input and output matching and fabricated in a 0.12-μm SiGe BiCMOS process is presented. The PA achieves a peak power gain of 17 dB and a maximum single-ended output power of 17.5 dBm with 12.8% of power-added efficiency (PAE). It has a 3-dB bandwidth of 15 GHz and draws 165 mA from a 1.8-V supply. Conductor-backed coplanar waveguide (CBCPW) is used as the transmission line structure resulting in large isolation between adjacent lines, enabling integration of the PA in an area of 0.6 mm^2. By using a separate image-rejection filter incorporated before the PA, the rejection at IF frequency of 25 GHz is improved by 35 dB, helping to keep the PA design wideband.**

***Index Terms*—BiCMOS, integrated circuits, microstrip, phased arrays, power amplifiers, radio transmitters, SiGe, silicon, silicon germanium.**

I. Introduction

THE millimeter-wave (mm-wave) bands offer exciting opportunities for various applications such as short-range communication (e.g., the 60-GHz band) and automotive radar (e.g., the 77-GHz band) [1]–[3]. There have been several recent efforts to implement critical mm-wave blocks such as low-noise amplifiers (LNAs), voltage-controlled oscillators (VCOs), and power amplifiers (PAs) in silicon [2]–[5]. Penetration of silicon integrated circuits to these bands can bring the unchallenged reign of compound semiconductors at these frequencies to an end. Although the performance of silicon-based implementations needs to improve to match that offered by III-V-based technologies, the true strength of silicon lies in its unmatched capability for integration, which will enable a new level of complexity encompassing microwave, analog, and digital blocks [6]–[8]. This unprecedented integration will result in new system level architectures at these frequencies previously impractical using lower yield compound semiconductor processes, resulting in globally optimum solutions in terms of cost and performance.

Perhaps the most challenging building block at mm-wave frequencies is the power amplifier (PA). Prior work in silicon PAs involved a 77-GHz SiGe amplifier with 15.5-dBm output power and 5% power-added efficiency (PAE) [4]. Also in [2] and [3] two SiGe PAs at 77 GHz and 60 GHz with 10–13-dBm output power and 3%–4% PAE have been reported. In [9], by using multiple parallel transistors, the output power level has been increased to 21 dBm, but the PAE has still been limited to 3%. Although by using power combining further improvement in the output power is possible, the main challenge for the silicon implementation so far has been improving the PAE. As a comparison point at similar frequencies, PAs using III-V technologies deliver 23–28 dBm of output power with 20%–40% of PAE [10]–[13].

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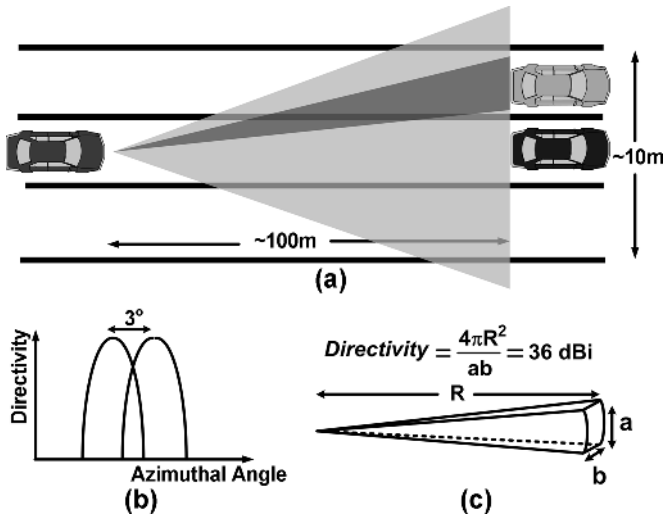

Fig. 1. (a) Typical range and resolution for a long-range car radar. (b) The required main beam width to be able to resolve two cars in two adjacent lanes. (c) Calculation of the directivity of the transceiver.

In this paper, a 77-GHz power amplifier with 17.5 dBm of output power and a peak PAE of 13% is described. The amplifier represents the best combination of output power and efficiency reported for an integrated silicon-based PA. In Section II, the automotive radar system in which the amplifier is intended to be used is briefly described, and the required amplifier output power is calculated. In Section III, the choice of transmission line structure to provide a high level of on-chip isolation is discussed. The large degree of isolation offered by this transmission line is necessary for compact realization of the PA and facilitates integration of the PA with sensitive elements of a single-chip transceiver. Design of the amplifier is detailed in Section IV, followed by measurement results presented in Section V.

II. The Required Amplifier Power for Automotive Radar Application

In long-range radar for cruise control and collision avoidance, the need to detect distant vehicles and to discriminate between closely spaced vehicles demands a small radiation beamwidth and fine beam steering resolution. As shown in Fig. 1, the required azimuthal resolution for the long-range radar should be around 3°. To avoid reflections from entrance of tunnels and bridges, the required beam width in the elevation plane (vertical plane) should also be less than 3°. The corresponding system directivity, as shown in Fig. 1, will be 36 dBi. For traditional car radar applications, the beam steering has been achieved using a dielectric lens or a Rotman lens [14]–[17]. Instead, in the radar system

for which the amplifier in this work is designed, a phased-array transceiver with beam steering in both transmit and receive (TX and RX) paths is employed [7], [8]. In this case, the directivity requirement of each path is relaxed; hence reducing the required array aperture. The 18-dB required directivity at each path can be achieved with 16 elements providing 12 dB of array directivity combined with a typical directivity of a patch or dipole antenna ($\sim$5 dB). Since there is no need to scan in the elevation plane, the required directivity in the elevation can be realized by narrowing the antenna beam in the elevation plane (e.g., using serially fed patches [17]–[19]). In this case, just four elements for beam steering in the azimuthal plane will be enough.

Assuming 18 dB of directivity for transmit and receive paths and 3 dB of insertion loss for the antenna, if each power amplifier in the 4-element phased array generates 15 dBm of output power, the received signal power calculated using the standard radar equation will be -116 dBm [20]. In this case, the target is assumed to have a radar cross section of 1 m^2 located at 100 meters away. Using a 4-element phased array system with a 6-dB signal-to-noise ratio (SNR) improvement due to the uncorrelated noise of different antennas and assuming a receiver noise figure of 8 dB [8], the radar SNR for a 300-MHz bandwidth will be -11 dB. By using multiple scans or pseudo-noise (PN) modulation [16], the radar sensitivity can be improved.

By employing a commonly used frequency modulated continuous wave (FM-CW) or pulse-Doppler technique, the transmitter power amplifier will experience a constant-envelope signal, relaxing its linearity requirements.

III. Conductor-Backed Coplanar Waveguide as the Transmission Line Structure

The conductor-backed coplanar waveguide (CBCPW) structure, shown in Fig. 2, is used for impedance matching. The use of vias to connect back and side ground planes eliminates unwanted parallel-plate modes [21]. Fig. 2(b) shows the magnetic field distribution in the transmission line, simulated with Ansoft HFSS 3-D field solver [22]. The characteristic impedance of the transmission line in this simulation is 50 Ω. The bottom plate carries very little current (small tangential component of the magnetic field) while the side-shield carries most of the return current.

The tub shape reduces surface wave propagation in the silicon substrate, improving isolation between lines. Fig. 3 shows the isolation between two adjacent 50-Ω lines versus their center-to-center spacing simulated using IE3D [23]. The lines are implemented using the top three metals of the process. The side shields increase isolation by more than 20 dB. The coupling in the secondary line is larger in the direction opposite to the wave direction of the primary line.

There is a tradeoff between the isolation of lines and their insertion loss. Since the side-shield increases unit length capacitance, in order to keep the characteristic impedance constant, the width of the line should be reduced. This increases the loss of the transmission line. The 50-Ω line without shield has a loss of 0.5 dB/mm, while the loss for the line with side-shield is 0.75 dB/mm. Since the PA is intended to be used in a single-chip transceiver [7], [8], it is imperative to minimize the interference generated by the high-power PA to sensitive elements such as the on-chip VCO. Therefore, the transmission lines were always

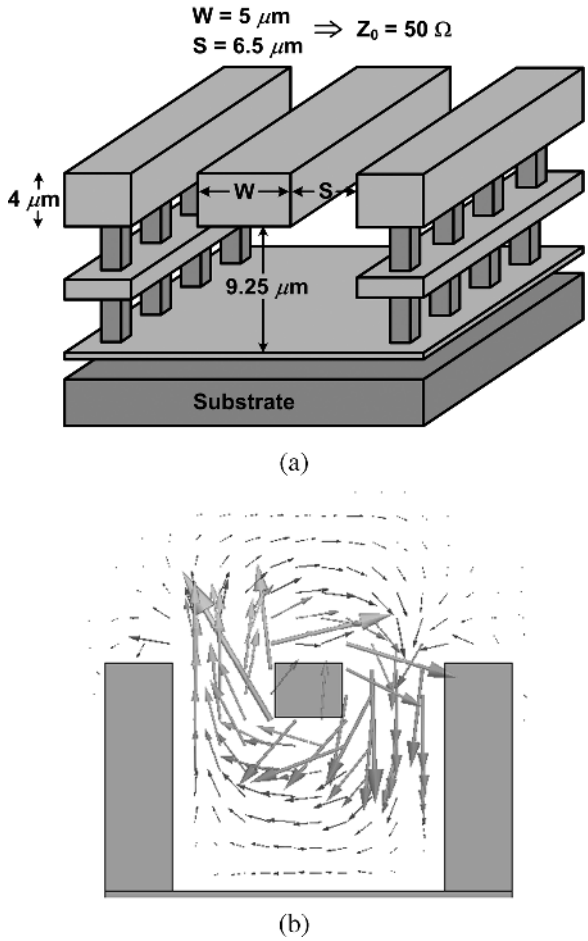

Fig. 2. (a) Conductor-backed coplanar waveguidemicrostrip tub transmission line structure used for impedance matching in the amplifier. (b) The simulated magnetic field distribution of the structure, showing most of the return current is coming from the side shields.

used with side-shield. The unloaded quality factor of the transmission line can be found by the expression

$$Q = \frac{\pi}{\lambda\alpha} \tag{1}$$

where λ is the guided wavelength and α is the attenuation in nepers per meter. The corresponding quality factor for this particular CBCPW line at 77 GHz is 9.2.

IV. Amplifier Design

The power amplifier has been designed in a 0.12-μm BiCMOS process featuring SiGe transistors with $f_T \approx 200$ GHz and $f_{\max} \approx 200$ GHz [24]. The process has five metal layers with three copper bottom layers, and two thick 1.25 μm and 4 μm aluminum layers as top metals. The breakdown voltages of the bipolar transistors are $\mathrm{BV_{CEO}} \approx 1.7$ V and $\mathrm{BV_{CBO}} \approx 5.5$ V. The substrate resistivity is 14 Ω·cm.

A. Circuit Architecture

The schematic of the amplifier is shown in Fig. 4. The amplifier consists of four gain stages, where the output stage is designed for maximum efficiency and the other stages are designed for maximum gain. The last three stages use one, two, and four identical transistor cells, respectively. This geometric

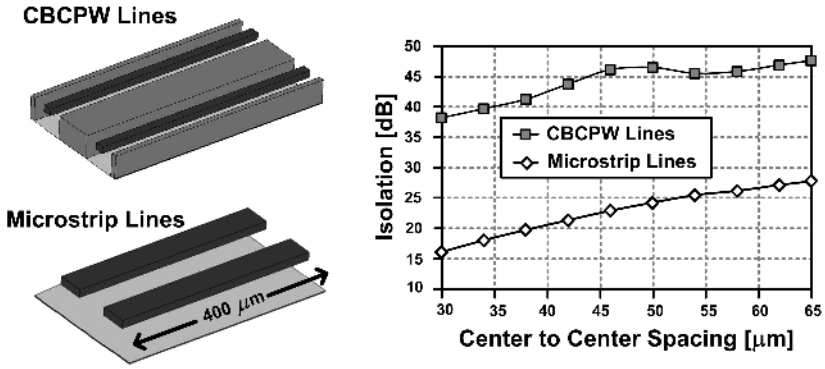

Fig. 3. The simulated isolation between two side-by-side 400-μm, 50-Ω CBCPW lines ($\mathrm{W} = 5\ \mu\mathrm{m}$, $\mathrm{S} = 7.5\ \mu\mathrm{m}$) and two microstrip lines with the same characteristic impedance and length ($\mathrm{W} = 13\ \mu\mathrm{m}$).

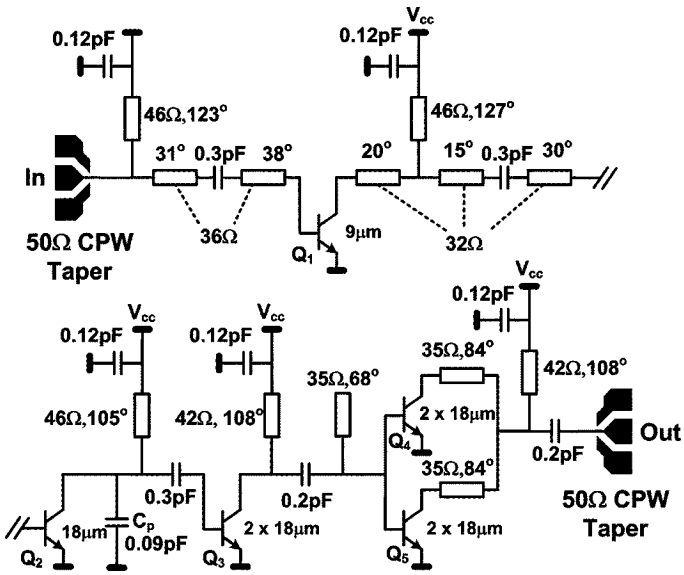

Fig. 4. Schematic of the 77-GHz power amplifier including element values.

scaling of transistor size from each stage to the next ensures that as long as the preceding stages have at least 3 dB of gain the output transistors will enter compression first. All the transistors have single emitter stripe, use minimum emitter width of 0.12 μm, and have two base and two collector contacts (CBEBC configuration). For a reliable operation, the collector junction has more than the minimum number of possible contacts (three rows of long rectangular vias in parallel). The amplifier is biased in class-AB mode. With 1.2 mA of current per 1 μm of emitter length, the transistors are biased at their maximum $f_{\max}$.

When the PA is driven into saturation, the collector voltage of the output transistor can exceed twice the supply voltage. For a large base impedance, the low open-base collector-emitter breakdown voltage, $\mathrm{BV_{CEO}}$, of 1.7 V limits the possible supply voltage to about 0.9 V. In a normal silicon transistor, the maximum dielectric breakdown field and velocity saturation pose a fundamental breakdown voltage versus speed tradeoff [25], [26]. The $\mathrm{BV_{CEO}}$ limitation is set by the impact ionization effect, in which the generation of electron–hole pairs by accelerated electrons constitute the necessary base recombination current. If the base is driven with a lower source impedance, the extra generated majority carriers will be extracted from the base and hence the breakdown voltage will increase [27]. In this case, the voltage swing is limited by $\mathrm{BV_{CER}}$ rather than $\mathrm{BV_{CEO}}$. In the process used, for R_B equal to 300-Ω, $\mathrm{BV_{CER}}$ is around 4 V [3]. Consequently, the bias circuitry is designed to provide a base resistance of 300 Ω at low frequencies, while the matching networks provide the necessary low base impedance at high frequencies. Stress tests for advanced SiGe technologies have shown a slight degradation of forward DC current gain at very low bias currents [28], [29]. Since the transistors in the PA are biased with a high current density, the operation above $\mathrm{BV_{CEO}}$ will not create a reliability issue. Degradation of the transistors' high-frequency performance is not observed [30].

B. Design of the Matching Networks

The matching networks use series transmission lines and parallel shorted stubs for power matching between stages as shown in Fig. 4. At the input of the last stage an open stub provides a lower matching network loss than a shorted stub does. At the output of second stage, the same objective was achieved with a parallel MIM capacitor (C_p).

The capacitors at the end of shorted parallel stubs are in parallel with a series *RC* network (which for simplicity is not shown in Fig. 4). A proper choice of *R* and *C* reduces the gain of the amplifier at low frequencies, enhancing stability.

The optimum impedance at the collector of each stage is determined with a large-signal power match. Similar to the design presented in [31], a load-pull simulation is performed to find the best load for the transistor. For the output stage, this point is chosen to maximize the efficiency and for the other stages to maximize the gain. Fig. 5 shows the result of the load-pull simulations for all of the four stages. These gain and PAE contours have peak values of 6 dB and 30%, and step sizes of 1 dB and 4%, respectively. The contours become denser as we move toward the output stage, indicating larger sensitivity of the amplifier to matching errors. The contours are opened and this sensitivity is reduced if a lower characteristic impedance is used for the transmission lines at the output stage. By having an initial assessment for the losses in the matching network, the load-pull simulations also provide an estimation for the transistor size. The exact size of the transistor is chosen by iterating through the design procedure after the matching network is designed and its corresponding insertion loss is determined. By knowing the insertion loss of the matching networks, the transistor sizes are scaled such that they can provide the necessary output power for the next stage (or the output

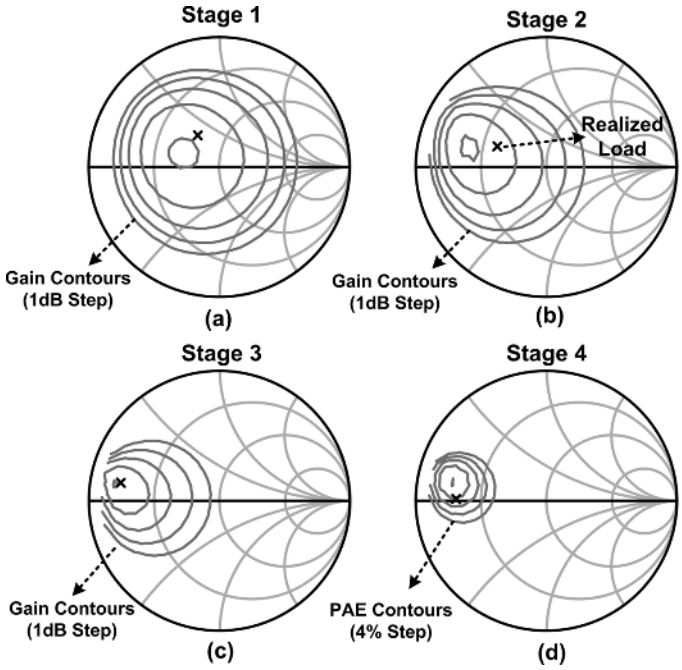

Fig. 5. Load-pull simulation of the four stages of the power amplifier, together with the actual realized load impedances.

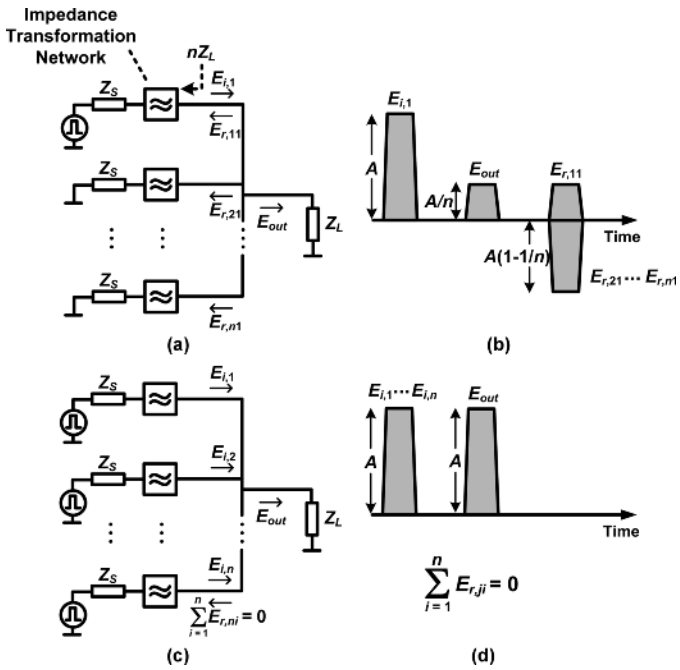

Fig. 6. (a) Power combining without individual branch match, but satisfying global match to the load. (b) Scattering behavior for one of the incident waves at the combining point. (c) Scattering behavior when all the branches are driven in-phase. (d) Cancellation of branch reflection through superposition and symmetry.

load). Unlike the linear load-line matching technique described in [32] and used in [4], the large-signal load-pull methodology for choosing transistor size and optimum load impedance captures the large-signal nonlinear behavior of the transistor, as depicted in the noncircular shape of the contours of Fig. 5. The constant gain and output power contours for a transistor with linear parameters have a circular shape [20].

The realized impedance is not located exactly at the peak of the contours. This is most evident in the output stage where the realized load provides a PAE that is 4% lower than the maximum possible PAE. This is because the optimum load impedance is not the only constraint in the design of the matching network; loss of the matching network also needs to be minimized. Similar to the design presented in [31], a weighted least-mean-square optimization with gradient-descent scheme was utilized to choose the length and characteristic impedance of the lines. The optimization goal was to minimize the weighted sum of the squares of the distance to the optimum load point and the loss in the matching network. Therefore, for having a reasonable passive efficiency, the realized load is not exactly at the center of load pull contours.

C. Output Stage Power Combining

When the power level of the output stage of a PA is increased, many parallel transistors can be used to generate the output power. This reduces the size of each transistor, and hence the compact lumped model of the transistor becomes more accurate. Division of the power generation core into smaller cells has additional advantages in terms of uniform on-chip heat distribution and also relaxed impedance transformation ratio [33], but necessitates the use of a power-combining structure. As shown in Fig. 4, this was done in the output stage of the PA.

In power-combining circuits with hybrid or corporate combiners, the power-combining network is matched to each transistor cell [34]. In this case, the output power degradation due to individual device failure will be graceful [35]. In a low-yield compound III-V process, there is a chance that one of the transistor cells in the power-combining network will fail to operate properly. In a silicon process with a high yield, the extra constraint of individual match can be traded for a simpler power-combining network with lower loss and, hence, higher amplifier efficiency. As shown in Fig. 6, as long as there is a global match between load and effective parallel impedance of all the branches, there will not be any reflection at the combining node. In Fig. 6, $E_{i,j}$ is the incident wave in branch j, and $E_{r,ji}$ is the reflected wave in branch j caused by the incident wave in branch i. Using Kirchhoff's Current Law (KCL), it can be shown that

$$\sum_{i=1}^{n} E_{r,ji} = \mathbf{0}. \tag{2}$$

Therefore, when all the branches are driven in-phase, due to superposition, reflection of each branch is canceled out. In other words, simply by connecting different branches and having a global power match, there would be no power loss due to reflection. By eliminating the complex corporate power-combining network, the passive loss is significantly reduced.

D. Simulation and Layout Methodology

The die photo of the amplifier is shown in Fig. 7. The circuit was simulated in ADS [36]. Electromagnetic simulations using IE3D [23] were performed to design the coplanar tapers and verify transmission line models and nonidealities, such as bends and T-junctions. Modal analysis of the combining stage using the method described in [37] showed no sign of odd-mode instability.

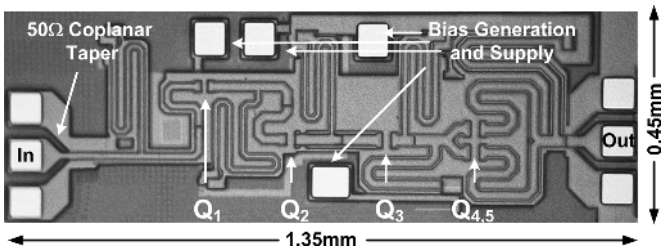

Fig. 7. Die micrograph of the 77-GHz power amplifier, chip size: 1.35×0.45 mm^2.

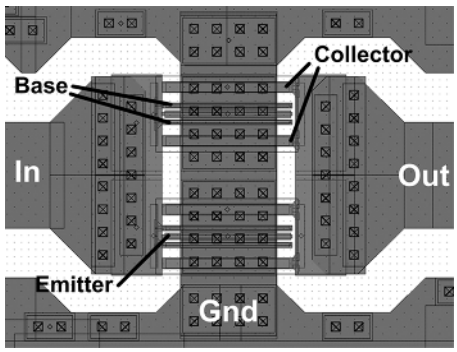

Fig. 8. Layout of one of the output parallel branches consisting of two transistors (depicted as Q_5 in the amplifier schematic and layout).

Parasitic capacitors are extracted on local nodes where the capacitance is not part of the distributed transmission-line structure. These nodes include connections to transistors, where the signal line is closer to the substrate. Parasitic collector-base capacitance is very important as it will be multiplied by the Miller factor and will appear at the input or might even cause oscillation. A careful layout minimizes the overlap of the collector and base connections.

The largest ratio of parasitic capacitance to device capacitance (around 60%) occurs at the output of the first stage, with 16.5 fF of parasitic capacitance. The layout of one of the output stage parallel branches is shown in Fig. 8. Each transistor has two base and collector contacts, where the spacing between transistors is dictated by design rules. Instead of a larger transistor with 32-μm emitter length, which has a lower $f_{\max}$, two 18-μm parallel transistors are used.

E. Transmitter Image-Rejection Filter

The power amplifier is designed to be used in a 77-GHz superheterodyne transmitter employing 26 GHz as the IF frequency [7]. In this case, the upconversion from 26 GHz to 77 GHz is done with a double-sideband mixer and the image signal at 26 GHz needs to be attenuated. While this can be achieved by making the PA narrowband, a better approach is to design broadband RF stages that are immune to process variations and use a separate image rejection filter. The notch frequency in the filter is controlled by the physical length of the transmission lines, which is set by lithography. Therefore, a third-order high-pass Chebyshev-I filter was designed and incorporated prior to the PA. Fig. 9(a) shows the schematic of the image-rejection filter. By using perfectly shorted parallel stubs, the attenuation of the filter at 26 GHz was 18 dB. By adding small capacitors to the end of the parallel stubs, a notch was introduced at the image frequency and the rejection of the filter was increased to 35 dB. To test the filter separately, a test structure was fabricated and connected to GSG pads through tapered lines [Fig. 9(b)]. Measurement results of the filter test structure shown in Fig. 9(c) and (d) reveal a good match with the simulation results. The insertion loss of the filter at 77 GHz, tested separately in a waveguide-based setup, is 2 dB.

V. Measurement Results

The small-signal gain of the amplifier has been measured with an HP 8757E scalar network analyzer. The network analyzer sweeps the output frequency of a high-power W-band backwave oscillator (BWO) from Resonance Instruments Inc. This is done with a 705B millimeter-wave sweeper from Micro-Now Instrument Company. The signal is fed through a WR-10 waveguide to a Pico-Probe WR-10 GSG probe. To calibrate the network analyzer, first a thru measurement was done and then the thru was replaced by the PA.

The BWO output power changes with frequency. To measure large-signal parameters of the amplifier, as shown in Fig. 10, a variable attenuator (Millitech DRA-10-R000) with Agilent W8486A W-band power sensor was used. The loss of the probe was measured and de-embedded.

The simulated and measured small-signal gain of the standalone PA is shown in Fig. 11. The amplifier has a peak gain of 17 dB around 75 GHz. Normally, the W-band waveguide measurement setup is used for the 75–110-GHz band. The TE10 mode cutoff frequency for this waveguide is 59 GHz, and it will not significantly affect the measurement results in the 65–75 GHz range. The amplifier has a 3-dB bandwidth of at least 15 GHz and has more than 6 dB gain up to 92 GHz. An acceptable match between simulated and measured results is observed. The ripple in the gain measurement is due to the BWO output power fluctuations and detector nonlinearity in the scalar network analyzer.

The large-signal parameters of the amplifier are measured and plotted in Fig. 12. This measurement is done with a supply voltage of 1.5 V. The amplifier can generate up to +16 dBm of output power, with a compressed gain of 10 dB. A peak PAE of 12.8% is achieved at the peak output power. The output-referred 1-dB compression point of the amplifier is +14.5 dBm. Additional gain and power in the input stages force the output stage to compress first.

The variation of the saturated output power and amplifier PAE versus supply voltage is measured and shown in Fig. 13. Here the amplifier is driven with a constant +6-dBm input power. Peak output power of 17.5 dBm can be generated with a supply voltage of 1.8 V. The amplifier reliably operates above the $\mathrm{BV_{CEO}}$ limit with no performance degradation observed during measurements.

The measured saturated power, gain, and PAE of the amplifier versus frequency are shown in Fig. 14. In this case the supply voltage is 1.5 V. Peak power and maximum PAE happen at 77 GHz, showing the effectiveness of the large-signal power match design methodology outlined in Section IV-B. The measured performance of the amplifier is summarized in Table I.

VI. Conclusion

Conductor-backed coplanar waveguide (CBCPW) structure with a high degree of on-chip isolation has been used to make a

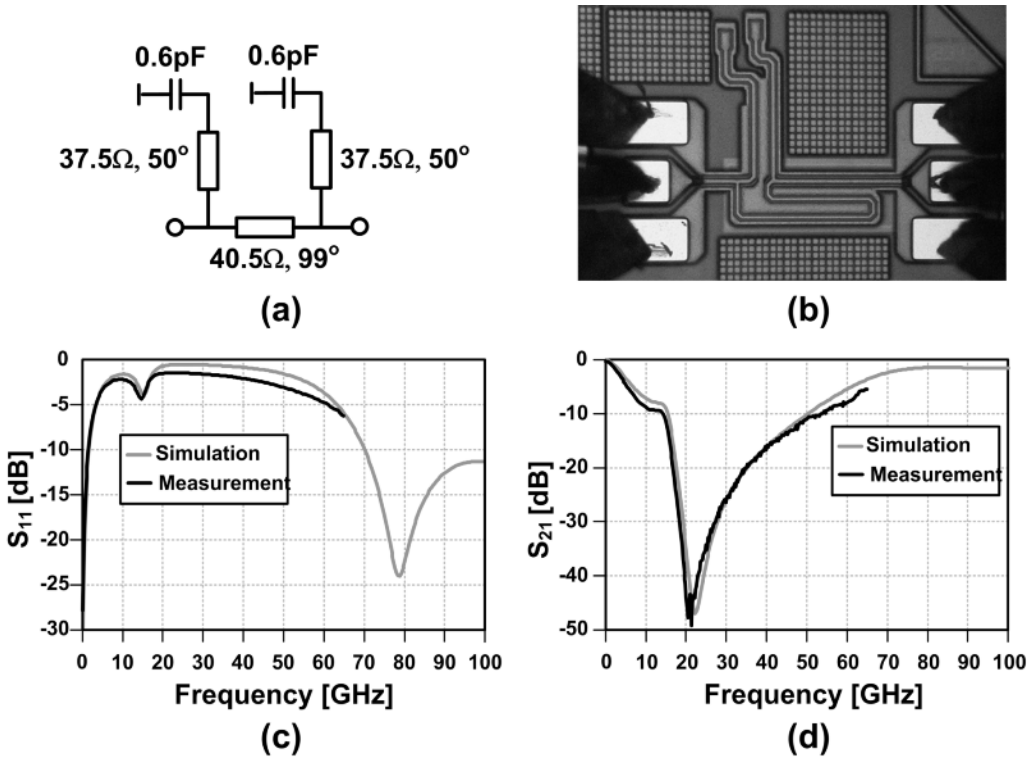

Fig. 9. (a) Schematic of the transmitter IF filter. (b) Layout of the filter test structure. (c) Simulated and measured reflection coefficient (S_{11}). (d) Transmission coefficient (S_{21}) of the filter test structure.

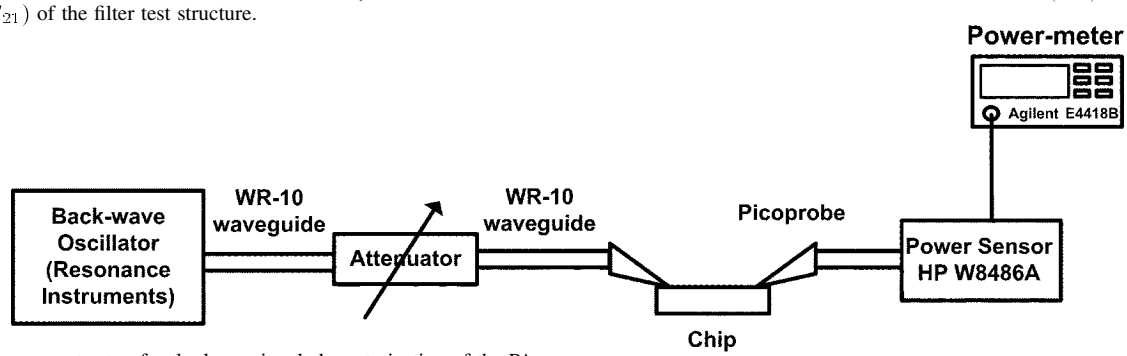

Fig. 10. Measurement setup for the large-signal characterization of the PA.

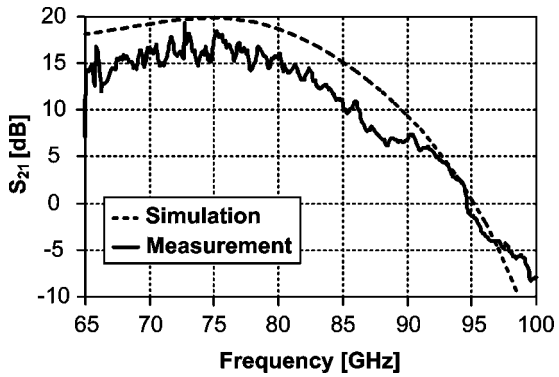

Fig. 11. Small-signal gain (S_{21}) of the amplifier simulated and measured between 65 and 100 GHz.

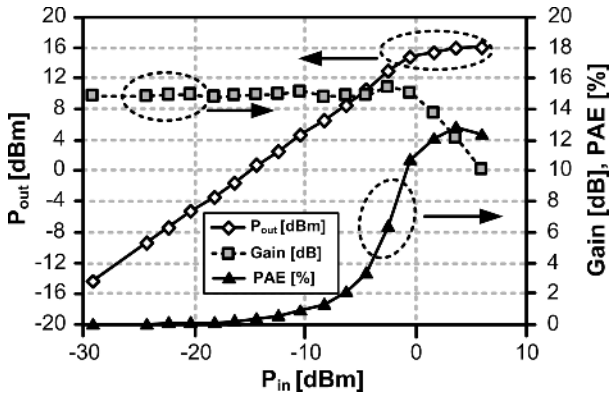

Fig. 12. Measured large-signal parameters of the amplifier at 77 GHz.

77-GHz power amplifier, fully integrated in a 0.12-μm BiCMOS SiGe process. The use of side-shields improves the on-chip isolation between adjacent parallel transmission lines by more than 20 dB. This large isolation enables tight meandering of the transmission lines, resulting in a small area of 0.6 mm^2 for the amplifier. It also facilitates the realization of a single-chip 77-GHz transceiver with on-chip power amplifiers co-integrated with sensitive elements, such as an on-chip VCO and antennas [7], [8]. The amplifier has more than 6-dB small-signal gain over a frequency range of 65–92 GHz. The measurement of the gain at the frequencies lower than 65 GHz is limited by frequency range of the waveguide measurement setup. Interstage large-signal power matching has resulted in the peak power and PAE occurring at the desired frequency of 77 GHz. By proper

TABLE II
COMPARISON

	Freq.	Device	P_{out} [dBm]	PAE_{max} [%]	Small-Signal Gain [dB]	Compressed Gain [dB]	Reference
Silicon Based PAs	**77GHz**	**0.12 μm SiGe**	**17.5**	**12.8**	**17**	**12**	**This Work**
	77GHz	0.12 μm SiGe	9.5	3.5	6.1	5	Pfeiffer *et al.* [2]
	61GHz	0.12 μm SiGe	13.2	4.3	10.8	-	Floyd *et al.* [3]
	77GHz	0.2 μm SiGe	15.5	5.4	-	-	Li *et al.* [4]
	85GHz	0.12 μm SiGe	21	3.4	-	8	Afshari *et al.* [9]
III-V Based PAs	62GHz	0.1 μm pHEMPT	27.5	21	13.5	9.8	Tang *et al.* [10]
	60GHz	0.1 μm InP HEMT	23.5	43	11	7.5	Kong *et al.* [11]
	95GHz	0.15 μm InP HEMT	26.1	20	12	8.9	Ingram *et al.* [12]
	62GHz	0.15 μm InP HEMT	27.1	25	20	15	Chen *et al.* [13]

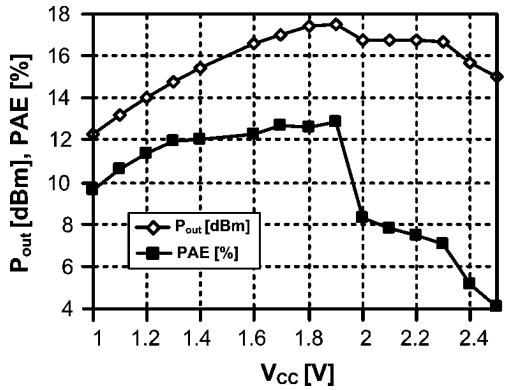

Fig. 13. Measured saturated power and PAE for a supply range of 1–2.5 V.

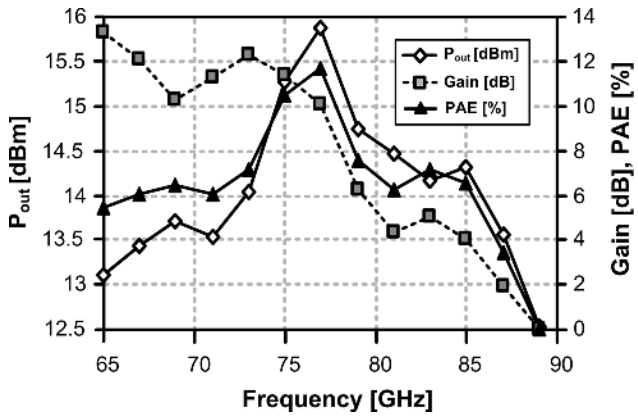

Fig. 14. Measured saturated power, gain, and PAE versus frequency.

choice of the bias circuitry impedance in the base, the amplifier operates reliably above the BV_{CEO} range and can be used with a supply voltage range of 1 to 2.5 V. The amplifier achieves the best combination of output power, efficiency, and gain using silicon technology at mm-wave band. A comparison of the power amplifier in this work and previous work on single-path (not externally-combined) mm-wave power amplifiers is presented in Table II.[1]

[1]References [2]–[4] add 3 dBm to the measured output power, as two amplifiers in parallel can deliver 3 dBm higher power to a 100-Ω differential load. This is true for any single-ended amplifier matched to a 50-Ω load, therefore for comparison this extra 3-dBm factor was not included in Table II.

TABLE I
AMPLIFIER PERFORMANCE SUMMARY

Process	0.12 μm SiGe BiCMOS
Frequency Range (gain > 6 dB)	65-96 GHz
Saturated Output Power (@ V_{cc} = 1.8 V, I_{cc}=225 mA)	17.5 dBm
Peak PAE	12.8%
3 dB Bandwidth (fractional bandwidth)	15 GHz (20%)
Small-Signal Power Gain @ 77 GHz	17 dB
Output-referred 1dB Compression Point (@ V_{cc} = 1.5 V, I_{cc}=180 mA)	14.5 dBm
Area	0.6 mm^2
Supply Range	1 V - 2.5 V
Current Consumption (@ V_{cc} = 1.8 V)	165 mA

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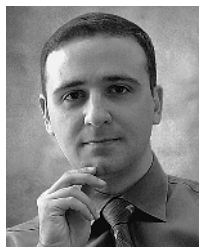

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