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2.2 A Wideband Beamformer for a Phased-Array 60GHz Receiver in 40nm Digital CMOS

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For high-data-rate wireless communication in the 7GHz band around 60GHz, the IEEE 802.15.3c standard [1] provides channels with a 0.88GHz bandwidth for the AV-OFDM mode. For the single-carrier modes, the ECMA 387 standard [2] foresees the possibility of bonding together adjacent channels, yielding higher data-rates. Radios for these 60GHz standards often use phased antenna arrays to relax the link budget. A phased-array receiver needs a variable phase shift on each antenna path and a combiner that sums the signals from the individual paths after phase shifting. The beamforming circuitry presented here handles 4 paths. It can operate both with one 0.88GHz channel and with bonding of two such channels. Phase shifts are realized with a resolution better than 20°. Bandwidth is high thanks to the use of current amplifiers with very low input impedance.

Phased-array receivers that implement beamforming in the RF signal path [3,4] suffer from large losses and need a high power consumption to overcome this. As an alternative, phase shifting in the LO paths [5] requires duplication of the I/Q mixers, but this is a limited overhead. However, it extends the LO buffering causing an increase in power consumption. In this design beamforming is implemented entirely at analog baseband. It requires less LO buffering, and is more robust because it is less sensitive to parasitics than mm-Wave frequency circuits.

The beamformer (see Fig. 2.2.1) fits in a direct downconversion receiver which yields baseband I and Q components for the received signal at each path. Those signals must be individually phase-shifted and combined to generate a single beamformed I/Q output. For path *m (m = 1,…, 4)* a phase shift φ is obtained from the I and Q components I_m and Q_m as follows:

$$I'_m = A\left[\cos(\varphi)I_m - \sin(\varphi)Q_m\right]$$
$$Q'_m = A\left[\sin(\varphi)I_m + \cos(\varphi)Q_m\right] \quad (1)$$

Factor *A* is an overall gain factor. The signals I_m and Q_m are the current outputs of the I/Q mixers. The phase-shifted replicas I'_m and Q'_m are also generated in the current domain, as currents are easier to combine than voltages. Therefore, phase shifters are implemented using 4 digitally controlled variable-gain current amplifiers (VGAs). Using switches as in [6], would limit phase resolution to 90 degrees. Further, the signals are combined in two levels (see Fig. 2.2.1). For a phased-array receiver with many antenna paths, there is an inevitable long distance between the output of the RF mixers at the extreme sides of the chip and the output after the final signal combination. To bridge these distances, repeaters are provided in the form of current amplifiers. Signals are combined at the inputs of these repeaters. Because of the signal combination at baseband these long distances are not bridged at RF, yielding lower power consumption for the repeaters and less sensitivity to losses and parasitics. The last combining stage is a transimpedance amplifier (TIA) providing a low output impedance.

The current amplifiers (see Fig. 2.2.2) have very low input impedance R_{in} due to the combination of common-gate stages (M_{1a-b}) and resistive shunt feedback (R_{fa-b}). The output impedance at the drains of M_{4a-d} is high. The use of two parallel branches (M_{4a-b} and M_{4c-d}) yields a coverage of the 4 quadrants in the complex I/Q plane. The current gain is the product of g_{m4} and R_f, where R_f is used to control the gain *A* in (1), whereas gm_4 steering sets the values for either *sin(φ)* or *cos(φ)*, both of which are digitally adjustable. The current amplifier acts as the load of the mixer described in [7], which only requires one transistor per branch between the inputs (in_a and in_b) and DC ground so that headroom problems are avoided. This transistor is included in the fabricated design.

The repeaters that bridge the long interconnects are similar to the current amplifiers, except that the branch with M_{4c-d} is omitted and the gates of M_{4a-b} are fixed to V_{DD}. The cascade of phase shifters and repeaters has a large bandwidth in spite of the parasitic capacitance C_{inter} of the interconnects, as the pole $-1/(R_{in}C_{inter})$ occurs at very high frequencies due to the very low value of R_{in}.

The TIA has the same input stage as the current amplifier, but low output impedance by applying resistive shunt feedback (via R_{fa-b}) at the output of source followers M_{3a-b}.

The circuit is fabricated in a 1P7M digital 40nm low-power CMOS technology. The chip (see Fig. 2.2.7), with an area of 2mm^2, is heavily bond pad limited. The area consumed by the phaseshifter is only 0.03mm^2. The chip consumes 35mW from a 1.1V V_{DD}. Power consumption per phase shifter is 7mW (including a branch shared with the mixer), which is similar to the LO phase shifter of [5]. However, LO buffering is much more demanding for the latter approach.

The chip is measured in a 50Ω system using off-chip baluns at input and output. Bandwidth is evaluated by deriving the overall transimpedance from S-parameters with one path active and for different gain settings (R_f values) of the amplifiers (see Fig. 2.2.3, Fig. 2.2.6 top). Clearly, bandwidth is sufficient for bonding of 2 channels.

Phase shifts are derived from a lookup table with gains of a single VGA (Fig. 2.2.4 left) as a function of the DAC settings at the gate of the M_4 transistors, which change g_{m4}. This method could be fully automated by applying an internal input signal (e.g. from a low frequency DAC) and measuring the amplitudes with an ADC at the end of the receiver chain. Phase shift is applied by checking the correct gain setting in the table to match *sin(φ)* or *cos(φ)* for a given φ. This approach is verified using an arbitrary waveform generator (AWG) providing I/Q signals for one path (Fig. 2.2.4) and observing output signals on an oscilloscope. The phase resolution in the vicinity of 0, 90, 180 and 270 degrees is limited by the resolution of the DAC.

The constructive combination of signals from all paths, measured at 500MHz, is shown in Fig. 2.2.5.

Noise is measured at the TIA output by presenting an open circuit to the input of one path and with other paths turned off (see Fig. 2.2.6, bottom).

The IP3 and 1dB compression point are measured at 500MHz (see Fig. 2.2.6, middle) by exciting the I inputs of all paths. Output IP3 is -6dBV, which is satisfactory as the signal strength right after downconversion is not yet high.

The presented circuit is the first beamformer that meets the specifications for 0.88GHz channels as provided in the AV-OFDM mode of IEEE 802.15.3c and has enough bandwidth to accommodate bonding of two such channels.

Acknowledgements:
The authors thank their colleagues from the INVOMEC division and P. Van Wesemael for support in digital synthesis and layout and V. Szortyka for support with the measurements.

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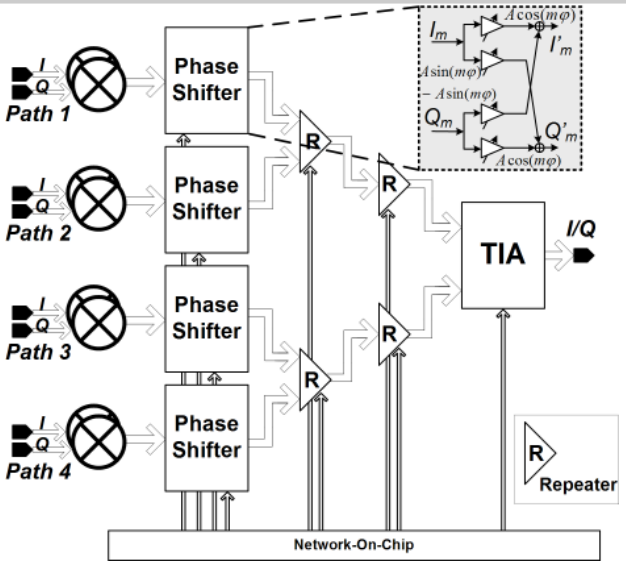

Figure 2.2.1: Architecture of the beamformer.

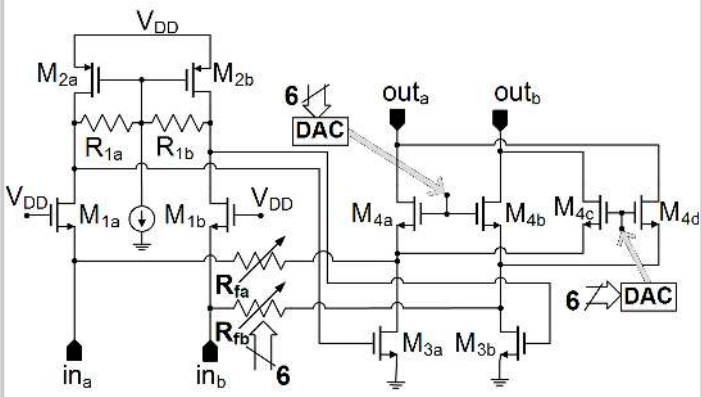

Figure 2.2.2: Simplified schematics of a variable current amplifier, combiner or repeater.

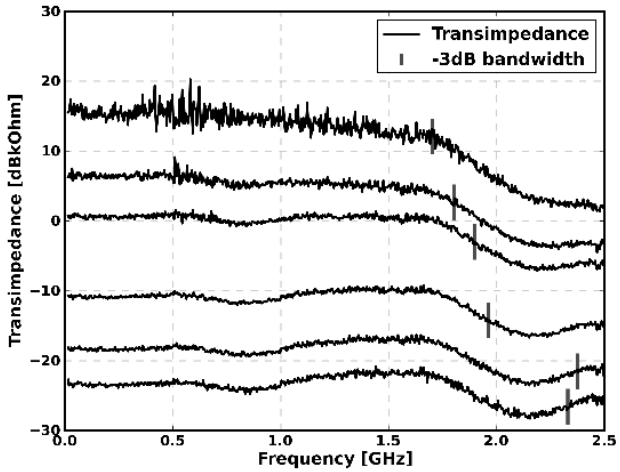

Figure 2.2.3: Overall transimpedance for different feedback settings (Rf values) in all amplifiers.

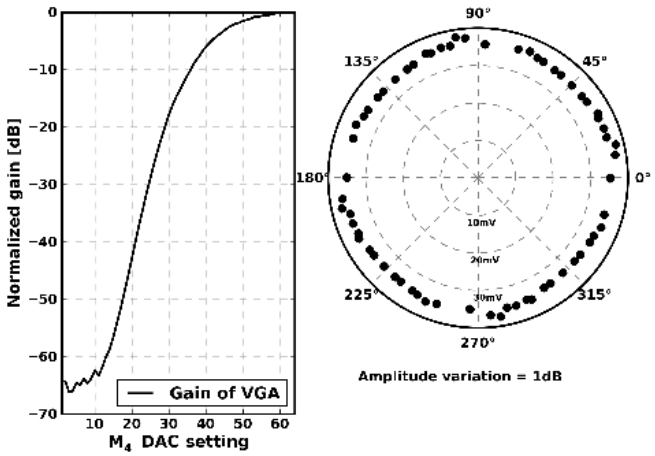

Figure 2.2.4: Gain of one current amplifier as a function of the DAC bit settings at the gate of the M4 transistors (left); phase and output amplitude at 500MHz (right).

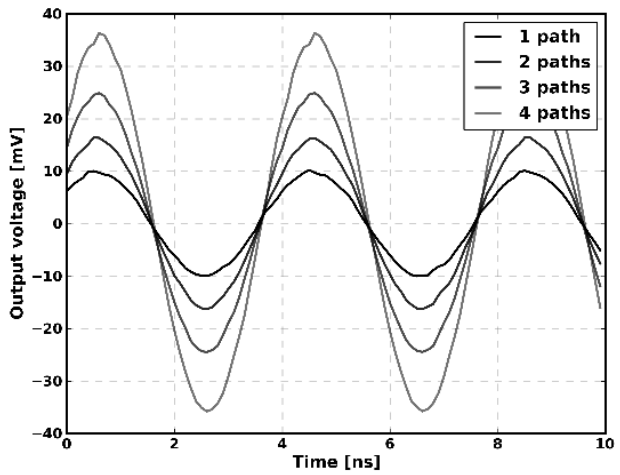

Figure 2.2.5: Measured signal combination at 500 MHz: 1, 2, 3 and 4 paths. Distortion in the waveforms is caused by the AWG.

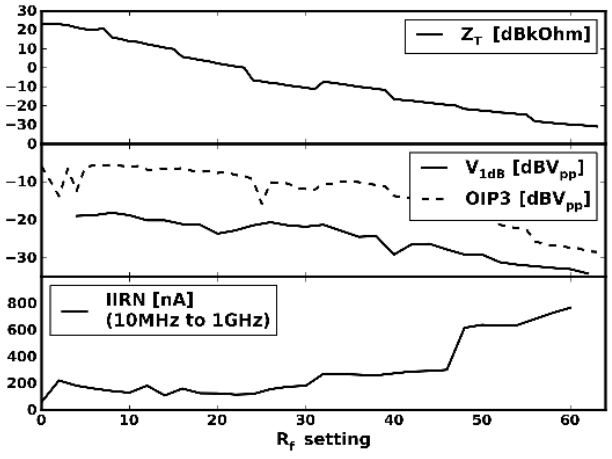

Figure 2.2.6: Measured transimpedance (ZT), third-order intercept point, 1dB compression point and input-referred noise current (integrated from 10 MHz to 1 GHz).

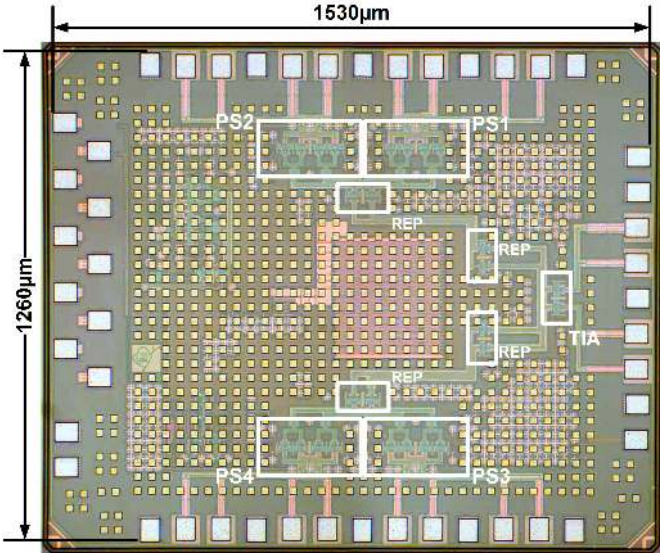

Figure 2.2.7: Chip micrograph.

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