# A Wideband CMOS Variable Gain Amplifier With an Exponential Gain Control

Hui Dong Lee, *Student Member, IEEE*, Kyung Ai Lee, and Songcheol Hong, *Member, IEEE*

***Abstract*—A CMOS wideband cascaded variable gain amplifier (VGA) with a temperature-independent exponential gain control characteristic is presented in this paper. The exponential gain control function is realized using parasitic bipolar transistors and a control signal converter. The bandwidth is extended using an inductive peaking technique for high-frequency operations. The gain of the VGA varies from −38.8 to 55.3 dB in relation to the control voltage that varies from 0 to 1.8 V. The bandwidth of the proposed VGA is approximately 900 MHz with a gain control range of 94.1 dB. The proposed VGA includes a dc offset cancellation loop to avoid amplification of the dc offset. The VGA is powered by 1.8 V with 11.4 mA. The VGA chip including bondpads occupies an area of 850 $\mu$m × 490 $\mu$m.**

***Index Terms*—CMOS analog integrated circuit, gain control, linear-in-decibel gain characteristic, temperature compensation, variable gain amplifier (VGA), wideband systems.**

## I. Introduction

THE variable gain amplifier (VGA) is an indispensable building block to maximize the dynamic range of modern wireless communication systems [1]–[3], as well as medical equipment, hearing aids, disk drives, and so on [4]–[7]. A VGA is typically employed in a feedback loop to realize automatic gain control (AGC). The VGA of an AGC loop is used to control the transmission signal power or to adjust the received signal amplitude.

There are two possible approaches to build the VGA. One is to build a discrete gain step VGA with a digital control signal [8]–[10], and the other is to build a continuous VGA controlled by an analog gain control signal [1]–[7]. In general, digitally controlled VGAs use binary weighted arrays of resistors or capacitors for gain variations [11] and analog VGAs adopt a variable transconductance or a variable resistance to control the gain. For a code division multiple access (CDMA) system requiring a power control range larger than 80 dB, the VGA with continuously variable gains is preferred because it avoids signal phase discontinuity that is expected to cause problems [3], [12] and it reduces the large number of control bits required with digitally controlled VGAs. Until now, VGA circuits based on various technologies such as bipolar, BiCMOS, and CMOS have been introduced [1]–[12]. Recently however, CMOS VGAs are preferred due to the low cost and easy integration with other CMOS analog/digital parts.

An important requirement for a CMOS VGA is a decibel-linear gain control characteristic, where the gain of the VGA changes exponentially with the control signal. The exponential gain control is required to achieve a wide dynamic range and to maintain the AGC loop settling time independent of the input signal level [12], [13]. However, it is difficult to realize this exponential function due to its inherent square or linear characteristics in CMOS technology. Although a transistor operating in a subthreshold region has an exponential characteristic, it is generally not preferred due to other unfavorable effects such as noise and bandwidth [14]. Another possible method is to use parasitic bipolar transistors to generate the desired exponential function. The linear-in-decibel gain control signal is generated using the relationship between a collector current $(I_C)$ and base-to-emitter voltage $(V_{\rm BE})$. This is strongly dependent on the temperature and processes. Therefore, various compensation techniques that guard against the temperature and the process variations are required to have an accurate signal power control mechanism. Obviously, temperature compensation is needed to control the output level in a linear-in-decibel manner over a wide dynamic range [15]. It is also preferable to minimize the resolution of the digital-to-analog converter, which drives the gain control terminal [12]. The method used to generate the temperature-independent exponential function requires complex circuits However, this method achieves a linear-in-decibel controlled range of more than 30 dB per stage, which is difficult to achieve using a pseudoexponential function in a short-channel CMOS.

Another important aspect of a wideband VGA is a large bandwidth. There are many systems for high-speed data communications such as ultra-wideband (UWB) systems, wireless local area networks (LANs), and Bluetooth [16], [17]. These systems provide a high data rate with relatively low power consumption in short-range wireless communications. For high-speed data communication, the bandwidth of a VGA must be very wide. Therefore, a wideband VGA is a key component.

In this paper, we introduce a wideband CMOS VGA with an exponential function generation. We discuss the VGA implementations in the view of the bandwidth and the obtainable gain range and, for that purpose, we compare some recently reported VGAs in Section II. In Section III, the method required to generate the exponential function is discussed and the simulation results are shown to prove the validity of the proposed

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The authors are with the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology, Daejeon 305-701, Korea (e-mail: eelove@kaist.ac.kr; kalee@eeinfo.kaist.ac.kr; schong@ee.kaist.ac.kr).

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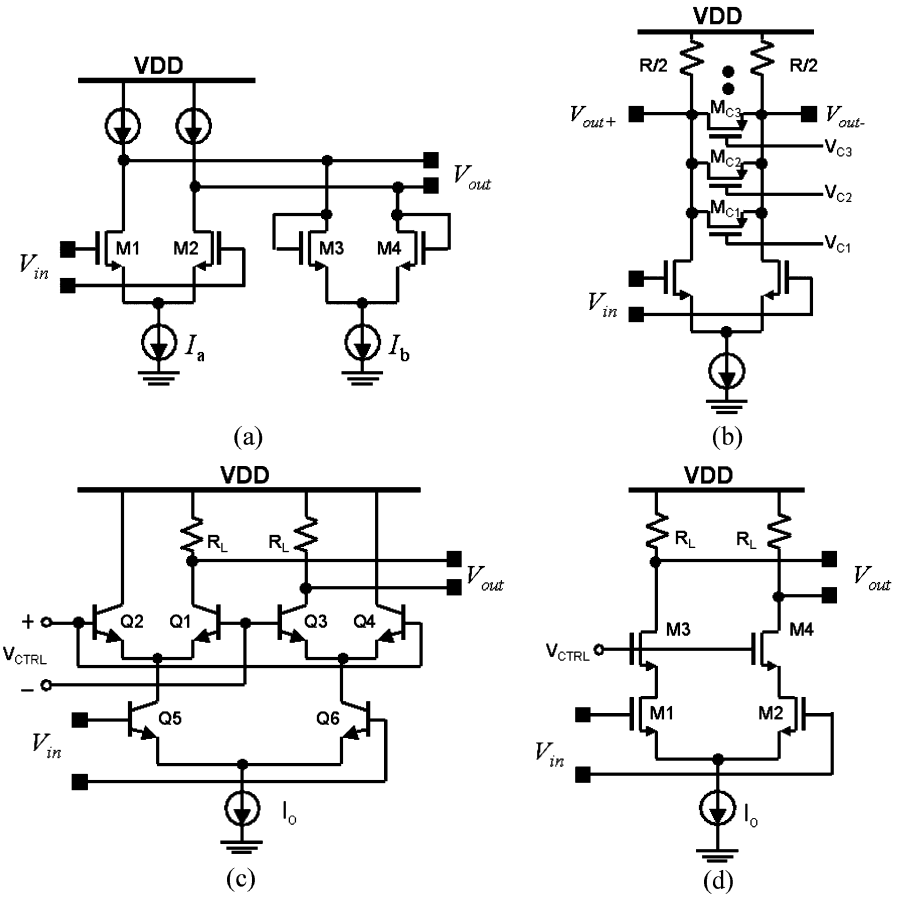


Fig. 1. Four types of VGA topologies.

approach. The proposed VGA is presented in Section IV, which also includes a detailed description of the circuit topology. The measured performance and conclusion follow in Sections V and VI, respectively.

## II. Comparison of VGA Circuits

There have been some challenges in the design of the VGAs to meet gain-control accuracy, stability, and linearity requirements. Here, the design techniques from previously presented CMOS VGAs focusing on both VGA cells with various gain control schemes and linear-in-decibel gain variation characteristics are discussed.

Most CMOS VGAs use a pseudoexponential function [4]–[6] expressed as $e^x \approx (1+x)/(1-x)$ for decibel-linear gain control characteristics. As shown in Fig. 1(a), the core of the VGA consists of a differential amplifier and diode connected loads. The differential gain of the VGA in Fig. 1(a) is equal to $g_{m-\mathrm{M1,2}}\, R_{\mathrm{out}}$, where $g_{m-\mathrm{M1,2}}$ is the transconductance of the input differential pair and $R_{\mathrm{out}}$ is the output impedance. Since the output is a diode connected load, $R_{\mathrm{out}}$ is proportional to $1/g_{m-\mathrm{M3,4}}$. Since $g_{m-\mathrm{M1,2}}$ and $g_{m-\mathrm{M3,4}}$ are functions of the bias current, the gain variation is obtained by controlling the bias currents of the input pair $(I_a)$ and diode loads $(I_b)$. CMOS-based VGAs that adopt this function offer less than 15 dB of gain range with a linearity error of less than $\pm 0.5$ dB [4]–[6]. Owing to the limited gain range in recent research, multiple stage VGAs have been used to satisfy the required dynamic gain range of wireless systems. To improve the gain control range, the control currents ($I_a$ and $I_b$) are generated by (1) based on the Taylor series approximation function [18]. The core VGA circuit is the same, i.e.,

$$e^{2ax} = \frac{e^{ax}}{e^{-ax}} \cong \frac{[k+(1+ax)^2]}{[k+(1-ax)^2]} \tag{1}$$

where $a$ and $k$ are fixed and $x$ is the independent control variable. The VGA exhibits a gain control range of more than 35 dB with a gain error of less than $\pm 1$ dB through the optimization of the values of $a$ and $k$; however, its operating frequency varies with the control currents.

In Fig. 1(b), the quasi-exponential function of a successive approximation was realized using a simple $R-r$ attenuation with a combination of the constant resistance $R$ of the rigid resistor and the variable resistance $r$ of the combined triode of MOSFETs [19], [20]. The $R-r$ attenuation can be expressed as $1/(1+R\times g_{\mathrm{ds}})$. Accordingly, we can approximate $1/(1+R\times g_{\mathrm{ds}})$ to $\exp(-2R\times g_{\mathrm{ds}})$. It is well known that $g_{\mathrm{ds}}$ is proportional to the gate source voltage $(g_{\mathrm{ds}} \propto V_{\mathrm{gs}})$ in the triode region. Thus, we can control the gain of the $R-r$ attenuator in the exponential function. In this scheme, as the control voltage increases, the quasi-exponential curve expands more and more by successive approximations. In addition, the more MOSFETs that are turned on, the wider the piecewise exponential curve becomes. This results from the overlap conductance of the MOSFETs previously turned on. However, using only a single stage

of the $R-r$ attenuation is not satisfactory to obtain the exponential function in the required dynamic range.

Fig. 1(c) shows a signal-summing VGA, which has advantageous low noise and low distortion characteristics [21], [22]. The signal-summing VGA can operate at a high frequency because the gain control stages are common base transistors. However, an unusable gain control range of approximately 20 dB remains around the maximum gain in this type of linear-in-decibel VGA. This unusable range damages the noise performance and reduces the operable gain range. In a bipolar linear-in-decibel VGA, a temperature stabilizing technique with an additional temperature-dependent current has been proposed [23]. However, this stabilizing technique itself is sensitive to the device parameters of temperature, and the reported results have shown that the variable gain characteristic is still sensitive to temperature. A MOSFET equivalent circuit, which can use the entire MOSFET's operation region from the square law region to the exponential law region, has also been reported [24]. However, its performance in high-frequency response, noise, gain, and gain error was lower than that of the bipolar linear-in-decibel VGA when compared [23].

To achieve both a high bandwidth over several hundred megahertz and a wide dynamic range, the CMOS VGA cell based on a differential cascode structure with a resistor load [25], as shown in Fig. 1(d), has been reported. By controlling the operating point of the input transistors (transistors M1 and M2) of the cascode amplifier in the VGA cell from saturation to the linear region, it is possible to control the transconductances of the MOSFETs and the linear range of input transistors with a low distortion without sacrificing bandwidth. It is also possible to maintain a good high-frequency characteristic by applying a constant tail current source $(I_0)$. This has achieved a high bandwidth characteristic using a cascode structure. However, it is difficult for a structure with a resistor load to operate with a comparable performance at a low voltage because there is no headroom for a larger output voltage swing. As reported in [2], the CMOS VGA adopts a differential cascode structure and a differential structure using the pseudoexponential function in Fig. 1(a). For a low-voltage and high-frequency operation, the CMOS VGA uses an active load instead of a resistive load. The current sharing bias scheme with a constant current also improves the dynamic range and linearity. However, the bandwidth of 350 MHz is insufficient for CDMA UWB operations.

From the viewpoint of a high-frequency and low-power operation, the cascode VGA and the VGA with $R-r$ attenuation are superior among the four types of VGAs presented here. For a wide dynamic range, the cascode VGA and the modified pseudoexponential function VGA are preferred. We adopted a cascode VGA with active loads because it is expected to provide the high-frequency operation and wide gain control range.

## III. Proposed Exponential Function Generator

Fig. 2 depicts the block diagram of the exponential function generator with compensation circuits. It consists of a voltage-to-current converter (VIC), a linear current multiplier, and an exponential function generator. An external control voltage $V_{\rm EXT}$ is converted to a control current $I_{\rm EXT}$ by the VIC. The current $I_{\rm EXT}$ is then linearly multiplied and compensated by the linear

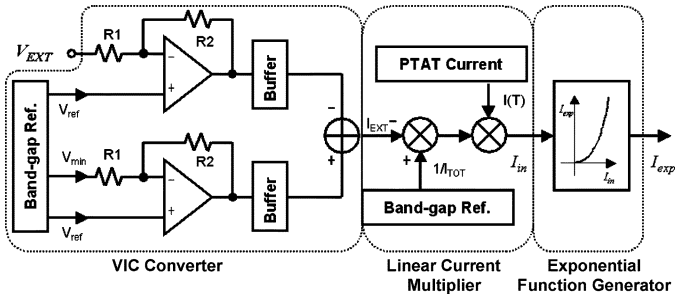


Fig. 2. Block diagram of the proposed exponential current generator.

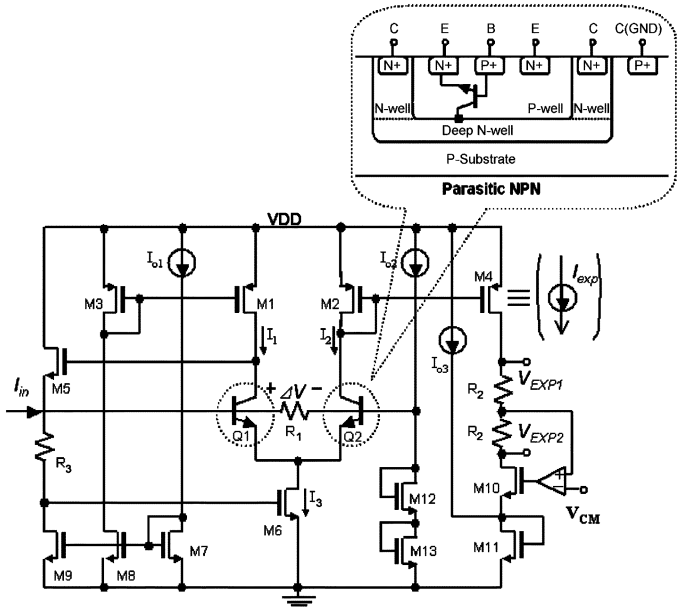


Fig. 3. Exponential function generator using parasitic NPN transistors (Q1 and Q2).

multiplier. Finally, the compensated linear current $I_{\rm in}$ is transformed to an exponential current $I_{\rm exp}$ using the exponential generator.

### A. Exponential Function Generator

Fig. 3 shows the exponential function generator and the cross section of a parasitic NPN transistor, which was used as Q1 and Q2. Today, most of the CMOS foundries provide the deep n-well technology. The deep n-well CMOS gives a chance to apply a different substrate bias to nMOS residing in another p-well, as well as excellent isolation against the substrate coupling noise between digital logic circuits and analog circuits [26]. We could obtain a high-performance NPN transistor whose current gain is almost 20, better than that of a conventional parasitic PNP transistor, $2 \sim 3$. Thus, we used this parasitic NPN transistor. The operation of exponential function generator is as follows.

The input control current $I_{\rm in}$ generates a voltage drop of $\Delta V = I_{\rm in} \times R_1$ between the bases of parasitic NPN transistors Q1 and Q2. Due to the exponential nature of Q1 and Q2, the collector currents $I_1$ and $I_2$ are $I_S \cdot \exp(V_{{\rm BE},Q1}/V_T)$ and $I_1 \cdot \exp(-\Delta V/V_T)$, respectively, where $I_S$ indicates the reverse saturation current of Q1 and Q2, and $V_{{\rm BE},Q1}$ denotes the base emitter voltage of Q1. As the current $I_1$ mirroring the constant

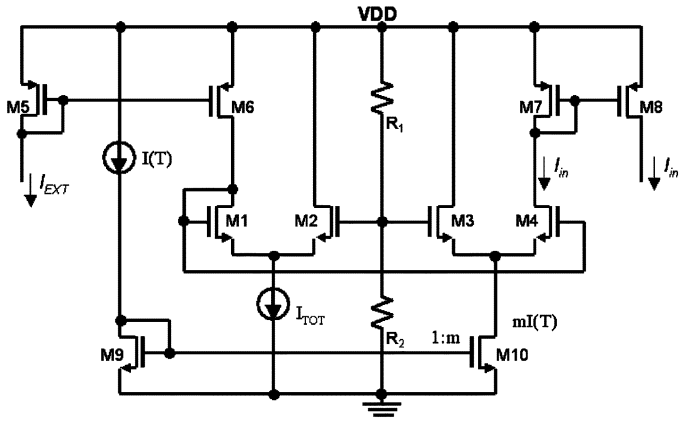


Fig. 4. Linear current multiplier.

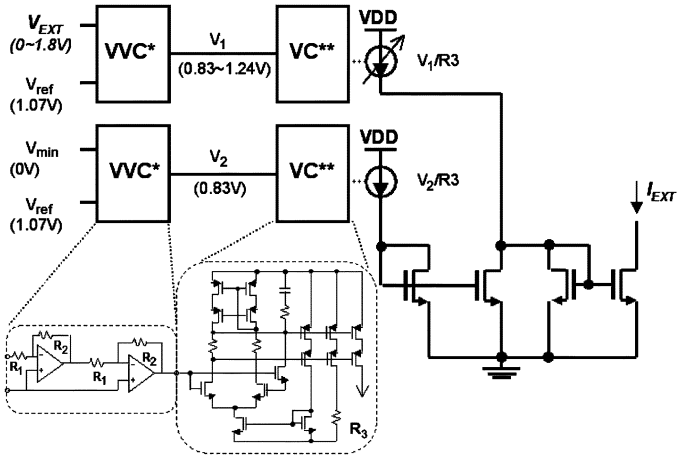


Fig. 5. VIC: *VVC and **VC denote the voltage-to-voltage converter and voltage copier, respectively.

current $I_{o1}$ is also constant, the current $I_2$ has an exponential characteristic as a function of $\Delta V$. The MOSFET transistors M2 and M4 perform the role of the current source mirroring the same current $I_2$. The output exponential current $I_{\exp}$ obtained through the current mirroring is then given by

$$I_{\exp} = I_1 \exp\left(\frac{-I_{\text{in}} \cdot R_1}{V_T}\right). \tag{2}$$

Accordingly, the output voltage difference $V_{\exp}$ between $V_{\text{EXP1}}$ and $V_{\text{EXP2}}$ has an exponential function, which is given by

$$V_{\exp} = V_{\text{EXP1}} - V_{\text{EXP2}} = 2R_2 I_{\exp} = 2R_2 I_1 \exp\left(\frac{-I_{\text{in}} \cdot R_1}{V_T}\right). \tag{3}$$

### B. Linear Current Multiplier

The linear current multiplier is realized using a current divider consisting of a differential pair, as shown in Fig. 4. Equations (2) and (3) include the thermal voltage $V_T$. This implies that the current varies with the temperature. The current $I_{\text{in}}$ should be proportional to absolute temperature (PTAT) current to compensate for the gain variation. $I(T)$ indicates a PTAT current from the PTAT bias circuit [27]. The control current $I_{\text{EXT}}$ and the constant current $I_{\text{TOT}}$ are independent of the temperature and supply voltage. These features will be explained in Section III-C regarding the VIC block. The gate-to-gate voltage of the differential pair (M3 and M4) is copied from the differential pair M1 and M2. Thus, the current dividing ratio for $I_{\text{in}}/mI(T)$ tracks $I_{\text{EXT}}/I_{\text{TOT}}$, where the input current $I_{\text{EXT}}$ is a control signal of the multiplier $(0 \leq I_{\text{EXT}} \leq I_{\text{TOT}})$ and $m$ is the size ratio of the mirroring CMOS devices. Thus, the output current $I_{\text{in}}$ is given by

$$I_{\text{in}} = mI(T) \cdot I_{\text{EXT}}/I_{\text{TOT}}. \tag{4}$$

This output current $I_{\text{in}}$ is fed to the exponential current generator. It is independent of the supply voltage variation and is linearly dependent on the absolute temperature.

### C. VIC

Fig. 5 shows the schematic of the VIC. The constant voltages $V_{\min}$ and $V_{\text{ref}}$ can be generated from the bandgap reference circuit and its buffers; the external control voltage $V_{\text{EXT}}$ can be varied from 0 to 1.8 V. In the figure, VVC indicates the voltage-to-voltage converter and VC denotes the voltage copier and its current generation. $V_{\text{EXT}}$ is converted to the control current $V_1/R3$ by the VVC and VC. For symmetry, the compared constant current $V_2/R3$ is obtained. These currents are subtracted; then the supply voltage and temperature-independent current $I_{\text{EXT}} = (V_1 - V_2)/R3$ is achieved. Additionally, another constant current $I_{\text{TOT}}$ is generated from the same circuit, as shown in Fig. 4. Here, $V_1$ is fixed at 1.24 V, and $V_2$ is fixed at 0.83 V. Finally, the current of $I_{\text{TOT}} = (1.24 - 0.83)/R3$ is obtained in place of $I_{\text{EXT}}$. The normalized current portion $I_{\text{EXT}}/I_{\text{TOT}}$ is insensitive to temperature, process, and voltage variations. Its relation sets the maximum and minimum values of the control voltage.

From the above currents and Fig. 2, we can rewrite the current $I_{\text{in}}$ in (4). If $I(T) = V_T/R_{BGR} \times \ln N$, then

$$I_{\text{in}} = m\frac{I_{\text{EXT}}}{I_{\text{TOT}}}\frac{V_T}{R_{BGR}}\ln N = m\frac{V_1 - 0.83\ \text{V}}{0.41\ \text{V}}\frac{V_T}{R_{BGR}}\ln N. \tag{5}$$

The procedure of the control signal conversion is summarized as follows. In Fig. 2, the external control voltage $V_{\text{EXT}}$ is a constant voltage independent of the temperature and supply voltage; thus, the VIC block needs an absolute voltage circuit to compare the absolute control voltage. The constant current $I_{\text{TOT}}$ and constant voltages $V_{\text{ref}}$ and $V_{\min}$ are obtained using the bandgap reference voltage circuit and an operational transconductance amplifier (OTA) circuit. The currents $I_{\text{TOT}}$ and $I_{\text{EXT}}$ are constant currents at a fixed external voltage independent of supply-voltage and temperature, as in Fig. 2, while the current $I(T)$ is linearly dependent on the temperature. The current $I_{\text{in}}$ is linearly dependent on the temperature and independent of the supply voltage. The temperature and supply-voltage compensation is achieved by making a proper $I_{\text{in}}$ in (5).

Finally, the exponential voltage $V_{\exp}$ in (3) is expressed as

$$V_{\exp} = 2R_2 I_1 \exp\left(-\frac{I_{\text{EXT}}}{I_{\text{TOT}}}\frac{m\ln N \cdot R_1}{R_{BGR}}\right). \tag{6}$$

This voltage is a function of the resistance and constant voltage, and the size ratio of mirroring the CMOS devices regardless

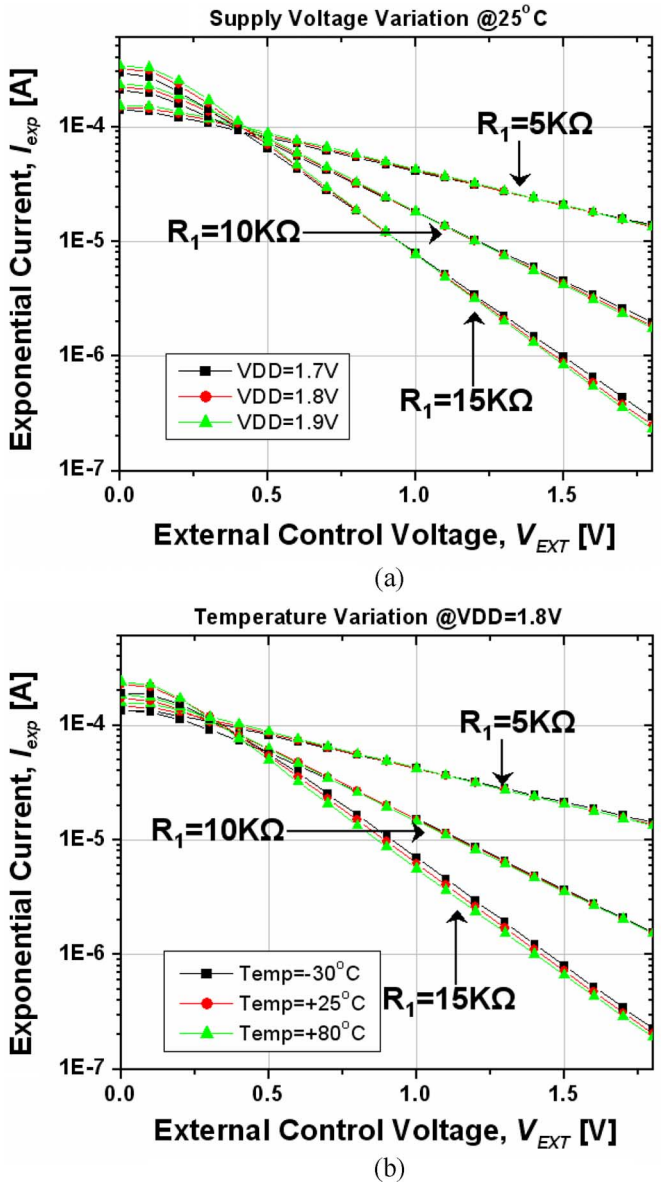


Fig. 6. Simulated *V–I* characteristics: (a) with VDD variations and (b) with temperature variations.

of the temperature and supply voltage. The exponential current $I_{\exp}$ also has the same function.

### D. Simulation Results for the Exponential Function Generator

The feasibility of the proposed method was verified through simulations using a 0.18-$\mu$m CMOS process. For the CMOS triple-well process, we adopted vertical NPN bipolar transistors, as in Fig. 3, and a bandgap reference circuit.

Fig. 6(a) shows the simulated exponential current characteristics of the proposed method versus an external gain control voltage at different supply voltages (VDD) of 1.7, 1.8, and 1.9 V. When the larger $R_1$ in (6) was used, a greater control range was obtained. When $R_1 = 10$ k$\Omega$, the exponential current changed through two decades. This indicated that the control range was more than 40 dB. In other cases ($R_1 = 5$ and 15 k$\Omega$), linear control ranges of 20 and 60 dB were obtained with a linearity error of less than $\pm$1.2 dB. Fig. 6(b) shows the simulated exponential current characteristics versus an external gain control voltage at $-30$ °C, 25 °C, and 80 °C. As with the differing resistances, the linear control ranges of 20, 40, and 60 dB were obtained with a linearity error of less than $\pm$1.2 dB. Fig. 6 indicates that the proposed exponential function generator operates successfully with the temperature and supply-voltage compensation circuits and accurately operates in a linear-in-decibel fashion.

The simulated results confirm that the current generator can obtain a wide control range ($\sim$40 dB) with a small linearity error and the temperature and supply voltage compensation techniques for gain variation are valid. In considering the voltage scaling and simulated data, the voltage $V_{\exp}$ within the required voltage control range is expressed by

$$V_{\exp} = a \cdot \exp(-b \cdot V_{\mathrm{EXT}}) \tag{7}$$

where $a = 2R_2I_1$, $b = kmR_1/R_{BGR} \times \ln N$, and $k$ is the coefficient of the voltage scaling and normalized process.

In summary, a new CMOS exponential function generator with compensation circuits has been developed. The exponential function is based on the relation between the emitter–base voltage and the collector current of a vertical NPN transistor. The inherent temperature dependence and supply-voltage variation are greatly reduced using compensation circuits. The exponential function generator is applied to the following CMOS VGA circuit.

## IV. Design of the Wideband CMOS VGA

As mentioned above, a VGA maintains a constant power level in the output of an AGC loop so that the subsequent circuitry has the better performance. The loop gain of the AGC remains constant across the entire operating range. This condition ensures identical loop transient responses regardless of the input signal level [13]. The VGA is a critical component of the AGC loop. Thus, it is very important to design the VGA considering specifications such as bandwidth, linearity, and so on. We will describe a wideband CMOS VGA that adopts the proposed exponential function generator.

### A. Architecture of the Proposed VGA Circuit

The architecture of the proposed CMOS VGA for wideband systems is shown in Fig. 7. The VGA circuit features a control voltage generator with the proposed exponential function generation and a main VGA circuit consisting of a dc offset canceller, three-stage VGA cells, and a fixed gain amplifier [28]. The differential signal $V_{\mathrm{in}}$ is amplified by the VGA cells and then amplified again by the fixed gain amplifiers to meet the targeted signal level at the output. The control voltage generator converts the external control voltage $V_{\mathrm{EXT}}$ to the required internal control signal $V_{\mathrm{ctrl}}$. In order to remove the dc offset voltage, a dc offset canceller is introduced between the output of the VGA and the output of the first VGA cell.

### B. VGA Circuit

Fig. 8 shows the schematic of the proposed VGA circuit. For operation at high frequencies, a differential cascode topology is

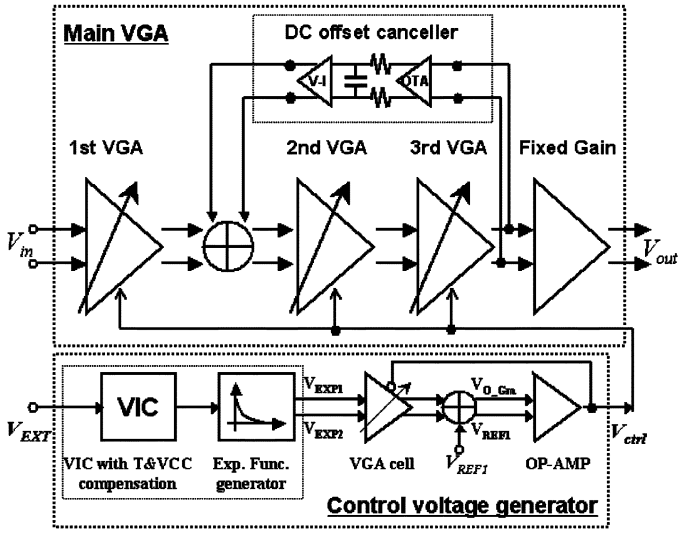


Fig. 7. Architecture of the proposed VGA circuit.

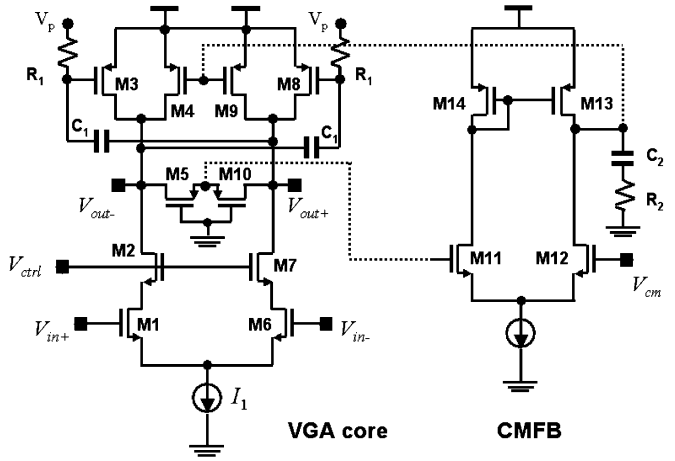


Fig. 8. Schematic of the proposed VGA circuit.

used to achieve a high gain and reduce the Miller effect. Conventionally, a differential structure has several advantages: it suppresses even harmonics, rejects common mode noises, and doubles the signal swing for a given supply voltage. Additionally, an active inductive load is exploited for wideband and low-voltage applications and can greatly improve the bandwidth [2], [28].

The VGA in Fig. 8 is constructed from a differential cascode structure (M1 and M6, M2 and M7) with a constant tail current $I_1$. The input transistors (M1 and M6) are designed to operate in a triode region or in a saturation region based on the internal control voltage $V_{\rm ctrl}$. When the input signal is small and $V_{\rm ctrl}$ is in a high state, the two input transistors remain in the saturation region and a high gain is obtained. The distortion is relatively low due to a small input signal. In contrast, when the input signal is large and $V_{\rm ctrl}$ is in a low state, the input transistors remain in the triode region and a low gain with low distortion is obtained. A variable gain can be achieved by controlling the gate voltage of transistors M2 and M7, $V_{\rm ctrl}$. In other words, by changing the voltage $V_{\rm ctrl}$, the transconductance ($g_{m1}$ or $g_{m6}$) of the cascode topology can be varied. The transconductance ($g_{m1}$ or $g_{m6}$) in

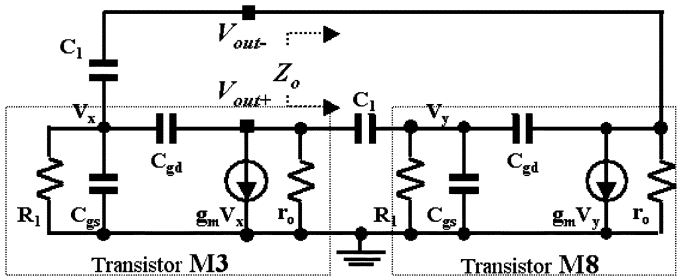


Fig. 9. Small-signal equivalent circuit to calculate the output impedance.

the triode and saturation regions are given by (8) and (9), respectively [28], as follows:

$$g_{m1} = \beta \cdot V_{\rm ds1} \tag{8}$$

$$g_{m1} = \sqrt{2\beta \cdot I_{\rm ds1}} \tag{9}$$

where $\beta = \mu C_{\rm OX}$W/L, $V_{\rm ds1}$ is the drain–source voltage of M1, and $I_{\rm ds1}$ is the drain current of M1.

A load network consists of active loads (M3, M8, $R_1$, $C_1$), bleeding current sources (M4, M9), and dc level sensing transistors (M5, M10) [28]. The dc level sensing transistors monitor the dc level of the output signals ($V_{\rm out+}$, $V_{\rm out-}$); then a common mode feedback (CMFB) network (M11 $\sim$ M14) compares this dc level with a reference voltage ($V_{cm}$) and sets the current dc level to $V_{cm}$ by automatically adjusting the bias currents of the bleeding current sources (M4, M9). With this bleeding technique, the current through the active load transistors (M3, M8) can be reduced. The output impedance is determined dominantly by the active loads because the impedances of the bleeding current sources and dc level sensing transistors are relatively large compared to those of the active loads. Fig. 9 shows a small-signal equivalent circuit that estimates the output impedance in Fig. 8. It is assumed that M3 and M8 are identical. From the small-signal equivalent circuit, the output impedance $Z_O$ at the operating frequency is given by

$$\begin{aligned} Z_O &\cong \frac{2r_o\left[1+sR_1(C_1+C_{\rm gd}+C_{\rm gs})\right]}{D(s)} \\ D(s) &= 1 + s\left[R_1(C_1+C_{\rm gd}+C_{\rm gs})\right. \\ &\quad \left. + r_o(C_1+C_{\rm gd}-C_1 g_m R_1 + C_{\rm gd} g_m R_1)\right] \\ &\quad + s^2 r_o R_1\left[4C_1C_{\rm gd} + (C_1+C_{\rm gd})C_{\rm gs}\right] \end{aligned} \tag{10}$$

where $g_m$ is the transconductance, $r_o$ is the output resistance, $C_{\rm gd}$ is the gate–drain capacitance, and $C_{\rm gs}$ is the gate–source capacitance of M3 or M8.

From (10), $Z_O$ is expressed by $2r_O$ in the low operating frequency region. In the high-frequency region near the $-$3-dB frequency of the gain, the output impedance can be approximated as (10). Gain boosting frequency is the zero point $\omega_Z = 1/R_1(C_1 + C_{\rm gd} + C_{\rm gs})$. It shows that this active load effectively acts like an inductive load in the high-frequency region, as shown in Fig. 10. The effective inductance $L_{\rm eff}$ of the active load equivalently forms a parallel resonance circuit associated with parasitic capacitance $C_p$ at the output node. Thus, by adjusting the size of capacitor $C_1$, it is possible to extend $-$3-dB frequency to a somewhat higher region by boosting the gain at

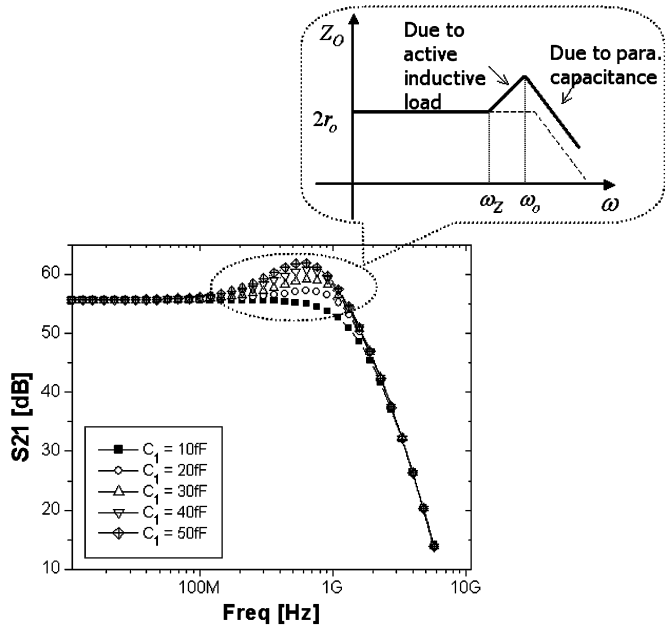


Fig. 10. Frequency response of the VGA using a gain boosting technique with various $C_1$ values (10 $\sim$ 50 fF).

high frequency. By simulation, we decided the optimal capacitor value as 20 fF to increase frequency range. Compared to the inductive active load in [28], this active load is simple and do not need additional current path. The capacitance value of $C_1$ is also much smaller (20 versus 200 fF).

Finally, we can obtain the overall gain $A_v$ of the circuit given by

$$A_v \approx -g_{m1} \cdot Z_O. \tag{11}$$

The gain also has a peaking point around the zero frequency $\omega_Z$ and the bandwidth of the circuit can be improved.

### C. Control Voltage Generator

We described the method for the temperature-independent exponential function in Section II: we utilize this method to generate the internal control voltage. The control voltage generator converts an external control voltage signal $V_{\rm ext}$ to an internal control voltage signal $V_{\rm ctrl}$. This is consistent with the theory illustrated in [25].

The exponential voltage from Section II is applied to the inputs of the scaled VGA cell that has gain $A_V$ and is then amplified by the VGA cell, as shown in Fig. 7. A constant voltage $V_{\rm REF1}$ is generated by an external current source and then subtracted from the output of the VGA cell. Therefore, if the gain of a VGA cell is $A_V$, the output of the VGA cell can be expressed as

$$V_{\rm in,OP} = V_{\rm exp} \cdot A_V - V_{\rm REF1} = a \exp(-bV_{\rm EXT}) \cdot A_V - V_{\rm REF1}. \tag{12}$$

The voltage of the VGA cell is amplified by an operational amplifier (OP-AMP); then the output voltage $V_{\rm ctrl}$ of the amplifier is fed back into the control node of the VGA cell. In a steady state, the input voltage $V_{\rm in,OP}$ of the amplifier approaches 0 due to the negative feedback loop. Therefore, the VGA gain can be expressed by

$$A_V(V_{\rm ctrl}) = V_{\rm REF1} \cdot \exp(bV_{\rm EXT})/a. \tag{13}$$

Equation (13) shows that the gain of the VGA cell has an exponential function for the external control voltage $V_{\rm EXT}$.

### D. DC Offset Canceller

In the proposed VGA, the cascaded gain cells may have a dc voltage problem due to a device mismatch and oxide gradients. The amplified offset voltage at the output of the entire VGA is cancelled out by an offset canceller with a negative feedback to the gain stage. The dc offset canceller shown in Fig. 7 is inserted between the output of the VGA and the output of the first VGA cell. The dc offset canceller is composed of an OTA, a low-pass filter (LPF), and a voltage-to-current (*V–I*) converter, which is included regardless of whether it is needed to cope with the device mismatch due to process deviations or not. In general, a large capacitance is used to keep the cutoff frequency of the LPF low. In the design of the LPF, effort has been made to maintain the capacitor value as low as possible so that the capacitor area is small.

The operation of the dc offset canceller can be explained as follows. The differential input signals, which contain the dc offset between the positive and negative components, is amplified by the OTA. The LPF extracts the dc levels of the output differential signals; the dc offset is then cancelled at the output of the first VGA cell via a negative feedback loop.

### E. Noise Analysis

The input referred noise of the VGA is dominated by the noise of the first variable gain circuit shown in Fig. 7, and the noise of the control stage and common mode feedback circuit is typically negligible. At relatively low frequencies, cascode devices contribute negligible noise [29]. The noise components of the variable gain circuit in Fig. 8 are illustrated in Fig. 11(a). In Fig. 11(a), the thermal noise of the transistors is modeled by the current sources connected between the drain and source terminals with a spectral density of $\overline{I_n^2} = 4kT(2/3)g_m$. To calculate the thermal component of $\overline{V_{n,\rm in}^2}$, we first obtain the total output noise with the input shorted together. Since the noise sources in the circuit are uncorrelated, superposition of the noise power quantities is possible. Furthermore, the source terminals of transistors M1 and M6 cannot be considered virtual ground, making it difficult to use the half-circuit concept. Thus, the effect of noise sources in each branch of the differential amplifier must be derived individually. The contribution of $I_{n1}$ is obtained by reducing the circuit in Fig. 11(b). As shown in Fig. 11(c), we can decompose $I_{n1}$ into two (correlated) current sources and calculate their effect at the output. Thus,

$$V_{n,\rm out}|_{M1} = I_{n1}(r_{O3}//r_{O4}//g_{m2}r_{O2}r_{O1})/2 + I_{n1}(r_{O8}//r_{O9}//g_{m7}r_{O7}r_{O6})/2. \tag{14}$$

Note that the two voltages are added directly because they both arise from $I_{n1}$ and are, therefore, correlated. If $r_{O3}//r_{O4}//g_{m2}r_{O2}r_{O1} = r_{O8}//r_{O9}//g_{m7}r_{O7}r_{O6}$, the total

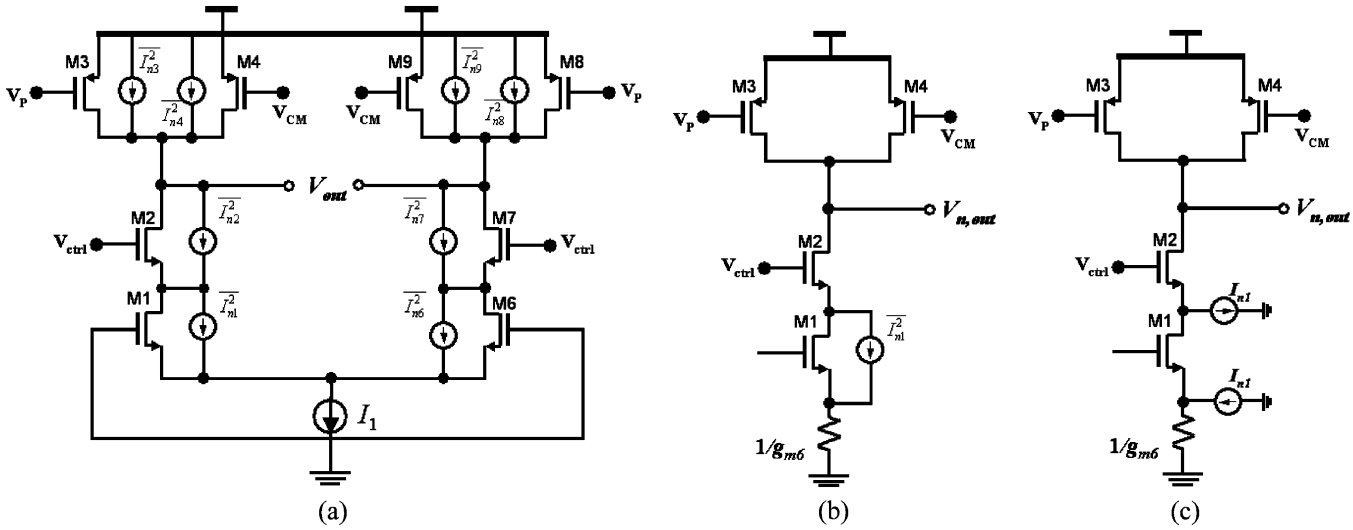


Fig. 11. Calculation of the input-referred noise of the proposed VGA.

input thermal noise in Fig. 11(a) is obtained taking into account the noise of M3, M4, M8, and M9 as follows:

$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_{m1,6}} + \frac{2g_{m3,8}}{3g_{m1,6}^2} + \frac{2g_{m4,9}}{3g_{m1,6}^2}\right). \tag{15}$$

Considering the effect of flick noise, the total input referred noise voltage per unit bandwidth of the variable gain circuit, as shown in Fig. 11(a), can be given as

$$\overline{V_{n,in}^2} = 8kT\left(\frac{2}{3g_{m1,6}} + \frac{2g_{m3,8}}{3g_{m1,6}^2} + \frac{2g_{m4,9}}{3g_{m1,6}^2}\right) + \frac{2K_N}{C_{\mathrm{OX}}(WL)_{1,6}f} + \frac{2K_P}{C_{\mathrm{OX}}f}\left(\frac{1}{(WL)_{3,8}}\frac{g_{m3,8}^2}{g_{m1,6}^2} + \frac{1}{(WL)_{4,9}}\frac{g_{m4,9}^2}{g_{m1,6}^2}\right) \tag{16}$$

where $K_N$ and $K_P$ are process-dependent constants of the corresponding MOS transistors in the order of $10^{-25}$ $\mathrm{V}^2$ F [29]. As shown in (16), at the maximum gain, $g_{m1,6}$ is maximized in order to minimize the total input-referred noise voltage given in (16). As the gain decreases, $g_{m1,6}$ reduces; thus, the total input-referred noise voltage as given in (16) increases. Consequently, the noise of the proposed VGA is a decreasing function of the gain.

Initially, we designed our VGA circuit in consideration of parasitic effects such as imperfect ground (substrate losses) and parasitic capacitors along the main signal path. We confirmed that initial simulation results were very similar to post simulation results with parasitic capacitors and resistors automatically generated by the Cadence Assura RCX tool.

## V. Simulation and Measurement Results

The proposed VGA integrated chip (IC) was fabricated using 0.18-$\mu$m CMOS technology. Fig. 12 shows the chip photograph of the implemented VGA IC. The active area occupies 0.85 mm $\times$ 0.49 mm including bondpads. The VGA is tested with a VDD supply of 1.8 V, and the dc current drawn with no applied input signal is 11.4 mA. The VGA IC was measured with a vector network analyzer (Agilent 8753ES), a signal source generator (Agilent E4433B), and a spectrum analyzer (HP 8564E). The input and output of the VGA were connected with a signal source and spectrum analyzer, respectively, through commercial balun (balanced to unbalance or vice versa) devices to convert the single-ended signal into the differential signals.

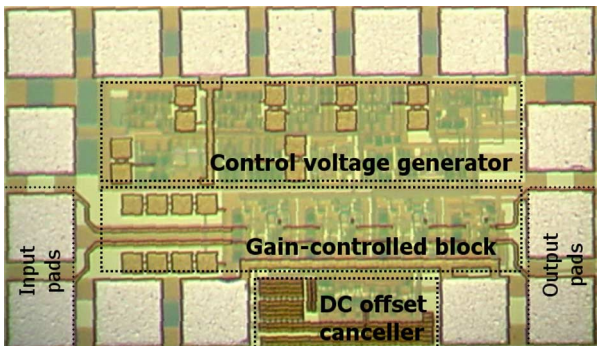


Fig. 12. Microphotograph of the fabricated VGA (core chip size: 0.59 mm $\times$ 0.33 mm, total size: 0.85 mm $\times$ 0.49 mm).

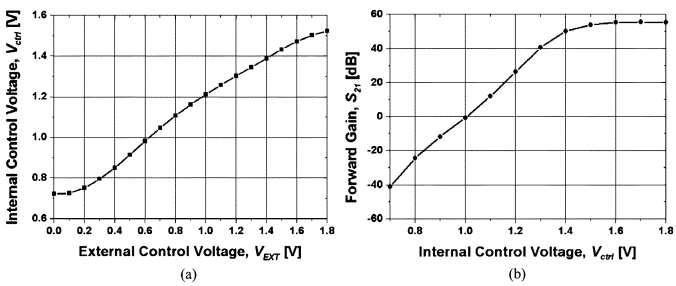


Fig. 13. (a) Internal control voltage generation and (b) gain characters with internal control voltage from [28].

Fig. 13(a) shows the relationship between the external control voltage and the generated internal control voltage through simulation using Cadence Spectre. This simulation shows the slope is linear from approximately 0.72 to 1.52 V according to

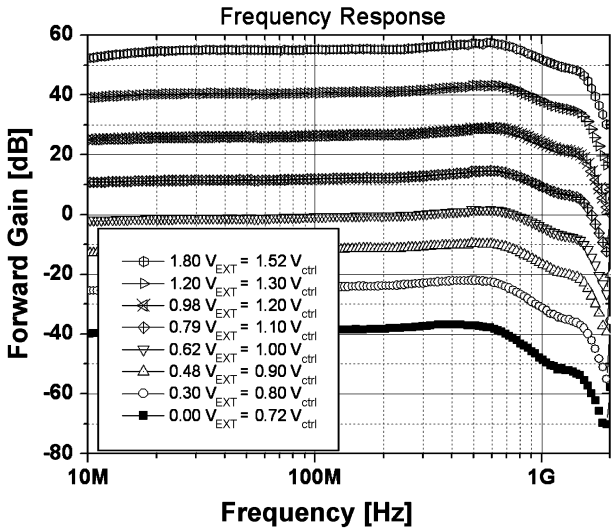


Fig. 14. Frequency response of the VGA under different control voltages; at all gain levels, the −3-dB bandwidth is larger than 900 MHz.

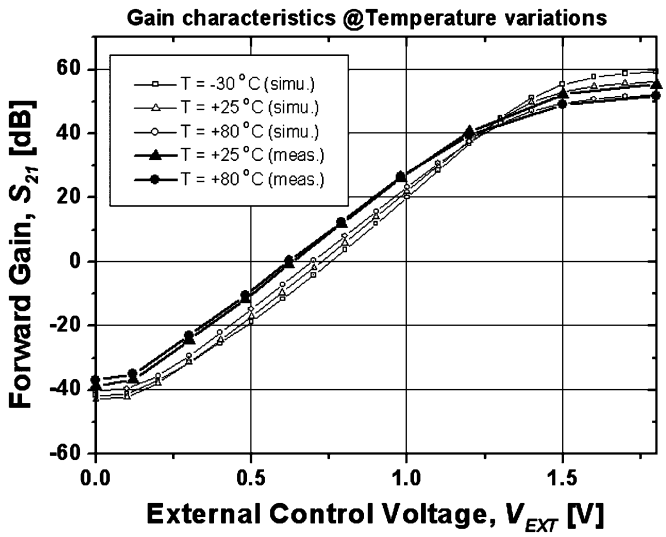


Fig. 15. Measured and stimulated gain characteristics with temperature variations at a test frequency of 100 MHz.

the external control voltage $V_{\mathrm{EXT}}$. The internal control voltage $V_{\mathrm{ctrl}}$ is applied to each VGA gain cell. Fig. 13(b) shows the measured gain $(S_{21})$ characteristics at the frequency of 100 MHz as a function of $V_{\mathrm{ctrl}}$. The VGA has linear-in-decibel gain characteristics when the input transistors (M1 and M2 in Fig. 8) are set in the triode region $V_{\mathrm{ctrl}} = 0.7 \sim 1.3$ V [28]. From Fig. 13, it is possible to obtain a linear-in-decibel gain feature in the $V_{\mathrm{EXT}}$ range of $0 \sim 1.8$ V, which will be described in the following two paragraphs.

Fig. 14 shows the frequency response of the proposed VGA at different control voltages. The measured bandwidth of the VGA is up to 900 MHz with a gain control range of 94.1 dB $(-38.8 \sim 55.3$ dB$)$. The large bandwidth was achieved using gain boosting around the −3-dB frequency (around 600 $\sim$ 700 MHz). At the minimum gain of −38.8 dB, the −3-dB bandwidth reached its minimum value of 750 MHz because the input transistors deviated from the operating point in the triode region and the bias current was reduced in relation to the change of the operating point. Moreover, we can see that the measured gain shows an average gain with ±1.5-dB gain flatness from 10 to 900 MHz at various control voltages. These results ensure that the constant current bias scheme can successfully prevent bandwidth variation according to the control bias, except in the minimum gain state.

Fig. 15 shows the measured and simulated forward gain $(S_{21})$ characteristics as a function of the control voltages at −30 °C,

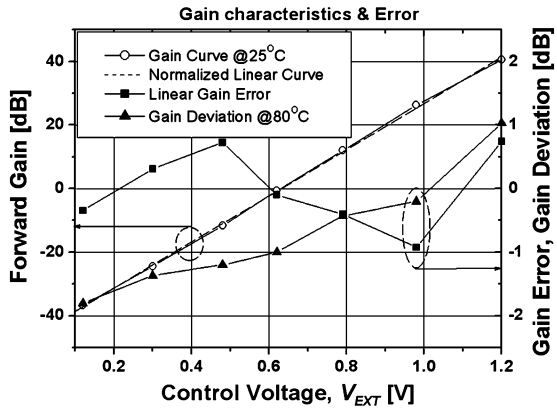


Fig. 16. Accurate linear-in-decibel gain curve at 25 °C, gain error, and gain deviation from the gain at 25 °C; a test frequency of 100 MHz was applied.

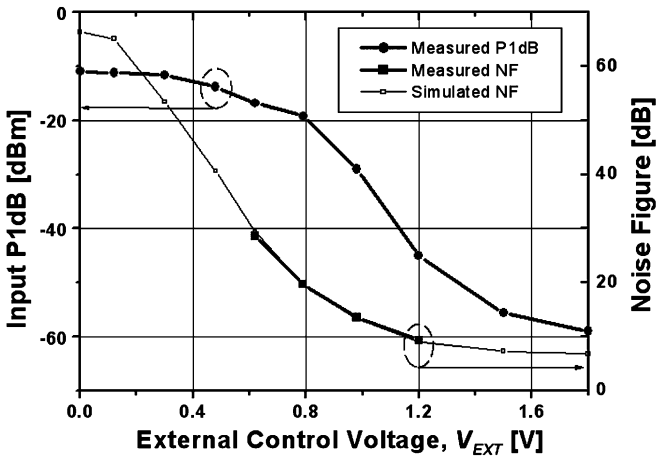


Fig. 17. Input P1dB and NF characteristics at a test frequency of 100 MHz.

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED VGA

| Parameters | Measurement Results |
|---|---|
| Technology | 0.18 μm CMOS |
| Die area (including bondpads) | 0.42 mm$^2$ |
| Supply voltage | 1.8 V |
| Current consumption | 11.4 mA |
| -3 dB Bandwidth | 900 MHz |
| Gain range | 94.1 dB |
| Gain error | ±3 dB |
| Linear-in-dB range | 79.4 dB (±1.0 dB) |
| Input P1dB | -59.1 dBm ~ -10.8 dBm |
| Noise figure* | 6.8 dB |

* Simulation data

TABLE II
PERFORMANCE COMPARISON OF THE PROPOSED AND PREVIOUSLY REPORTED VGAS

| Year [Ref.] | Tech. [μm] | Freq. range [MHz] | $V_{DD}/I_{DD}$ [V/mA] | Gain range | Method of exp. gain | Noise [dB] | Active area [$mm^2$] | Input P1dB [dBm] |
|---|---|---|---|---|---|---|---|---|
| 1995 [4] | 0.6 CMOS | 0.01~85 | 10mW | 30 ~ 0 | Eq. of (1+x)/(1-x) | - | - | - |
| 2000 [5] | 0.6 CMOS | 1~20 | 3.3/7.0 | 34 ~ 0 | Eq. of (1+x)/(1-x) | - | 0.43 | - |
| 2000* [7] | 0.35 CMOS | 0.01-21 ($G_{MAX}$) | 1.5/16.5 | 20 ~ -6 | Eq. of (1+x)/(1-x) | - | - | - |
| 1998 [6] | 0.5 CMOS | 20~150 | 3.3/3.8 | 10 ~ -5 | Eq. of (1+x)/(1-x) | - | 0.15 | - |
| 2000 [23] | BiCMOS | 50~500 | 3.0/12 | 43 ~ -35 | Bipolar & CSC** | 5 @$G_{MAX}$ | 1.0 | - |
| 2002 [3] | 0.25 CMOS | 30~210 | 2.5/11 | 55 ~ -35 | Sub-threshold region*** | 8 @$G_{MAX}$ | 0.49 (core size) | -40 ~ -8 |
| 2002 [24] | 0.25 CMOS | 380 | 2.5/25.3 | 11 ~ -70 | Sub-threshold region & CSC** | 11 @ $G_{MAX}$ | 2.02 | - |
| 2003 [2] | 0.18 CMOS | 20~350 | 1.8/3.0 | 42 ~ -42 | Parasitic NPN & signal converter | 7 @ $G_{MAX}$ | 0.19 (core size) | - |
| 2005 [18] | 0.18 CMOS | 1~40, 1000 ($G_{MAX}$, $G_{MIN}$) | 1.8/3.6 | 36 ~ -48 | Using Eq. (1) | - | 0.4 | -48 ~ -17 |
| Proposed VGA [27] | 0.18 CMOS | 4~900 | 1.8/11.4 | 55 ~ -39 | Parasitic NPN & signal converter | 6.8* @$G_{MAX}$ | 0.42 | -59 ~ -11 |

*Simulation results
**Signal-summing VGA with control signal converter (CSC)
***Master–slave control circuits with MOSFETs in a subthreshold region

25 °C, and 80 °C when the test signal frequency is 100 MHz. The measured gain characteristics are in good agreement with the simulated ones. The difference between the gain curves is a result of the errors of current mirroring and reference voltages. The simulation results show that the gain deviations from the gain characteristics at room temperature are within ±3 dB over a 96-dB gain range at various control voltages. In the case of measurement, gain errors of ±3 dB occurred within the 94.1-dB gain control range. These results confirm the validity of the proposed ideas for obtaining linear-in-decibel variable gain characteristics with temperature compensation. However, the exact linear range is limited to 79.4 dB, as shown in Fig. 16, because the nonlinear range of the internal control voltage, $V_{\text{ctrl}} = 1.3 \sim 1.52$ V in Fig. 13, is utilized in order to obtain a higher gain. Additionally, the imperfect effects in the process of the control signal conversion, such as inaccurate current mirroring and device modeling, particularly, the lateral NPN transistors, degraded the gain characteristics. In the gain range of 79.4 dB, the linearity errors from the normalized linear curve and the gain deviations from the gain at 25 °C were ±1.0 and ±1.8 dB, respectively.

The measured input P1dB and measured/simulated noise figures (NFs) of the proposed VGA are presented as a function of the control voltage at a test frequency of 100 MHz in Fig. 17. The input P1dB varies from −10.8 to −59.1 dBm. It is maximized at the minimum gain state and, as the gain increases, it decreases so that decreasing the allowable input signal swing results in the reduction of P1dB, as shown in Fig. 17. The minimum NF is +6.8 dB at a maximum gain of +55.3 dB and the NF increases as the gain decreases. Through simulations, the total spot output noise is $6.03e-13$ $V^2/Hz$ at 100 MHz and the main noise sources are the input transistors (M1 and M6) and load transistors (M3, M4, M8, and M9) described in (16). The measured NF data were obtained in the gain range of $-5 \sim 40$ dB due to the limitation of the NF equipment.

The measurement results are summarized in Table I and a comparison with previous studies is given in Table II. The proposed VGA achieves the best performance in terms of high-frequency performance with a high gain, wide decibel-linear gain controllability with temperature compensation, and chip area.

## VI. CONCLUSION

A wideband CMOS VGA with a temperature compensation circuit has been presented. The proposed VGA utilizes an exponential function generator with PVT compensation circuits. In addition, wideband operation with a high gain was achieved using a cascode configuration and a gain boosting technique. The current bleeding technique in the load network was also used to improve the linearity. The VGA has a 94.1 dB (−38.8 ∼ 55.3 dB) gain control range and, particularly, 79.4-dB linear-in-decibel gain characteristics. Furthermore, the VGA operates up to a −3-dB frequency of 900 MHz. It consumes a total current of 11.4 mA under a single power of 1.8 V and occupies an area of $0.85 \times 0.49$ $mm^2$. Temperature-compensated performance was confirmed from 25 °C to 80 °C.

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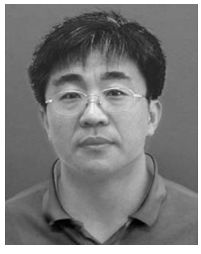
**Hui Dong Lee** (S'02) received the B.S. and M.S. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2000 and 2002, respectively, and is currently working toward the Ph.D. degree at KAIST.

His research interests include analog, RF, and microwave integrated circuit design for wireless communications in CMOS and BiCMOS technologies. His focus is on the analysis and design of various VGAs for multistandard applications.

**Kyung Ai Lee** received the B.S. degree in electrical engineering from Kyungpook National University, Dae-gu, Korea, in 2002, the M.S degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2004, and is currently working toward the Ph.D. degree at KAIST.

Her research interests include analog, RF, and microwave integrated circuit design for wireless communications in CMOS and HBT and HEMT technologies. Her focus is on the analysis and design of a power amplifier for military and commercial applications.



**Songcheol Hong** (S'87–M'88) received the B.S. and M.S. degrees in electronics from Seoul National University, Seoul, Korea, in 1982 and 1984, respectively, and the Ph.D. degree in electrical engineering from The University of Michigan at Ann Arbor, in 1989.

In May 1989, he joined the faculty of the Department of Electrical Engineering and Computer Science, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea. In 1997, he held short visiting professorships with Stanford University, Palo Alto, CA, and Samsung Microwave Semiconductor, Gyeonggi-do, Korea. His research interests are microwave integrated circuits and systems including power amplifiers for mobile communications, miniaturized radars, millimeter-wave frequency synthesizers, and novel semiconductor devices.