A Wideband High Dynamic Range Continuous-Time Sigma-Delta ADC for Wireless Applications

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Abstract

In recent years, the research toward the development of high speed and high resolution analog-to-digital converters (ADCs) has been equally driven by the demand of high-speed wire line and wireless communication services. Delta-Sigma ADCs are widely used in wireless applications due to their oversampling and noise shaping characteristics.

This thesis aims to design a continuous-time sigma-delta modulator which can provide a dynamic range of 75 dB over a 25 MHz signal bandwidth. The proposed topology is a 4th order 3-bit low-pass sigma-delta modulator, which employs a combination of feedforward and feedback schemes. The design starts from system level using Matlab/Simulink. Then the behavioral level design is performed using Cadence VerilogA. Finally, the first integrator in the loop, which is the most critical block in the modulator, is implemented at transistor level using 90nm CMOS technology.

The most important non-idealities of the continuous time sigma-delta modulator, such as clock jitter, excess loop delay, DAC mismatch and time constant variance are considered. Their effects are analyzed and compensation techniques are proposed and introduced in the MATLAB models.

Combining all the issues, the modulator achieves the SNDR 75.02dB, dynamic range 77.58dB over signal bandwidth 25MHz at system level. The modulator with a SNDR 75.71 dB, dynamic range 76.14 dB over signal bandwidth 12.5MHz has been verified at system level together with the schematic design of the first integrator in 90nm CMOS technology.

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List of Abbreviations

CT   Continuous Time

DT   Discrete Time

DAC   Digital to Analog Converter

A/D   Analog-Digital

ADC   Analog to Digital Converter

DR   Dynamic Range

OSR   Over Sampling Ratio

SNAD   Signal to Noise and Distortion

SFDR   Spurious-Free Dynamic Range

PSD   Power Spectrum Density

NTF   Noise Transfer Function

STF   Signal Transfer Function

IBS   In-band noise suppression

OBG   out-band gain

ELD   excess loop delay

INL Integral Non-Linearity

LSB Least Significant Bit

Opamp   Operational Amplifier

CMFB Common Mode Feed Back

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Reference

1 Introduction

1.1 Background

Analog-to-digital converters (ADCs) are widely used in wireless applications. Modern wireless base-station receivers require the ADCs with bandwidth up to 20 MHz and resolutions of 10-14 bits or better. The evolving research toward the development of ADCs with higher speeds and higher resolutions is being equally driven by the demand of high-speed wire line and wireless communication services. 1.1 shows the basic diagram of a popular direct conversion wireless receiver which employs a sigma-delta ADC.
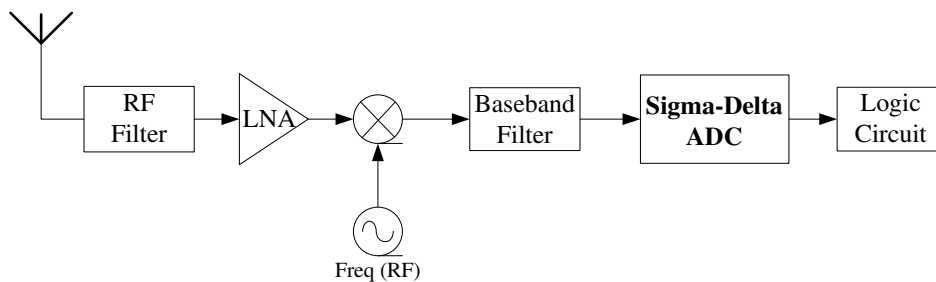
FIGURE 1.1 BASIC DIAGRAM OF A DIRECT CONVERSION WIRELESS RECEIVER

In such systems, pipeline ADCs are usually employed. Recently continuous-time sigma-delta (CT ΣΔ) modulators become attractive. Compared with Nyquist rate ADCs, oversampling ADCs trade digital signal processing complexity for relaxed requirements on the analog components [38]. Delta-Sigma analog-to-digital converters (ADCs) are widely used in wireless applications [1,2,3,4] due to their oversampling, high dynamic range, and low power consumption characteristics.

Most reported MHz range sigma-delta modulators are implemented using switched-capacitor(SC) techniques[1,2,13-18], mainly due to mature design methodologies and robustness. The discrete-time Sigma-Delta ADC offers a good degree of accuracy. But the circuit speed is limited by the settling of switched-capacitor integrator.

Compared with the traditional discrete-time (DT) counterparts, the continuous-time (CT) sigma-delta ADCs have the advantages of higher speed and lower power consumption. Absence of stringent settling requirements enables CT modulators to digitize signals up to several hundreds MHz. Moreover, they provide implicit anti-alias filtering, thus reducing the need for explicit anti-alias filtering prior to the modulator. Input-signal sampling errors, like settling error, charge injection and some other discrete-time problems do not exist in continuous-time circuits.

However, continuous-time sigma-delta modulators also face a lot of design challenges. They are very sensitive to clock jitter, excess loop delay and DAC mismatch. They suffer from the large loop coefficient variations due to the process variations of resistors and capacitors. All these issues limit their overall performance.

Some early studies either have high resolution for low bandwidth [20-24], or have high bandwidth but low resolution [25-28]. In recent years, more and more work success in both the wide bandwidth and the high resolution. [29-35] There are still lots of space for improvement in continuous-time sigma-delta modulator design.

This thesis work targets a 75dB dynamic range, 25MHz input signal bandwidth continuous-time sigma-delta modulator. The most important non-idealities of continuous time sigma-delta modulator, such as clock jitter, excess loop delay, DAC mismatch and time constant variance are considered. Their effects are analyzed and techniques to compensate these effects are studied at system level using MATLAB environment.

1.2 Thesis Organization

The thesis work covers the theoretical analysis, the system level and the circuit level design of a wideband, high resolution continuous-time sigma-delta A/D converter.

Chapter 2 gives an overview of sigma-delta A/D converters, including performance metrics, design choices and methodology.

Chapter 3 analyses the issues for continuous-time sigma-delta A/D modulators. Effects of various non-idealities and potential solutions to deal with them are discussed.

Chapter 4 presents the details of system level design of the modulator, including the simulation results in Matlab and Cadence.

Chapter 5 covers the details of circuit level designs, including the transistor level design of the first integrator.

Chapter 6 concludes the thesis project and proposes recommendations for future improvement of this work.

2 Overview of Continuous-time Sigma-delta Modulator

This chapter gives an overview of continuous-time sigma-delta modulator design. It begins with an introduction of the background knowledge. Then the performance metrics, which are used to evaluate the modulator performance, are described. After that, the design choices are discussed, which become the main considerations for composing the sigma-delta modulator architecture. Finally, the design methodology of continuous-time sigma-delta modulator is presented.

2.1 Overview

The system architecture of a general oversampling sigma-delta modulator is shown in Figure 2.1. The analog input first passes through an anti-aliasing filter to attenuate out-of-band frequency components so that its output becomes band-limited and, aliasing due to sampling inside the following sigma-delta A/D modulator can be suppressed. The sigma-delta A/D modulator converts the analog signal to a high speed, low-resolution digital signal. The last stage, called the decimation filter, converts the modulator output into a high-resolution digital signal at a lower speed usually equal to twice the frequency of the desired signal bandwidth.
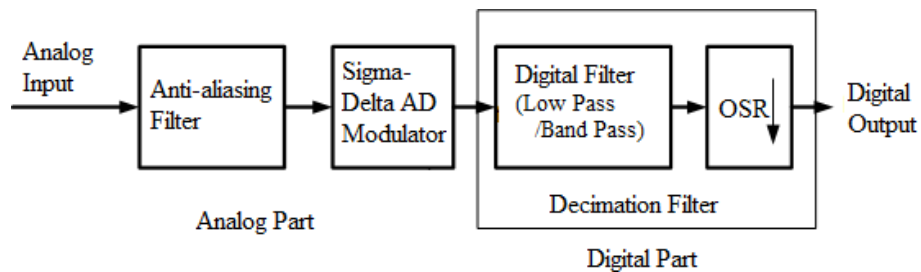
FIGURE 2.1 BLOCK DIAGRAM OF AN OVERSAMPLING A/D CONVERTER[36]

Sigma-delta A/D modulators employ oversampling techniques to push quantization noise and errors due to imperfect analog circuits into a higher frequency band. Noise shaping techniques shape the spectral density such that most of the quantization noise power is outside the band of interest, shown in Figure 2.2 with a first-order sigma-delta modulator. The noise power is then removed by digital filtering so that high in-band signal-to-noise ratio can be obtained.
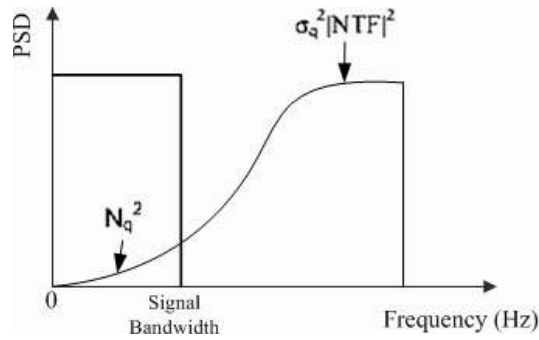
FIGURE 2.2 OUTPUT SPECTRUM OF A FIRST-ORDER SIGMA-DELTA MODULATOR

Figure 2.3 shows the basic block diagram of a sigma-delta modulator and its corresponding linear model.
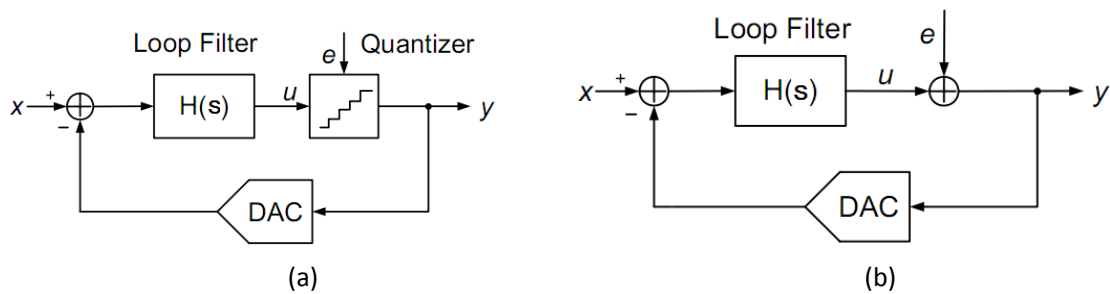
FIGURE 2.3 BASIC ARCHITECTURE AND LINEARIZED MODEL OF A ΔΣ A/D MODULATOR [37]

The sigma-delta analog-to-digital converter consists of three important components:

1. A loop filter or loop transfer function H(s)

The loop filter has large gain within the signal band while it attenuates out-of-band signals. A loop filter is realized with continuous-time integrators in a CT implementation.

2. A clocked quantizer

The quantizer is a strongly-nonlinear circuit in an otherwise linear system. Thus the sigma-delta A/D modulators cannot be considered as a linear system. However, if the inherent quantization noise can be modeled as white noise, the nonlinear quantizer can thus be approximated by a linearized model, as shown in Figure 2.3(b).

3. A feedback digital-to-analog converter (DAC)

The feedback DAC is employed to convert the digital modulator output to analog and subtract it from the modulator input. It is normally implemented with a charge-redistribution DAC in DT converters while current-steering DACs are used in CT converters.

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In Figure 2.3, the quantizer is replaced by an adder. The quantization noise is represented by e, which assumed to be independent of the signal input x. The output of the modulator may now be written in terms of the two inputs X(s) and E(s) as

$$Y(s) = \frac{H(s)}{1 + H(s)} X(s) + \frac{1}{1 + H(s)} E(s)$$
(2.1.1)

$$Y(s) = STF(s) \times X(s) + NTF(s) \times E(s)$$
(2.1.2)

where STF(s) and NTF(s) are the signal transfer function and noise transfer function respectively. Seen from equation (2.1.1), the poles of H(s) become the zeros of NTF(s), hence inside the input signal bandwidth where H(s) >>1,

$$Y(s) \approx X(s)$$
(2.1.3)

In other words, the input and output spectra are in greatest agreement at frequencies where the gain of H (s) is large.

2.2 Performance metrics

This section reviews the performance metrics, such as SNDR, dynamic range and so on, which are needed to evaluate the sigma-delta modulators performance.

Signal-to-noise ratio (SNR) is the ratio of the RMS signal amplitude to the RMS value of the noise spectral components, excluding the signal harmonics and leaving only the noise terms.

$$SNR = 10\log \left(\frac{Signal_{RMS}}{Noise_{RMS}}\right) \ [45]$$
(2.2.1)

Signal-to-Noise-and-Distortion Ratio (SNDR) is the ratio of the rms signal amplitude to the noise spectral components, including harmonics. SINAD is a good indication of the overall dynamic performance of an ADC because it includes all components which make up noise and distortion.

$$SNDR = 10\log \left(\frac{Signal_{RMS}}{Noise_{RMS} + Distortion_{RMS}}\right) \ [45]$$
(2.2.2)

SNDR is often converted to effective-number-of-bits (ENOB) using the relationship for the theoretical SNR of an ideal N-bit ADC, SNR = 6.02N + 1.76 dB. The equation is solved for N, and the value of SNDR is substituted for SNR:

$$ENOB = \frac{SINAD - 1.76 \text{ dB}}{6.02} \quad [45] \qquad (2.2.3)$$

Note that equation (2.2.3) assumes a full-scale input signal. A full-scale input is one whose magnitude equals the maximum magnitude of the quantizer feedback, assuming a quantizer whose output is centered at 0. However, due to the possible overloading and stability problem, the input signal usually cannot be as large as full-scale amplitude. If the signal level is reduced, the value of SNDR decreases and the ENOB decreases. It is necessary to add a correction factor for calculating ENOB at reduced signal amplitudes as shown in equation (2.2.4):

$$ENOB = \frac{SNDR_{measured} - 1.76 \text{ dB} + 20\log\left(\frac{Fullscale\ Amplitude}{Input\ Amplitude}\right)}{6.02} \quad [45] \qquad (2.2.4)$$

The oversampling ratio (OSR) is defined as the ratio between the sampling frequency fs and the Nyquist frequency fn, which is double of the signal bandwidth fb.

$$OSR = \frac{f_s}{f_n} = \frac{f_s}{2f_b} \quad [36] \qquad (2.2.5)$$

Dynamic range (DR) is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal.

Practically, the maximum input signal level is the input level where the SNDR drops 3 dB beyond the peak. For an analog-to-digital converter (ADC), if the signal is too large, it will over-range the ADC input. If it is too small, the signal will get lost in the quantization noise of the converter.

To actually find the DR for a given modulator, SNDR is plotted against input amplitude. The input amplitude range which gives SNDR≥ 0 is precisely the dynamic range. Meanwhile, the maximum SNDR can be easily found from the plot.

Signal-to-quantization-noise-ratio (SQNR) can be expressed as a function of OSR, number of bit in the quantization (N), and loop order (L), as follows. [38]

$$SQNR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 \times OSR^{2L+1} \qquad (2.2.6)$$

This is useful to asses some of the design parameters such as L or OSR. But the overall DR needs to account for device noise and noise induced by clock phase noise as these may be dominating in some cases.

Spurious-free dynamic range (SFDR) is the difference, expressed in dB, between the rms value of the input signal and the peak spurious signal at the output spectator. A spurious signal is any signal present in the output spectrum that is not present at the input. SFDR is a useful metric in communication applications, where the distortion component can be much larger than the signal of interest due to the intermodulation of unwanted interferential signals.

Another important metric is intermodulation distortion, which is a multi-tone distortion product that results when two or more signals are present at the input of a non-linear device. Especially for sigma-delta modulator when the input is a sine wave, strong higher order harmonics fall outside the signal band and will be filtered, leading to the wrong conclusion that the modulator is linear. Two-tone tests are applied to assess the distortion of the modulator. In these tests, the intermodulation tones fall close to the input tones, hence within the signal band.

2.3 Design Choices

2.3.1 OSR Selection

Extending the sigma-delta A/D converters to broadband applications requires lowering the oversampling ratio (OSR) in order to be realizable within the nanometer CMOS technologies and to meet a moderate power budget. For sigma-delta modulators with signal bandwidth up to megahertz range, the clock frequency cannot be increased without reducing OSR.

2.3.2 Multi-bit Quantizer and High Loop Order

The high resolution at a low OSR can be achieved either: 1) by using a higher order loop filter, and/or 2) by increasing internal quantizer resolution. [24]

The SNDR improvement gained by increasing the loop filter order however leads to the stability problem. The integrator gain or maximum input amplitude should be reduced to maintain the stability when the loop order is increased.

Another way to achieve high resolution is to use multi-bit internal quantization. There are several benefits of the multi-bit quantizer. Multi-bit quantization enhances modulator stability as well as relaxes slew rate and settling requirements on the operational amplifiers. More than $20\log_{10}(2N-1)$ dB dynamic range improvement can be expected compared with single-bit quantization. Then a more aggressive noise-shaping transfer function can be employed to suppress the in-band noise, with the benefit of extra dynamic range. Besides, multi-bit quantization lowers the clock jitter sensitivity if a NRZ multi-bit DAC is used. However, the linearity of a multi-bit sigma-delta modulator is limited by the multi-bit

feedback D/A converter. Linearization techniques are required to correct the mismatch errors in the DAC elements.

2.3.3 Multi-loop Topology VS. Single-loop Topology

To achieve high-order noise shaping without inherent stability problems in single-loop higher-order sigma-delta modulator, multi-loop (MASH) topologies, with two or three cascaded loops of first-order and/or second-order may be used for sigma-delta modulators. The basic idea of MASH, taking a two-stage modulator as an example, is to feed the quantization error of the first stage into the second stage. The digital outputs of the two stages are combined through digital cancellation logic so that the first stage quantization error is removed and only the noise shaped second stage quantization error is left. [24]

In multi-loop cascaded topologies, perfect matching is required between the analog noise-shaping transfer function and the digital noise cancellation logic. Thus, multi-loop topologies are viable solutions for switched-capacitor implementations, thanks to the excellent matching properties of on-chip capacitors. However, for continuous-time multi-loop cascaded implementations, large RC time constant variation introduces mismatch. Significant SNDR degradation may result. On the other hand, single-loop topologies are more tolerant of non-idealities such as RC time-constant variation and more suitable for continuous-time sigma-delta modulator design.

2.3.4 Feedforward VS. Feedback

There are two commonly used loop filter architectures for single-stage modulators, CIFF (chain of integrators with weighted feedforward summation) and CIFB (chain of integrators with distributed feedback) [38]. The examples of the 4th-order sigma-delta modulators with feedforward and feedback compensation are shown in Figure 2.4(a) and (b) respectively.
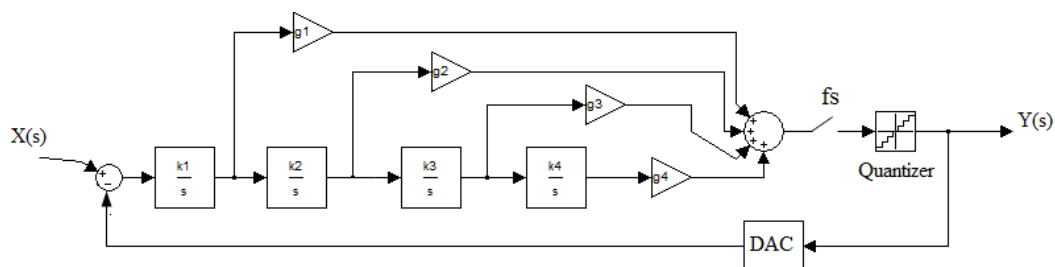
(a)   Modulator with Feedforward Compensation
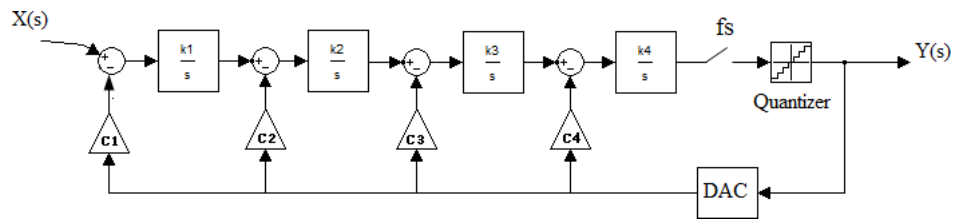
(b) Modulator with Feedback Compensation

FIGURE 2.4 FOURTH-ORDER SIGMA-DELTA MODULATORS
WITH FEEDFORWARD AND FEEDBACK COMPENSATION[42]

As it can be seen from Figure 2.4(b), the feedback structure requires several DACs feeding back to each integrator output, though it does not need a large adder before the quantizer.

In the feed-forward structure, only one DAC is needed in the feedback path, which is more area-efficient. However, the feed-forward architecture requires a multi-input adder to sum all feedforward branches before the quantizer. Due to the requirement of RC/GmC time constant tuning, the active adder is usually preferred for the continuous-time modulator. But the adder will become the speed bottleneck of the whole loop as well as consume much power.

One more advantage of the feedforward structure is the small output swing of the first integrator. With a certain output range, the first integrator allows a bigger loop gain, and hence lower performance requirements on the following stages.

Generally, the signal transfer function (STF) of a feedforward architecture has an out-of-band peaking at a certain frequency. This implies that at the peaking frequency the maximum stable input level is reduced by the gain of the peaking. As a result, the dynamic range is reduced and a lot of big out-of-band interferers exist. The feedback filter does not suffer from significant peaking.

Besides the above fundamental topologies, local feedback paths can add zeros to noise transfer function, which benefit to shift the DC gain of the integrators to a finite resonance frequency. In this way, the gain can be spread more equally in the signal band. The quantization noise at the end of the signal band can be suppressed more, as shown in Figure 2.5. With local feedback paths, it is possible to implement an inverse Chebyshev NTF rather than a Butterworth NTF. [42]
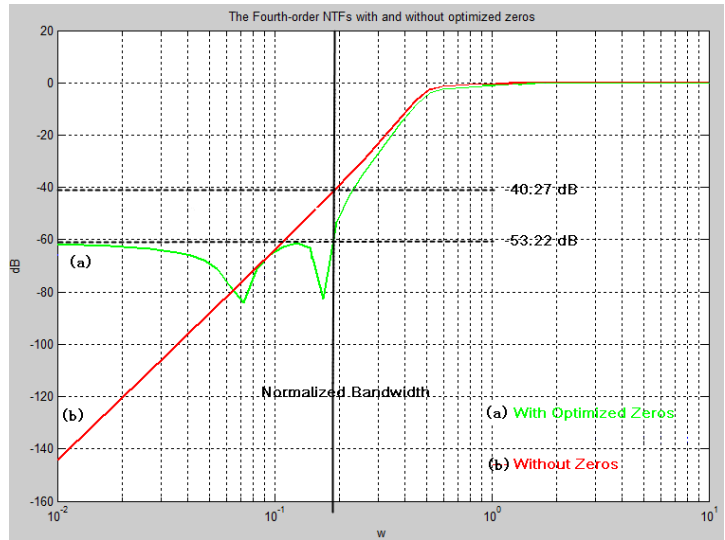
FIGURE 2.5 NTF OF FIFTH-ORDER SIGMA-DELTA MODULATOR WITH FEEDFORWARD COMPENSATION

(A) WITH LOCAL FEEDBACK, AND (B) WITHOUT LOCAL FEEDBACK

An example of the fifth-order modulators with local feedback paths is shown in Figure 2.6.
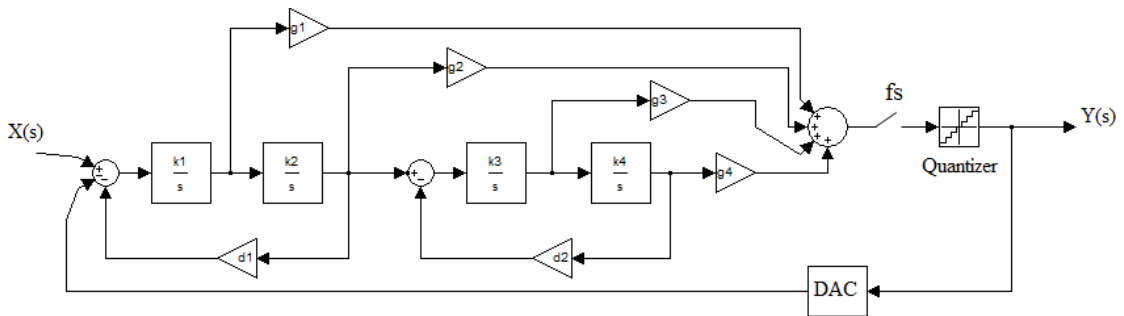
(a) Modulator with Feedforward Compensation and Local Feedback
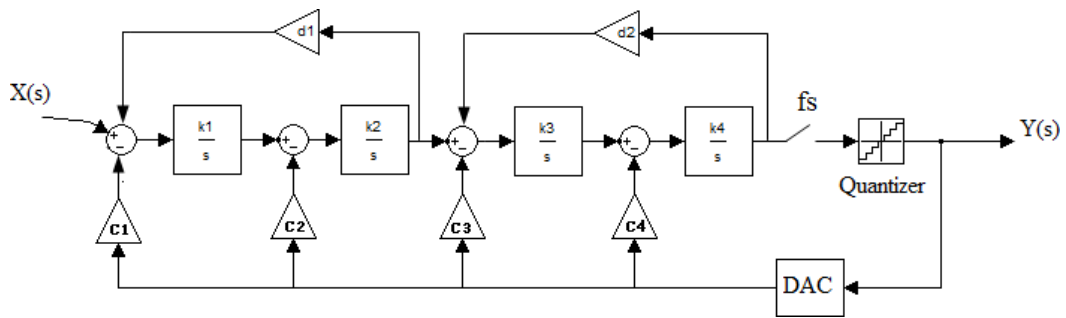
(b) Modulator with Feedback Compensation and Local Feedback

FIGURE 2.6 FOURTH-ORDER SIGMA-DELTA MODULATORS

WITH A COMBINATION OF FEEDFORWARD AND FEEDBACK

2.3.5 Feedback Pulse of DAC

Before choosing the transfer function, the DAC pulse shape usually has to be decided. Continuous-time sigma-delta modulators are sensitive to every deviation from the ideal

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shape of the DAC feedback pulse, as the analog continuous-time feedback waveform is integrated over time. Any non-idealities and non-uniformities will tend to degrade performance.

The two most common DAC feedback pulses are NRZ (None-return-zero) pulse, and RZ (Return-zero) pulse, shown in Figure 2.7. Their waveforms can be generated by simply switching the feedback current or voltage sources on and off using the clock and its edges [43].

$$r_{NRZ}(t) = \begin{cases} 1, & 0 \le t < T_s \\ 0, & \text{otherwise} \end{cases}$$

$$R_{NRZ}(s) = \frac{1 - e^{-sT_s}}{s}$$

(a)

$$r_{RZ}(t) = \begin{cases} 1, & t_1 \le t < t_2 \\ 0, & \text{otherwise} \end{cases}$$

$$R_{RZ}(s) = \frac{e^{-st_d}(1 - e^{-st_p})}{s}$$

(b)
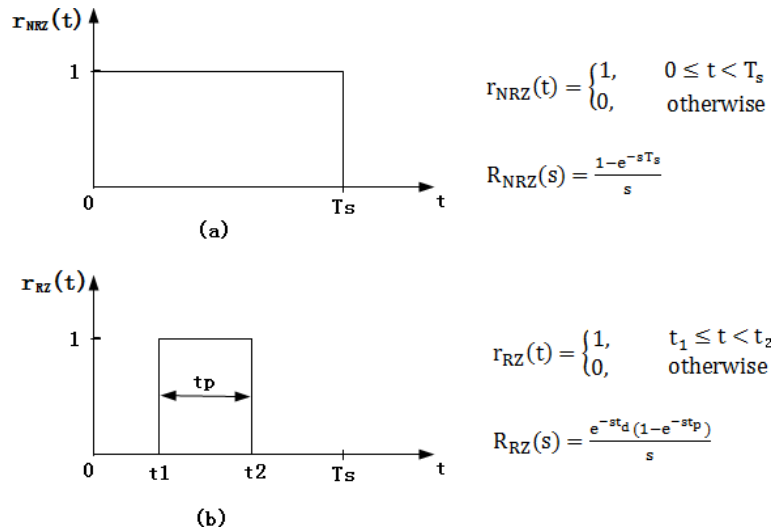
FIGURE 2.7 COMMON DAC FEEDBACK IMPULSE RESPONSES

AND THE CORRESPONDING LAPLACE TRANSFORMS

(A) NRZ DAC (B) RZ DAC

The rectangular feedback realization arises one major non-ideality, the sampling clock jitter. Any timing jitter in the sampling clock modulates directly the ADC decision point as well as the rising and falling edges of the DAC output, and thus the quantity of the DAC feedback signals. The resulting DAC error is directly introduced into the modulator input, thus clock jitter can limit the overall sigma-delta modulator performance.

It is meaningful to compare NRZ feedback and RZ feedback. NRZ DAC pulse is preferred because of low sensitivity to clock jitter. As illustrated in figure 2.8, assuming that the duty cycle of the RZ pulse shaping is 0.5, the amplitude of the RZ DAC has to be twice as high as that of the NRZ DAC, to keep the area of the DAC output waveform unchanged. Thus, with the same clock jitter variance, the modulator with NRZ feedback can achieve higher SNR than that with RZ feedback. If the noise introduced by the random clock jitter is assumed to have a white spectrum, the SNR improvement (in dB) of NRZ pulse shaping over RZ pulse shaping can be derived as [24]

$$SNDR_{NRZ-RZ} = 10log_{10}(\frac{8*\delta^2_{I_{DAC,NRZ}}}{\delta^2_{\Delta I_{DAC,NRZ}}})$$

(2.3.3)

Where $\delta^2_{I_{DAC,NRZ}}$ is the variance of the NRZ DAC output current, and $\delta^2_{\Delta I_{DAC,NRZ}}$ is the variance of $\Delta I_{DAC,NRZ}$.

Besides, the RZ feedback DAC pulse also has the advantage of reducing distortion and makes it more linear. A lot of the distortion performance in a DAC is associated with the transient seen at the output when the DAC swings from one output level to the next one. In a RZ DAC the output always starts from ground and return to ground, hence there is no memory of the prior sample, reducing code dependence and distortion. Also the DAC can be designed in such a way that all internal node glitches die out before the output is turned on. It allows the designer to mask all internal code-dependent glitches, keeping them inside the DAC, before the output is generated, hence making it more linear. Conversely, in an NRZ DAC the output is always active so the transient could vary depending on the present output level and the next one, which may cause distortion. Any undesired glitch originating in an internal node of the DAC will be visible at the output.
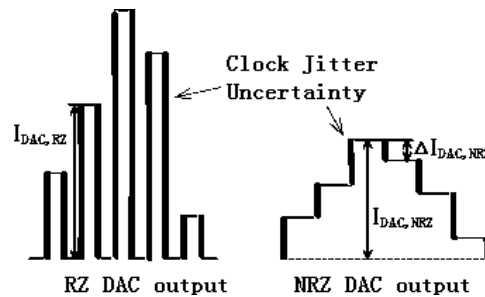
FIGURE 2.8 FEEDBACK DAC PULSE SHAPING WITH CLOCK JITTER

Another unavoidable problem is the excess loop delay, which is caused by the non-zero switching time of the quantizer latch and the feedback DAC [37]. The delay in the feedback path changes the overall loop transfer function in a way that moves the poles of the linearized equivalent system toward the right plane, hence degrading its stability. If the delay becomes excessive, the loop will degrade its stability and could oscillate. The delayed NRZ pulse can be presented as a linear combination of two pulses, as shown in Figure 2.9.
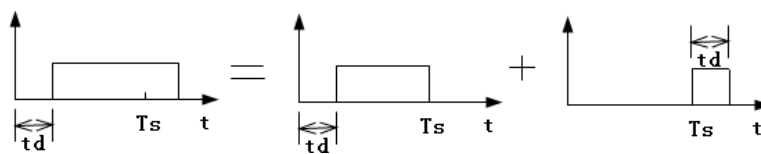
FIGURE 2.9 DELAYED NRZ PULSE AS A LINEAR COMBINATION

2.4 Design Methodology

The typical top-down design flow for continuous-time sigma-delta modulator is shown in Figure 2.10. Firstly, the ADC has been designed at system level using Matlab/Simulink. Various high-level simulations have been performed including non-ideal behaviors of the sigma-delta ADC components in order to count for the real circuit behavior of the design. The modulator performance, such as desired SNDR and stability must be achieved and the specifications for every building block derived. After that, the sigma-delta ADC is implemented using behavioral description language in Cadence environment. After validating the model at behavioral level, the most critical block of the ADC was replaced by its circuit level implementation using 1.2V 90nm CMOS technology.
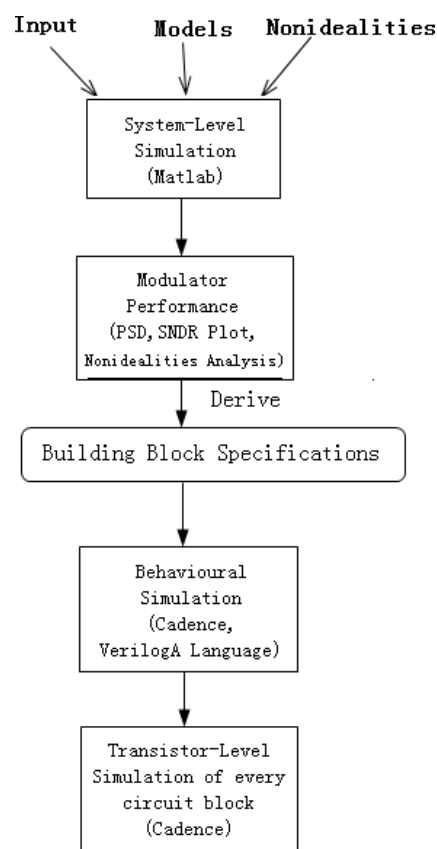
FIGURE 2.10 TYPICAL TOP-DOWN DESIGN FLOW FOR CONTINUOUS-TIME MODULATORS

At the system level, the design follows the flow shown in Figure 2.11. The design specifications are defined first. According to the specifications, initial design parameters are chosen, including sampling frequency, loop order, quantizer resolution and the DAC feedback pulse.

The transfer function is designed directly in continuous-time domain. Zeros and poles are optimized based on the analysis in Section 3.1. The clock jitter issue is also taken into account during the selection of the transfer function. Before building the topology, stability is predicted using the methodology described in Section 3.2. The modulator topology which

implements the transfer function is designed. Coefficients are tuned and scaled to achieve higher performance. Stability is measured again by checking the signal in time domain as well as using the previous methodology with the actual transfer function realized by the designed topology. During the examination of stability, one of the critical issues, excess loop delay will be analyzed carefully.

When the modulator achieves the required performance with certain margin in the ideal case, various non-idealities are added to examine their effects based on the methods and equations described in Chapter 3. The other main issues, such as DAC feedback mismatch and time constant variance are involved here. Some techniques are explored to compensate the performance degradation. Finally, the building block specifications for the circuit level design are derived.
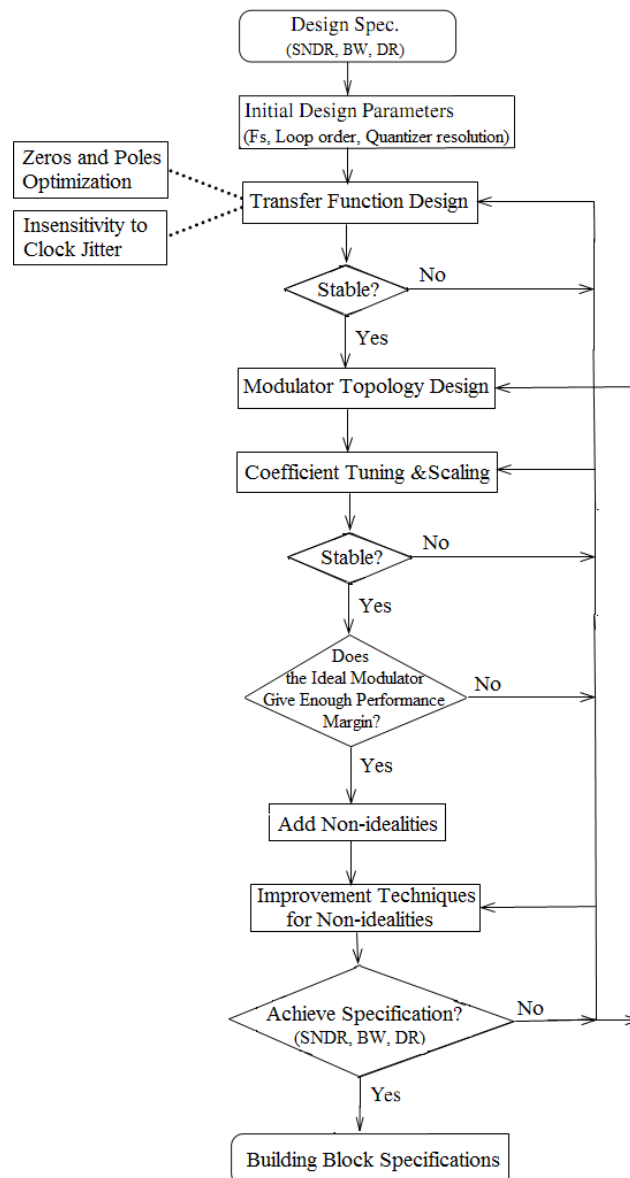
FIGURE 2.11 SYSTEM-LEVEL DESIGN FLOW OF CONTINUOUS-TIME MODULATOR

3 Design Issues of Continuous-time Sigma-delta Modulators

After selecting the basic parameters, such as oversampling ratio (OSR), quantizer number of bits, loop order and DAC feedback pulse, and the modulator topology, the design starts with the transfer function selection. For a modulator design, not only the required signal-to-noise-and-Distortion ratio (SNDR) must be fulfilled, but the stability should also be assured.

The non-idealities, including finite operational amplifier gain, bandwidth, slew rate, quantizer delay, multi-bit feedback DAC element mismatch, loop filter coefficients variation and clock jitter affect the performance and stability of continuous-time sigma-delta modulators. To guarantee a successful design, a thorough understanding of these non-ideal phenomena is required. They will be analyzed by adding them into the ideal architecture.

This chapter discusses the critical design issues, including the transfer function selection, the stability measurement and the analysis of non-idealities. Among the non-idealities, excess loop delay, clock jitter, multi-bit DAC mismatch and time constant variance are four key problems in the design of continuous-time sigma-delta modulators.

3.1 Transfer Function

At the beginning stage, there are two considerations when choosing a transfer function, the required SNDR and stability. A desired modulator should be stable for high input signal amplitude and simultaneously achieve maximum SNDR.

Significant improvement of the SNDR can be obtained by separating zeros over the signal range for high attenuation in the signal band and laying poles far away from the zeros. However, a system can be made more stable by placing poles near to zeros.

For the continuous time sigma-delta modulator, the excess loop delay and clock jitter are two main inevitable problems. The selection of transfer function becomes more complicated when these two effects are taken into account. They will be covered in the following section.

3.1.1 NTF Zero Optimization

Zeros are optimized assuming that the quantization noise is white, and the poles of the NTF have no significant effect on the in-band noise. The zeros are constrained for efficient noise shaping to the signal-band region.

Figure 3.1 shows the frequency responses of the NTFs without zeros, with zeros and with the best optimized zeros, and the simulated SNDR of the modulators with different NTFs. Seen

from the figure, shifting the zeros from dc results in a great SNDR improvement. An even greater benefit can be expected by optimizing the location of zeros of higher-order NTFs.
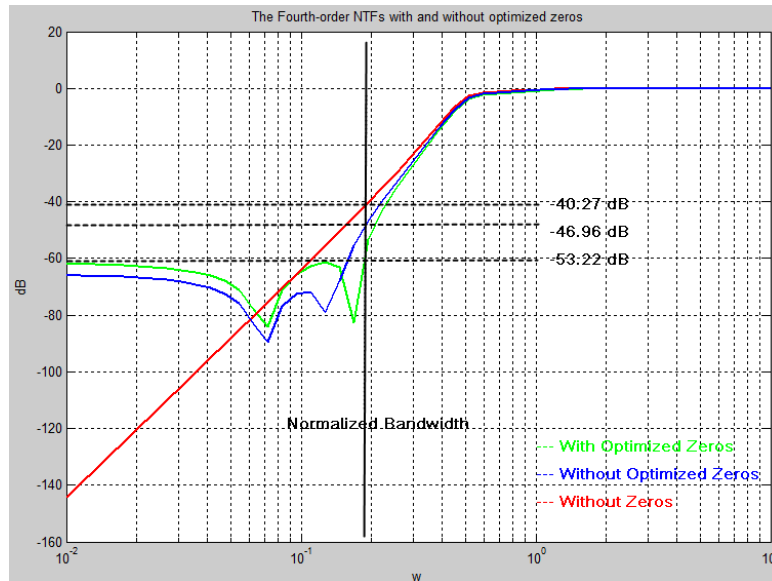
FIGURE 3.1 THE FOURTH-ORDER NTFS WITH AND WITHOUT OPTIMIZED ZEROS

The optimized zeros can be obtained by the filter design tools embedded in Matlab. They can be chosen according to the normalized cut off frequency and the required in-band noise suppression (IBS). More studies of zeros are done based on the 4th-order sigma-delta modulator, which has two pairs of zeros. The four zeros result in three areas of noise floor, the noise floor at low frequency, the noise floor between two zeros, and the noise floor at the edge of the bandwidth. The distance between the two pairs of zeros can have an effect on the noise floor. As the blue line plot in figure 3.1, although a little closer distance of the two pairs of zeros reduces the noise floor between two zeros, it increases the noise floor at the bandwidth edge by about 6.26dB, which can kill the performance largely. Through several simulations, the most optimized zero locations make the noise suppression equal in band, which is important for the suppression of quantization noise at the end of the signal band.

Moreover, the zeros can also be calculated theoretically. As the values of all the NTF zeros is relative to the normalized noise power, given by the integral of the squared magnitude of the NTF over the signal band, the optimal zeros can be found by equating the partial derivatives of the integral to zero. The method chooses $\pm\sqrt{\frac{3}{7} \pm \sqrt{(\frac{3}{7})^2 - \frac{3}{35}}}$[39], which is normalized to the bandwidth rad/ sec, as the optimized zero values for the 4th-order sigma-delta modulator. The values are the same with that obtained using the previous method.

3.1.2 NTF Pole Optimization

After the zeros are optimized, the choice of the poles can further reduce the quantization noise power in the signal band by increasing the distance of the poles from zeros, which leads an increase in the out-of-band NTF gain (OBG) at high frequencies, and consequently, leads to an increase in the total quantization noise power. Thus, the system becomes prone to instability.

Looking deeply into a fourth-order modulator, the relationship between the in-band noise suppression (IBS) and the out-of-band NTF gain (OBG) is not exactly a direct proportion. A fourth-order modulator has two pairs of poles. Figure 3.2 plots the relationship between IBS and OBG when adjusting each pair of poles. The simulation is performed based on the architecture shown in Figure 2.4 (a). It can be seen that there is a large difference in the amounts of IBS in two cases at the same OBG steps. The IBS can have a difference of 7.7dB when the OBG is 4dB. This means that it is possible to achieve a higher IBS without increasing the OBG by adjusting the two pairs of poles.
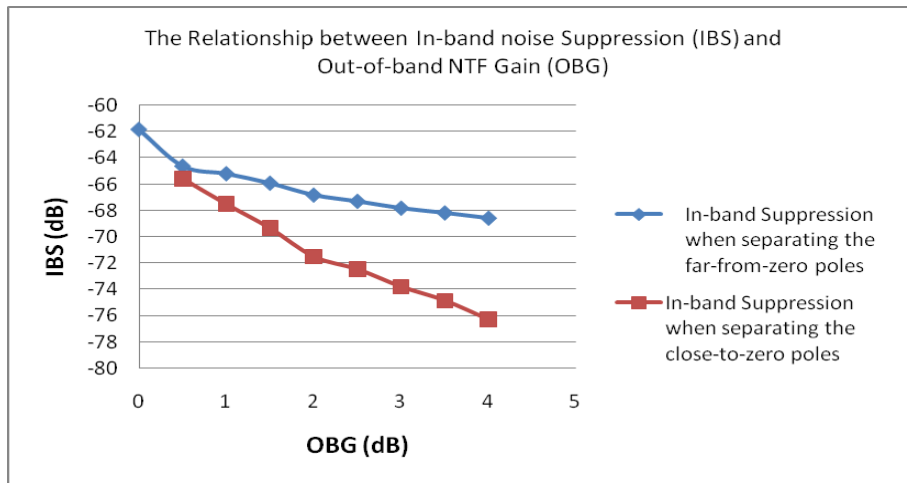
FIGURE 3.2 THE RELATIONSHIP BETWEEN IN-BAND NOISE SUPPRESSION (IBS)

AND OUT-OF-BAND NTF GAIN (OBG)

In this section, the zeros and poles are discussed mainly for the purpose of a better in-band noise shaping, as the first step. The critical concern is stability, which is largely determined by the poles. Hence, the location of the poles should be partially based on stability considerations. The problem will be studied in the next section.

3.2 Stability

For higher-order sigma-delta modulators, the tendency to instability is an important issue. A system is defined to be stable when all the integrator outputs remain bounded over time. A more stable system allows larger input amplitude.

Because of the non-linear quantizer, it has not been possible to find a mathematical solution for guaranteed loop stability of higher-order modulators. However, an insight to stability can be based on the analysis of limit cycles in order to predict the stability of the system. The first work here is to define the good measure ways used in the design.

Before the analysis, it is necessary to define the overloading input level (OVL), which is an important measure of the stability. The input signal above the overloading input level (OVL) makes the noise shaping useless, and adds more intolerable noise present inside the signal band. To have a comparison with the full-scale level (0dB), the OVL is expressed in dB to reference level (dBFS). In an ideal system, the OVL equals to full-scale level (0dBFS). In a realistic system, the OVL is usually a few dB lower than the full-scale level because of the modulation of the quantization noise with the input signal spectral components. The OVL varies with loop order, loop topology, quantizer resolution and NTF aggressiveness.

3.2.1 Root Locus

After the noise transfer function has been selected, the NTF is analyzed using the linear model first. Although the multi-bit quantizer cannot avoid the non-linearity problem, it is ignored in the first step. There are many ways for linear stability analysis: root locus, bode plot, etc. The root locus is more visible for the effect of the poles and zeros locations on the stability.

Figure 3.3 shows the model used in the root locus analysis. Before the quantizer, a gain k is inserted to model the effective quantizer gain kq, which is used as the variable gain of the root locus. The open loop transfer function H(s) is needed for the root locus calculation.
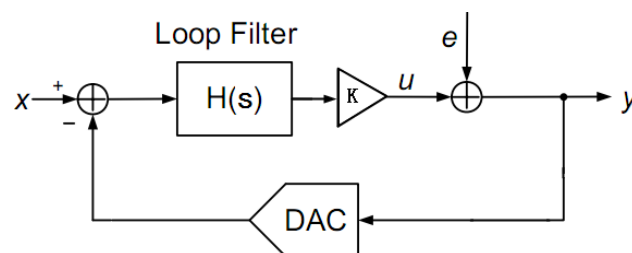
FIGURE 3.3 MODEL USED IN ROOT LOCUS ANALYSIS

Using this method, the root locus of a set of NTFs is plotted in Figure 3.4(b). Figure 3.4(a) shows the poles and zeros of the chosen NTFs. The NTFs are chosen as a group of Chebyshev I filters with gradually closer poles to the same zeros.

(a) Poles and Zeros of the NTFs   (b) Root Locus of the NTFs
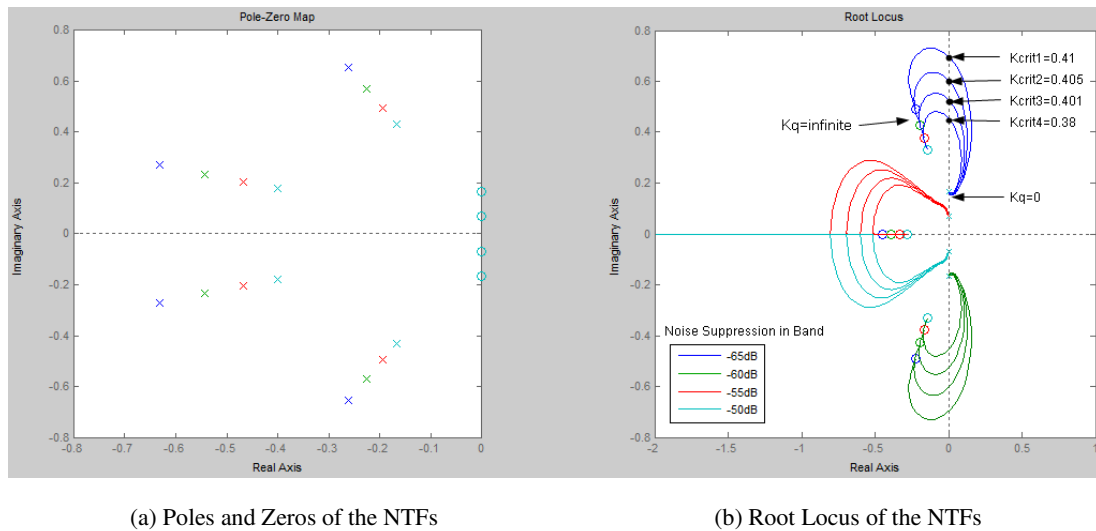
FIGURE 3.4 ROOT LOCUS OF A FOURTH-ORDER MODULATOR

WITH DIFFERENT SETS OF NTFS

As it can be seen in Figure 3.4, the pair of poles, which is closer to zeros, starts at dc s=(0,0) for kq=0, then goes towards kq=infinite. When kq=1, the pole values are exactly the poles of the chosen NTFs plot in Figure 3.4 (a). The possible instability arises from the poles, which leave the left plane for small quantizer gains kq and enter the right plane at a critical gain kcrit. The four sets of NTFs in the plot achieve a conditional stability, if the quantizer gain is larger than the critical gain. Moreover, for the fourth-order modulator, the other pair of poles, which is far from zeros, is always located inside the right plane. So they do not become a threat to the stability.

The critical gain is the minimum limitation of the effective quantizer gain to keep the system stable. Meanwhile, a high effective quantizer gain corresponds to a small quantizer input signal and thus to a limitation of the modulator input u, since the quantizer output is fixed to the reference. So the critical gain can be used to predict the overloading input level, which reflects the potential of stability. The system with a smaller Kcrit allows a larger OVL. That means the NTFs with a smaller Kcrit have more potential to build a stable system.

The four noise transfer functions are mapped to real modulator architecture for simulation. The OVLs are found as in Table 3.1, which proves the above analysis.

TABLE 3.1 THE CRITICAL GAIN AND OVERLOADING INPUT LEVEL

No.	IBS	SNDR	Kcrit	OVL
1	-50 dB	79.9 dB	0.38	-1dBFS
2	-55 dB	85.28 dB	0.401	-1.4dBFS

3	-60 dB	89.68 dB	0.405	-2dBFS
4	-65 dB	92.78 dB	0.41	-3dBFS

The question is how much accuracy the method provides. To what extent, the linear approach can predict the stability of the real system? As it can be seen in Figure 3.5(a), when the chosen NTF is mapped to the architecture, the simulated output power spectrum does not agree with the theoretical NTF curve closely. The figure is obtained from the simulation of the system with the 4th NTF in the above table. The simulated PSD is similar with the theoretical curve in shape, but the in-band noise is about 5 dB higher, and the 3rd harmonic distortion can be seen.
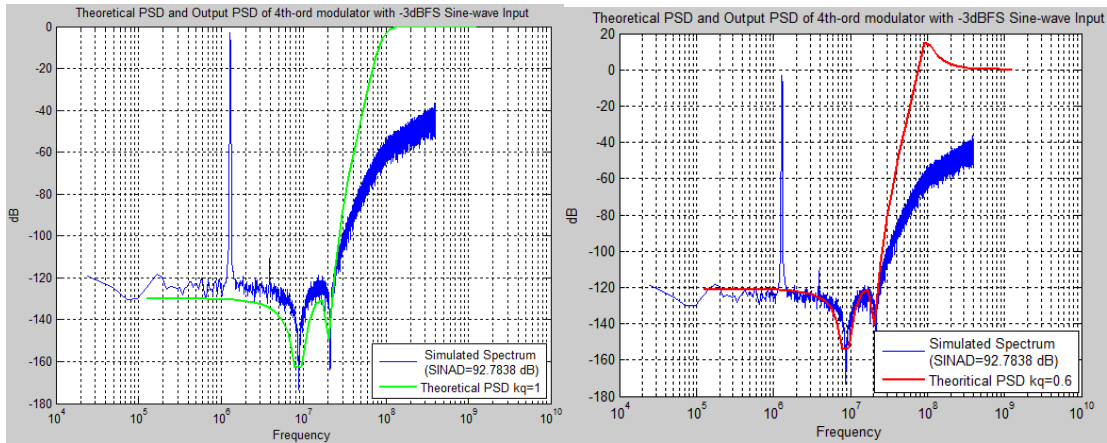
(a) The Mismatched Case with kq=1   (b) The Matched Case with kq=0.6

FIGURE 3.5 COMPARISON BETWEEN THE SIMULATED PSD AND THEORETICAL PSD

The inconsistence makes the stability measure using root locus less accurate. To take the disagreement between the simulated PSD and the theoretical PSD into account, it is useful to find out the actual NTF realized by the simulated modulator and come back to measure the stability using root locus again. Then the prediction of stability becomes more accurate.

The method is as follows. Assume the NTF chosen at the beginning is NTF_1, while the actual NTF from the simulation is NTF_k. As mentioned previously, the NTF_1 has its poles at kq=1. When the input amplitude is lowered, simulations show that the optimal value of the quantizer gain changes slightly. Thus, the NTF_k can be presented as

$$NTF_k = \frac{NTF_1}{kq+(1+kq)NTF_1} \quad [39] \qquad (3.2.1)$$

The effective quantizer gain kq is evaluated to achieve the match between the simulated power spectrum and the theoretical plot. In the above example, simulations indicated that a

more accurate NTF with small inputs can be derived if k is assumed to be 0.6. The new result is shown in Figure 3.5(b).

The root locus of the NTF_k is shown in Figure 3.6. The critical gain increases to 0.637dB, which means that the implemented system is less stable than the previous prediction.

(a) Poles and Zeros of the NTF   (b) Root Locus of the NTF
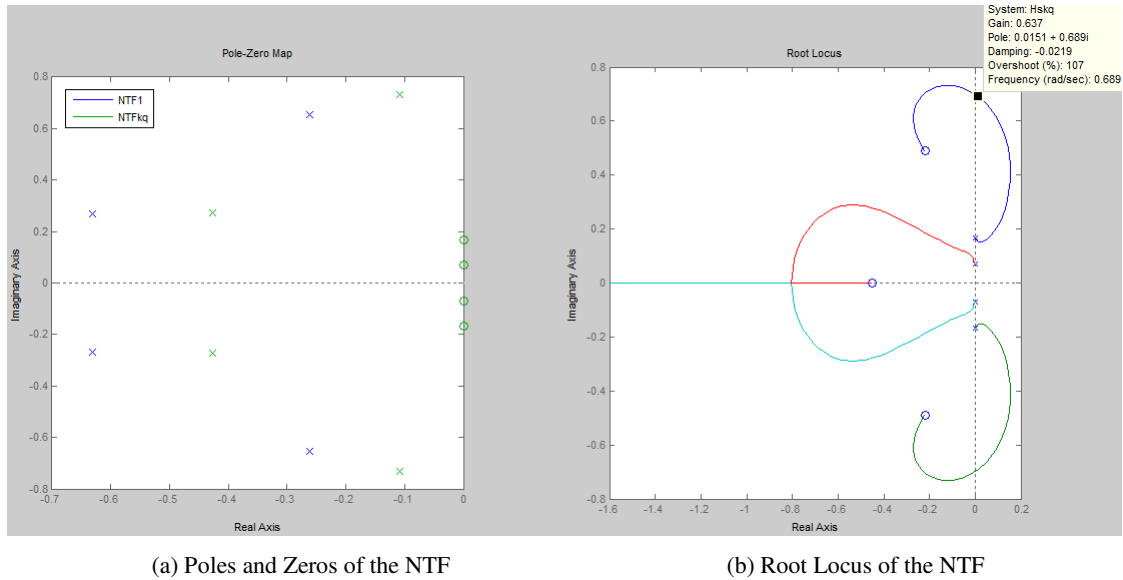
FIGURE 3.6 POLE ZERO LOCATION AND ROOT LOCUS OF THE MORE ACCURATE NTF

In conclusion, the implemented system could be less stable than the theoretical one. It is very dangerous if the stability is only predicted with the theoretical NTF using the linear model. It is necessary to take the nonlinearity effects in the reality into account to get an accurate prediction of the stability.

3.2.2 NTF Aggressiveness

The stability is the cost paid for the system aggressiveness. It is necessary to define the aggressiveness, as the concept will be used frequently in the later analysis.

As it is mentioned in many books, the NTF aggressiveness equals to a higher OBG. However, the conclusion mainly comes from the simulation based on 2nd-order sigma-delta modulators, but not exactly true for higher-order modulators which has several pairs of poles.

An aggressive NTF means to move more in-band noise outside, and hence achieve a higher SNDR. This is mainly achieved by a high IBS. A higher OBG can suppress the in-band noise floor further. However, OBG can also be kept flat with the adjustment of pole locations, as mentioned in section 3.1.2. On the other hand, in the system with the same IBS, a higher OBG may sharpen the slop at the bandwidth edge, which benefit to the SNDR. So the NTF aggressiveness must be evaluated by both IBS and OBG.

3.3 Excess Loop Delay

Excess loop delay arises because of nonzero transistor switching time, which makes the edge of the DAC pulse begin after the sampling clock edge. Practical comparators have non-zero time to generate the correct outputs. This delay is mainly determined by the comparator design and IC process, together with the finite time for the feedback DAC to respond, and the delay between the quantizer clock edge and valid DAC output.

For an NRZ DAC pulse, the excess loop delay can be depicted as in Figure 3.7. [37]
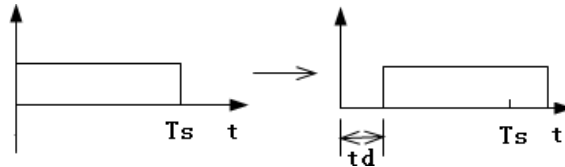
FIGURE 3.7 ILLUSTRATION OF EXCESS LOOP DELAY ON NRZ DAC PULSE

The loop delay t_d can be expressed as a fraction of the sampling period

$$t_d = \beta T_s \text{ [37]} \qquad (3.3.1)$$

3.3.1 Excess Loop Delay, NTF Aggressiveness and Stability

The main problem caused by excess loop delay is the stability of the modulator. The excess loop delay in an aggressive system is pushing the system easily to instability. As defined in Section 3.2.2, the NTF aggressiveness is associated with both IBS and OBG. So the excess loop delay is examined using NTFs with different IBS and OBS.

Firstly, a set of NTFs with different IBS and same OBG are simulated. The three NTFs 1-3 in Section 3.2.1 are used again here to check their tolerance for excess loop delay. They have 5 dB differences in IBS and the flat OBG 0dB. Figure 3.8 and Figure 3.9 shows the simulation results. The NTFs are marked by numbers and their IBS (dB). In Figure 3.8 the tolerance to loop delay and OVL of each NTF are indicated near each plot, when in Figure 3.9 the dynamic range is indicated together with the tolerance.

It can be seen that the more aggressive the NTF is, the less tolerance to excess loop delay the system has. The dynamic range of the most aggressive NTF (No.3) drops earliest. NTF No.2 is chosen for the following analysis, because it is moderate aggressive and achieves the dynamic range, which gives enough margins for other non-idealities.
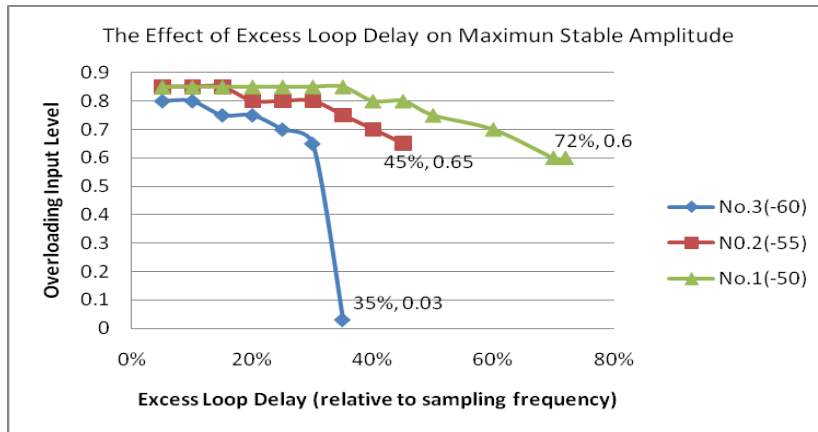
FIGURE 3.8 THE EFFECT OF EXCESS LOOP DELAY ON MAXIMUM STABLE AMPLITUDE (DIFFERENT NTFS WITH DIFFERENT IBS)
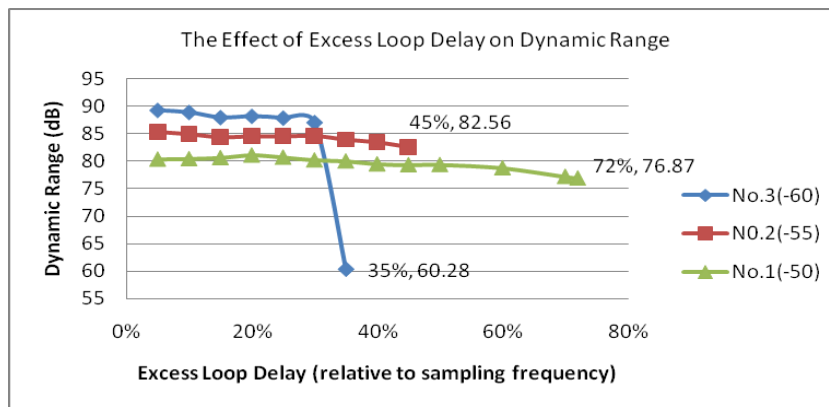
FIGURE 3.9 THE EFFECT OF EXCESS LOOP DELAY ON DYNAMIC RANGE (DIFFERENT NTFS WITH DIFFERENT IBS)

Further improvement in performance can be achieved by increasing the out-of-band gain, which degrades the tolerance to excess loop delay. So it is also meaningful to check the delay tolerance when the OBG is larger than 0dB. The simulations are performed using a set of NTFs based on the NTF No.2. The NTFs have the OBG which gradually increases. The IBS is increased from -55dB due to the non-zero OBG. Figure 3.10 and Figure 3.11 show the simulation results. The NTFs are marked by numbers, its IBS (dB) and OBS (dB).
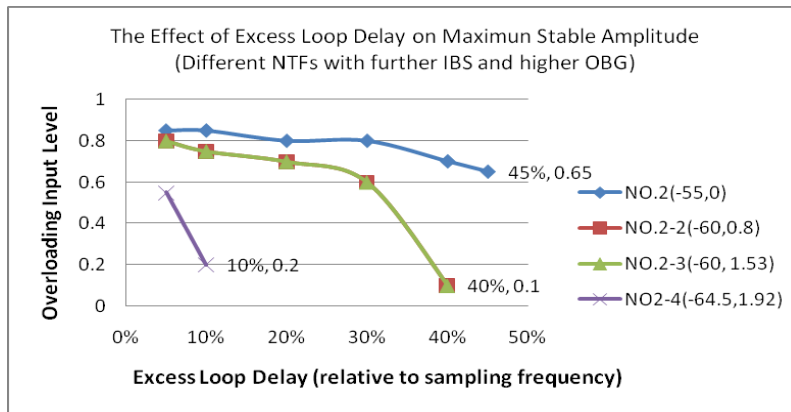
FIGURE 3.10 THE EFFECT OF EXCESS LOOP DELAY ON MAXIMUM STABLE AMPLITUDE (DIFFERENT NTFS WITH FURTHER IBS AND HIGHER OBG)
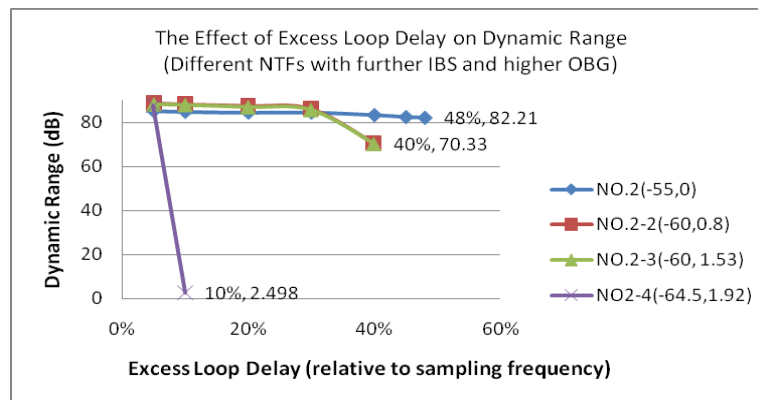
FIGURE 3.11 THE EFFECT OF EXCESS LOOP DELAY ON DYNAMIC RANGE (DIFFERENT NTFS WITH FURTHER IBS AND HIGHER OBG)

It can be seen from the figures, the NTFs No.2-2 and 2-3 have 5 dB IBS more than NTF No.2 due to a higher OBG. But their OVLs drop from 0.8 to 0.6 due to the stability problem caused by the higher OBG. Finally, the benefit of high IBS is counteracted by the decreased OVL. NTF No.2 achieves the same dynamic range because its OVL remains higher than NTFs No.2-2 and 2-3.

When the delay is larger than 30%, NTFs No.2-2 and 2-3 cannot tolerant any more loop delay and the systems go unstable immediately. The NTF No.2 is still stable until the delay is larger than 45%. The NTF No.2-4 with the largest IBS and OBG suffer the worst delay tolerance.

The conclusion here is that, non-zero OBG is of course an easy way to increase the IBS for higher SNDR. However, OBG should be monitored seriously when the system suffers excess loop delay. It would be better to keep OBG flat if the excess loop delay may become large. The above analysis shows that the high OBG does not benefit a lot in my case, so NTF No.2 is kept for the other analysis.

3.3.2 Compensation of Excess Loop Delay

The study of the excess loop delay compensation is simplified based on a second-order feedback architecture. Two main techniques have been used during the research, classical ELD compensation and ELD compensation using a differentiator.

In the classical ELD compensation, one extra DAC feedback path is added from the modulator output to the quantizer input, as shown in Figure 3.12.
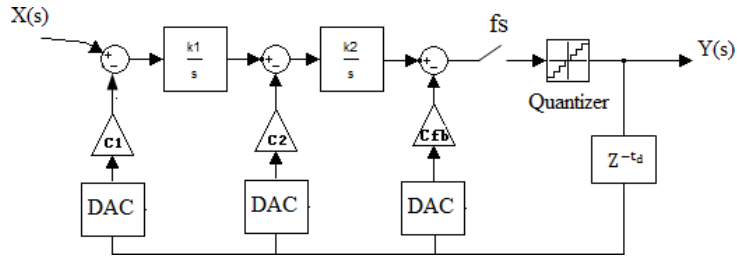
FIGURE 3.12 CLASSICAL ELD COMPENSATION

If the loop gains of the modulator without the extra DAC feedback are k1' and k2', the coefficients of the modulator with ELD compensation can be calculated with

$$\begin{cases} K_1 = \dfrac{K_1'}{1+K_1't_d} \\ K_2 = K_2'(1+K_1't_d) \\ C_3 = \dfrac{1}{2}K_2't_d(2+K_1't_d) \quad \text{[34]} \end{cases} \qquad (3.3.1)$$

In this way, the excess loop delay of up to one clock period may be compensated. However, this approach requires at least one additional DAC as well as one differential summing amplifier.

For the ELD compensation using a differentiator, the excess loop delay compensation path is moved from the output of the last integrator to its input, as shown in Figure 3.13.
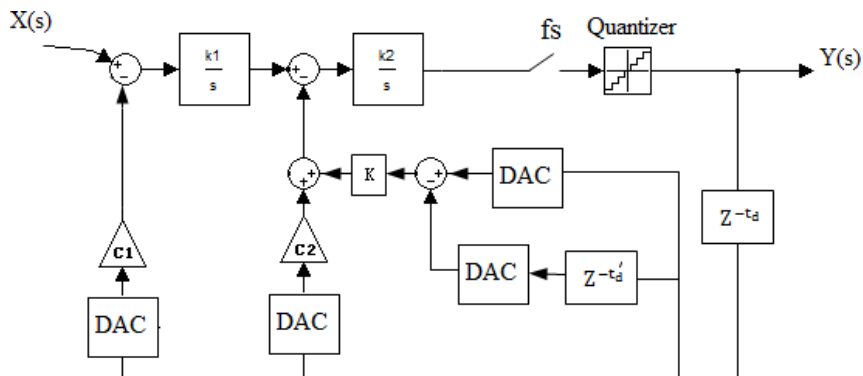
FIGURE 3.13 ELD COMPENSATION USING A DIGITAL DIFFERENTIATOR [34]

The delay t_d' added to compensate the excess loop delay must meet the requirement (3.3.2)

$$t_d' + t_d \leq \frac{1}{f_s}$$

The compensation feedback coefficient K can be calculated with

$$K = \frac{C_3}{t_d' K_2'} \quad [34]$$

(3.3.3)

since for low frequencies

$$1 - z^{-t_d'} \approx \frac{t_d'}{f_s} s \quad [34]$$

(3.3.4)

In this method, the differentiator is realized by an NRZ and a half-delayed return-to-zero DAC. This compensation technique avoids the use of summing amplifier.

By applying this compensation technique, the dynamic range of the modulator is improved. Table 3.2 and Figure 3.14 show the comparison.

TABLE 3.2 DYNAMIC RANGE VS EXCESS LOOP DELAY

Delay	Dynamic Range (dB)	
	Without Compensation	With Compensation
10%	84.94	84.94
20%	84.55	84.55
30%	84.62	84.62
40%	83.44	83.59
50%	82.21	82.74
60%	68.48	71.33
70%	62.95	67.1
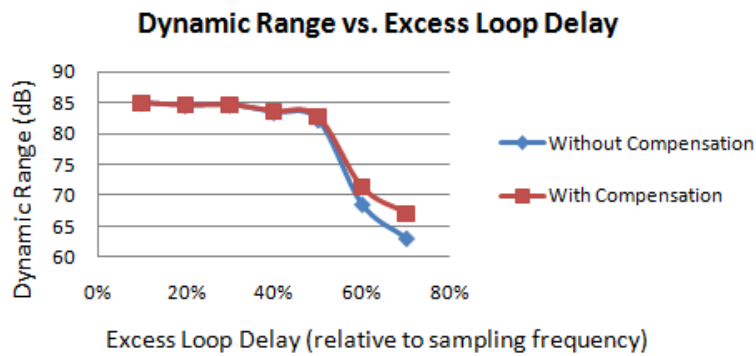
FIGURE 3.14 DYNAMIC RANGE VS EXCESS LOOP DELAY

3.4 Clock Jitter

The clock jitter causes a slight random variation in the amount of charge feedback per clock cycle, which causes the out-band noise to fold into the signal band, raising the noise floor and degrading the resolution.

There are two sources of clock jitter, the jitter at the internal ADC input and the timing error of the feedback DAC in the main loop. As the clock jitter of feedback DAC is critical, only this source is considered.

The error caused by clock jitter is the error in the area of the feedback pulses for every sampling period. [37] A reason for this is that the feedback pulse is at least integrated once in the loop filter. This integrated value corresponds with the area of the pulses, and hence, only the area is significant at the sampling instants at sampler S, instead of the actual shape of the pulse. For a NRZ feedback pulse, the expression of this area error is

$$\Delta A[n] = (y[n] - y[n-1]) * \Delta T_{DAC}[n] \qquad (3.4.1)$$

The additive error sequence $e_j[n]$ equals to the area error in the feedback pulses divided by the ideal timing T.

$$e_j[n] = \frac{\Delta A[n]}{T} = (y[n] - y[n-1]) * \frac{\Delta T_{DAC}[n]}{T} \quad {}^{[37]} \qquad (3.4.2)$$

This equation leads to the model in Figure 3.15. The jitter variance is generated by a Gaussian noise source.
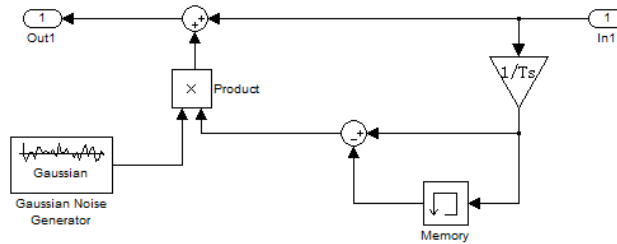
FIGURE 3.15 MODEL OF CLOCK JITTER

The clock jitter adds noise in band and raises the in-band noise floor. The Figure 3.16 shows the out power spectrum of the modulator implementing NTF No.2 with three different values of jitter deviation. It can be seen that the noise floor rises gradually when the jitter deviation increases. Although the noise floor of the system with 1% jitter deviation is the same as that of the system without jitter, the noise suppression benefit from separated zeros is reduced. The in-band noise is still dominated by the quantizer noise. With the increasing clock jitter, the notches produced by zeros are covered by the jitter-induced noise, which reduces the SNDR largely.
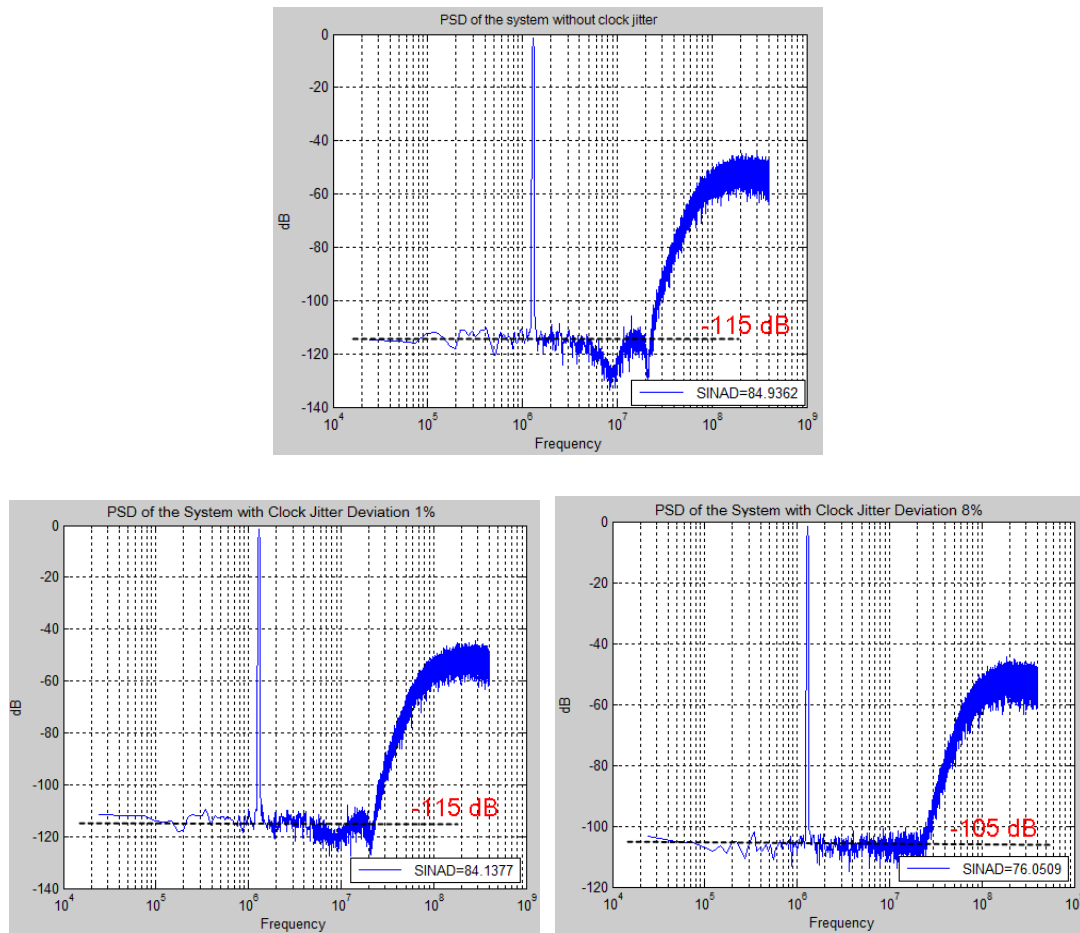
FIGURE 3.16 PSD OF THE MODULATOR WITH DIFFERENT CLOCK JITTER DEVIATION

Further simulations are done based on the set of NTFs used in the previous simulation. To show the effects more clearly, two more NTFs (No.4 and 5) are added. They are chosen with the same way as NTF No.1-3, setting different IBS. Figure 3.17 shows the simulation results. In the figure, the NTFs are marked with the number and their IBS.

It can be seen from the figure that the system performance benefits from the high IBS, only when the clock jitter deviation is small. However, when the jitter goes higher, the system with the most aggressive NTF (No.5) suffers first and merges with the plot of NTF No.3. The dynamic range of NTFs No. 1-3 and 5 become the same when the clock jitter equals to 5% of fs. That means there is no use to have higher IBS when the system has clock jitter larger than 5% of fs. Meanwhile, the systems with NTFs NO.1 and 4 do not suffer jitter-induced noise when the clock jitter is less than 6% of fs, hence the dynamic range remains stable.

The effect of Clock jitter on Dynamic Range

Legend:
- NO.5(-65)
- NO.3(-60)
- NO.2(-55)
- NO.1(-50)
- NO.4(-40)
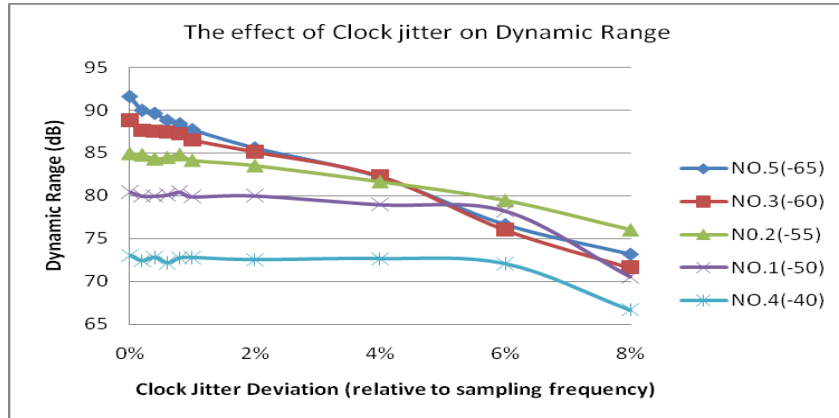
FIGURE 3.17 THE EFFECT OF CLOCK JITTER ON SNDR

(DIFFERENT NTFS WITH DIFFERENT IBS)

From the above analysis, the conclusion is reached that although an aggressive system can achieve better performance in ideal case, it can be more sensitive to even small clock jitter. When the clock jitter is taken into account, the NTF achieving the highest dynamic range is no longer the best choice.

In many previous works, the NTF is usually chosen at first according to the requirements of performance without taking the clock jitter into account. Afterwards, the techniques of reducing clock jitter are applied to release the sensitivity. However, the above analysis shows the necessity to choose a NTF less sensible to clock jitter at early stage of the design. As long as the required performance is guaranteed, the insensitivity to clock jitter can be achieved by minimizing the in-band noise suppression.

By taking the clock jitter and the stability into consideration, the proposed noise transfer function is chosen as

$$NTF = \frac{s^4 + 0.028s^2}{s^4 + 1.321s^3 + 0.905s^2 + 0.366s + 0.074} \qquad (3.4.3)$$

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3.5 Multi-bit DAC Mismatch

For a high-speed modulator with MHz range input signal, low oversampling ratios (<32) are a must for a reasonable high clock frequency. In such cases, a multi-bit quantizer is needed to lower the quantization noise, improve the loop stability and reduce the clock jitter sensitivity for CTsigma-delta modulators. The multi-bit quantizer also means a multi-bit DAC in the feedback path. While a single-bit DAC has inherent linearity, a multi-bit DAC leads to unavoidable element mismatch and nonlinearities. The nonlinearity problem may severely limit the modulator performance.

The DAC mismatch error is added directly to the input signal directly, and goes through the signal transfer function together with the signal. This means the DAC mismatch experiences no attenuation in the signal band when it appears in the modulator output. High DAC linearity requires precise matching of the DAC unit element. However, current CMOS processes can only provide 0.1% matching accuracy (10-bit) for capacitors, and matching accuracy for transistors is even poorer than that of capacitors. To obtain more than 10-bit resolution, DAC mismatch errors must be suppressed below the modulator overall linearity requirement.

3.5.1 DAC Architecture

Figure 3.18 (a) shows the integrator using resistor based DAC feedback for continuous time sigma-delta modulators. The currents from both paths are summed and integrated on Ci. Moreover, due to the necessity of high-precision calibration, it is more common to implement the DAC using current sources, especially in CMOS technologies, as shown in figure 3.18 (b). Both the circuits can be extended for multi-bit DACs by adding DAC paths, independently connected to the same Vref.

(a) RC Integrator with DAC Resistors   (b) RC Integrator with Current-steering DAC
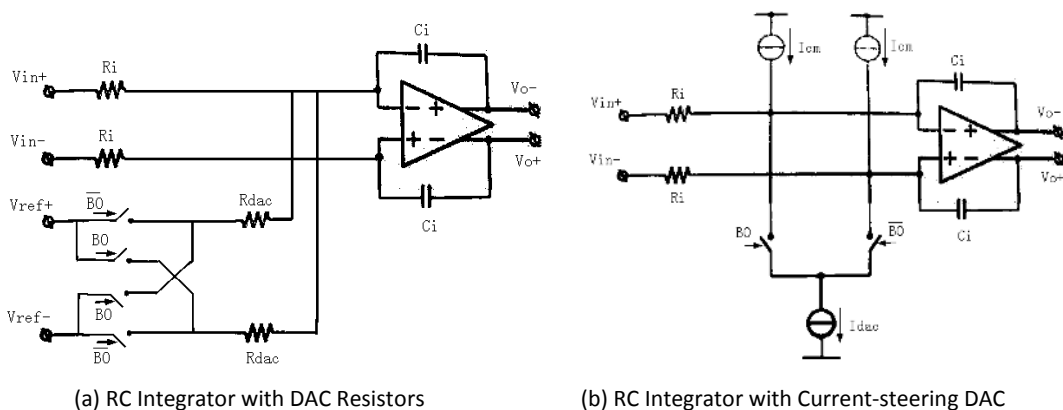
FIGURE 3.18 RC INTEGRATORS WITH DAC FEEDBACK FOR CONTINUOUS TIME IMPLEMENTATION

Since the reference and sum elements as well as switches are relatively easy to implement, the current-steering DAC is commonly used for continuous-time modulators in a CMOS process. The current-steering DAC is suitable for high-speed high-resolution applications.

The disadvantage is its sensitivity to device mismatch, glitches, and current source output impedance. So special care should be taken to improve the matching of the DAC.

Figure 3.19 shows the N-bit current steering DAC architectures with binary weighted code and thermometer code. In a binary weighted DAC, the current sources, which are controlled by the input bits bi, are binary weighted, as shown in figure 3.19(a). The output current Iout is given by

$$I_{out}(k) = I_{LSB} \cdot b_0 + 2I_{LSB} \cdot b_1 + \ldots + 2^{N-1}I_{LSB} \cdot b_{N-1} = I_{LSB} \cdot k \qquad (3.5.1)$$

The advantage of binary weighted DAC is that the number of switches and digital encoding circuits become minimal in this architecture. The disadvantage is that for a large number of bits, the difference between the MSB(b_{N-1}) and LSB(b_0) weight is very large and the converter is very sensitive to mismatch errors.

(a) Binary Weighted Coded DAC   (b) Thermometer Coded DAC
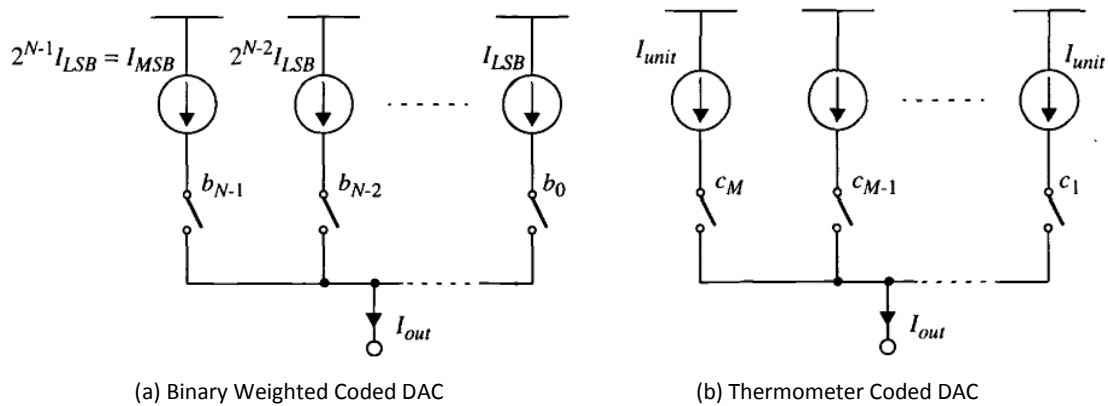
FIGURE 3.19 N-BIT CURRENT-STEERING DACS

In the thermometer coded DAC, the binary input code is encoded into a thermometer code as illustrated in Table 3.3. The current sources representing the reference elements are all equally weighted and the matching of the individual elements becomes simpler than for the binary case. The transfer function of the DAC is monotonic and the requirement on element matching is relaxed. However, there are M=2^N-1 thermometer coded bits for N binary bits. The number of switches and current sources is increased to M, which makes the circuit more complicated.

TABLE 3.3 DECIMAL, BINARY OFFSET, THEMOMETER CODE REPRESENTATIONS

Decimal	Binary Offset	Thermometer
0	000	0000000
1	001	0000001

2	010	0000011
3	011	0000111
4	100	0001111
5	101	0011111
6	110	0111111
7	111	1111111

The mismatch error of a current source can be modeled as an additional current source in parallel with the nominal current source, as shown in Figure 3.20 for the current source corresponding to bit i.
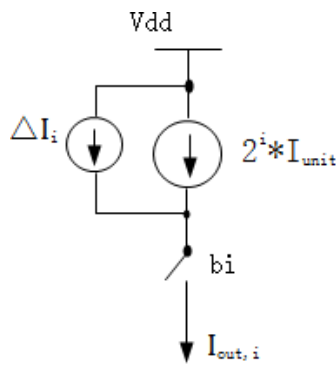
FIGURE 3.20 MODELING OF CURRENT SOURCE WITH ERROR CURRENT SOURCE $\triangle I_i$

The actual output is then given by

$$I_{out,i} = b_i * (2^i * I_{unit} + \triangle I_i) \qquad (3.5.2)$$

In the thermometer-coded DAC, the currents from the selected elements are summed to compose the output current. The total current error equals to the sum of the error of every element, as given by

$$I_{out,actual} = I_{out,ideal} + \triangle I = I_{out,ideal} + \sum_{i=0}^{N-1} \Delta I_i(b_i) \qquad (3.5.3)$$

$\triangle I_i(b_i)$ is estimated by the relative error current in the i-th bit, $\delta_i(b_i)$. For one specific DAC the matching error associated with one current source is fixed. Assume the design is used for a large number of chips, the matching error will be Gaussian distributed and uncorrelated with each other.

3.5.2 Dynamic and Element Matching

A multi-bit DAC can utilize the principle of noise shaping to reduce its nonlinearity effects. The procedure of suppressing the mismatch error is the same as that of sigma-delta data conversion: use filtering to suppress the noise spectrum in the signal band and to shift its power to out-of-band frequencies.

There are two signal-processing techniques to enhance the linearity of multi-bit sigma-delta modulators due to DAC element mismatch, dynamic element matching (DEM) and digital calibration. The digital calibration schemes are usually expensive to implement in terms of system design complexity, hardware requirement, and power consumption. The dynamic element matching (DEM) is the most extensively used technique to reduce the DAC mismatch error. However, DEM introduces additional delay in series with the DAC that leads to additional excess loop delay which must be accounted and dealt with.

For the DAC built with unit elements, DEM technique encodes the quantizer output bits into thermometer codes, and rearranges them according to certain strategies for the selection of the unit elements. The element selection logic determines the DEM algorithm to be employed.

In a conventional thermometer coded DAC, the input number is represented by fixed reference elements in the DAC, which causes the matching errors to be strongly signal-dependent. The rearrangement of the DAC elements does not affect the data value, but changes the priority of selecting the unit elements. By doing this, different references are chosen to represent the input number so that the matching errors are no longer signal dependent. The average DAC output matches the ideal mean value. The unit-element DAC structure is shown in Figure 3.21. For the DEM technique, it is commonly assumed that the offset and gain errors of the DAC are acceptable, and only the DAC nonlinearity error is of concern.
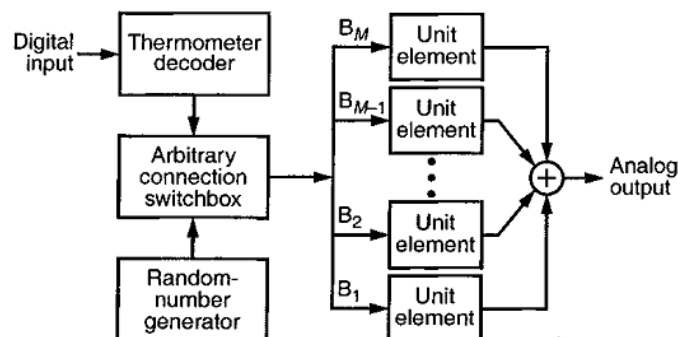
FIGURE 3.21 UNIT-ELEMENT DAC WITH RANDOMIZED ELEMENT SELECTION

Among the commonly used strategies of DEM technique, data-weighted averaging (DWA) is selected in this design. DWA algorithm uses all the DAC elements at the maximum possible rate while ensuring that each element is used the same number of times. The unit elements participating in the D/A conversion are selected sequentially from the DAC array, beginning with the next available unused element, as it is shown in figure 3.22. Through such a rotational element-selection process, DWA achieves first-order high-pass shaping of the DAC mismatch errors. The DAC errors will quickly sum to zero, moving distortion to high frequencies. Besides, compared with other algorithms, DWA algorithm preserves the modulator noise shaping.
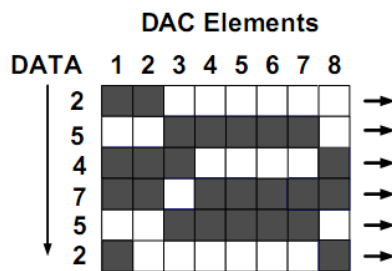
FIGURE 3.22 ILLUSTRATION OF DWA

However, DWA has some disadvantages. Firstly, it suffers the in-band tonal problem resulting from its intrinsic periodicity. For example, if a dc level signal is applied to the ADC, the DWA will continue repeating the same sequence of elements. Since these elements contain mismatch, the corresponding mismatch sequence will create a fixed repetitive pattern, namely it will generate an oscillation. The tones introduced by the DWA out of band mix with out of band noise and other undesired signals, and then is downconverted back into the desired signal band.

The DWA DAC used in this design is shown in figure 3.23. Its input comes from the quantizer, which is in the range {-1, -1+LSB, … 1-LSB, 1}. The element selection logic consists of a thermometer encoder and a barrel shifter. In addition, the barrel shifter consists of a modulo-N block, a unit delay, and a bit counter. At each sample time n, the bit counter counts the number of 1's in the incoming code. The barrel rotator uses the output z[n] originated from the bit counter to control the operation of rotation, so that the input digital signal is converted to analog signal using the next unused unit elements of DAC. The control data z[n] at sample time n is calculated as $(z[n-1]+B[n]) \mod (2^{BN}-1)$. BN is the bit number of the DAC.
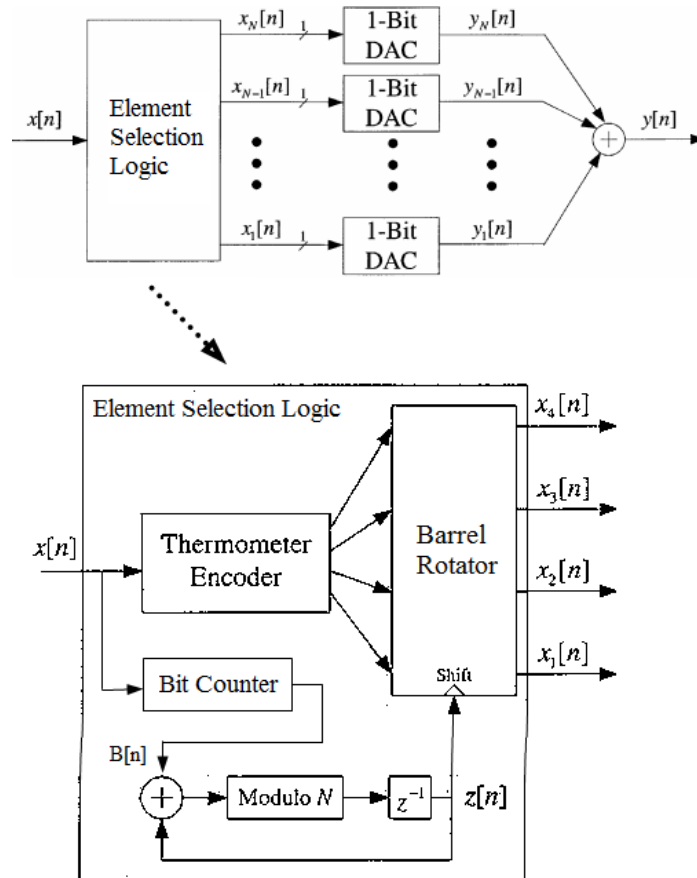
FIGURE 3.23 THE DWA DAC

Based on the algorithm in the above figure, the model is built in Matlab, as shown in Figure 3.24.
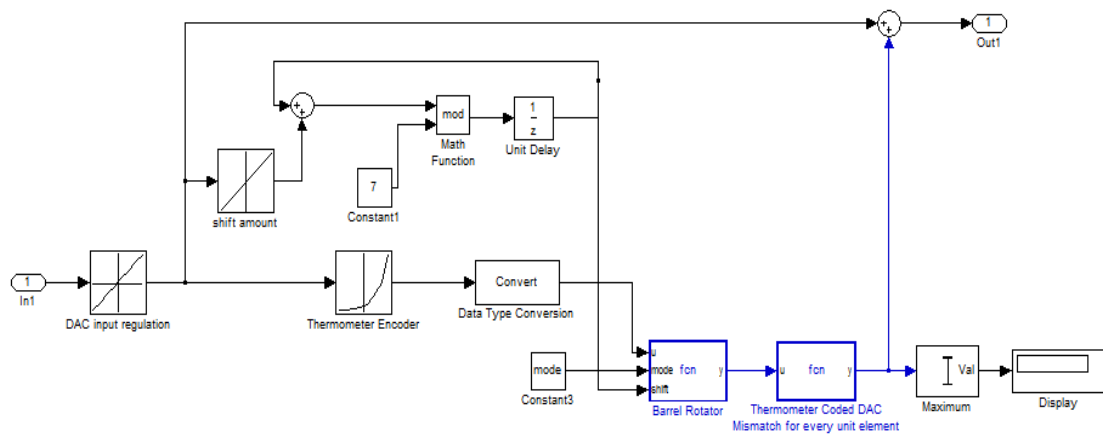
FIGURE 3.24 MODEL OF DWA DAC

Table 3.4 and Figure 3.25 show the effects of DAC mismatch on the SNDR when the modulator uses nonlinear DAC and the DAC applying DEM technique.

TABLE 3.4 THE EFFECT OF DAC MISMATCH ON SNDR

INL	SNDR (dB)	
	Nonlinear DAC	DEM DAC
0.002%	81.95	82.47
0.03%	73.05	79.66
0.04%	74	77.95
0.05%	72.79	75.32
0.06%	72.08	74.52
0.10%	60.8	65.99
0.30%	57.19	61.04
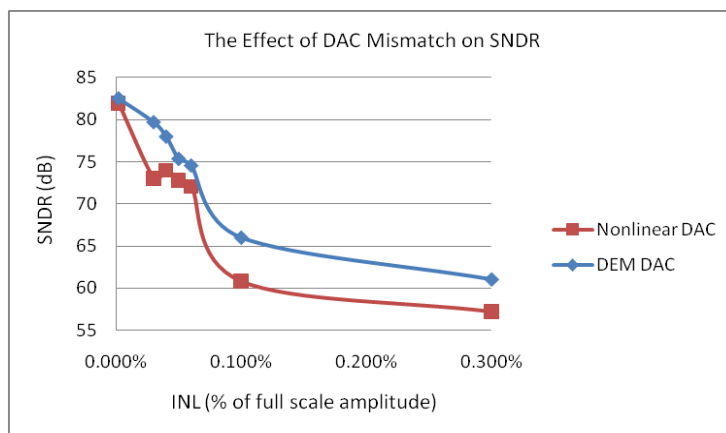
FIGURE 3.25 THE EFFECT OF DAC MISMATCH ON SNDR

3.6 Time Constant Variance

In a continuous time sigma-delta modulator, the transfer functions depend on the absolute values of resistors and capacitors, which largely vary over process, supply voltage, temperature, etc. Process variations of the absolute component values may be 10-20%, which increases the possible variation of the RC-product to more than 30%. Therefore, the time constant variance is very important to investigate in continuous time sigma-delta ADCs.

The common way to keep control over the transfer function variation over PVT (process-supply voltage-temperature) variations is to calibrate the resistors, capacitors and other parameters, e.g. amplifier transconductances etc. Some automatic resistor and capacitor trimming scheme can be employed to tune the time constants of the active RC integrators.

A model can be built at system level to investigate the tolerance of the time constant variance for the modulator. The integrator transfer function is modified by adding the

variance term $\triangle$rc, as follows. The additional term with $\triangle$rc can be modeled as an equivalent gain error GErc of the integrator.

$$H(s) = \frac{1}{sR_{IN}C_{FB}(1+\Delta rc)} = GErc * \frac{1}{sR_{IN}C_{FB}} \quad [41] \qquad (3.6.1)$$

$$GErc = \frac{1}{1+\Delta rc} \qquad (3.6.2)$$

The gain variations add in-band noise (IBN), which is given in the following equation for multi-bit Nth-order single-loop modulator.

$$IBN(GE) \approx \frac{\pi^{2N}}{2N+1} \frac{LSB^2}{12} \frac{1}{OSR^{2N+1}} \frac{1}{GErc^2} \quad [41] \qquad (3.6.3)$$

Figure 3.26 shows the effect of the RC time constant variation on IBN and SNDR by plotting both the calculated IBN and simulated IBN. The RC variance is swept in the range from -40% to 40%.
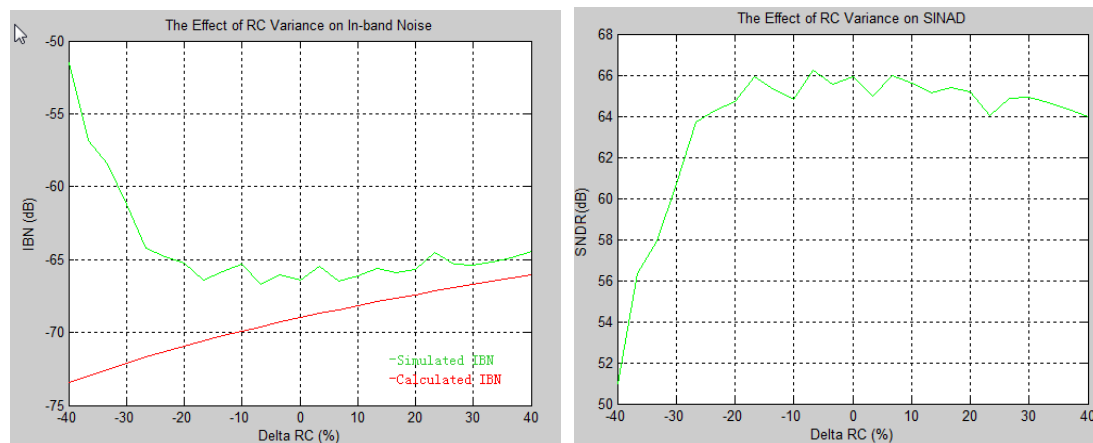
FIGURE 3.26 THE EFFECT OF TIME CONSTANT VARIANCE ON IBN AND SINAD

The analysis can be divided into two parts. Firstly, when the RC variation is positive, the simulated values are very close to the calculated values. According to equation (3.6.3), the gain error leads to a reduced integrator gain; hence the in-band noise is increased. Fortunately, the SNDR is reduced only a little. This is because the variation of the integrator gain varies the poles of the NTF slightly, but not the zeros at dc.

Secondly, when the RC variation is negative, the increased integrator gain results in aggressive noise shaping. The simulation results show that a slight increase in SNDR can be achieved. However, when the negative RC variation is larger, the simulation results do not agree with the calculated values anymore and dropped dramatically. By checking the signals in the time domain, the quantizer is found to be overloaded. That means a large negative RC

variation results in the instability problem, hence largely decreased SNDR. The equation (3.6.3) is only limited to the stable system.

It is gained from the above analysis that the task to increase the tolerance of time constant includes two parts. One is to enlarge the range of closed loop gain of the integrator. The other is to set a symmetric tolerance of negative and positive time constant by adjusting the loop gain at the middle of its range.

To enlarge the range of loop gain is actually to minimize the negative edge of time variance range. This is because the positive edge is set according to the performance requirement, while the negative edge is limited by the instability. There has a trade-off between time constant variance and excess loop delay. The loop gain is tuned to achieve the maximum range in a stable system.

After the range of loop gain is enlarged, the loop gain is set to have a symmetric tolerance of negative and positive time constant. Table 3.5 and Figure 3.27 show the SNDR of the modulator with asymmetrical tolerance range and symmetrical tolerance range. The asymmetrical range (-40%~10%) is adjusted to the symmetrical range (-30%~30%) by increase the loop gain. The increased loop gain reduces the tolerance of negative time constant to allow more tolerance of positive constant.

TABLE 3.5 THE ADJUSTMENT OF TIME CONSTANT VARIANCE TOLERANCE RANGE

Delta RC (%)		-50	-40	-30	-20	-10	10	20	30	40
SNDR (dB)	Asymmetrical Tolerance	74.38	80.96	79.65	79.4	79.85	79.2	76.77	75.12	73.96
	Symmetrical Tolerance	69.97	74.21	80.77	80.01	79.69	79.32	79.39	79.12	76.98
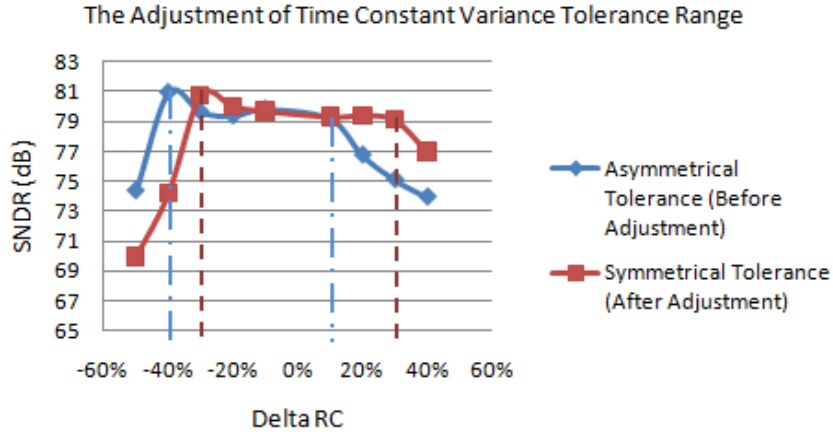
FIGURE 3.27 THE ADJUSTMENT OF TIME CONSTANT VARIANCE TOLERANCE RANGE

3.7 Other Non-idealities

3.7.1 Finite Opamp Gain

The finite operational amplifier gain affects the transfer function of the continuous time integrator.

The main building block for continuous time sigma-delta modulator is an ideal low-pass filter or integrator, which implements a transfer function with its only pole at DC:

$$H(s) = \frac{a}{s}$$ (3.7.1)

where a is the gain-bandwidth product (GBW) of the integrator.

To implement this function, an active RC integrator can be used, as shown in Figure 3.28.
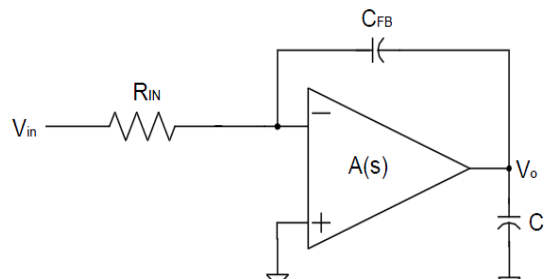
FIGURE 3.28 ACTIVE RC INTEGRATOR USED IN CT SD MODULATORS

The transfer function of the ideal integrator is

$$H(s) = \frac{1}{sR_{IN}C_{FB}}$$ (3.7.2)

where R_{IN} is the value of input resistror, and C_{FB} is the value of the integration capacitor.

When a finite amplifier gain is taken into account, the integrator transfer function changes to

$$H'(s) = \cfrac{1}{\cfrac{1}{A_{DC}} + sR_{IN}C_{FB}}$$ [44]   (3.7.3)

where A_{DC} is the dc gain of opamp.

The equation shows that both the DC gain of the integrator and its pole are affected by the finite DC gain of the amplifier. The pole is pushed away from dc to $1/A_{DC}R_{IN}C_{FB}$. However, the pole of the loop filter becomes the zero of the NTF. The away-from-dc zero at the frequency given by $f=(2\pi A_{DC}R_{IN}C_{FB})^{-1}$ reduces the amount of attenuation of the quantization noise in the baseband. High A_{DC} is beneficial.

The equation for the in-band noise caused by the leaky integrators in a 2nd-order modulator is shown as follows:

$$IBN(A_{DC}) \approx \frac{\Delta^2}{12}\left(\frac{\pi^4}{5}\frac{1}{OSR^5} + \frac{2\pi^2}{3}\frac{1}{OSR^3A_{DC}^2} + \frac{1}{OSRA_{DC}^4}\right)$$ [41]   (3.7.4)

As it can be seen from the equation, if the dc gain A_{DC} of the Opamp is set in the range of the oversampling ratio $A_{DC} \approx OSR$ of the modulator, every part of the in-band noise keeps proportional to $1/OSR^5$. Even though the modulator can still benefit from large dc gain, the CT sigma-delta modulators have more relaxation on the dc gain compared with DT implementations.

3.7.2 Finite Gain-Bandwidth Product

For a continuous-time implementation, the finite gain-bandwidth product of the amplifier affects the in-band quantization noise power by changing the NTF shape. It introduces a gain error and an additional second pole into the ideal transfer function of the integrator.

To consider the influence of finite gain bandwidth GBW, the ideal integrator with a transfer function $H(s) = \frac{1}{sR_{IN}C_{FB}}$ is replaced with a single-pole amplifier, whose transfer function is given as follows.

$$A(s) = \cfrac{A_{DC}}{1 + \cfrac{sA_{DC}}{\omega_A}}$$ [44]   (3.7.5)

$$GBW = A_{DC} * \omega_A \text{ [rad/s]}$$ (3.7.6)

The integrator transfer function changes to

$$H(s) = \frac{1}{sR_{IN}C_{FB}} \times \frac{GE}{\frac{s}{\omega_2}+1}$$

(3.7.7)

$$GE = \frac{GBW}{GBW + \frac{1}{R_{IN}C_{FB}}} \quad [31]$$

(3.7.8)

$$\omega_2 = GBW + \frac{1}{R_{IN}C_{FB}}$$

(3.7.9)

where GE is the gain error factor and w_2 is the additional second pole.

From these equations, if the gain bandwidth GBW is large, GE$\approx$1 and ω_2 >> $1/R_{IN}C_{FB}$. However, when GBW is finite and not large enough, the problems raise up. The effect of gain error can be analyzed in the same way as described in section 3.6.

The non-ideal integrator is modeled as a cascade of an ideal integrator and a first-order low-pass filter [31], as depicted in Figure 3.29.
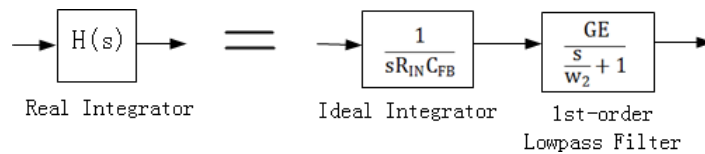
FIGURE 3.29 SYSTEM-LEVEL DESCRIPTION OF A REAL INTEGRATOR

The finite DC gain and finite gain-bandwidth product (GBW) parameters values were swept to examine their effects on SNDR. DC voltage gain VS SINAD and Gain-Bandwidth product VS SINAD are plotted in Fig. 3.30 and Fig.3.31 respectively.
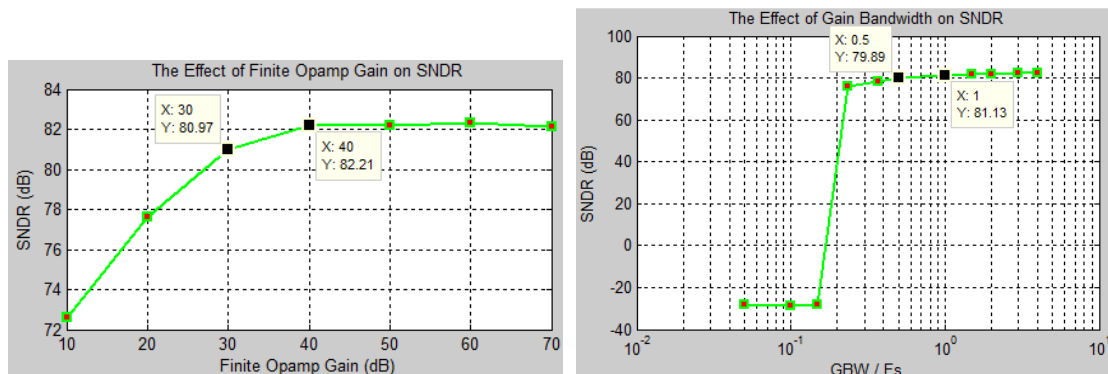
FIGURE 3.30 THE EFFECT OF FINITE OPAMP GAIN ON SNDR

FIGURE 3.31 THE EFFECT OF UNIT GAIN BANDWIDTH ON SNDR

It can be seen from the figures that the dc gain of 40dB is enough and the limitation of gain bandwidth can be around 1 or 2 times of the sampling frequency. Compared with the typical gain bandwidth limitation GBW≥5fs in DT implementation, the requirement in CT implementation is relaxed a lot. Figure 3.31 also shows that the unit gain bandwidth can be half of the sampling frequency and the SNDR remains 79.89 dB.

3.7.3 Integrator Output Swing

The limitation of the integrator outputs, also known as clipping, is principally a signal-dependent variation of the system states from their ideal values. An Mth-order sigma-delta modulator has M states whose values at sampling instants completely determine the modulator behavior. The integrator output voltages are precisely the system states. So the output swing of the opamp must be made large enough to produce the required state values, otherwise the modulator behavior will be altered or even signal-dependent.

The limitation of the integrator output signals results in severely increasing baseband noise as well as distortion. The clipping can be avoided by proper parameter scaling or the optimized architecture.

To keep a reasonable signal swing for CMOS 90nm technology, three ways are proposed. Firstly, the feedforward path is added from the input signal to the quantizer input directly to reduce the output of the first integrator. Secondly, the closed loop gain of the integrator can be reduced in the case that the noise shaping is still guaranteed for the required SNDR. But the loop gain with the negative time constant variance also turns to be large. Finally, make the modulator work at lower input amplitude to keep the system stable with a large closed-loop gain. However, the benefit is not big as the reduced input also reduces SNDR.

3.7.4 Thermal Noise

The thermal noise is one of the serious problems at high conversion bandwidths. The performance could be limited by white thermal noise rather than shaped quantization noise.

The thermal noise of the first op-amp must be kept small. It is inversely proportional to the transconductance gm of the input MOS differential pair, which can be controlled by sizing the input devices appropriately. However, the large gm consumes more power. The transconductor of the first integrator in a continuous-time sigma-delta modulator is the most important for overall thermal noise.

4 System Level Design

In this chapter, the system level design of a 4th-order 3-bit continuous-time sigma-delta modulator for wireless applications is presented, including the considerations of system level parameters selection, the loop filter architecture design and the optimization of the modulator architecture. The simulation results are shown taking various non-idealities into consideration based on the methods and equations described in Chapter 3.

4.1 System Level Parameters

Selecting the system level parameters is the first step to design a sigma-delta modulator, including oversampling ratio (OSR) selection, quantizer number of bit (N) and loop order (L). The target is to design a continuous-time sigma-delta modulator with 75 dB dynamic range and 25 MHz bandwidth. The power consumption is not a consideration.

Before making the decisions, a survey has been done on several previous designs. Table 4.1 lists the performance gained with different parameters selection.

TABLE 4.1 SURVEY ON THE PREVIOUS WORK OF CONTINUOUS-TIME SIGMA-DELTA MODULATOR

References	[24]	[31]	[30]	[29]
Loop Ord	3rd	4th	3rd	5th
Quant Bit	5	4	4	3
Technology, supply	0.5um CMOS, 3.3V	0.13um CMOS, 1.5V	0.13um CMOS, 1.2V	0.18um CMOS, 1.8V
OSR	16	10	16	32
Clock Freq	35.2MHz	300MHz	640MHz	640MHz
DR	88dB	67dB	80dB	87dB
Bandwidth	1.1MHz	12-15MHz	20MHz	10MHz

The sampling rate of the continuous-time sigma-delta modulator is limited by the device speed in a given technology. For a 25 MHz bandwidth the OSR cannot be very large because of the limited sampling rate. If the OSR is selected to be 16, multibit quantizer bit is necessary to keep 75dB dynamic range. The number of bit in the quantization and loop order can then be chosen using the following equation

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N-1)^2 \times OSR^{2L+1}$$

(4.1.1)

As realized in the previous papers, for the modulators with dynamic range 70-90dB and bandwidth 10-20MHz, the quantizer bit is set around 3-5bits and the loop order is set around 3rd-5th order. Considering the linearity and stability, a 3-bit 4th-order architecture has been chosen.

Due to the large loop coefficients variation in CT modulators, it is difficult to achieve sufficient matching between analog loop and digital cancellation logic, thus a multi-stage topology is not preferred in this case. A single-stage topology is chosen.

The NRZ (None-return-zero) pulse is chosen because of the less sensitivity to clock jitter and higher SNDR. To avoid the inter-symbol interference problem, the modulator has been designed as a fully differential system.

4.2 Loop Filter Architecture

After selecting the oversampling ratio (OSR), quantizer number of bits (N) and loop order (L), the second step is to design the noise transfer function together with the modulator architecture.

The noise transfer function (NTF) is designed directly in continuous time domain using filter design tools. The choice considers not only the optimization of zeros and poles, but also the effects of non-idealities, as discussed in Chapter 3. For example, although a NTF can be chosen with the best optimized zeros and poles to achieve the most aggressive in-band suppression and the highest SNDR, the modulator with this NTF can be more sensitive to clock jitter. That means even though the quantization noise is suppose to be suppressed with the designed NTF, jitter-induced noise can be dominate in this wideband continuous-time modulator.

To take the jitter-induced noise into consideration during the selection of NTF, the RMS value of real clock jitter is investigated first in the current technology. Many modulators use advanced clock generators based on LC voltage-controlled oscillators (VCOs), and a signal-dependent clock based on a current switch driven by a pre-charged RC latch. The clock jitter of 2-5ps is common in the current technology [29-33]. In [31], the modulator is designed to be tolerant for 30ps clock jitter for 300MHz clock frequency. Based on the analysis in Section 3.4, we can choose a NTF, keeping a stable modulator and meeting the specifications when the clock jitter is in range of 0-40ps.

The next step is to determine the loop filter architecture. Considering the advantages of both the feedforward and feedback structures discussed in Section 2.3.4, a combination of these two topologies is a good choice for the continuous-time sigma-delta modulator design. The local feedback paths add zeros to introduce notched in band, so that a Chebyshev NTF is realized.

To implement the NTF in Equation 3.4.3, one pair of zeros is separate from dc. This pair of zeros is used to suppress the in-band noise, while the other pair is kept at dc. Compared with the traditional architecture shown in Section 2.3.4, one local feedback is omitted, as shown in Figure 4.1.
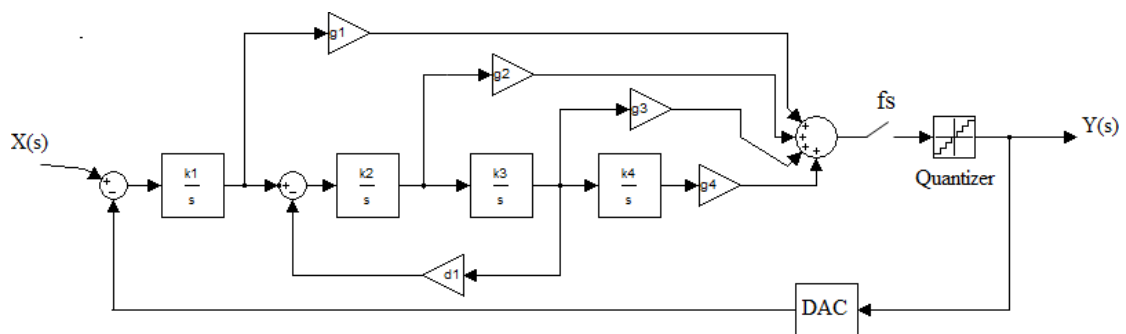
FIGURE 4.1 FOURTH-ORDER THREE-BIT CONTINUOUS-TIME SIGMA-DELTA MODULATOR

4.3 Architecture Optimization

After designing the basic architecture, it can be optimized further to have better performance and reduce the effect of non-idealities. Several optimization techniques are analysed.

Firstly, the excess loop delay is examined through system level simulations to see how much delay the modulator can actually tolerate. As described in Section 3.3.2, the excess loop delay issue can be easily solved by adding a second feedback path to the input of the quantizer, as shown in Figure 4.2. One extra DAC is used an its coefficient is chosen using the approach described in Section 3.3.2 to compensate the corresponding delay. In implementation, the coefficient is usually made programmable to compensate a variable delay.
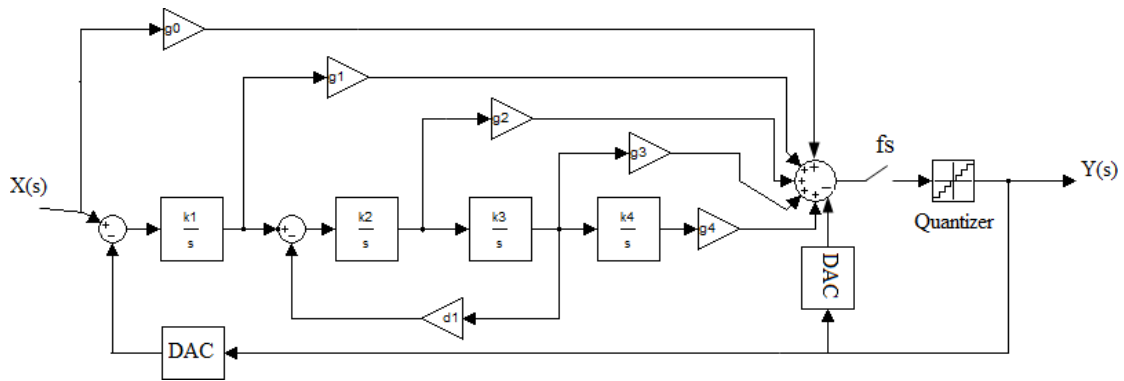
FIGURE 4.2 FOURTH-ORDER THREE-BIT CONTINUOUS-TIME SIGMA-DELTA MODULATOR

WITH EXCESS LOOP COMPENSTATION AND FEEDFORWARD G0

The second improvement seen in Figure 4.2 is the signal feedforward path directly from the morulator's input to the quantizer's input. With this feedforward path added, the signal swings at the output of the first integrator are reduced. The reason is as follows. As the input signal is added directly to the quantizer's input, the quantizer's input amplitude is increased. However, the high loop gain of the modulator at low frequencies tries to keep the quantizer's input signal level relatively constant by reducing signal swings at the integrator outputs.

The direct feedforward path not only relaxes the output swing requirement of the operational opamp, but also allows high integrator gains. The integrator gains k1 to k4 can be scaled up to suppress circuit noise. To guarantee stability of the modulator with a large input signal, the loop filter coefficients are scaled accordingly so that the three integrators have gradually increased signal levels from the first stage to the final stage.

Finally, the summation operation before the quantizer is moved forward to the input of the last integrator, as shown in the following figure. The last integrator performs the summation operation as well as the integration. This approach avoids the additional summing amplifier, which may introduce loop delay and increase power consumption.

In this approach, the order of every loop is increased by one and the first order loop is missing. One extra DAC feedback is added to realize the first order loop together with the last integrator.
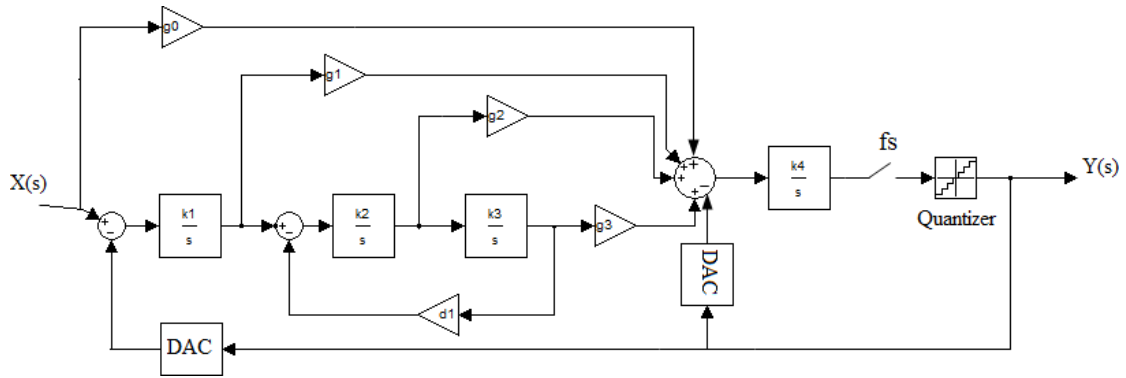
FIGURE 4.3 FOURTH-ORDER THREE-BIT CONTINUOUS-TIME SIGMA-DELTA MODULATOR
WITH THE SUMMATION OPERATION MOVED FORWARD

As known, the first integrator involved in the first order loop is the most critical block. Since any error introduced into it will appear at the modulator output without noise shaping, the first integrator must be the most accurate. The non-idealities, including the finite dc gain, unit gain bandwidth, limited swing, DAC feedback mismatch, must be examined carefully. By moving the summation operation forward in front of the last integrator, the first integrator is moved out of the first order loop. Then the requirements of the first integrator can be relaxed a lot.

Moreover, the feedforward paths require a multi-input adder to sum all the feedforward branches before the quantizer. The adder is usually implemented by a summing amplifier. The summing amplifier introduces additional loop delay, which becomes a speed bottleneck of the whole loop. Meanwhile, the power consumption is also increased. To avoid this, a differentiation operation can be introduced in the direct feedback path which allows the signal to be fed to the input of the last integrator.

In the view of circuit implementation, more feedforward branches give more pressure on the last integrator, so feedforward gain g0 is omitted. Though, the architecture realizes the same transfer function. The final architecture is shown in the Figure 4.4. The compensation technique of excess loop delay is also improved for this situation, using the principle analyzed in Section 3.3.2.
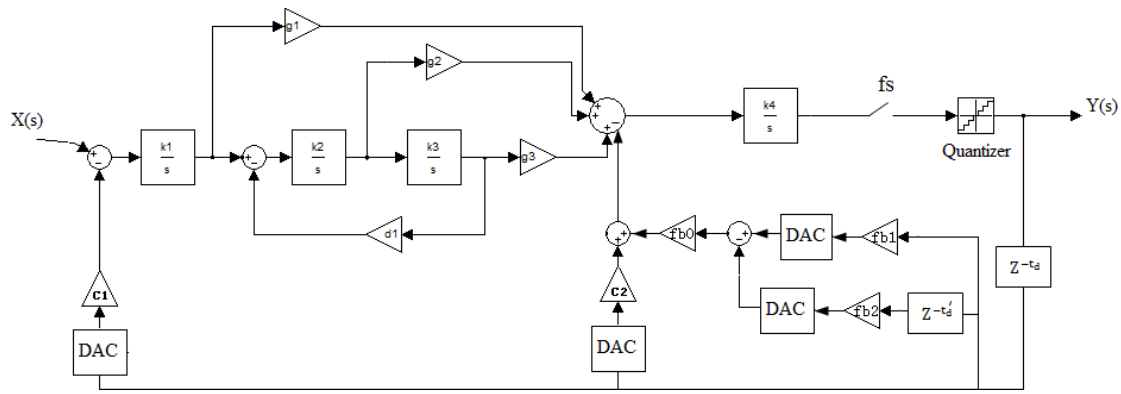
FIGURE 4.4 FOURTH-ORDER THREE-BIT CONTINUOUS-TIME SIGMA-DELTA MODULATOR

The noise transfer function and signal transfer function are shown in Equation 4.3.1 and Equation 4.3.2.

$$NTF = \frac{Y(s)}{E(s)} = \frac{s^4 + k_2 k_3 d_1 s^2}{s^4 + c_1 * [k_1 g_1 s^3 + (k_1 k_2 g_2 + k_2 k_3 d_1) s^2 + (k_1 k_2 k_3 g_3 + k_1 k_2 k_3 d_1 g_1) s + k_1 k_2 k_3 k_4 g_4]}$$

(4.3.1)

$$STF = \frac{Y(s)}{E(s)} = \frac{k_1 g_1 s^3 + (k_1 k_2 g_2 + k_2 k_3 d_1) s^2 + (k_1 k_2 k_3 g_3 + k_1 k_2 k_3 d_1 g_1) s + k_1 k_2 k_3 k_4 g_4}{s^4 + c_1 * [k_1 g_1 s^3 + (k_1 k_2 g_2 + k_2 k_3 d_1) s^2 + (k_1 k_2 k_3 g_3 + k_1 k_2 k_3 d_1 g_1) s + k_1 k_2 k_3 k_4 g_4]}$$

(4.3.2)

The resulted coefficients are presented in the following Table 4.2.

TABLE 4.2 COEFFICIENTS OF THE MODULATOR

k1	k2	k3	k4	g1	g2	g3	d1	c1	c2	fb	fb1	fb2
0.35	0.70	0.30	0.35	1.85	1.07	0.72	0.13	4	3.77	0.53	0.38	0.20

4.4 Loop Filter Design

The behavioral building blocks described by VerilogA language are used to build the whole modulator. The opamp of the integrator, quantizer and DACs are modeled in verilog A language. The integrating capacitors and resistors are implemented with analog components. Figure 4.5 shows the top level circuit diagram of the continuous-time sigma-delta modulator. The fourth-order loop filter of this design is implemented with active RC operational amplifiers and one resonator. The RC integrators have better linearity and larger signal swing than the GmC counterparts. Moreover, several feedforward branches in this design can be simply implemented using resistors. The resonator realizes two integrators and the local feedback. The role of the resonator is to shift the poles of the loop filter, hence shift the zeros of noise transfer function from dc in order to reduce the in-band quantization noise.

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As in the architecture the summation operation is moved forward to the input of the last integrator, the last integrator works not only for integration, but also as summation operation.
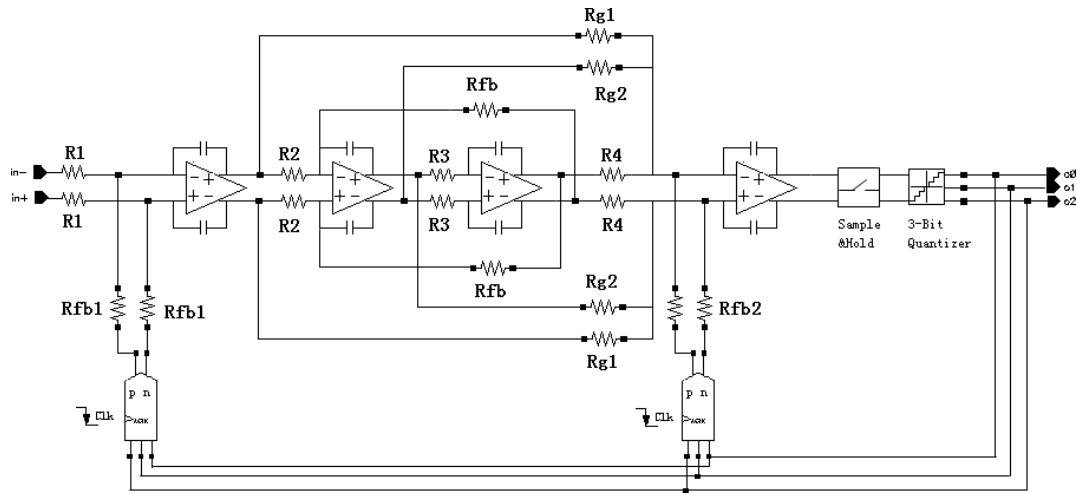
FIGURE 4.6 TOP LEVEL CIRCUIT DIAGRAM OF THE CONTINUOUS-TIME SIGMA-DELTA MODULATOR

The coefficients in system level design are translated to the values of resistors and capacitors using

$$R \times C = \frac{1}{K \times F_s} \quad (4.4.1)$$

For a high speed A/D modulator, the sampling frequency is high, up to hundreds MHz, which leads to small resistors and capacitors. The small resistors and capacitors make the closed-loop gain bandwidth large; therefore give a heavy pressure on the open-loop unit gain bandwidth. Seen from Equation (4.4.1), the other way is to scale down coefficient K so that the requirement of the Opamp unit gain bandwidth can be relaxed. However, the reduced unit gain bandwidth caused by the small coefficient K makes it difficult to cover the wide signal bandwidth. Moreover, the small resistors also become the loads for the previous integrator, which makes it a challenge to achieve the high DC gain.

The values of resistors used in the design are listed in Table 4.3. The capacitors are set to 0.5pF.

TABLE 4.3 RESISTOR VALUES

	R1	R2	R3	R4	Rg1	Rg2	Rfb	Rfb1	Rfb2
Resistor(Ω)	14.29k	7.14k	16.67k	21.76k	7.73k	13.4k	57.64k	14.29k	21.76k

4.5 Simulation Results

The simulation results are shown in this section. Finally, the circuit specifications will be determined. Figure 4.6 shows the output power spectrum in the ideal case. The spectrum is normalized to the maximum signal power. The SNDR reaches 82.37 dB.
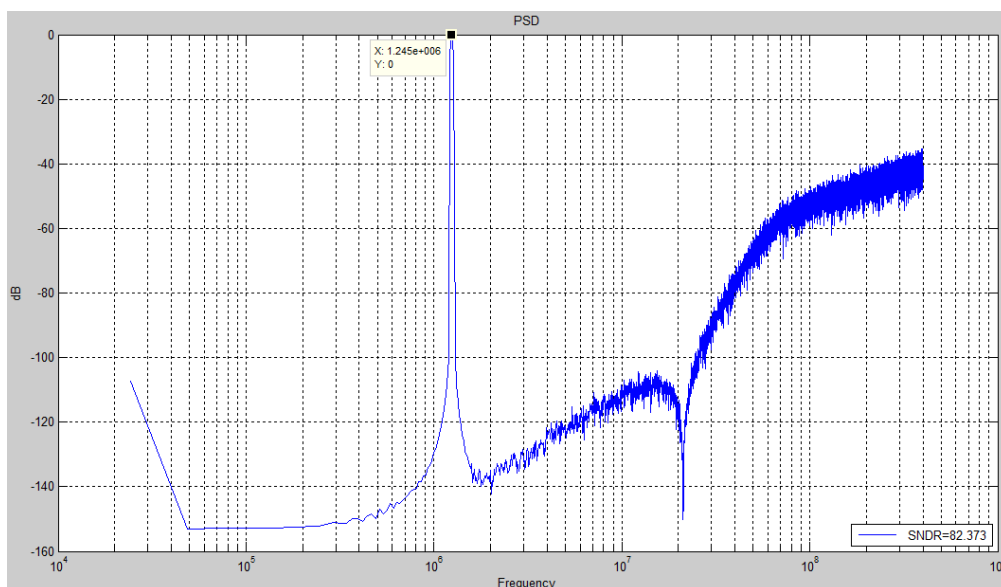
FIGURE 4.6 OUTPUT POWER SPECTRUM DENSITY IN IDEAL CASE,

NORMALIZED TO THE MAXIMUM POWER

Then various non-idealities are added to the modulator. Based on the analysis in Chapter 3, a conclusion is given here. By choosing a noise transfer function with intermediate aggressiveness, the clock jitter, 5% of sampling period can be tolerant. The stability of the modulator can be guaranteed, when the excess loop delay is less than 50% of sampling period. The finite opamp dc gain is set as 40dB, when the unit gain bandwidth is half of the sampling frequency, 400MHz. The loop gain of the first integrator is tuned to achieve symmetric range of time constant variance tolerance. After tuning, the first integrator can tolerate -20%~20% time constant deviation with ±0.8V output swing. The modulator can sustain 0.03% INL, which equals to 0.002 LSB with DEM DAC.

Figure 4.7 shows the output power spectrum for the modulator with all the non-idealities and the compensation techniques added. The modulator achieves SNDR 75.02 dB and SFDR 97.37 dB finally. The spur in the figure is at the frequency of 3nd harmonics. Figure 4.8 shows SNDR VS input amplitude and the dynamic range can be seen that is 77.58 dB.
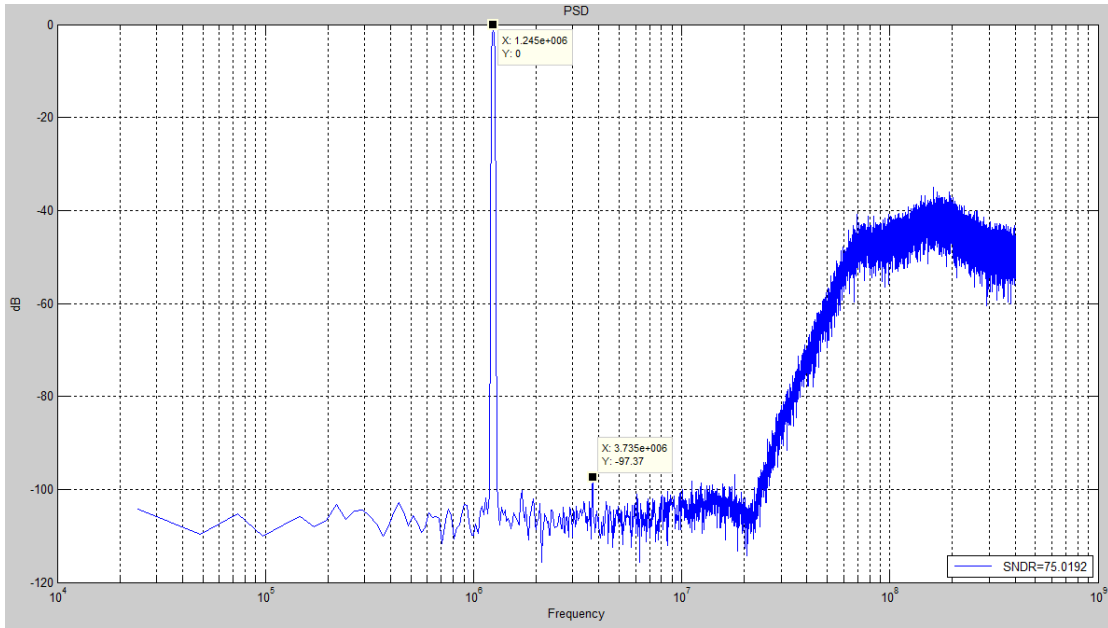
FIGURE 4.7 OUTPUT POWDER SPECTRUM DENSITY WITH ALL NON-IDEALITIES ADDED,
NORMALIZED TO THE MAXIMUM POWER
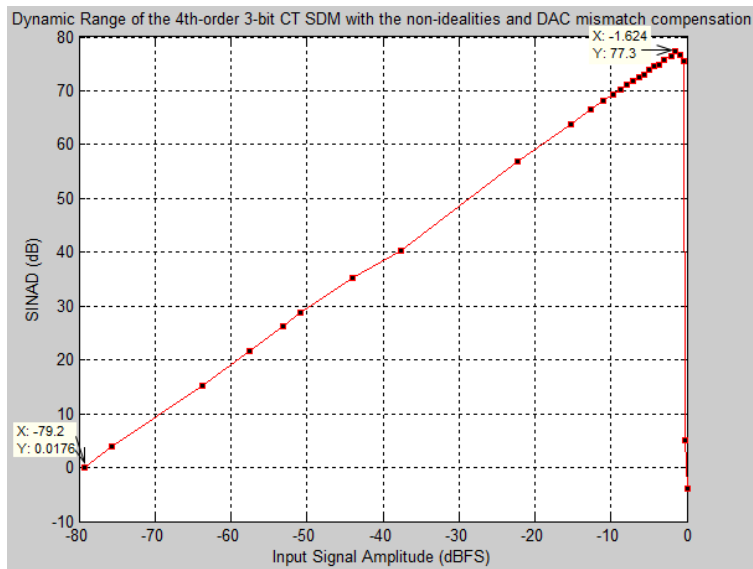
FIGURE 4.8 DYNAMIC RANGE OF THE MODULATOR WITH ALL NON-IDEALITIES ADDED

Table 4.4 summaries all the non-idealities values used in the final simulation.

TABLE 4.4 NONIDEALITIES SUMMARY

Finite Opamp Gain (1st Integrator)	40dB
Time Constant Variance	20% RC
Finite Amplifier Gain-Bandwidth	Half of Sample Frequency, 400MHz

Output Swing	-0.8~0.8
Clock Jitter	5% Ts
Excess Loop Delay	50% Ts
DAC Mismatch	≤0.03% INL, 0.002 LSB
Thermal Noise	0.2u

For detecting and evaluating the 3rd order inter-modulation (IM3) of in-band led by intermodulation which affects the original input signal largely, two-tone test based on two input signals which are 1.25MHz and 1.78MHz with 530kHz interval used in the test. The test result is shown in Figure 4.9.
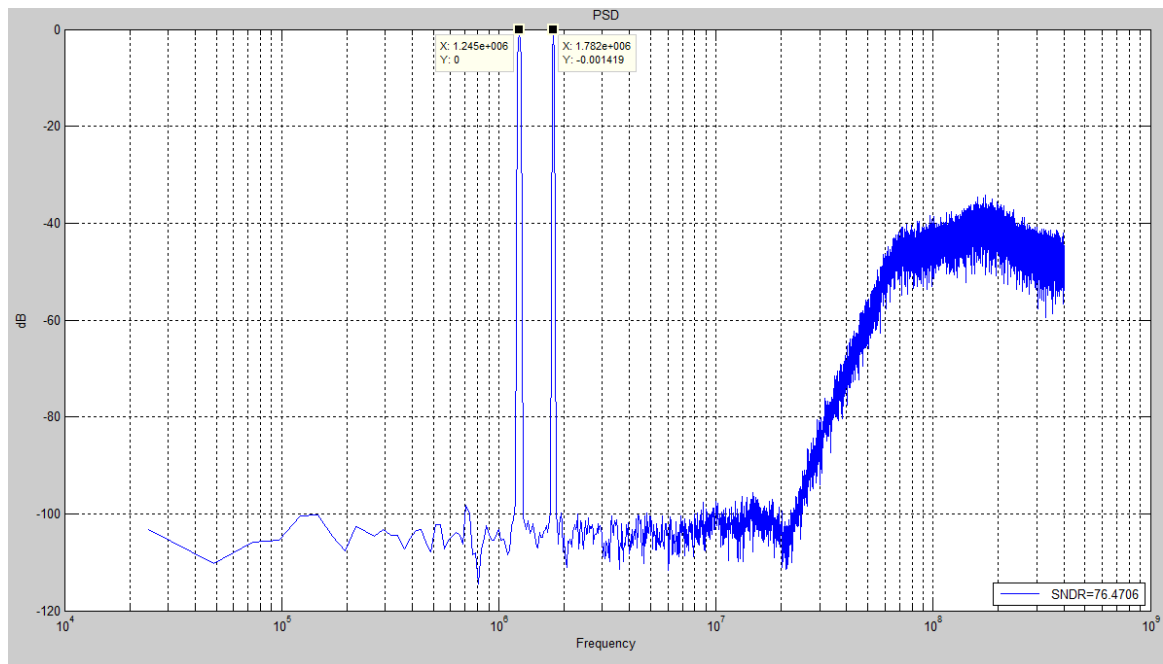
FIGURE 4.9 TWO TONE TEST OF THE MODULATOR

The modulator is then simulated using verilog A blocks. Figure 4.10 shows the power spectrum density. The models using verilog A do not include all the non-idealities that have been included in the Matlab model. To compare the result with the models in Matlab, Figure 4.10 also plots the power spectrum density of the Matlab models having the same non-idealities and the same simulation conditions. The DC gain, limited united gain bandwidth and output swing are included.
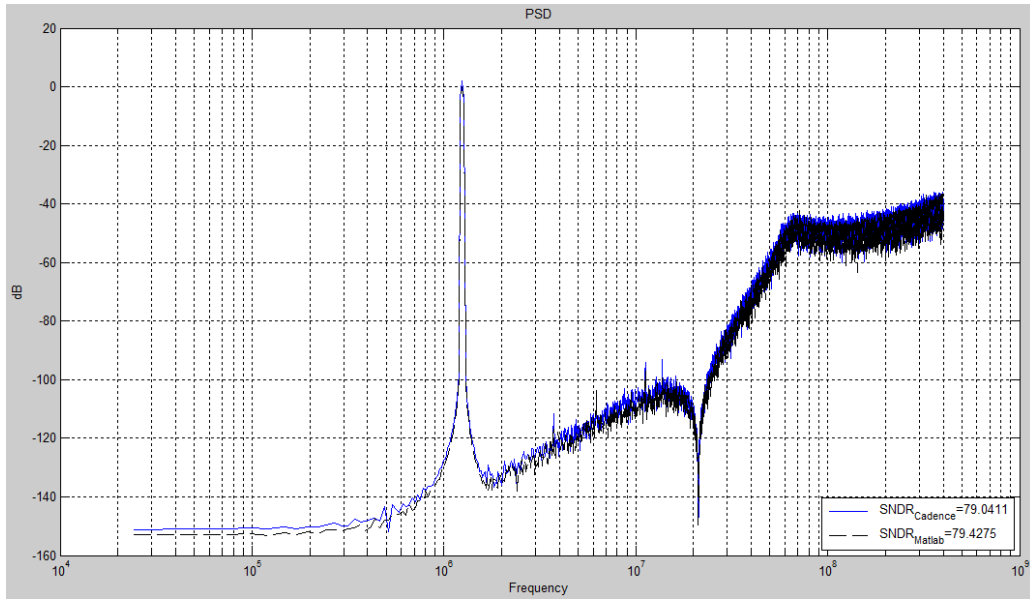
FIGURE 4.10 OUTPUT POWER SPECTRUM OF THE MODULATOR USING VERILOGA BLOCKS

It can be seem from the figure that the behavioral level modeling in Cadence matches with the system level modeling in Matlab. The SNDR and noise shaping are similar. The SNDR reaches 79.04 dB, which leaves some margin for other non-idealities.

5 Circuit Level Design

In this chapter, the circuit level design of the continuous-time sigma-delta modulator will be described. The circuit design challenges of wideband high dynamic range A/D modulator will be discussed. The circuit of the first integrator is designed on transistor level using 90nm CMOS technology.

In fact, the design of the modulator is an iterative process between the system level and the circuit level. When moving from the system level to circuit level, the circuit should be realizable to implement the mathematical coefficients in system level design. The voltage levels should be corresponding to the values on the system level.

5.1 Transistor level of the OpAmp in the First Integrator

The first integrator is implemented by a fully differential two-stage amplifier. As in this modulator active RC integrators are chosen to realize the loop filters, the resistive load makes one-stage opamp less efficient in terms of DC gain than the two-stage opamp. So in this design, all stages employ two-stage amplifiers.

The fully differential two-stage amplifier composes of a folded cascode opamp as the first stage and a unity-gain source follower as the second stage. The circuit schematic of the opamp is shown Figure 5.1. The biasing circuits are modeled by ideal voltage source in the simulation.

The folded-cascode opamp provides a good gain-signal swing tradeoff over the telescopic topology, especially under the 1.2V voltage condition. PMOS Transistors PM1-PM2 form the differential input pair. NMOS transistors NM3-NM4 are the folded-cascode transistors.

The output stage uses the common-drain structure, realized by the transistors M12-M13 and M14-M15. The output pole introduced by this stage is given by the approximation of

$$\omega_{out} \approx - \frac{1}{\frac{1}{g_{m,NM7}} \times C_L}$$, where the C_L is the equivalent load capacitance. To avoid the influence of the output pole, the compensation capacitor is added to split two poles. The transistors NM13-NM14 are added to approximately cancel the introduced zero.

FIGURE 5.1 THE SCHEMATIC OF FULLY DIFFERENTIAL OPAMP

Figure 5.2 shows the continuous-time common-mode feedback circuit (CMFB) used in this design. The CMFB circuit is designed to set the output common mode voltage as expected, which is normally half of the supply voltage. It senses the positive and negative signals, compares the average value of their common mode level with a certain reference voltage, and finally provides the feedback bias "CMFB" to the current source in the main circuit.

The circuit composes resistive divider and a source-coupled differential pair. The gate of PM11 is connected to the desired output voltage, Vcntrl. The resistors R0 and R1 sense and average the output voltages of the differential folded cascoded opamp. Transistor PM9 is the tail-current source and NM17, NM18 are the diode-connected loads. The gate of NM18 is connected to the current source of the opamp and completes the feedback loop.

FIGURE 5.2 THE SCHEMATIC OF CMFB CIRCUIT

5.2 Design Analysis and Equations

The opamp design starts with the DC gain, which is given by

$$|A0| = g_{m,PM1} *R_{out} \qquad (5.2.1)$$

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where $g_{m,PM1}$ is the transconductance of the differential input pair, and R_{out} is the output resistance of the first stage. They are given by the following equations respectively.

$$g_{m,PM1} = \sqrt{2u_p C_{ox}(\frac{W_{PM1}}{L_{PM1}})I_{ss}} \qquad (5.2.2)$$

$$R_{out} = [g_{m,NM3} *r_{o,NM3} * (r_{o,PM1} // r_{o,NM1})] // (g_{m,PM4} *r_{o,PM4} *r_{o,PM6}) \qquad (5.2.3)$$

For the nano-meter technology, the power consumption is significantly reduced. Although the power consumption is not a concern in this design, approximately 100uA current is assigned to the input pairs and the two cascode branches as the initial guess according to the power consumption. Combining the above equations, the dimensions of the input PMOS transistors are set.

The 3-dB frequency is determined by the dominant pole generated by the first stage. It can be expressed as

$$\omega_{-3dB} \approx -\frac{1}{R_{out}A_{out}C_{comp}} \qquad (5.2.4)$$

where C_{comp} is the compensation capacitor and A_{out} is the small signal gain of the output stage which should be approximately 1 and makes no influence on ω_{-3dB}. In order to guarantee the stability, usually the degree phase margin should reach at least 60 degree. To achieve enough phase margin, the value of C_{comp} must be large enough so that the output pole ω_{out} should fulfill the relation $\omega_{out} \geq 2\omega_u$, which indicates that

$$\frac{g_{m,NM7}}{C_L} \geq \frac{2g_{m,PM1}}{C_{comp}} \qquad (5.2.5)$$

However, a zero is introduced in the right half of the s-plane, which degrades the amplifier's phase margin. The zero gives one more limitation on the unit gain bandwidth to ensure the stability, $\omega_u << |z|$. Transistor NM13-NM14 work as nulling resistors, which approximately cancel the zero. The dimensions of NM13-NM14 are set as the same as those of NM5-NM6. The resistance that cancels the zero is given by these two transistors in triode region and is equal to $1/g_{m,NM5}$.

The output swing affects the linearity of the filter, which is a stringent requirement with a supply voltage only 1.2V. With the swing requirement ±0.8V, the total voltage available for each cascode branch is only 0.4V. The overdrive voltages for the other transistors are allocated according to the output swing. Considering the fact that NM1-NM2 bears the largest current and PMOS transistors M14-M17 suffer from low mobility, more overdrive voltage should be allocated to those transistors than others. With the bias current and

overdrive voltage of each transistor known, the dimensions of the cascode devices are set using the following equation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{od}^2$$ (5.2.6)

The bias voltages are assigned to allow the maximum output swing using the following equations

$$V_{CMFB} = V_{GS,NM1} = V_{TH,NM1} + V_{OD,NM1}$$ (5.2.7)

$$V_{bias1} = V_{DD} - /V_{GS,PM6}/ = V_{DD} - (/V_{TH,PM6}/ + /V_{OD,PM6}/)$$ (5.2.8)

$$V_{bias2} \leq V_{DD} - (/V_{GS,PM4}/ + /V_{OD,PM6}/)$$ (5.2.9)

$$V_{bias3} \geq V_{GS,NM1} = V_{TH,NM1} + V_{OD,NM1}$$ (5.2.10)

In the CMFB circuit, $V_{CMFB} = V_{GS,NM17}$, when $V_{cntrl} = (V_{out1} + V_{out2})/2$ and $I_{D,PM10} = I_{D,PM11} = I_{D,PM9}/2$. The small signal gain of this CMFB circuit is given by $\alpha_{CMFB} = -\frac{V_{CMFB}}{V_{cntrl}} = \frac{1}{2}\frac{g_{m,PM10}}{g_{m,NM7}}$. The loop gain of the CMFB circuit should be comparable with the one of the main circuit to avoid limiting the gain and swing.

5.3 Circuit Design Challenges and Specifications of the Opamp

The modulator with both wide band and high dynamic range leads to great challenges in the design of opamp. Firstly, as the coefficients from system level are mapped to resistors and capacitors values using RC=1/kFs, high sampling frequency Fs (up to hundreds MHz) leads to small integration resistors and capacitors. Then the closed-loop gain bandwidth becomes large, which gives a heavy pressure on the open-loop unit gain bandwidth. So the closed-loop gain k must be scaled down. However, to keep the noise shaping for the whole wide signal band, the closed-loop gain must be large enough. There is a trade-off between the wide signal band and the unit gain bandwidth. Finally, the small resistor also becomes the load for the previous integrator, which makes it difficult for the previous integrator to achieve high gain and wide band.

Table 5.1 lists the specifications for the Opamp realized in this design. The resistor load is set by the value of the second integrator's resistor.

TABLE 5.1 SPECIFICATIONS FOR THE OPAMP

Unit Gain Bandwidth	200MHz

DC Gain	40dB
Output Swing	-0.8V~0.8V
Resistor Load	7.143 kΩ

5.4 Circuitry Parameters and Simulation Results

Table 5.2 gives a summary of the circuitry parameters of two-stage fully differential amplifier and CMFB amplifier.

TABLE 5.2 CIRCUITRY PARAMETERS OF TWO-STAGE FULLY DIFFERENTIAL AMPLIFIER

Component	Type	Length(nm)	Width(μm)
1st Stage Amplifier			
PM1	P_12_ll	180	60
PM2	P_12_ll	180	60
PM3	P_12_ll	360	240
PM4	P_12_ll	90	20
PM5	P_12_ll	90	20
PM6	P_12_ll	90	20
PM7	P_12_ll	90	20
NM1	N_12_ll	360	24
NM2	N_12_ll	360	24
NM3	N_12_ll	360	24
NM4	N_12_ll	360	24
2nd Stage Buffer & Compensation			
Ccomp	1.5p F		
NM13	N_12_ll	360	96
NM14	N_12_ll	360	96
NM5	N_12_ll	360	96
NM6	N_12_ll	360	96
NM7	N_12_ll	90	36
NM8	N_12_ll	90	36

TABLE 5.3 CIRCUITRY PARAMETERS OF CMFB AMPLIFIER

Component	Type	Length(nm)	Width(μm)

NM17	N_12_ll	90	24
NM18	N_12_ll	90	24
PM9	P_12_ll	180	72
PM10	P_12_ll	180	72
PM11	P_12_ll	180	72
R0=R1	1M Ohms		

Figure 5.3 shows the open-loop frequency response of the amplifier. The DC gain is 41.3 dB and the unit gain bandwidth is 200.39 MHz.
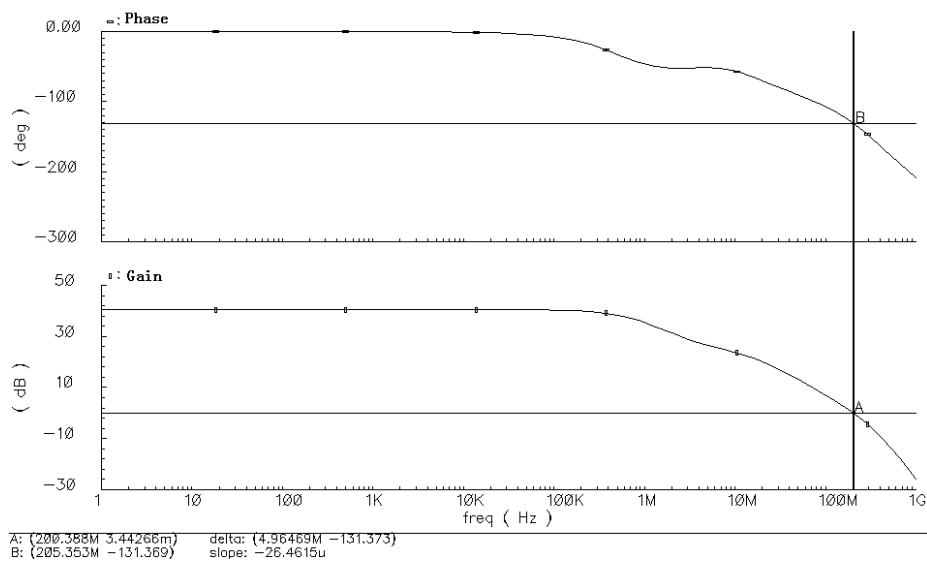
FIGURE 5.3 OPEN-LOOP FREQUENCY RESPONSE OF THE AMPLIFIER

Figure 5.4 shows the input and output signals in time domain. The input signal goes through the four integrators and finally is converted to the output signal with eight levels.
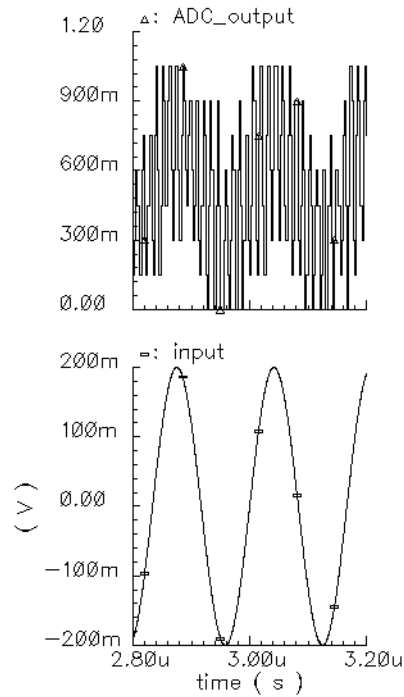
(a)   ADC Input and Output in Time Domain
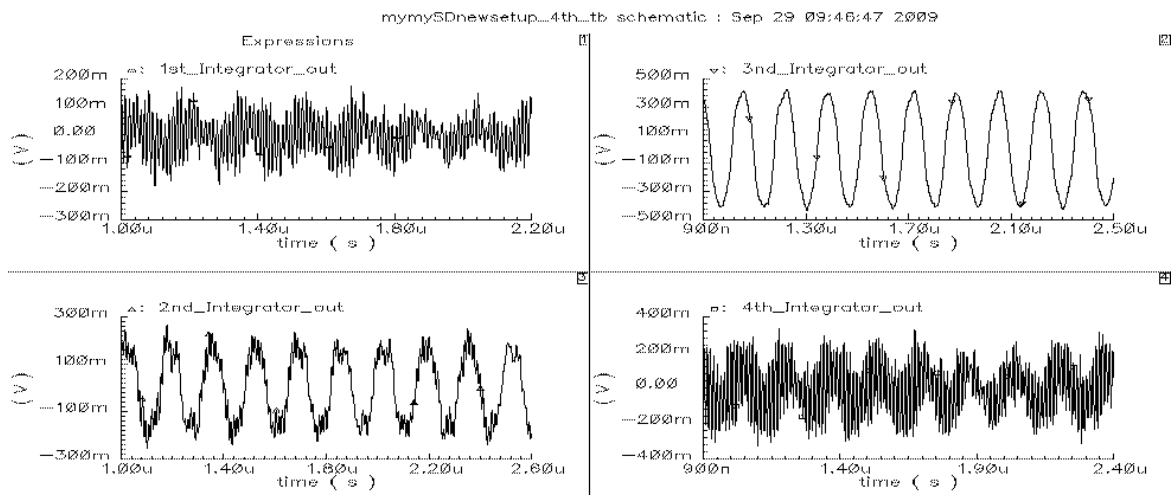
(b) Outputs of Integrators in Time Domain

FIGURE 5.4 SIGNALS IN TIME DOMAIN

In conclusion, due to the requirements of the wideband continuous-time sigma-delta modulator, there are lots of spaces at circuit design to achieve wideband operational amplifier. This section gives an analysis and raises up the design challenges, which is useful for the future research.

6 Conclusion and Future Work

6.1 Conclusion

In this thesis work, a 4th-order 3bit continuous time sigma delta modulator for wireless application has been proposed. The system-level simulations show that the modulator can achieve a SNDR 75.02dB, dynamic range 77.58dB over a signal bandwidth 25MHz. The behavioral-level simulations using verilog A show that the modulator with only the finite DC gain, unit gain bandwidth and swing added can achieve 79.04dB. An Opamp has been designed to achieve 40dB DC gain and 200MHz unit gain bandwidth.

The following techniques have been utilized to achieve the above performance:

1. A simulation-based design methodology has been used to synthesize a continuous-time sigma delta modulator by designing loop filter directly in continuous time domain.

2. A high-order loop filter and a multi-bit quantizer were employed to provide sufficient noise shaping.

3. A thorough study has been made to choose the noise transfer function and determine the system-level coefficients, based on the considerations of the dynamic range requirement, stability and clock jitter sensitivity.

4. The effect of clock jitter in continuous-time sigma-delta modulator has been analyzed. The jitter issue is considered when the transfer function is selected. The clock jitter sensitivity is reduced at a cost of the relatively weaker in-band noise suppression. Moreover, NRZ (Non-return-to-zero) feedback DAC pulse was adopted to reduce the jitter sensitivity.

5. A more predictable measurement is defined to get control of the whole system's stability. As an important factor of stability, the effect of the excess loop delay is examined using this approach. The compensation technique using one extra DAC feedback is implemented to suppress the effect.

6. A thermometer-code current steering DAC and its mismatches are modeled in the feedback path. Data-weighted averaging (DWA) technique is selected to compensate DAC mismatch.

7. Time constant variance, one of the important issues is examined and its effect is compensated based on the trade-off excess loop delay.

8. The modulator architecture is a combination of feedforward and feedback. Moreover, compared with a traditional topology, the summing amplifier and the last integrator are combined into one. The architecture is simplified and the power has more chance to be saved.

9. The circuit design challenges and bottleneck of the wideband high dynamic range modulator are explored, which are useful experiences for the future research. An opamp has been designed.

6.2 Future Work

To design continuous-time sigma-delta A/D modulators for such a wide bandwidths with high resolution, several design issues can be further explored in the future.

1. Besides building a system which is less sensitive to clock jitter itself, some techniques could be used to reduce the jitter sensitivity further. One possible way is to use non-rectangular, e.g., exponential decaying feedback DAC waveforms, and switched capacitor controlled current mode feedback.

2. At the transistor-level design, the wideband operational amplifier can be applied to the high speed systems instead. The rapid development of wireless application raises the need of the wideband operational amplifier.

3. Although the optimization technique, moving the summation forwards to the last integrator's input is used for reducing the power consumption, the design does not put efforts on the power issues. However, as the power efficient system is one of the trends, it would be meaningful to do a research on the power consumption. Various design strategies can be adopted in the future to lower the power consumption.

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