AN ABSTRACT OF THE DISSERTATION OF

Xuefeng Chen for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on March 15, 2007.

Title: A Wideband Low-Power Continuous-Time Delta-Sigma Modulator for Next Generation Wireless Applications.

Abstract approved:

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Gábor C. Temes

Delta-Sigma ($\Delta\Sigma$) analog-to-digital converters (ADCs) are widely used in wireless transceivers. Recently, continuous-time (CT) $\Delta\Sigma$ ADCs gain growing interest in wireless applications for their lower power consumption and wider input bandwidth as compared with the discrete-time (DT) counterparts.

In this thesis, a wideband low-power CT $\Delta\Sigma$ modulator for next generation wireless applications is proposed to achieve 10-bit dynamic range within a 25 MHz signal bandwidth. On the system level, a low-power, mainly feed-forward architecture is used to realize the loop filter. Feed-in branches are added and optimized to eliminate the out-of-band peaking in the signal transfer function. On the circuit level, two-stage operational amplifiers with class-AB output stages are used to implement low-power active RC integrators. Capacitor tuning is used to compensate the variation of RC time constants. In addition, a fast current adder, an 11-level internal flash ADC and three current feedback DACs are also integrated on the chip which was manufactured in TSMC 0.18 $\mu$m CMOS technology. The test results show that the modulator draws less than 10 mA from the 1.8 V supply voltage.

# A Wideband Low-Power Continuous-Time Delta-Sigma Modulator for Next Generation Wireless Applications

by
Xuefeng Chen

A DISSERTATION

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APPROVED:

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Director of the School of Electrical Engineering and Computer Science

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Xuefeng Chen, Author

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To my beloved parents and family

# A Wideband Low-Power Continuous-Time Delta-Sigma Modulator for Next Generation Wireless Applications

# CHAPTER 1. INTRODUCTION

Delta-Sigma (ΔΣ) analog-to-digital converters (ADCs) are widely used in wireless applications due to their oversampling, high dynamic range, and low power consumption characteristics. Compared with the traditional discrete-time (DT) counterparts, the ΔΣ ADCs that employ continuous-time (CT) technique behave even better in terms of power consumption and allowable input bandwidth. This thesis describes a new synthesis method of the CT loop filter from a DT target and discusses several design challenges of the CT ΔΣ modulators as well as the solutions. After that, the detailed design of a wideband (25 MHz) CT ΔΣ modulator which utilizes several low-power techniques at both the system level and circuit level is described.

## 1.1. Motivation

ΔΣ ADCs are very popular in wireless applications [1, 2, 3, 4] due to the following three reasons. First, thanks to the advance of both the semiconductor technology and the design techniques, the input signal bandwidth which the ΔΣ ADCs can handle is extended to the MHz range. Second, ΔΣ ADCs are more suitable for low-power design which is one of the most important concerns in the battery-powered wireless equipments (e.g., mobile phones) because the over-sampling characteristics of the ΔΣ ADCs greatly reduce the performance requirement of the anti-aliasing filters which are power hungry blocks in the wireless transceiver. Last but not least, ΔΣ ADCs spectrally shape most of the analog circuit error away

from the band of interest to achieve high accuracy only in a narrow band, which matches the usual case that the bandwidth of an analog signal of interest in a wireless transceiver is much narrower compared with practical data-converter sample-rates and digital filter clock rates.

Fig. 1.1 shows the basic diagram of a popular direct conversion wireless receiver which employs a ΔΣ ADC. Fig. 1.2 describes the relationship between the bandwidth (BW) and the dynamic range (DR) of the ΔΣ ADCs used in several most popular wireless applications. From this plot, we can see that both the 2nd-generation (e.g., GSM, GPRS and EDGE) and the 3rd-generation (e.g., WCDMA, CDMA2000 and TD-SCDMA) cellular systems widely used ΔΣ ADCs in their receivers of the mobile phones. In addition, the ΔΣ ADCs are also suitable for wireless connection (e.g., Bluetooth) and wireless internet access (e.g., WLAN) applications.

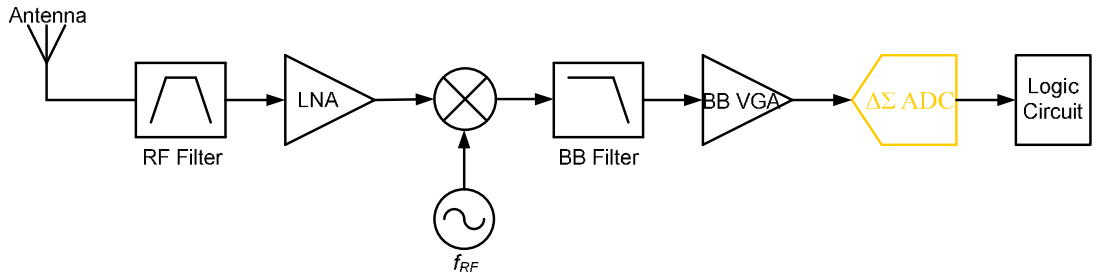



Figure 1.1: Basic diagram of a direct conversion wireless receiver

While most of current commercial ΔΣ ADCs for wireless applications were implemented by using switched-capacitor techniques [1, 2] which are also known as discrete-time (DT) ΔΣ ADCs mainly due to mature design methodologies and robustness, more and more continuous-time (CT) ΔΣ ADCs were reported [3~11] and showed impressive performance. Compared with DT counterparts, the CT ΔΣ ADCs have two main advantages. First, the inherent anti-aliasing characteristics of the CT ΔΣ ADCs reduce the performance requirement of the anti-aliasing filter further and hence reduce the power consumption of the

transceiver. Second, the bandwidth requirement of the operational amplifiers (opamps) in CT ΔΣ ADCs is much lower than that of the opamps in DT ones for a given sampling-rate, so the CT ΔΣ ADCs are more suitable for wideband applications.

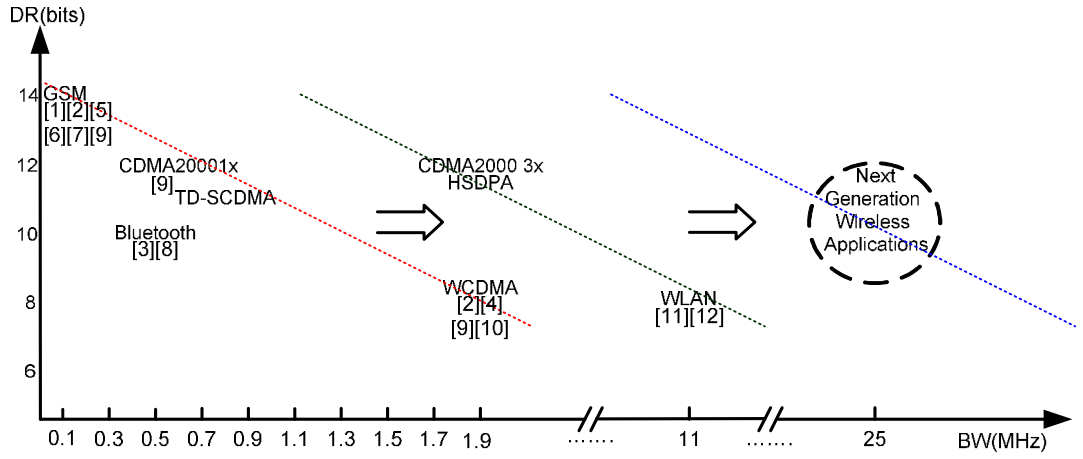



Figure 1.2: Performance of ΔΣ ADCs in some wireless applications

It is reasonable to believe that the signal bandwidth of the next generation wireless applications (e.g., the 4$^{th}$-generation cellular system) will be much higher (e.g., 10x) than for the current one. Assuming that other specifications of the receiver are similar to those of the 3$^{rd}$-generation cellular system [13], the dynamic range requirement of the ΔΣ ADCs will be around 60 dB. So, CT ΔΣ ADCs are more suitable than DT ones for next generation wireless applications.

The target of this research is to design a low-pass real CT ΔΣ modulator with the widest bandwidth to date (25 MHz) to achieve 60 dB dynamic range by consuming very low power (less than 20 mW). This CT ΔΣ modulator will be a very good candidate for the next generation wireless applications.

## 1.2. Thesis Organization

This thesis covers theoretical analysis of the CT ΔΣ modulator and a novel synthesis method of the CT loop filter from its DT target. After describing the design issues of the CT ΔΣ modulator as well as the solutions, the detailed design procedure of the prototype modulator as well as the chip evaluation work are presented. The thesis is organized as following:

Chapter 2 provides some basic background knowledge about ΔΣ ADCs to help understand the rest of the thesis.

Chapter 3 describes the equivalence between the DT and CT loop filters in terms of impulse-invariant transformation (IIT) and proposes a novel synthesis method of the CT loop filter from its DT target based on simulation.

Chapter 4 covers some main design issues of the CT ΔΣ modulators, which include excess loop delay, clock jitter, and RC time constant variation, as well as the solutions to those issues.

Chapter 5 proposes a system level design procedure which combines many aspects of the design considerations of the wideband low-power CT ΔΣ modulator.

Chapter 6 presents detailed circuit level and layout level design of this wideband modulator.

Chapter 7 covers the issues of high speed test board design as well as the chip evaluation work.

Chapter 8 concludes the thesis and discusses some future work.

# CHAPTER 2. OVERVIEW OF OVERSAMPLING ΔΣ ADC

This chapter provides some basic background knowledge about ΔΣ ADCs to help understand the rest of the thesis. The concepts of quantization, oversampling and noise-shaping are introduced and illustrated with examples. Two common architectures of the ΔΣ modulators, single-loop and multi-stage (cascaded, MASH), are compared.

## 2.1. Sampling and Quantization

In order to properly interface the real analog world which is composed of continuous-time and continuous-amplitude analog signals (e.g., voice, audio or video) with the digital signal processor which can only process discrete-time and discrete-amplitude signals, analog-to-digital conversion is required (see Fig. 2.1). The AAF block stands for the anti-aliasing filter which is used to limit the bandwidth of the input signal to half of the sampling rate (Nyquist theorem). Otherwise, the undesired higher frequency components will alias into the band of interest and interrupt the desired signal while sampling which changes the input signal from continuous form to discrete form in the time domain. The sampled signal should be "frozen" for a sufficient time to be determined and represented by one of some discrete levels, which is known as quantization. For this reason, the quantizer that carries out the quantization should be preceded by a sample-and-hold (S/H) or track-and-hold (T/H) block.

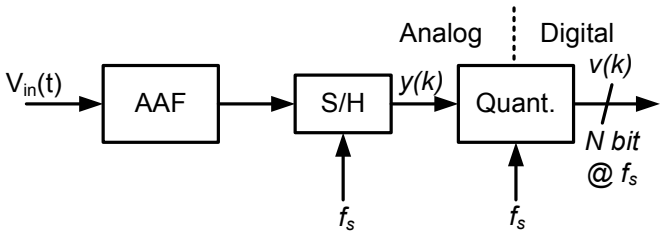
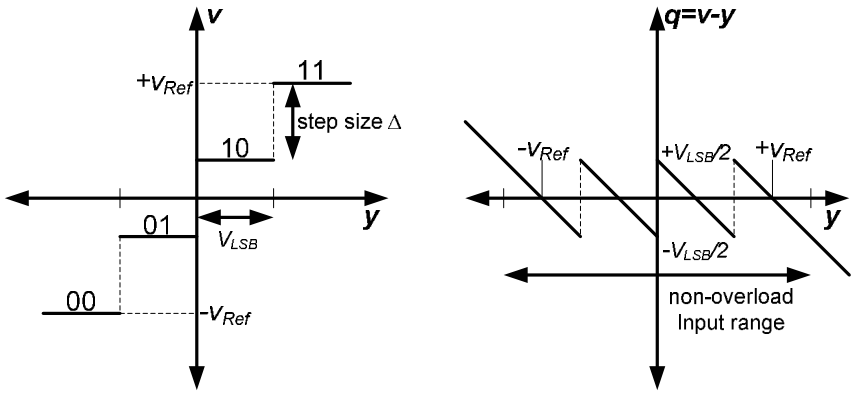



Figure 2.1: Analog-to-digital conversion

The quantizer is assumed to be a memoryless nonlinear device completely defined by its static input-output characteristics, i.e., by its *y*-*v* transfer curve. An example of such a curve is shown in Fig. 2.2a, where the number of quantization level is 4 which can be represented by a 2-digit binary code, and the difference of two adjacent quantized values, Δ, is the same as the difference between input thresholds, also known as least-significant bit size or LSB size, given by $V_{LSB}$. The difference between the lowest and highest levels is called the full-scale (FS) of the quantizer, given by $2V_{Ref}$. The deviation between the sampled input and the quantized output is called the quantization error, or the quantization noise. Fig. 2.2b shows the relationship between the quantization noise *q* and the input *y*. From this figure, it can be seen that as long as *y* is between $-(V_{Ref}+V_{LSB}/2)$ and $+(V_{Ref}+V_{LSB}/2)$, the error *q* is between $-V_{LSB}/2$ and $+V_{LSB}/2$. The range of *y* where this condition is satisfied is called the non-overload input range. For a *N* bit ADC, the quantization step as well as the LSB size is given by $\Delta = V_{LSB} = FS/(2^N-1)$, which is, in this case, $2V_{Ref}/3$.

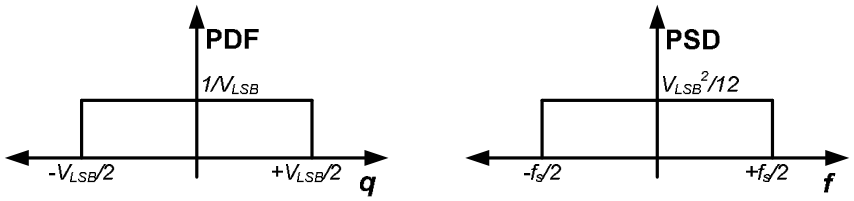



(a) (b)

Figure 2.2: (a) Transfer curve and (b) error function of a 4-level quantizer

The ideal quantizer is a deterministic device. The output *v* and hence the error *q* are fully determined by the input *y*. However, under certain circumstances, for example, if the

input $y$ stays within the non-overload input range of the quantizer, and changes by sufficiently large amounts from sample to sample so that its position within a quantization interval is essentially random, then it is permissible to assume that $q$ is a white noise process with samples uniformly distributed between $-V_{LSB}/2$ and $+V_{LSB}/2$. The probability density function (PDF) and power spectral density (PSD) of the quantization noise are shown in Fig. 2.3.




(a) (b)

Figure 2.3: Probability density function and power spectral density of quantization noise

The impact of the quantization noise on the ADC's performance can be found by calculating its maximum signal-to-quantization-noise ratio ($SQNR_{max}$). This parameter is obtained by dividing the power of a sinusoidal input signal by the power of the quantization noise. The power of a sinusoidal signal is given by $A_u^2/2$, where $A_u$ is the amplitude of the signal. The power of the quantization noise is given in Eq. 2.1.

$$\sigma_q^2 = \frac{1}{V_{LSB}} \int_{-V_{LSB}/2}^{V_{LSB}/2} q^2 dq = \frac{V_{LSB}^2}{12} \tag{2.1}$$

To get the $SQNR_{max}$, $A_u$ should be equal to half of the non-overload input range of the quantizer, which is $V_{Ref}+V_{LSB}/2$.

$$SQNR_{\max} = \frac{\left(V_{\mathrm{Re}f} + \frac{V_{LSB}}{2}\right)^2 \Big/ 2}{V_{LSB}^2 \Big/ 12} = \frac{\left(2^{N-1} V_{LSB}\right)^2 / 2}{V_{LSB}^2 \Big/ 12} = \frac{3}{2} 2^{2N} \tag{2.2}$$

Expressed in dB, this becomes Eq. 2.3, which is widely used to assess the performance of the data converter.

$$SQNR_{\max}[dB] = 10\log_{10}(SQNR_{\max}) = 6.02N + 1.76 \tag{2.3}$$

## 2.2. Oversampling

An alternative way to calculate the power of the quantization noise is to integrate its power spectral density over the full bandwidth of operation of the ADC:

$$\sigma_q^2 = \frac{1}{f_s}\int_{-f_s/2}^{f_s/2} \frac{V_{LSB}^2}{12} df = \frac{V_{LSB}^2}{12} \tag{2.4}$$

From above equation, it is obvious that if the bandwidth of interest is much lower than the bandwidth of operation, the resolution of the ADC can be improved by filtering the output to the desired bandwidth which reduces the total power of the quantization noise. This technique, illustrated in Fig. 2.4, is called oversampling.

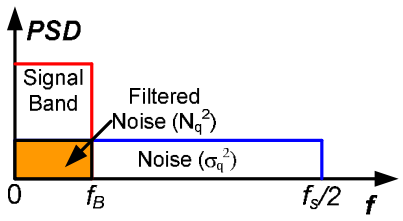



Figure 2.4: Oversampling

Now, the power of the in-band quantization noise is given in Eq. 2.5.

$$N_q^2 = \frac{1}{f_s}\int_{-f_B}^{f_B} \sigma_q^2 df = \sigma_q^2 \frac{2f_B}{f_s} = \frac{\sigma_q^2}{OSR} \tag{2.5}$$

where OSR, defined as $f_s/2f_B$, is called oversampling ratio which is one of the most important parameters used to characterize the oversampling data converters. The power of input signal is

not modified since it is assumed that it has no frequency content above $f_B$. Therefore, the maximum SQNR is given by:

$$SQNR_{\max}[dB] = 6.02N + 1.76 + 10\log_{10} OSR \tag{2.6}$$

It is obvious that if the sampling rate is equal to twice the Nyquist rate ($OSR$ = 2), the SQNR is improved by 3 dB. Eq. 2.6 shows that oversampling can improve the SQNR with the OSR at a rate of 3 dB/octave, or 0.5 bit/octave.

## 2.3. Noise Shaping

The previous section shows that oversamping can be used to trade speed for resolution of ADC. However, the rate of this trading is only 3 dB/octave with plain oversamping.

It is noticed that the quantization noise in previous section has a flat power spectral density over the full bandwidth ($-f_s/2 \sim f_s/2$). A more efficient way to use oversampling is to shape the spectral density such that most of the quantization noise power is outside the band of interest. ΔΣ or ΣΔ modulators can be used to do this noise shaping without affecting the desired signal band. Fig. 2.5 shows a ΔΣ modulator that can shape the quantization noise with a first-order high-pass transfer function.

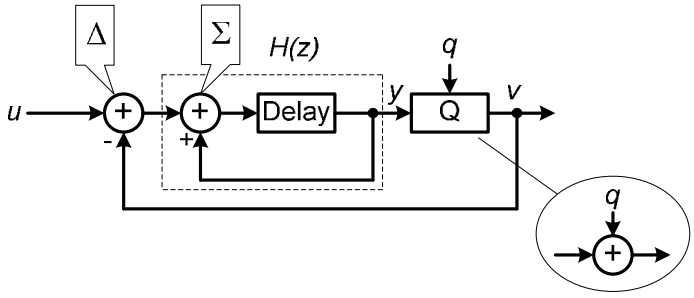



Figure 2.5: First-order ΔΣ modulator

Again, it is assumed that the quantization noise is uniformly distributed and not dependent on the input signal $u$. The modulator can be completely linearized by replacing the

quantizer with a summation block. This system has two inputs, $u$ and $q$, and one output, $v$. The transfer function from $u$ to $v$, which is called signal transfer function (STF), is given by:

$$STF(z) = \frac{V(z)}{U(z)} = \frac{H(z)}{1+H(z)} = z^{-1} \tag{2.7}$$

This means that the input signal $u$ is delayed and appears unaltered at the output $v$. As for the noise transfer function (NTF) which is defined as the transfer function from $q$ to $v$, it is given out by:

$$NTF(z) = \frac{V(z)}{Q(z)} = \frac{1}{1+H(z)} = 1 - z^{-1} \tag{2.8}$$

This equation shows that the quantization noise is shaped by a first-order high-pass transfer function. The order of noise shaping is associated with the order of the NTF.

To calculate the SQNR of the output $v$, it is necessary to find the squared magnitudes of the transfer functions which are given out as followings:

$$\left|STF(e^{j\Omega})\right|^2 = \left|e^{-j\Omega}\right|^2 = 1 \tag{2.9}$$

$$\left|NTF(e^{j\Omega})\right|^2 = \left|1-e^{-j\Omega}\right|^2 = \left|1-\cos\Omega + j\sin\Omega\right|^2 = 2-2\cos\Omega = \left(2\sin\left(\frac{\Omega}{2}\right)\right)^2 \tag{2.10}$$

where $\Omega$, defined as $\Omega = 2\pi f/f_s$, is the normalized angular frequency.

The power spectral density of the quantization noise at output $v$ can be calculated by multiplying that of $q$ with the squared magnitude of the NTF (see Fig. 2.6). So, the power of the quantization noise within the band of interest is given by:

$$N_q^2 = \frac{1}{2\pi}\int_{-\Omega_B}^{\Omega_B} \sigma_q^2 \left|NTF\right|^2 d\Omega = \frac{\sigma_q^2}{\pi}\int_0^{\pi/OSR} \left(2\sin(\Omega/2)\right)^2 d\Omega \tag{2.11}$$

If the oversampling ratio is very large, which is a common case for $\Delta\Sigma$ data converters, $\Omega_B = \pi/OSR$ is much less than 1. Then, the following approximation is valid in the signal band.

$$2\sin\left(\frac{\Omega}{2}\right) \approx 2 \cdot \frac{\Omega}{2} = \Omega \tag{2.12}$$

Therefore, the result of Eq. 2.11 can be as simple as:

$$N_q^2 \approx \frac{\sigma_q^2}{\pi} \int_0^{\pi/OSR} \Omega^2 d\Omega = \frac{\sigma_q^2 \pi^2}{3OSR^3} \tag{2.13}$$

Use this result to calculate the maximum SQNR in dB, following expression can be obtained:

$$SQNR_{\max}[dB] = 6.02N + 1.76 + 30\log_{10} OSR - 10\log_{10}\frac{\pi^2}{3} \tag{2.14}$$

Compared with Eq. 2.6, it is obvious that the trading rate of speed and resolution with this 1st-order noise shaping is triple that of plain oversampling, which is 9 dB/octave, or equivalently, 1.5 bit/octave. However, the total noise power at the output (for full bandwidth) is higher than that of a Nyquist rate data converter. Thus, there is a lower limit of OSR, below which ΔΣ converters don't provide any benefits.

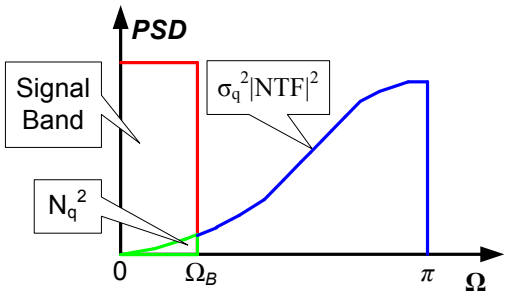



Figure 2.6: Output spectrum of a first-order ΔΣ modulator

A general structure of ΔΣ modulator is shown in Fig. 2.7 [14]. In this diagram, the modulator is divided into two parts: a linear part (the loop filter) containing memory elements and a memoryless nonlinear part (the quantizer). The loop filter is a two-input system whose output *y* can be expressed as a linear combination of inputs *u* and *v*. In *Z* domain, this is:

$$Y(z) = L_0(z)U(z) + L_1(z)V(z) \tag{2.15}$$

So, the first-order ΔΣ modulator shown in Fig. 2.5 is just a special case of the general structure, in which $L_0(z) = -L_1(z) = H(z)$.

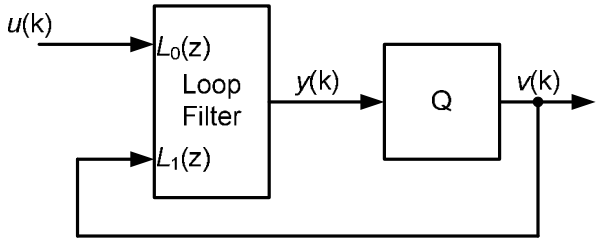



Figure 2.7: General structure of a single-quantizer ΔΣ modulator

The operation of the quantizer is, as usual, described as the addition of an error signal:

$$V(z) = Y(z) + Q(z) \tag{2.16}$$

Using Eq. 2.15 and 2.16, the modulator output $v$ can be written as the linear combination of two signals, namely the modulator input $u$ and the quantization error $q$, in $Z$ domain:

$$V(z) = STF(z)U(z) + NTF(z)Q(z) \tag{2.17}$$

where

$$STF(z) = \frac{L_0(z)}{1 - L_1(z)} \text{ and } NTF(z) = \frac{1}{1 - L_1(z)} \tag{2.18}$$

Conversely, given the desired $STF(z)$ and $NTF(z)$, one can computer the loop filter's transfer functions which are required to implement them.

$$L_0(z) = \frac{STF(z)}{NTF(z)} \text{ and } L_1(z) = 1 - \frac{1}{NTF(z)} \tag{2.19}$$

By properly designing $L_0(z)$ and $L_1(z)$, higher order NTF can be realized while keeping the STF just a few delays. A simple example of the $L^{th}$-order high pass NTF is given by:

$$NTF(z) = \left(1 - z^{-1}\right)^{L} \tag{2.20}$$

Following the same analysis as that used in the first-order modulator, if *OSR* » 1, the in-band integrated noise power will be given by:

$$N_q^2 = \frac{\sigma_q^2 \pi^{2L}}{(2L+1)OSR^{2L+1}} \tag{2.21}$$

and the maximum SQNR in dB can be expressed as following:

$$SQNR_{\max}[dB] = 6.02N + 1.76 + (20L+10)\log_{10} OSR - 10\log_{10}\frac{\pi^{2L}}{2L+1} \tag{2.22}$$

In general, the SQNR will improve with the OSR at a rate of 6*L*+3 dB/octave, or equivalently, *L*+0.5 bit/octave with the $L^{th}$-order noise shaping.

## 2.4. Multi-Stage Noise Shaping

According to Eq. 2.22, the SQNR of a ΔΣ modulator can be improved by increasing the resolution of the quantizer, oversampling ratio and the order of noise shaping. However, the resolution of the quantizer is usually no more than 6 bits. Otherwise, both the circuit complexity and the power consumption of the modulator will be too high. In addition, the sampling rate and hence the OSR is limited by both the semiconductor technology and power consumption. Compared with other two ways, increasing the order of noise shaping is relatively cheap. However, in a single-loop ΔΣ modulator, the order of the loop filter is severely limited by the stability issue [14].

One way to avoid the stability problem in a high-order ΔΣ modulator is to implement it with a cascade of multiple stable low-order loops. This type of noise shaping is called Multi-stAge noise SHaping, or MASH.

Fig. 2.8 gives out a general MASH structure. The first stage ($ADC_1$) is a low-order ΔΣ modulator. Each of the remaining stages ($ADC_2$ to $ADC_n$) can be a ΔΣ modulator as well or a plain Nyquist-rate ADC. If the quantization error $q$ of each stage is acquired and converted to digital format by a subsequent stage, all errors except that of the last stage can be cancelled out at the MASH output $v$ in the digital domain. Proper design of the noise cancellation logic will make the output of the modulator $v$ equal to:

$$V = U \cdot STF_1 \cdot STF_2 \cdots STF_n + Q_n \cdot NTF_1 \cdot NTF_2 \cdots NTF_n \tag{2.23}$$

where the order of the noise transfer function is the summation of the individual orders, $L_1$ to $L_{n.}$.

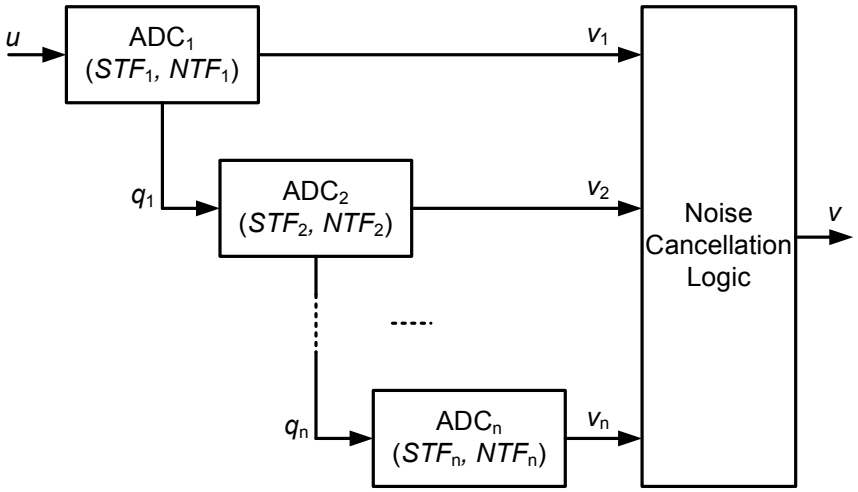



Figure 2.8: A general structure of MASH

When referring to a MASH ADC, it is usual to indicate the number of stages and the order of each stage. For example, a 2-2 MASH (see Fig. 2.9) has two stages, and both stages are second-order ΔΣ modulators.

The quantization noise of the first stage, $q_1$, is obtained by subtracting the input of the quantizer from its output. For this example, the output $v$ of the modulator is given by:

$$V = U \cdot z^{-4} + Q_1\left(ANTF_1 - DNTF_1\right)z^{-2} - Q_2 \cdot ANTF_2 \cdot DNTF_1 \tag{2.24}$$

where $ANTF_1$ and $ANTF_2$ refer to the noise transfer functions of the first and second stages, which are implemented in the analog domain. $DNTF_1$ is the noise transfer function following the second stage, which is implemented in digital domain. Assuming that everything is ideal, i.e., that $ANTF_1 = DNTF_1$, the quantization noise $q_1$ is cancelled, and only the second-stage's quantization noise $q_2$, shaped by the product of the two NTFs, will appear at the output:

$$V = U \cdot z^{-4} - Q_2 \cdot ANTF_1 \cdot ANTF_2 \tag{2.25}$$

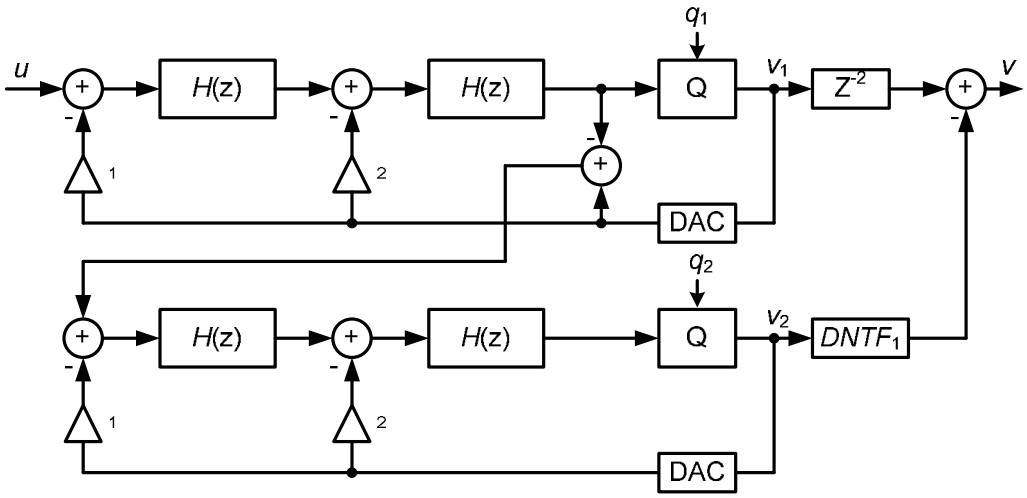



Figure 2.9: 2-2 MASH ΔΣ modulator

However, if the analog and digital transfer functions don't match exactly, a problem known as quantization noise leakage will occur. If noise leakage happens, the quantization noise $q_1$, shaped only by a low-order NTF, will appear at the output and greatly degrade the accuracy of the MASH ΔΣ modulators. The problem of noise leakage is more serious in the continuous-time MASH modulators than in the discrete-time counterparts because the accuracy of the CT analog transfer function is dependent on the absolute RC time constant which is much more inaccurate than the ratio of the capacitors in modern semiconductor process. So, single-loop structure is more popular in the CT ΔΣ modulators.

# CHAPTER 3. SYNTHESIS OF CONTINUOUS-TIME ΔΣ MODULATOR

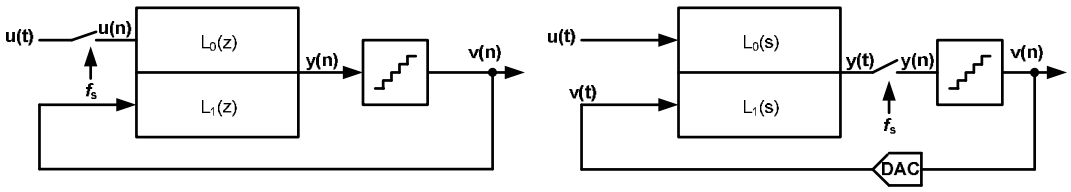
ΔΣ modulators are usually thought of mathematically in the discrete-time (DT) domain as we did in the Chapter 2 because the majority of published designs are built with DT, e.g., switched-capacitor [1, 2] or switched-current [15] circuitry. However, for a continuous-time (CT) ΔΣ modulator, there are two ways to synthesize its loop filter, direct synthesis in the CT domain [16, 17] or equivalently transformation from DT origin [18, 19]. Since the design methodologies of the DT ΔΣ modulators have been thoroughly studied during the past decades, many good design tools, e.g., the ΔΣ MATLAB toolbox written by Richard Schreier [20], are available on hand. In addition, it is easier to simulate a DT ΔΣ modulator with computer. So, it is more popular to synthesize the CT loop filter by equivalently transforming from its DT target.

## 3.1. Impulse-Invariant Transformation

The quantizer in a CT ΔΣ modulator is clocked, which means there is an implicit sampling action inside the modulator, and sampled circuits are DT circuits, so we can make the sampling explicit by placing the sampler immediately prior to the quantizer (see Fig. 3.1b) without changing the behavior of the modulator. For comparison, the general structure of a DT ΔΣ modulator which was shown in Fig. 2.7 is redrawn in Fig. 3.1a.

As we mentioned in the section 2.3, if the quantization is described as the addition of an error signal, a ΔΣ modulator can be treated as a two-input system (see Fig. 3.2) whose output $v$ can be expressed as the linear combination of modulator input $u$ and quantization noise $q$.

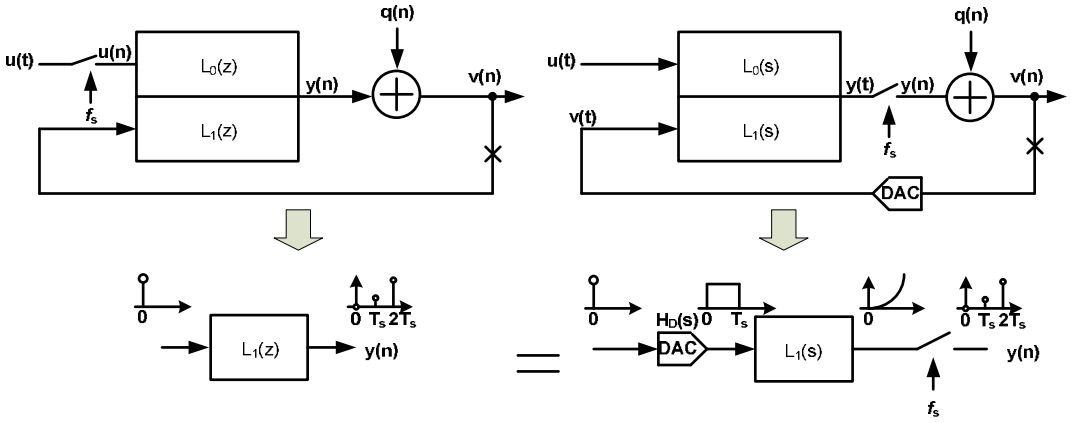
$$V = STF \cdot U + NTF \cdot Q \tag{3.1}$$




(a) (b)

Figure 3.1: General structures of (a) DT and (b) CT ΔΣ modulator

From Fig. 3.2b, it can be seen that, in a CT ΔΣ modulator, both the quantization noise $q$ and modulator output $v$ are discrete-time signals, so it is reasonable to believe that a CT ΔΣ modulator can find its equivalent DT counterpart in terms of the noise transfer function. How to find this equivalence?




(a) (b)

Figure 3.2: Linearized (a) DT and (b) CT ΔΣ modulator and their open loop equivalence

It is well known that the NTF is given by:

$$NTF = \frac{1}{1 - LTF}, \tag{3.2}$$

where LTF stands for the loop transfer function which is the same as $L_1(z)$ in DT modulator, so the NTFs will be the same as long as both modulators have the same LTFs. To find the

equivalent LTFs, it is instructive to zero both inputs of the modulators and open both loops around the quantizers, which leads to bottom two diagrams of Fig. 3.2. In the CT open-loop diagram, the DAC can be thought of as a "discrete-to-continuous converter" which makes a CT pulse $v(t)$ from the quantizer output $v(n)$ which is a discrete-time quantity. This pulse is filtered by $L_1(s)$ (the CT loop filter) to produce $y(t)$ at the quantizer input, which is then sampled to produce the DT quantizer input $y(n)$. If this quantizer input is equal to that of the DT modulator at each sampling instant (Eq. 3.3), then both modulators will produce the same output sequences $v(n)$ and hence the same LTFs:

$$y(n) = y(t)\Big|_{t=nT_s} \tag{3.3}$$

Above equation can be satisfied if the impulse response of the open-loop diagrams in Fig. 3.2 are equal at the sampling instants, leading to the condition:

$$Z^{-1}\{L_1(z)\} = L^{-1}\{H_D(s)L_1(s)\}\Big|_{t=nT_s} \tag{3.4}$$

or, in the time domain:

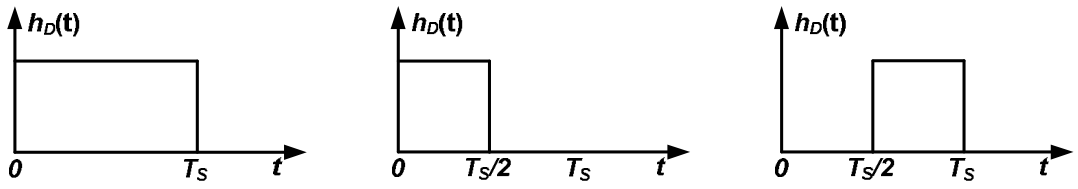
$$l_1(n) = \{h_D(t) * l_1(t)\}\Big|_{t=nT_S} = \int_{-\infty}^{+\infty} h_D(\tau) l_1(t-\tau) d\tau \Big|_{t=nT_S} \tag{3.5}$$

where $H_D(s)$ and $h_D(t)$ are the transfer function and impulse response of the DAC. Since this equivalence requires the DT and CT impulse responses to be the same, this transformation between them is called impulse-invariant transformation (IIT).

## 3.2. Simulation-Based Synthesis of a CT Loop Filter

To synthesize a CT loop filter from a DT target based on IIT in a practical design, it is necessary to determine the shape of the feedback DAC waveform first because different DAC pulses will result in different CT loop filters for a given DT origin according to Eq.3.4 or 3.5.

The most commonly used DAC waveform is the rectangular pulse which includes non-return-to-zero (NRZ), return-to-zero (RZ) and half-delay-return-to-zero (HRZ) pulses [18]. The impulse responses of those DAC waveforms are shown in Fig. 3.3.




(a) (b) (c)

Figure 3.3: Impulse response of rectangular DAC pulses: (a) NRZ; (b) RZ; (c) HRZ

Besides the rectangular DAC waveform, some other waveforms are proposed to reduce the clock jitter sensitivity of the modulator [21, 22]. The research on the DAC jitter sensitivity will be presented in detail in the Chapter 4.

After determining the feedback DAC waveform, the CT loop filter $L_1(s)$ can be calculated manually based on the tables and steps described in reference [18]. To realize the $L_1(s)$ with a given loop filter architecture, e.g., feedback or feed-forward, the symbolic expression of the transfer function has to be obtained. After that, the coefficients of the expression can be calculated by solving an equation set that is acquired by mapping $L_1(s)$ to the symbolic expression (see Appendix A of [23]).

The synthesis method described above needs too much manual calculation, which makes this process very complex, especially for a high-order loop filter. In addition, this method is difficult to use while the non-rectangular DACs are employed in the feedback loop because the equivalence between the S-domain and the Z-domain becomes much more complex while using other shaped DACs, e.g., the exponential decaying DAC pulse [24].

A novel synthesis methodology that combines the impulse-invariant transformation and the mapping between $L_1(s)$ and a given loop filter structure was developed in this work. In

this methodology, most of the transformation-domain calculation is replaced by the time-domain simulations, which greatly simplifies the synthesis process. In addition, it can be used to synthesize the loop filter with different DAC waveforms.

In a linear time invariant (LTI) system described by linear equation:

$$Q(D)\,y(t) = P(D)\,f(t)\,, \tag{3.6}$$

where $Q(D)$ and $P(D)$ are polynomials of D-operators (Differentiation), the output response can be divided into two parts: natural response and forced response. The former is usually given by the following equation:

$$y_n(t) = \sum_{j=1}^{n} c_j e^{\lambda_j t} \tag{3.7}$$

where the $\lambda_j$ are the roots of the characteristic equation $Q(\lambda) = 0$.

Fig. 3.4 shows the diagram of a 5$^{th}$-order feed-forward CT ΔΣ modulator. In this LTI system $L_1(s)$, the natural response is determined by those two local loops which form the non-DC poles of the transfer function. On the other hand, the forced response is related to all those feed-forward paths.

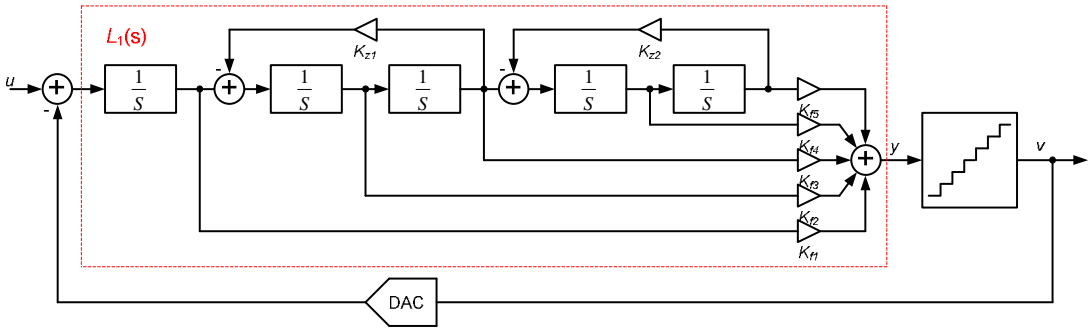



Figure 3.4: Diagram of a 5$^{th}$-order feed-forward CT ΔΣ modulator

The impulse-invariant transformation described in the section 3.1 will map the poles in S-domain to those in Z-domain with following equation while keeping the multiplicity [18].

$$Z_P = e^{S_P} \tag{3.8}$$

In addition, the non-DC poles of the $L_1(s)$ in Fig. 3.4 have the following relationship with the coefficients of the local feedback branches, namely $K_{Z1}$ and $K_{Z2}$:

$$S_{P_{1,2}} = \pm j\sqrt{K_{Z1}} \text{ and } S_{P_{3,4}} = \pm j\sqrt{K_{Z2}} \tag{3.9}$$

Using these two equations, we can easily get the relationship between the non-DC poles of the $L_1(z)$, which are also the non-DC zeros of the NTF, and the coefficients of $K_{Z1}$ and $K_{Z2}$ in the CT loop filter:

$$K_{Z1} = \left(angle(Z_{P_{1,2}})\right)^2 \text{ and } K_{Z2} = \left(angle(Z_{P_{3,4}})\right)^2 \tag{3.10}$$

After determining the natural response of the CT loop filter, we have to identify a set of coefficients that can be used to adjust the gain of each loop independently. In this example, those feed-forward paths ($K_{f1} \sim K_{f5}$) are just the independent path gain factors that we need to find. For example, the gain of the first-order loop that only contains one integrator can be adjusted arbitrarily by the coefficient $K_{f1}$ without affecting the gains of other loops.

To determine those independent coefficients, we have to "ping" the loop filter for each coefficient by setting it to be one and the others zero, which can be performed with the time-domain simulation in some commercial simulators, e.g., SIMULINK. Fig. 3.5 shows the simulation diagram of the open-loop CT modulator. The block $DAC(t)$ is used to generate a specific DAC impulse response. For each feed-forward coefficient, we can get a sampled impulse response at the output $v$. Because those coefficients are independent of each other, the total impulse response should be the linear combination of those individual impulse responses:

$$h(k) = \sum_{i=1}^{5} \alpha_i \cdot h_i(k) \tag{3.11}$$

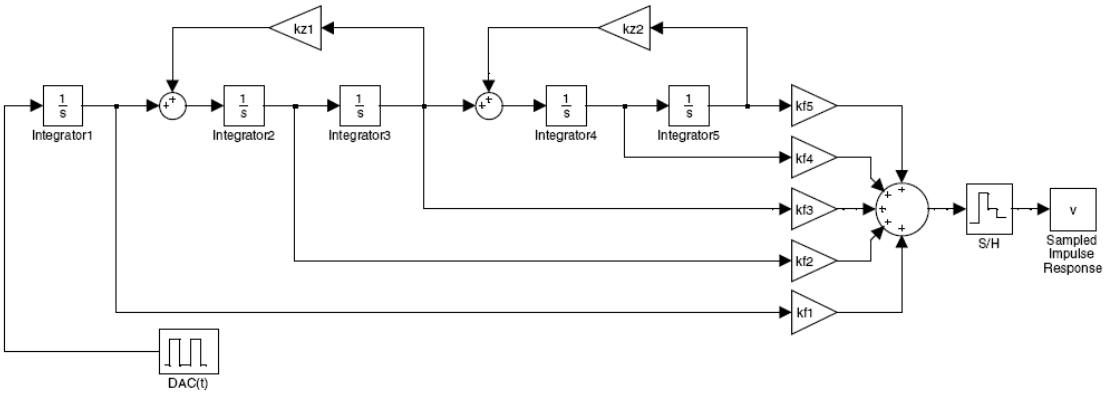



Figure 3.5: Simulation diagram used to determine the feed-forward coefficients

We can build up an equation set by equating the above impulse response with that of the $L_1(z)$, which is also easily obtained by simulation, at several first time instants, e.g., $h(1)$, $h(2)$, …, and $h(5)$.

$$\begin{aligned}
&h_1(1)\alpha_1 + h_2(1)\alpha_2 + h_3(1)\alpha_3 + h_4(1)\alpha_4 + h_5(1)\alpha_5 = h_d(1)\\
&h_1(2)\alpha_1 + h_2(2)\alpha_2 + h_3(2)\alpha_3 + h_4(2)\alpha_4 + h_5(2)\alpha_5 = h_d(2)\\
&h_1(3)\alpha_1 + h_2(3)\alpha_2 + h_3(3)\alpha_3 + h_4(3)\alpha_4 + h_5(3)\alpha_5 = h_d(3)\\
&h_1(4)\alpha_1 + h_2(4)\alpha_2 + h_3(4)\alpha_3 + h_4(4)\alpha_4 + h_5(4)\alpha_5 = h_d(4)\\
&h_1(5)\alpha_1 + h_2(5)\alpha_2 + h_3(5)\alpha_3 + h_4(5)\alpha_4 + h_5(5)\alpha_5 = h_d(5)
\end{aligned} \tag{3.12}$$

where $h_d(k)$ is the impulse response of DT loop filter $L_1(z)$. It is easy to solve the above equation set in MATLAB and get the answer of $\alpha_i$.

$$\begin{bmatrix}\alpha_1\\ \alpha_2\\ \alpha_3\\ \alpha_4\\ \alpha_5\end{bmatrix} = \begin{bmatrix} h_1(1) & h_2(1) & h_3(1) & h_4(1) & h_5(1)\\ h_1(2) & h_2(2) & h_3(2) & h_4(2) & h_5(2)\\ h_1(3) & h_2(3) & h_3(3) & h_4(3) & h_5(3)\\ h_1(4) & h_2(4) & h_3(4) & h_4(4) & h_5(4)\\ h_1(5) & h_2(5) & h_3(5) & h_4(5) & h_5(5)\end{bmatrix}^{-1}\begin{bmatrix} h_d(1)\\ h_d(2)\\ h_d(3)\\ h_d(4)\\ h_d(5)\end{bmatrix} \tag{3.13}$$

By making the feed-forward coefficients equal to corresponding $\alpha_i$, the total impulse response of the open-loop CT modulator ($DAC(t)$ * $h(t)$) at the sampling instants will be the same as that of DT loop filter $L_1(z)$.

This novel synthesis methodology of the CT ΔΣ loop filter realizes the impulse-invariant transformation (IIT) and the mapping of the CT transfer function for a given loop filter topology at the same time. The procedure is summarized as following:

Step 1: Synthesize the target DT NTF and hence the $L_1(z)$ based on the specification of the ADC by using ΔΣ toolbox [20]. Get the impulse response of $L_1(z)$ by simulation.

Step 2: Determine the DAC waveform and the structure of the CT ΔΣ modulator. Build the simulation diagram in SIMULINK.

Step 3: Calculate the coefficients of the local feedback loops in the CT modulator by substituting the non-DC zeros of the DT NTF to Eq. 3.10.

Step 4: Identify a set of coefficients that can adjust the gain of each loop in the CT modulator independently.

Step 5: Simulate the impulse response of each loop by setting the corresponding coefficient to be one and the others to be zero. The expression of the total sampled impulse response of the CT modulator is the linear combination of those individual responses.

Step 6: Build up an equation set for the coefficients of the linear combination by equating those two impulse response obtained in Step 1 and 5. Solve this equation set to get the coefficients.

Step 7: Calculate the coefficients of the branches in the CT loop filter based on those independent coefficients acquired in Step 6.

## 3.3. Signal Transfer Function (STF)

The synthesis of a CT ΔΣ modulator from a DT target by using IIT only considers the equivalence in terms of the noise transfer function, so this transformation cannot guarantee the

signal transfer function of the CT modulator is the same as the DT one (usually they are different).

According to the general structure shown in Fig. 3.1b, the STF of the CT modulator can be given by:

$$STF(s) = \frac{L_0(s)}{1 - LTF(z)} = L_0(s) \cdot NTF(z)\Big|_{z=e^s} \tag{3.14}$$

In a feedback CT ΔΣ modulator (see Fig. 3.6), the transfer function of $L_0(s)$ is an all-pole system whose poles are the same as the zeros of the NTF in the band of interest. So, the magnitude of the STF in the signal band is flat and equal to one if the feed-in branch coefficient is equal to that of the first feedback branch in magnitude. In addition, outside the signal band, the STF shows low-pass characteristics. Fig. 3.7 shows the magnitude response of $L_0(s)$, $NTF(z)$ and $STF(s)$ of the modulator shown in Fig. 3.6.

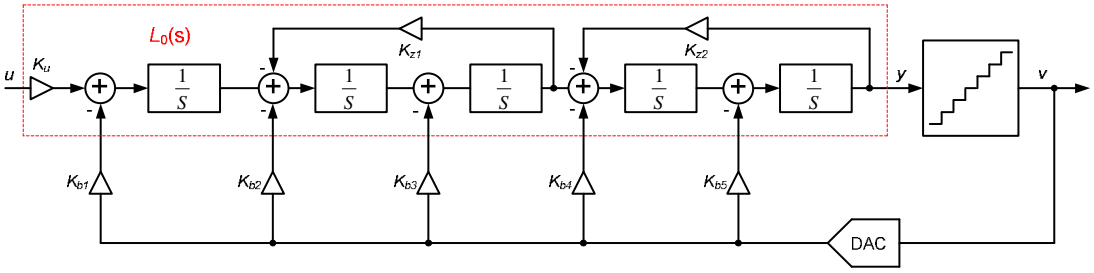



Figure 3.6: Diagram of a 5th-order feedback CT ΔΣ modulator

As for the feed-forward CT modulator like that shown in Fig. 3.4, the $L_0(s)$ shares the same circuits with $L_1(s)$. The poles of the $L_0(s)$ are still the same as the zeros of the NTF in the signal band. However, it also shows zeros in its transfer function, which are introduced by the feed-forward paths. Those zeros will cause the out-of-band peaking in the STF magnitude. Fig. 3.8 shows the magnitude response of $L_0(s)$, $NTF(z)$ and $STF(s)$ of this feed-forward modulator.

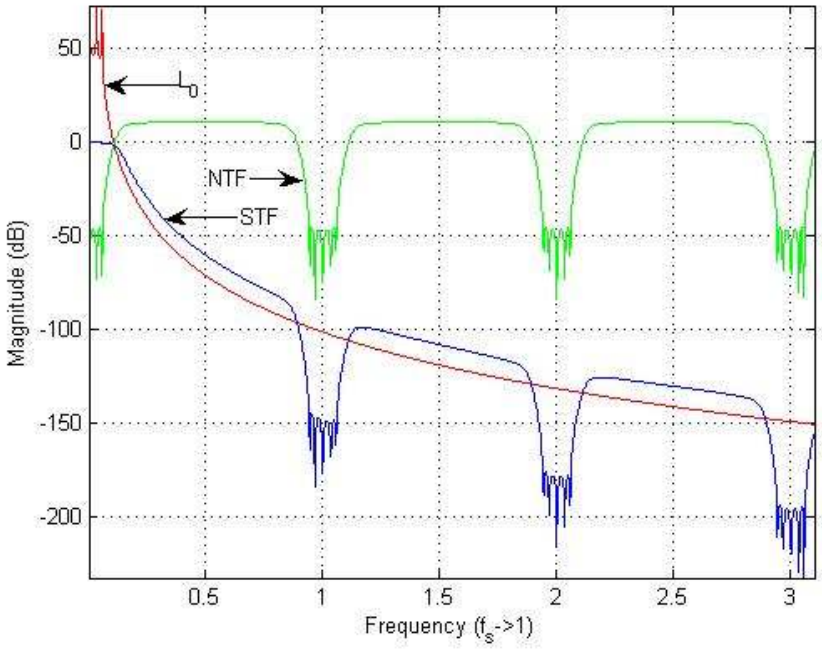



Figure 3.7: Magnitude response of $L_0(s)$, $NTF(z)$ and $STF(s)$ of a 5$^{th}$-order feedback CT $\Delta\Sigma$ modulator

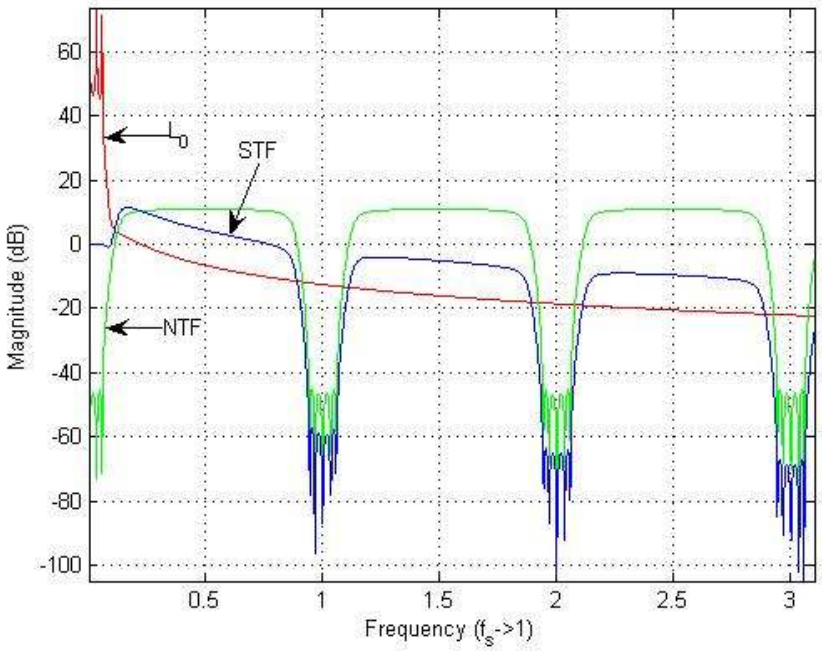



Figure 3.8: Magnitude response of $L_0(s)$, $NTF(z)$ and $STF(s)$ of a 5$^{th}$-order feed-forward CT $\Delta\Sigma$ modulator

The same out-of-band peaking appears in the DT feed-forward ΔΣ modulator, but it is easy to cancel it by adding a direct feed-in branch to the input of the quantizer [25] because the zeros of the new transfer function, $1+L_0(z)$, are the same as the poles of the NTF. However, in the CT case, the out-of-band peaking cannot be cancelled in the same way because the zeros of the new transfer function, $1+L_0(s)$, are still different from the poles of the NTF in terms of Eq. 3.8.

In order to compensate the out-of-band peaking in the STF of the feed-forward CT modulator, some new ideas were proposed in publications [8, 26]. One of them is to modify the STF by adding a low-pass (usually first-order) transfer function in series with the original STF. Two methods can be used to realize this idea without affecting the loop transfer function that should be the same as the DT origin in terms of impulse response. One is to directly add the low-pass filter at the front end of the CT modulator (Fig. 3.9a), and the other is to add the low-pass filter in the loop with a compensation high-pass filter. The transfer function of the high-pass filter should be $1/LPF(s)$ (Fig. 3.9b) or $1 - LPF(s)$ (Fig. 3.9c). All of those three CT modulators have a filtering STF:

$$STF(s) = LPF(s) \cdot STF(s)_{feed-forward} = LPF(s) \cdot H(s) \cdot NTF(z)\Big|_{z=e^s} \qquad (3.15)$$

These approaches showed good results in high OSR modulators but they are not suitable for low OSR design. Because, in a low OSR modulator, the out-of-band peaking is very close to (or even in) the signal band, the added low-pass filter will introduce attenuation around the edge of the signal band. It is difficult to find a good trade-off between the effectiveness of the filtering and the amount of the in-band attenuation. In this work, a new way is proposed to cancel the out-of-band peaking in the STF, which will be described later.

A very important characteristic that makes the CT ΔΣ modulators superior to the DT counterparts is the inherent anti-aliasing. As we mentioned in the chapter 2, an anti-aliasing

filter is needed before an ADC otherwise the out-of-band signals, especially those within the frequency ranges of ($nf_s$-$f_B$, $nf_s$+$f_B$), will alias into the band of interest after sampling. However, from both Fig. 3.7 and 3.8, those obvious notches around the multiples of the sampling frequency can be seen in the magnitude response of the STF. This is known as inherent anti-aliasing. From Eq. 3.14, we can see that the zeros of the NTF are also the zeros of the STF except those which are cancelled by the poles of $L_0$ within the signal band. Because the zeros of the NTF reside around the multiples of the sampling frequency, the CT ΔΣ modulators can attenuate the signals in those bands and hence are inherent anti-aliasing.

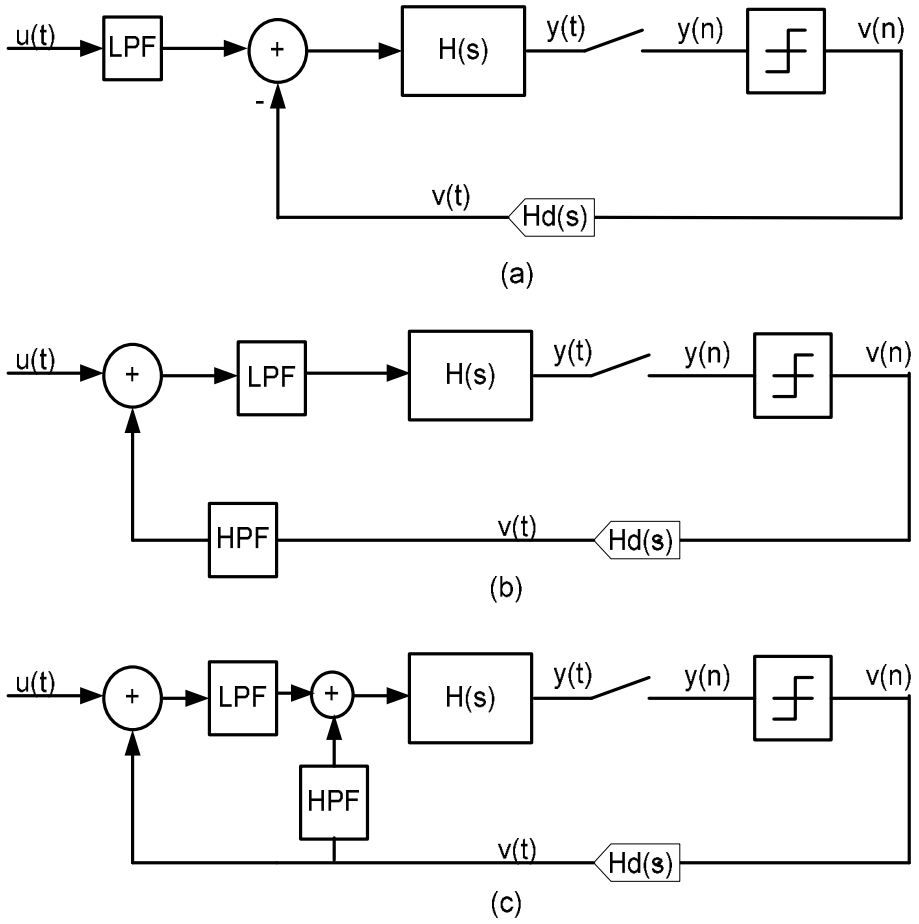


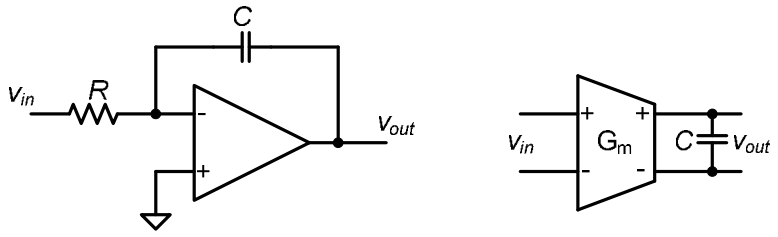

Figure 3.9.Three feed-forward CT ΔΣ modulators with filtering STF

# CHAPTER 4. DESIGN ISSUES OF CONTINUOUS-TIME ΔΣ MODULATOR

After successfully synthesizing the continuous-time (CT) loop filter from the discrete-time (DT) target for a given feedback DAC waveform, we need to realize the modulator with real circuit blocks. However, the non-idealities of those circuit blocks as well as the clock source will influence the performance, even the stability, of the CT ΔΣ modulator. In this chapter, some the most critical design issues are discussed in detail, which include the non-idealities of the CT integrators and the internal flash ADC, clock jitter, and element mismatch of the multi-bit feedback DAC. For each issue, detailed analysis and example simulation are presented, and then the possible solutions are discussed.

## 4.1. Non-Idealities of CT Integrators

The basic circuit blocks of which a CT loop filter consists are the CT integrators. Many kinds of CT integrators are available but the most commonly used ones are RC integrators and $G_mC$ integrators (see Fig. 4.1).




$$V_{out} = -\frac{1}{sRC}V_{in} \qquad V_{out} = \frac{G_m}{sC}V_{in}$$

(a) (b)

Figure 4.1: (a) RC and (b) $G_mC$ integrators

The advantages of the RC integrators over the $G_mC$ counterparts include higher linearity and larger input signal swing. Because the RC integrators are based on the closed-loop applications of the operational amplifiers (opamps), the opamps' inputs are virtual ground and only experience very small signal swing regardless of that of the integrator's input. On the contrary, the transconductor, which performs voltage-to-current (V-I) transformation with a known (or well-controlled) transconductance, operates under the open-loop condition in the $G_mC$ integrators, so its inputs have to experience the full swing of the integrator's input, which degrades the linearity of the integrator. Due to this reason, the input signal of the $G_mC$ integrator has to be small enough to keep a reasonable linearity.

When using RC integrators to build a CT $\Delta\Sigma$ modulator, the virtual ground provided by the closed-loop opamp application will also greatly improve the linearity of the feedback current DAC whose outputs are connected with the inputs of the opamp. However, in a CT $\Delta\Sigma$ modulator based on $G_mC$ integrators, the feedback DAC's outputs have to be connected with the output of the integrator and hence experience the full output swing, which degrades the linearity of the DAC.

On the other hand, due to the same open-loop working condition, the speed performance of the $G_mC$ integrator is better than the RC counterparts. In other words, the power consumption of the $G_mC$ integrator will be lower for a given bandwidth requirement.

According to the above analysis, the RC integrators are preferred in our prototype CT modulator, so only the non-idealities of the RC integrators will be discussed in this section.

### *4.1.1. Finite Gain Bandwidth of Opamp*

Operational amplifiers are the basic blocks of the RC integrators. An ideal opamp can be seen as a voltage-controlled voltage source whose voltage gain is infinitely large across the

whole frequency domain. However, a real opamp has a finite DC gain and several poles and zeros in its transfer function. In analysis, it is popular and reasonable to approximate the real opamp's characteristics with a single-pole model given by:

$$A(s) = \frac{A_{DC}}{1 + \frac{s}{\omega_P}} \tag{4.1}$$

where $A_{DC}$ and $\omega_P$ stand for the DC gain and the pole frequency of the opamp, respectively.

Using this opamp model in a general $n$-input RC integrator shown in Fig. 4.2, the integrator transfer function (ITF) from the $i^{th}$ input to the output can be calculated by using the Kirchhoff Current Law (KCL) at the negative input point of the opamp.

$$ITF(s)\Big|_{V_{in-i} \sim V_{out}} = -\frac{1}{R_i} \frac{1}{\frac{C}{A_{DC}\omega_P} s^2 + \left( \frac{(A_{DC}+1)C}{A_{DC}} + \frac{1}{A_{DC}\omega_P} \left( \sum_{k=1}^{n} \frac{1}{R_k} \right) \right) s + \frac{1}{A_{DC}} \left( \sum_{k=1}^{n} \frac{1}{R_k} \right)} \tag{4.3}$$

If $A_{DC}$ » 1, which is a common case in real opamps, the above equation can be simplified as:

$$\begin{aligned} ITF(s)\Big|_{V_{in-i} \sim V_{out}} &= -\frac{1}{R_i} \frac{1}{\frac{C}{A_{DC}\omega_P} s^2 + \left( C + \frac{1}{A_{DC}\omega_P} \left( \sum_{k=1}^{n} \frac{1}{R_k} \right) \right) s} \\ &= -\frac{1}{sR_iC} \cdot \frac{1 - \frac{\left( \sum_{k=1}^{n} \frac{1}{R_k C} \right)}{GBW + \left( \sum_{k=1}^{n} \frac{1}{R_k C} \right)}}{1 + \frac{s}{GBW + \left( \sum_{k=1}^{n} \frac{1}{R_k C} \right)}} \end{aligned} \tag{4.4}$$

where $GBW = A_{DC} \cdot \omega_P$ stands for the gain bandwidth product of the opamp.

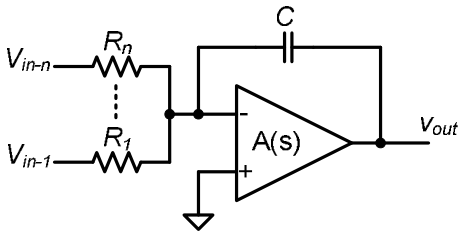



Figure 4.2: An *n*-input RC integrator

It is convenient to normalize the RC time constants of the integrators to the sampling period, $T_s$ or $1/f_s$, of the CT ΔΣ modulator because the $T_s$ is usually assumed to be one while synthesizing the CT loop filter using the IIT. So, we have following equation:

$$\frac{1}{R_k C} = \frac{K_k}{T_s} = K_k f_s \tag{4.5}$$

where $K_k$ is the scaling coefficient.

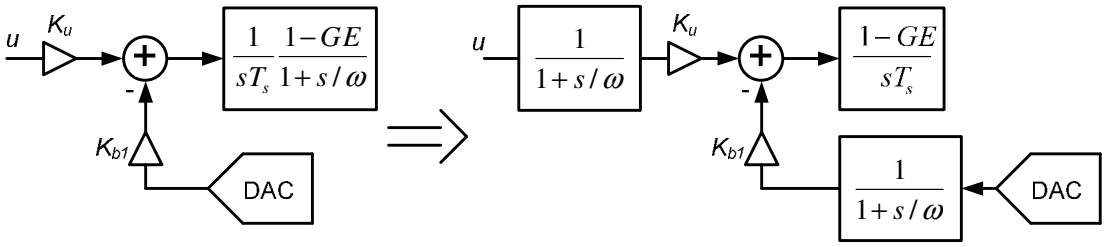
Compared with the ideal integrator transfer function shown in Fig. 4.1a, Eq. 4.4 represents the gain error (GE) and second pole ($\omega$) which are introduced by the finite gain bandwidth of the opamp:

$$GE = \frac{\sum_{k=1}^{n} K_k f_s}{GBW + \sum_{k=1}^{n} K_k f_s} \text{ and } \omega = GBW + \sum_{k=1}^{n} K_k f_s \tag{4.6}$$

So, the integrator transfer function can be represented as

$$ITF(s)\big|_{V_{in-i} \sim V_{out}} = -\frac{K_i}{sT_s} \cdot \frac{1-GE}{1+\frac{s}{\omega}} \tag{4.7}$$

Fig. 4.3a shows a typical diagram of the first stage of the CT ΔΣ modulator, in which the integrator block is modeled with Eq. 4.7.




(a) (b)

Figure 4.3: The first stage of CT modulator with finite GBW opamp

To understand the effect of the gain error and the second pole of the integrator on the modulator, we redraw the diagram as Fig. 4.3b. The effect of the gain error is equivalent to that of the RC time constant variation which will be discussed in the next section. It can be compensated by adjusting the coefficient $K_k$ with some kind of tuning techniques. The second pole of the integrator equivalently adds a low-pass filter in both the feed-in and feedback branches. For the feed-in branch, this low-pass filter has little effect because the signal frequency is usually much lower than the pole frequency $\omega$. However, this is not the case in the feedback branch. As discussed in [27], the low-pass filter in the feedback path equivalently introduces a delay which affects the modulator in the same as the excess loop delay introduced by the quantizer. The solution to compensate this delay will be described in the section 4.2.

### *4.1.2. Variation of RC Time Constant*

As we discussed before, the accuracy of the integrator transfer function is related to that of the RC time constant. In modern semiconductor process, the absolute values of resistors and capacitors can vary as large as ±15% independently due to the change of process, supply voltage and temperature (PVT), so it is reasonable to believe that the RC product and hence the integrator gain can vary ±30%.

In order to see the effect of the RC time constant variation on a CT ΔΣ modulator, a system-level simulation is performed on the feed-forward modulator shown in Fig. 3.4. In this simulation, the normalized time constant is swept in the range from 0.7 to 1.7.

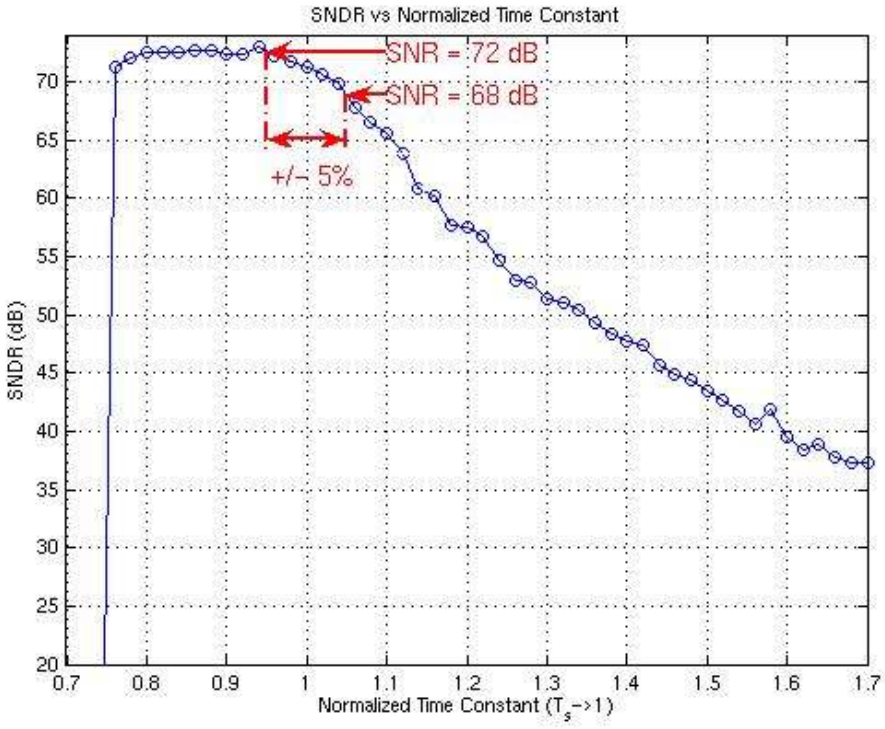



Figure 4.4: The effect of RC time constant variation on the CT modulator

From the simulation results shown in Fig. 4.4, we find that when the time constant deviates from its nominal value $T_s$, the performance of the modulator will degrade. When the time constant becomes smaller, a better signal-to-noise ratio (SNR) may result due to the higher loop filter gain. However, the system becomes unstable when the normalized time constant decreases to be about 0.76. If the time constant is larger than $T_s$, although the modulator is more stable, the noise shaping is less efficient due to the smaller loop filter gain, and hence the in-band noise power increases. So, during the system level design, the in-band noise increasing due to the time constant variation should be considered in the whole noise

budget. If only 2-dB degradation in SNR is allowed, above simulation results show that the variation of less than ±5% is necessary.

To make the RC product variation as small as ±5%, some kind of tuning technique has to be used. In the past several decades, many useful tuning techniques were published for designing continuous-time filters [28 ~ 31]. In a CT ΔΣ modulator based on RC integrators, it is more convenient to tune the capacitors instead of the resistors to adjust the RC product because the integration capacitor is shared by all input resistors. Fig. 4.5 shows the diagram of a tunable capacitor array which consists of binary-weighted capacitors.

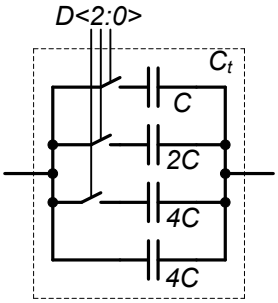



Figure 4.5: A 3-bit binary-weighted tunable capacitor

The *D*<2:0> is a 3-bit tuning code. The nominal value of it is "100", which leads the total capacitance $C_t$ equal to that of eight unit capacitors. The tuning range of this capacitor array is from -50% to +37.5% with the step size of 12.5%. If we want to reduce the step size to increase the tuning accuracy, the always-on capacitance should be increased. For example, if we set it to be *8C* instead of *4C*, then the tuning accuracy is increased to be about 8.3%. However, the tuning range is reduced, which is from -33.3% to +25%.

## 4.2. Non-Idealities of Quantizer

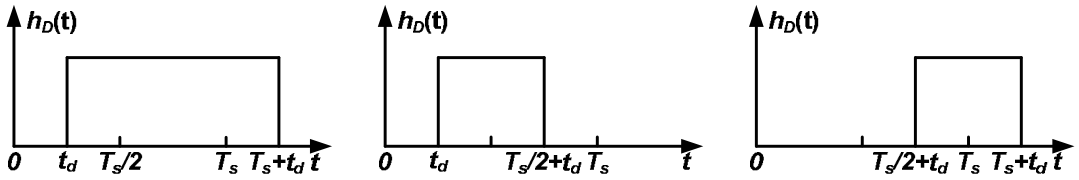
In a wideband CT ΔΣ modulator, a multi-bit quantizer is usually used to reduce the quantization noise as well as the clock jitter sensitivity. The non-idealities of this fast multi-bit

quantizer, which include the excess delay, comparator offset, hysteresis, and metastability, will greatly affect the performance of the whole modulator.

### *4.2.1 Quantizer Delay (Excess Loop Delay)*

When we synthesize the CT loop filter $L_1(s)$ from a DT target $L_1(z)$ for a given feedback DAC waveform in the section 3.1, it is assumed that the delay between the sampling instant of the loop filter output and the generation of new output is zero. However, in the real circuits, this delay, known as excess loop delay, is non-zero due to the finite speed of transistors. The excess loop delay usually consists of the delays introduced by the quantizer (including the dynamic element matching (DEM) logic if necessary), DAC, and loop filter. In section 4.1.1, the delay caused by the loop filter has been analyzed and replaced with the equivalent one in the feedback path so the total excess loop delay can be modeled with a delay cell in the feedback path.

If the excess loop delay is considered, the impulse response of those three rectangular DAC pulses shown in Fig. 3.3 is changed to be that in Fig. 4.6.




(a) (b) (c)

Figure 4.6: Impulse responses of the rectangular DAC pulses including excess loop delay: (a) NRZ; (b) RZ; (c) HRZ

For NRZ and RZ pulses, the delay $t_d$ includes the whole excess loop delay. However, if using HRZ DAC pulse, the quantizer delay, and even the delay introduced by the DEM logic, can be absorbed by the explicit half clock delay of the DAC pulse, so the $t_d$ in Fig 4.6c

mainly refers to the DAC switching delay and the equivalent delay caused by the finite gain bandwidth of the integrators in the loop filter.

As analyzed in [18], if the falling edge of the DAC pulse exceeds the time instant $T_s$, the order of the equivalent DT loop filter of the CT one is higher by one than under ideal conditions, which makes the CT modulator uncontrolled. The excess loop delay degrades the dynamic range of the modulator by reducing the effectiveness of the noise shaping as well as the maximum stable input signal swing. If the excess loop delay is too large compared with the clock period, the CT modulator will be unstable. Fig. 4.7 shows the simulation results of the feed-forward CT modulator given by Fig. 3.4 with three different excess loop delays $t_d$.

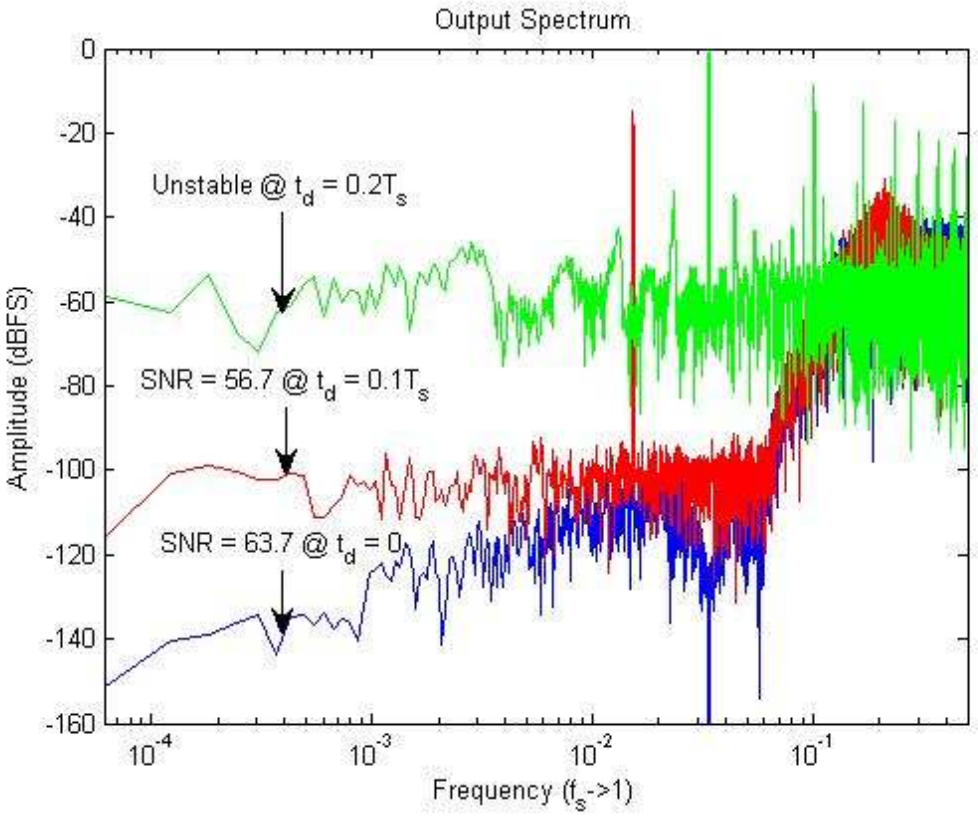



Figure 4.7: The effect of the excess loop delay on the CT modulator

In order to compensate the excess loop delay, the RZ pulse can be used as the DAC waveform. From Fig.4.6b, it can be seen that if the excess loop delay is smaller than half clock period, then the falling edge is still within the range of $0 \sim T_s$, and hence the equivalent DT loop filter has the same order of the CT one. However, in most wideband CT ΔΣ modulators, the NRZ DAC pulse is superior to the RZ (or HRZ) counterpart in terms of clock jitter sensitivity which will be analyzed in detail in section 4.3. In addition, because the exact value of the excess loop delay $t_d$ is unknown while synthesizing the CT loop filter, the resulting CT modulator still cannot realize the same noise shaping as the DT target even using RZ DAC pulse.

A common solution to the excess loop delay while using NRZ DAC pulse is to introduce an explicit full clock delay in the feedback path to absorb the varying quantizer delay as well as the other delays caused by the possible logic circuits (see Fig. 4.8). However, due to this full clock delay, the impulse response of the CT loop at the sampling instant $T_s$ is zero. To compensate this response sample, an extra feedback branch is added directly to the quantizer input to make the total impulse response equivalent to the DT target [32]. Because the loop formed by the extra feedback branch doesn't include any integrator, we call this loop zero-order loop.

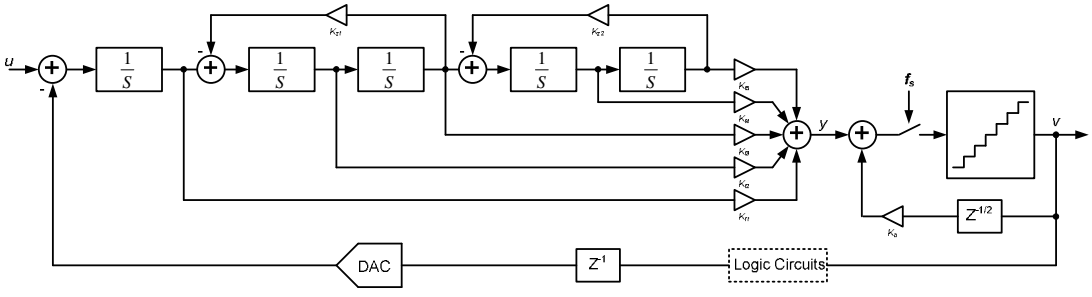



Figure 4.8: The feed-forward CT ΔΣ modulator with excess loop delay compensation

As an example, the impulse-invariant transformation with this excess loop delay compensation is performed between the above CT modulator and a DT target. The resulting impulse responses are shown in the Fig. 4.9. It is obvious that the zero-order loop doesn't affect any other samples of the impulse response which are formed by those original loops. Although a half clock delay is used in the direct feedback path to compensate the quantizer delay in this example, the real delay of the quantizer can be any value between 0 and $T_s$, which greatly relaxes the speed requirement of the quantizer.

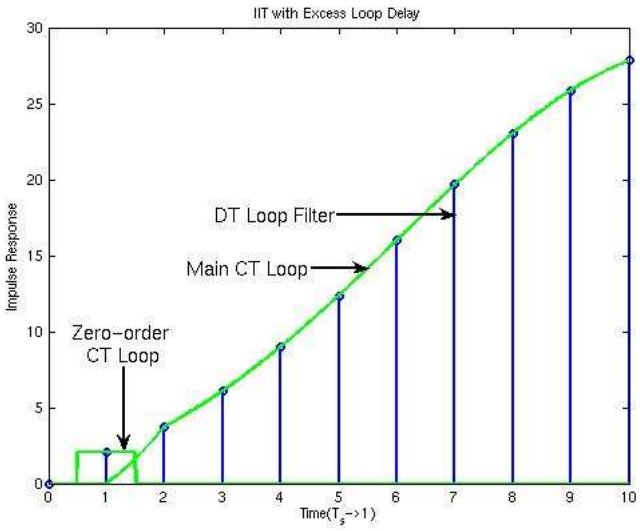



Figure 4.9: Impulse-invariant transformation with the compensation for excess loop delay

It should be mentioned here that above scheme cannot compensate the DAC delay and the equivalent delay caused by the finite integrator GBW. However, compared with the quantizer delay, those two delays are much smaller which can be partially compensated by adjusting the timing relationship between the quantizer and DAC clock signals.

### *4.2.2. Real Characteristics of Comparator*

The quantizer in a ΔΣ modulator is usually a flash ADC which consists of a comparator array and a resistor string to generator a thermometer-code output (see Fig. 4.10).

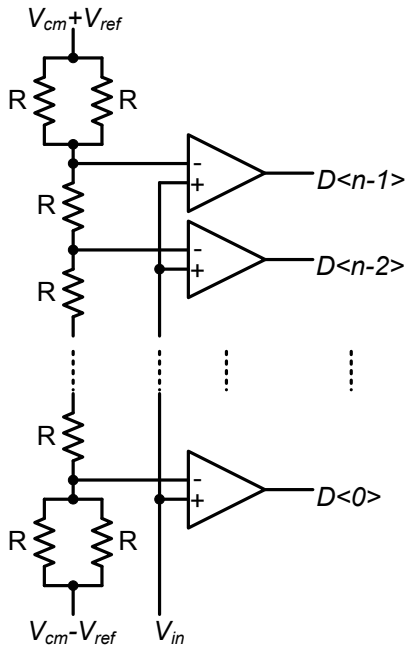



Figure 4.10: Diagram of the quantizer (flash ADC)

$V_{cm}$ is the common mode voltage of the input signal $V_{in}$ and $2V_{ref}$ is the full-scale of the quantizer.

Besides the excess loop delay, the offset, hysteresis and metastability of the comparators are three important non-idealities of the quantizer which will affect the performance of a CT ΔΣ modulator.

In a commonly used latched comparator, a preamplifier is usually added before the latch to reduce its input-referred offset (see Fig. 4.11). As for the offset of the preamplifier itself, some input offset storage techniques, e.g., auto-zeroing, were proposed to reduce it. So, the total input-referred offset of the comparator is given by [33]:

$$V_{OS(total)} = \frac{V_{OSA}}{1+A_0} + \frac{\Delta q}{C_s} + \frac{V_{OSL}}{A_0} \tag{4.8}$$

where $V_{OSA}$ and $V_{OSL}$ are the input offset of the preamplifier and the latch respectively, $\Delta q$ is the error due to the charge injection, and $A_0$ is the gain of the preamplifier. From this equation, we can see that the offset of the comparator is attenuated by $A_0$ which is normally between 10 and 20, so the comparator offset won't become a big problem in a ΔΣ modulator.

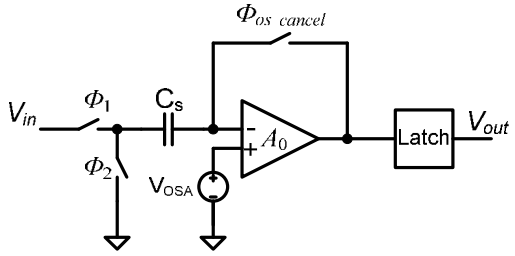



Figure 4.11: Input offset cancellation of a comparator

Hysteresis refers to the memory characteristics of a quantizer, which means the quantizer does not make a decision to change the output when it should. Like a DC offset, the hysteresis will also degrade the noise performance of the ΔΣ modulators. In order to reduce the hysteresis, the comparator should be reset before entering the regeneration period. For example, the differential internal nodes in the latch can be shorted to one of the power supplies or connected together using switches in the reset phase [34].

Metastability refers to the phenomenon that the regeneration time of the comparator becomes longer when the input signal is very small. Besides the signal magnitude, the slope of the input signal also affects the regeneration time. This varying delay will cause the output limit cycle behavior and variant feedback charge which folds the out-of-band noise into signal band in the same way the clock jitter does (see detail in section 4.3) Reference [35] proposed several methods to mitigate the performance loss due to the metastability, such as scaling the quantizer input to have as large as possible span; decreasing regeneration time by inserting a preamplifier stage and increasing the gain-bandwidth product of the regenerative circuits; adding additional latching stages and using improved modulator architectures.

In conclusion, the real characteristics of a comparator can be that shown in Fig. 4.12.

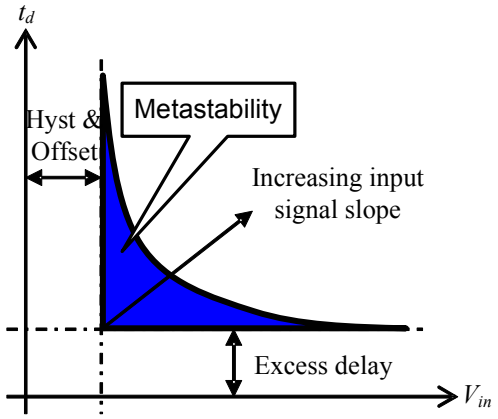



Figure 4.12: Real characteristics of a comparator

where $t_d$ refers to the delay of the comparator and $V_{in}$ is the input signal amplitude.

## 4.3. Clock Jitter

In a DT ΔΣ modulator, the continuous-time signal is sampled at the modulator input, so the sampling error caused by the clock jitter is directly added to the output without any attenuation. On the other hand, the sampling action in the CT modulator happens at the input of the quantizer, so the jitter-induced error is shaped by the loop filter before it appears at the output and hence may be negligible.

However, the DAC output of the CT modulator is continuous, which means the feedback signal affects the loop filter at all time instead of just at the sampling instants, so the timing error of the feedback signal transition edges caused by the DAC clock jitter is equivalent to the feedback signal error itself. Because the DAC error also appears at the modulator output without any attenuation, the DAC clock jitter is one of the most important issues which should be considered while designing the wideband CT ΔΣ modulator.

### *4.3.1. Jitter Noise in NRZ DAC*

To ease the analysis of the effect of the DAC clock jitter on the CT modulator, the timing error of the DAC output signal transition edges is modeled as an equivalent error in the signal magnitude. Fig. 4.13 shows this equivalence for the NRZ DAC pulse.

If the timing error of the signal transition edge between the $(n\text{-}1)^{th}$ and the $n^{th}$ clock period is $\Delta t(n)$, then the equivalent magnitude error $e_{j,NRZ}(n)$ for the $n^{th}$ DAC pulse with ideal timing is given by

$$e_{j,NRZ}(n) = \frac{\Delta A(n)}{T_s} = \big(y(n) - y(n-1)\big) \cdot \frac{\Delta t(n)}{T_s} \tag{4.9}$$

where $\Delta A(n)$ is the area difference between the ideal waveform and the jittered waveform during the $n^{th}$ clock period, and $y(n)$ is the modulator output.

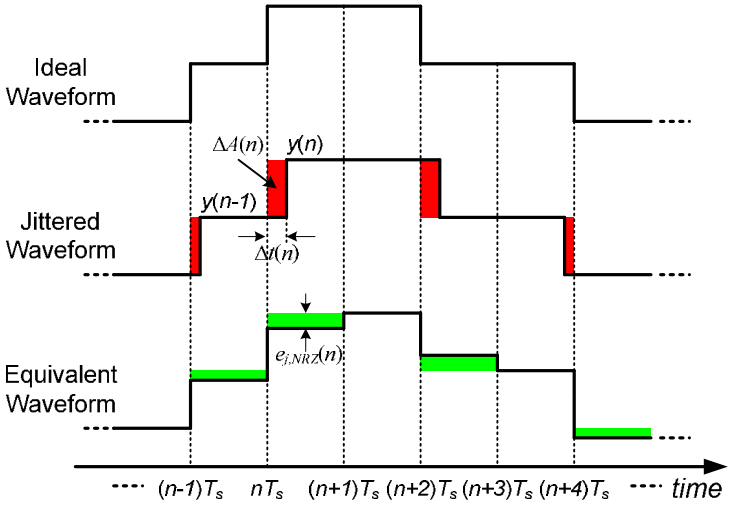



Figure 4.13: Model of the jitter-induced noise for NRZ DAC

Assuming the modulator output $y(n)$ and the clock jitter $\Delta t(n)$ are statistically independent on each other and the clock jitter is a white noise process, the autocorrelation of $e_{j,NRZ}(n)$, namely $r_{ej,NRZ}(l)$, is given by

$$r_{e_{j,NRZ}}(l) = \frac{1}{T_s^2}\sigma_{jitter}^2 \cdot \sigma_{dy}^2 \cdot \delta(l) \tag{4.10}$$

where $\sigma_{jitter}^2$ and $\sigma_{dy}^2$ are the variances of the clock jitter and the signal $dy(n) = y(n) - y(n\text{-}1)$, respectively. So, the total jitter-induced noise power in the band of interest is

$$\sigma_{e_{j,NRZ}(inband)}^2 = \frac{1}{OSR}\left(\frac{\sigma_{jitter}}{T_s}\right)^2 \cdot \sigma_{dy}^2 = 4 \cdot OSR \cdot BW^2 \cdot \sigma_{jitter}^2 \cdot \sigma_{dy}^2 \tag{4.11}$$

where BW stands for the signal bandwidth.

To calculate the variance of $dy(n)$, it should be expressed as shown below

$$\begin{aligned} dy(n) &= y(n) - y(n-1) = u(n) - u(n-1) + ntf(n) * (q(n) - q(n-1)) \\ &= du(n) - ntf(n) * dq(n) \end{aligned} \tag{4.12}$$

where $u(n)$ and $q(n)$ stand for the modulator input and the additive quantizer noise, and the signal transfer function is assumed to be one.

For a sinusoidal input, $u(n) = A \cdot sin(\omega_{sig}(nT_s))$, we have the following expression for the difference between the adjacent input samples $du(n)$:

$$\begin{aligned} du(n) = u(n) - u(n-1) &= 2A\cos\left(\omega_{sig}(2n-1)\frac{T_s}{2}\right)\sin\left(\omega_{sig}\frac{T_s}{2}\right) \\ &= 2A\sin\left(\frac{\pi}{2OSR_{sig}}\right)\cos\left(\omega_{sig}\frac{(2n-1)T_s}{2}\right) \end{aligned} \tag{4.13}$$

where $OSR_{sig}$ is defined as $OSR_{sig} = f_s/(2f_{sig})$, which is larger than or equal to the OSR for an in-band signal.

If the oversampling ratio is high and hence $\pi/(2OSR_{sig})$ is much less than 1, then the approximation of $sin(x) \approx x$ can be applied to the sinusoidal item in the above equation, leading to:

$$du(n) = \frac{A\pi}{OSR_{sig}} \cos\left( \omega_{sig} \frac{(2n-1)T_s}{2} \right) \tag{4.14}$$

So, the power of the signal-related component of the $d_y(n)$ is given by

$$P_1 = \frac{(\pi A)^2}{2OSR_{sig}^2} \tag{4.15}$$

To get the power of the quantization-noise-related component of the $dy(n)$, we need to calculate the autocorrelation of $dq(n)$, namely $r_{dq}(l)$:

$$r_{dq}(l) = E[dq(n) \cdot dq(n-l)] = E[(q(n) - q(n-1)) \cdot (q(n-l) - q(n-l-1))]$$

$$= r_q(l) - r_q(l+1) - r_q(l-1) + r_q(l) = 2r_q(l) - r_q(l+1) - r_q(l-1) \tag{4.16}$$

So, the power spectral density of $dq(n)$ can be calculated by applying the Fourier Transform to the $r_{dq}(l)$:

$$R_{dq}(e^{j\omega}) = F[r_{dq}(l)] = 2R_q(e^{j\omega}) - R_q(e^{j\omega})(e^{j\omega} + e^{-j\omega}) = 2R_q(e^{j\omega})(1 - \cos\omega) \tag{4.17}$$

where $\omega$ is the normalized angular frequency.

So, the power of the quantization-noise-related component of the $dy(n)$ is given by

$$P_2 = \frac{1}{2\pi} \int_{-\pi}^{\pi} \left[ \left| NTF(e^{j\omega}) \right|^2 \cdot R_{dq}(e^{j\omega}) \right] d\omega$$

$$= \frac{1}{\pi} \int_{-\pi}^{\pi} \left[ \left| NTF(e^{j\omega}) \right|^2 \cdot R_q(e^{j\omega}) \cdot (1 - \cos(\omega)) \right] d\omega \tag{4.18}$$

Assuming the quantization noise is a white noise process with samples uniformly distributed between $-V_{LSB}/2$ and $+V_{LSB}/2$ ($V_{LSB}$ is defined in section 2.1), and not related to the modulator input $u$, the total power of $dy(n)$ is simply equal to the sum of $P_1$ and $P_2$:

$$\sigma_{dy}^2 = P_1 + P_2 = \frac{\pi^2}{2} \left( \frac{A^2}{OSR_{sig}^2} \right) + \frac{\Delta^2}{12\pi} \int_{-\pi}^{\pi} \left[ \left| NTF(e^{j\omega}) \right|^2 \cdot (1 - \cos(\omega)) \right] d\omega \tag{4.19}$$

where $\Delta$ is the quantization step which is the same as $V_{LSB}$ in a unit-gain quanitzer.

If the following notation is used:

$$\sigma_H^2 = \frac{1}{\pi}\int_{-\pi}^{\pi}\left[\left|NTF(e^{j\omega})\right|^2 \cdot (1-\cos(\omega))\right]d\omega = \frac{1}{2\pi}\int_{-\pi}^{\pi}\left|NTF(e^{j\omega})(1-e^{-j\omega})\right|^2 d\omega \quad (4.20)$$

then Eq. 4.19 can be simplified as

$$\sigma_{dy}^2 = P_1 + P_2 = \frac{\pi^2}{2}\left(\frac{A^2}{OSR_{sig}^2}\right) + \frac{\Delta^2\sigma_H^2}{12} = \frac{\pi^2}{2}\left(\frac{A^2}{OSR_{sig}^2}\right) + \frac{V_{ref}^2\sigma_H^2}{3(M-1)^2} \quad (4.21)$$

where $M$ is the number of the quantizer level and $V_{ref}$ is half of the quantizer full scale.

Substituting the $\sigma_{dy}^2$ in Eq. 4.11 with the above expression, the in-band jitter-induced noise power can be written as

$$\sigma_{e_{j,NRZ}(inband)}^2 = 4 \cdot OSR \cdot BW^2 \cdot \sigma_{jitter}^2 \cdot \left(\frac{\pi^2}{2}\left(\frac{A^2}{OSR_{sig}^2}\right) + \frac{V_{ref}^2\sigma_H^2}{3(M-1)^2}\right)$$

$$\leq 2\pi^2 \frac{A^2 \cdot BW^2 \cdot \sigma_{jitter}^2}{OSR} + \frac{4OSR \cdot V_{ref}^2 \cdot \sigma_H^2 \cdot BW^2 \cdot \sigma_{jitter}^2}{3(M-1)^2} \quad (4.22)$$

where the condition of $OSR \leq OSR_{sig}$ for in-band signal was used.

If the first item in the right side of Eq. 4.22 is dominant, then the signal-to-jitter-noise ratio (SJNR) is given by

$$SJNR_{P_1} = \frac{OSR}{4\pi^2 \cdot BW^2 \cdot \sigma_{jitter}^2} \quad (4.23)$$

From this equation, it is obvious that the $SJNR_{P1}$ can be improved only by increasing the oversampling ratio for a given modulator and clock source.

To analyze the second item of the jitter-induced noise, which is related to the quantization noise, it is more convenient to normalize the input signal amplitude to the $V_{ref}$ as $A = A_n V_{ref}$. The SJNR for this item is given by:

$$SJNR_{P_2} = \frac{3A_n^2(M-1)^2}{8OSR \cdot \sigma_H^2 \cdot BW^2 \cdot \sigma_{jitter}^2} \quad (4.24)$$

From this equation, we can see that four parameters can be used to improve the $SJNR_{P2}$ for a given modulator bandwidth and clock source. First, unlike the $SJNR_{P1}$ which isn't related to the input signal amplitude, the $SJNR_{P2}$ can be improved if the maximum stable input is increased. Second, if more quantizer levels and hence smaller quantization step are used, a better $SJNR_{P2}$ results. Third, if $\sigma_H$, the RMS value of the transfer function $NTF(z)(1-z^{-1})$, can be decreased by reducing the aggressiveness of the noise shaping or optimizing the shape of the NTF [36], then the $SJNR_{P2}$ can be improved. The last parameter is OSR. It is interesting that the $SJNR_{P2}$ is inversely to the oversampling ratio. So, if we want to optimize the total jitter-induced noise power by changing the OSR, it is necessary to know first which part of the noise power is dominant.

### *4.3.2. Jitter Noise in RZ DAC*

The same method can be used to analyze the jitter-induced noise in a CT ΔΣ modulator which employs return-to-zero DAC waveform (see Fig. 4.14)

To calculate the equivalent additive magnitude error sequence $e_{j,RZ}(n)$ for the RZ DAC pulse, the ideal NRZ timing is used in the equivalent waveform. So, the $e_{j,RZ}(n)$ is given by

$$e_{j,RZ}(n) = \frac{\Delta A(n)}{T_s} = y(n) \cdot \left( \frac{T_s}{T_0} \right) \frac{\left( \Delta t_r(n) + \Delta t_f(n) \right)}{T_s} \tag{4.25}$$

where $T_0$ is the duty cycle of the RZ pulse. The factor of $T_S/T_0$ is introduced to keep the full scale of the RZ DAC the same as that of the NRZ one. $\Delta t_r(n)$ and $\Delta t_f(n)$ refer to the random timing errors of the rising and falling edges of the $n^{th}$ DAC pulse.

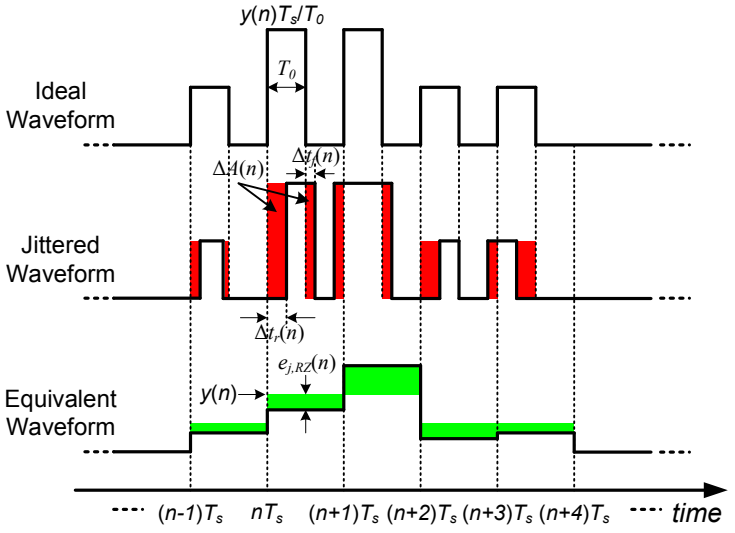



Figure 4.14: Model of the jitter-induced noise for RZ DAC

Assuming that the modulator output and the clock jitter are statistically independent and the clock jitter is a white noise process, the autocorrelation of $e_{j,RZ}(n)$, namely $r_{ej,RZ}(l)$, is given by:

$$r_{e_{j,RZ}}(l) = \frac{2}{T_0^2}\sigma_{jitter}^2 \cdot \sigma_y^2 \cdot \delta(l) \tag{4.26}$$

where $\sigma_y^2$ is the variance of $y(n)$. So, the total jitter-induced noise power in the band of interest is given by:

$$\sigma_{e_{j,RZ}(inband)}^2 = \frac{2}{OSR}\left(\frac{\sigma_{jitter}}{T_0}\right)^2 \cdot \sigma_y^2 \tag{4.27}$$

Comparing the above result with that in Eq. 4.11, the SJNR improvement of the NRZ DAC pulse over RZ one is

$$SJNR_{NRZ-RZ}(dB) = 10\log_{10}\left(\frac{\sigma_{e_{j,RZ}(inband)}}{\sigma_{e_{j,NRZ}(inband)}}\right) = 10\log_{10}\left(2\cdot\left(\frac{T_s}{T_0}\right)^2 \cdot \frac{\sigma_y^2}{\sigma_{dy}^2}\right) \tag{4.28}$$

For example, in a 1-bit CT ΔΣ modulator, if $T_0 = 0.5T_s$ is assumed, the SJNR improvement of NRZ over RZ is about 6 dB. If a multi-level quantizer is used, the ratio of $\sigma_y^2/\sigma_{dy}^2$ can be even larger, and hence this SJNR improvement can be more significant.

## 4.4. Element Mismatch Effects in a Multi-Bit DAC

In a wideband ΔΣ modulator, the oversampling ratio is usually limited by the circuit speed and power consumption. At the same time, the order and the aggressiveness of the noise shaping are also limited by the stability issue. So, in order to decrease the in-band noise power, an effective way is to use a multi-bit quantizer to reduce the quantization noise in the modulator. In a CT ΔΣ modulator, an extra bonus of using multi-bit quantizer is the reduction of the jitter sensitivity.

However, the use of a multi-bit quantizer leads to a multi-bit DAC in the feedback path. The nonlinearity of this DAC severely limits the performance of the modulator. The nonlinearity can be seen as an additive error $e(k)$ to the ideal output of the DAC (see Fig. 4.15). The transfer function from the DAC error to the modulator output, the error transfer function (ETF), is given by

$$ETF = \frac{L_1}{1 - L_1} \tag{4.29}$$

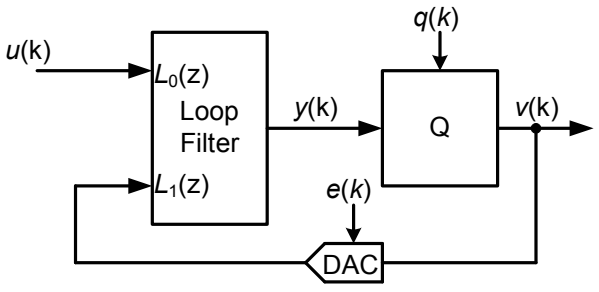



Figure 4.15: DAC error in the ΔΣ modulator

Because the loop filter gain is very high in the signal band, the in-band gain of the ETF is almost equal to one, which means the power of the DAC error will be directly added to the modulator output without much attenuation. So, the linearity of the modulator cannot be higher than that of the DAC.

A very common DAC structure is built from unit elements, in which the nonlinearity of the DAC is mainly caused by the element mismatch. For this DAC structure, an extensively used technique to reduce the DAC error is dynamic element matching (DEM). Using DEM, the bits in the thermometer-code output of the quantizer are rearranged following certain rules by a digital process before they are applied to the DAC. This rearrangement does not affect the data value, but it changes the priority on the selecting of the unit elements in the DAC, which can result in two effects. First, the DAC error becomes uncorrelated with the DAC input, eliminating the signal dependent tones that will appear in the modulator output otherwise. Second, the so-called mismatch shaping will move the error power from low frequencies to high frequencies. The DEM has many versions of implementation [37 ~ 39], using different rules for bit rearranging. Some of them have both effects but some only have one.

As an example, the scheme of the data-weighted-averaging (DWA), a widely used first-order mismatch shaping algorithm, is illustrated in a 9-level DAC shown in the Fig. 4.16.

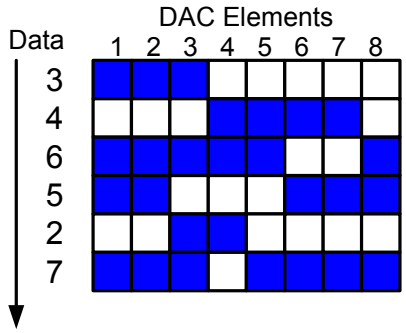



Figure 4.16: Illustration of DWA

The dark grid cell represent the currently used DAC elements while the white cells indicate those not used. The number of the elements that would be used to generate the new output is equal to the current input data value, and the elements are selected in a circular way such that every element has the same probability of usage. Hence, the mismatch between those unit elements can quickly average out and the DAC error is effectively first-order shaped.

However, the effect of the mismatch shaping depends on the OSR. In the wideband applications, where the OSR may have to be pushed down to as low as 4, the error shaping from the DEM is too weak to satisfy the high resolution requirements. As for the CT modulator, the delay caused by the DEM logic will increase the excess loop delay and hence affect the performance and even the stability of the modulator (see section 4.2.1).

Another technique to tackle DAC mismatch errors, which has been used in monolithic high-resolution current steering DACs, is self-calibration [40]. The basic idea of this technique is to use a reference current as a standard to trim each current source. The calibration is done circularly so that the calibration is continuous.

# CHAPTER 5. SYSTEM LEVEL DESIGN

In this chapter, the system level design of a prototype CT ΔΣ modulator for next generation wireless applications is presented in detail, which includes the determination of the system level parameters, the optimization of the modulator architecture, the noise budget, and the system level simulations with non-idealities.

## 5.1. System Level Parameters

The first step to design a ΔΣ modulator is to determine the most important system level parameters based on the modulator specifications and the semiconductor technology which will be used to realize this modulator. In our case, the target is to successfully design a low-power CT ΔΣ modulator to reach 60 dB dynamic range (DR) within a 25 MHz bandwidth (BW) in a 0.18 $\mu$m mixed-signal CMOS process.

However, for a wideband CT ΔΣ modulator, another important specification, the clock jitter sensitivity, will significantly affect the selection of the system level parameters. Although many advanced clock generators based on LC voltage-controlled oscillators (VCOs) can achieve subpicosecond jitter performance [41 ~ 44], it is not practical to integrate them on the same chip in our case. It is reasonable to assume that the prototype modulator will be evaluated with a clock signal generated by an instrument, e.g., the HP 8665A, so the jitter value of the final clock signal entering the modulator is determined by the quality of the instrument signal and the noise introduced by all circuits on the clock path, either off-chip or on-chip. In our case, the RMS value of the target jitter tolerance is 5 ps.

The system-level parameters include the oversampling ratio (OSR), the loop filter order ($L$), the number of the quantizer level ($M$) and the aggressiveness of the noise shaping

which is determined by the maximum gain of the noise transfer function ($NTF_{max}$) in the ΔΣ toolbox. The sampling rate of the CT ΔΣ modulator is limited by the device speed in a given technology. For the 0.18 $\mu$m CMOS process, 500 MHz is a reasonable upper limitation for the sampling rate considering the gain-bandwidth requirement of the opamp with acceptable power consumption, so the OSR should be less than 10.

The power consumption of the quantizer increases proportionally to the number of quantization levels, so, for a low-power design, the number of the quantization levels should be minimized. On the other hand, according to Eq. 4.22, the jitter-induced noise power can be reduced by increasing the number of the quantizer level. So, a trade-off between the power consumption and the jitter sensitivity has to be made while determining the number of the qantizer levels $M$.

Increasing the loop filter order is cheap, but the loop stability issue limits the loop order. Usually, the order should be no more than 5. The aggressiveness of the noise shaping is also limited by the stability issue. In addition, as we analyzed in section 4.3.1, the RMS value of the transfer function $NTF(z)(1-z^{-1})$, which is proportional to the aggressiveness of the noise shaping, will affect the jitter-induced noise power. So, the $NTF_{max}$ is also limited by the jitter issue.

In order to realize a low-power design, the in-band quantization noise should only occupy a very small portion of the total noise, e.g., one-tenth. In addition, the real input amplitude cannot reach the peak input value. The finite RC time constant accuracy will also reduce the effectiveness of the noise shaping as shown in section 4.1.2. So, the target peak signal-to-quantization-noise ratio (SQNR) should be larger than 75 dB. As for the jitter-induced noise, the budget of 40% total noise is a reasonable value, which means the signal-to-jitter-noise ratio (SJNR) should be at least 66 dB. Based on these initial requirements, a large

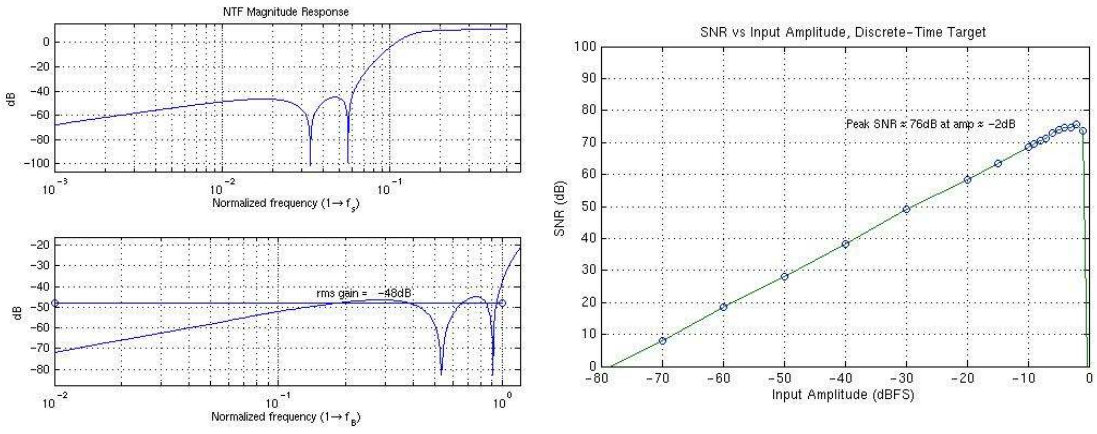
amount of simulations were performed by using the toolbox to explore the parameter space. Table 5.1 shows three the most efficient combinations in terms of power consumption.

Table 5.1: Three combinations of the system level parameters

| OSR | Order | Number of Quantizer Levels | $NTF_{max}$ | SJNR (dB) | Peak Input (dBFS) | Peak SQNR (dB) |
|---|---|---|---|---|---|---|
| 6 | 5 | 17 | 5.5 | 66.9 | -2 | 76 |
| 8 | 5 | 11 | 3.5 | 66.4 | -2 | 76 |
| 10 | 5 | 9 | 2.5 | 66.6 | -1 | 75 |

In our wideband modulator, the allowable $NTF_{max}$ is limited by the jitter sensitivity instead of the stability issue for a given number of quantizer levels, so the loop filter order in all of three choices can be as high as five without showing instability.

Which one is the best choice in terms of power consumption? Based on intuitive analysis, the second combination may be the best one. Fig. 5.1 shows the magnitude response of the NTF as well as the Input-SQNR relationship of the DT target with those system level parameters.




(a) (b)

Figure 5.1: (a) NTF magnitude response; (b) Input-SQNR relationship of the DT target

## 5.2. Architecture of the Loop Filter

After getting the target noise transfer function, a CT loop filter can be synthesized for a given architecture by using the method described in section 3.2, so the second step of the system level design is to determine the structure of the loop filer.

Two popular architectures, feedback and feed-forward, are widely used in the ΔΣ modulators. Both of them have their own advantages and disadvantages. The advantages of the feedback structure include the low-pass characteristics of the STF and that no large adder is needed before the quantizer. However, in terms of low-power design, the feed-forward one is preferred because the output swing of the first stage in the feed-forward loop filer is much smaller than that of the feedback counterpart, which allows a bigger first stage gain and hence lower performance requirements on the following stages. Fig. 5.2 shows the comparison between the output swings of the first stages in those two architectures realizing the same noise shaping. It can be seen that with the same first stage gain, the swing in the feed-forward structure is only 1/10 that in the feedback one.

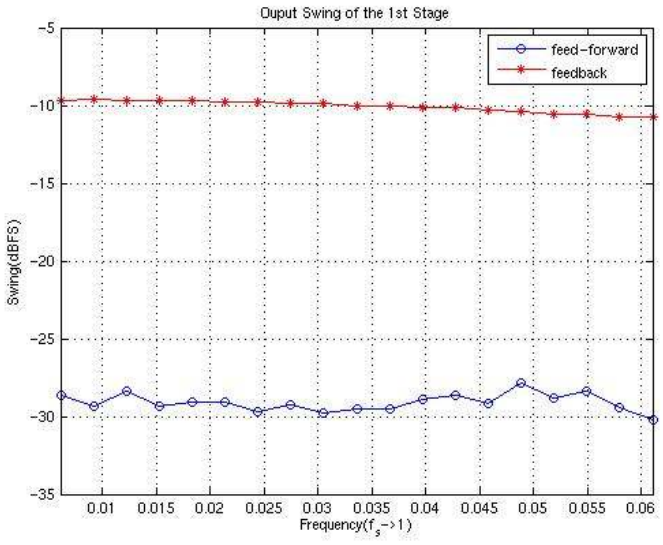



Figure 5.2: The 1st-stage output swings of the feed-forward and feedback loop filters

However, the feed-forward architecture has two drawbacks corresponding to those two advantages of the feedback counterpart. First, as we mentioned in section 3.3, there is an out-of-band peaking in the signal transfer function of the feed-forward loop filter, which equivalently reduces the dynamic range of the modulator in the wireless applications where a lot of big out-of-band interferers exist. Second, a multi-input adder is needed to sum all feed-forward branches before the quantizer. Usually, two kinds of the adders, passive and active, can be used. The passive adder is sensitive to the input parasitic capacitance of the quantizer. In addition, in a CT modulator, the passive adder makes the $RC/G_mC$ time constant tuning very complicated, so the active adder is preferred. However, this large active adder will become the speed bottleneck of the whole loop as well as consume much power.

The system level simulations show that, in a CT $\Delta\Sigma$ modulator, the loop stability is more sensitive to the accuracy of the first several samples of the loop impulse response than to that of the other samples. In other words, the bandwidth of the low order loops, which contribute more to those first several samples than the high order loops, are more critical for the loop stability. Fig. 5.3 shows this interesting phenomenon in a $5^{th}$-order feed-forward CT modulator. From this simulation result, it can be seen that the allowable excess delay which is introduced by the limited loop bandwidth is much bigger in high order loops than in low order ones.

In a traditional feed-forward structure, the first-order loop consists of the first integrator which is the most accurate one in the loop filter because any error introduced by it will appear at the modulator output without noise shaping. Considering the loop stability issue, this “golden” integrator has to be not only highly accurate but also highly fast so the power consumption of it would be very high. If the first integrator is moved out of the first-order

loop, the bandwidth requirement and hence the power consumption of this integrator can be reduced.

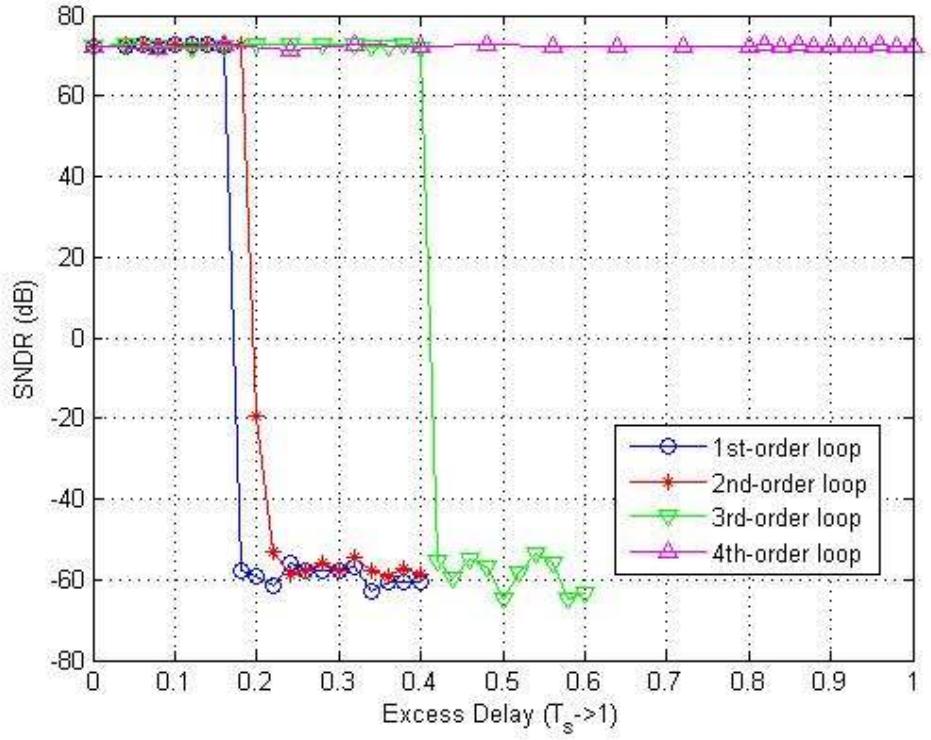



Figure 5.3: The effect of the excess delay in different order loops on the stability

An extra feedback DAC, DAC2, is introduced to not only divide the bigger adder into two smaller ones but also to move the first integrator out of the first-order loop (see Fig. 5.4).

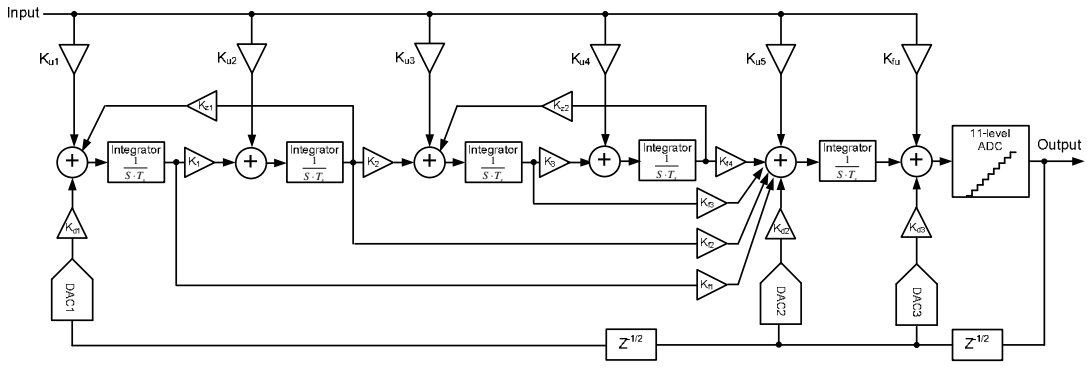



Figure 5.4: The architecture of the prototype CT ΔΣ modulator

Now, the first-order loop is composed of the last integrator which doesn't need to be very accurate. As we mentioned in section 4.2.1, the direct feedback path which is composed of the DAC3 is used to compensate the impulse response sample at the time instant $T_S$, which allows us to insert an explicit delay in the main loop to absorb the varying excess loop delay.

It should be mentioned here that the feedback signal of the 1st-order loop is delayed by only half clock instead of a full clock for two reasons. First, as shown in Fig. 5.5, if this feedback signal is also delayed by a full clock (sloping dotted-line), then the sample of the impulse response at $T_s$ has to be completely contributed by the zero-order loop (rectangular dotted-line), which makes the direct feedback coefficient and hence the DAC current very large. Second, the half clock delay will make the contribution of the 1st-order loop to the impulse response sample at $2T_s$ accurate even with the excess loop delay caused by the DAC switching and finite integrator GBW. Although using half clock delay in the 1st-order loop will introduce the error of impulse response at $T_s$ if there is any excess delay in this loop, this error can be compensated by adjusting the feedback timing or the bias current of the DAC3.

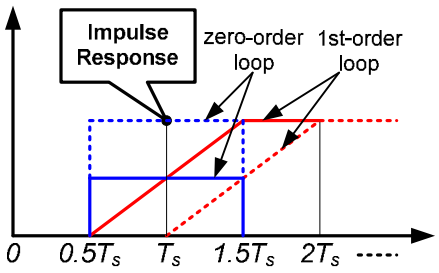



Figure 5.5: Impulse response of the zero-order and 1st-order loops

In addition, to remove the out-of-band peaking which is caused by the zeros in the transfer function $L_0(s)$, five extra feed-in branches are introduced to change those zeros to be equal to the poles of the $NTF(z)$ in terms of $z = e^{sT_s}$, which results in a unit-magnitude signal transfer function except at the frequencies around the multiples of the sampling rate, where an

attenuation of about 60 dB is provided to realize the inherent anti-aliasing characteristics of the CT ΔΣ modulator (see Fig.5.6).

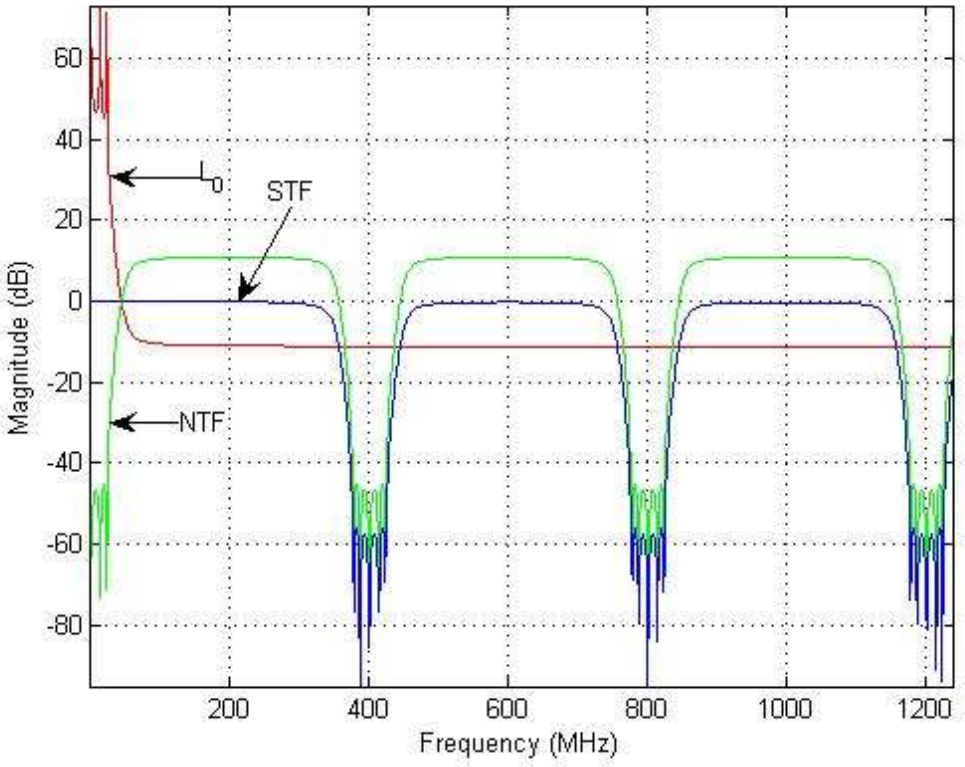



Figure 5.6: Magnitude responses of $L_0(s)$, $NTF(z)$ and $STF(s)$

## 5.3. Noise Budget

After determining the architecture of the modulator, it is necessary to translate the dynamic range requirement into the noise specifications of those individual circuit blocks, e.g., the integrators, the quantizer, and the feedback DACs, which is called noise budget.

To obtain a 10-bit dynamic range, we set the target signal-to-noise ratio (SNR) to be 62 dB with -3 dBFS input, which means the power of the total in-band noise should be lower than -65 dBFS. The system level simulation shows that, with a 5% RC time constant deviation, the signal-to-quantization-noise ratio (SQNR) is about 73 dB for -3 dBFS input. In other

words, the in-band quantization noise is about 9% of the total noise power. In addition, the simulation with 25MHz input signal shows the in-band jitter-induced noise is about -69 dBFS which means about 39% the total noise is caused by the DAC clock jitter.

To determine the specifications of the quantizer offset and DAC mismatch, a statistical simulation should be performed. The simulation results show that if the RMS value of the comparator input offset $\sigma_{off}$ and the relative mismatch between the unit resistors in the resistor string $\sigma_{Rmis}$ are assumed to be $4\%V_{ref}$ and 0.2%, respectively, then the quantizer will introduce extra 10% noise (error) with 90% yield.

Also, the statistical simulation shows that, without using any dynamic element matching schemes, the 0.1% DAC element mismatch will use up 12% of the noise budget with 90% yield. If this relative mismatch increases to 0.2%, 47% noise budget has to be assigned to the DAC error for the same yield.

Another import noise source is the thermal noise which is mainly contributed by the input resistors of the first integrator and the current DAC in the main feedback loop. However, the thermal noise in a CT ΔΣ modulator is not as significant as in the DT counterpart where the thermal noise, i.e., the $kT/C$ noise, is usually dominant in the noise budget. Based on some calculations, we set the percentage of the thermal noise in the total noise to be 20%, which means the SNR should be at least 69 dB with a -3 dBFS input while only considering the thermal noise. Due to the gain of the first stage, the input-referred noise from following stages is greatly attenuated. If it is assumed that 80% the total thermal noise is from the first stage, the power of the in-band thermal noise introduced by this stage should be as low as -73 dBFS.

As a conclusion, the detailed noise budget highlighted by the gray shade is given out in Table 5.2.

Table 5.2: Noise budget of the modulator

| Noise + Distortion Sources | Noise Budget | Simulation Results (SNR) | Simulation Conditions |
|---|---|---|---|
| Quantization Noise | 9% | 72.6 dB | TC* = 1.05, Input = -3 dBFS |
| Quantization Noise + Quantizer Error | 19%*(10%)<br>13% (4%) | 69.3 dB @ 90%<br>70.8 dB @ 50% | TC = 1.05, Input = -3 dBFS, $F_{in}$ = 2.44 MHz, $\sigma_{off}$ = 4%$V_{ref}$, $\sigma_{Rmis}$ = 0.2% |
| Quantization Noise + QNoise-Induced Jitter | 35% (26%) | 66.6 dB | $F_{in}$ = 150 kHz, TC = 1.05, Input = -3 dBFS, $\sigma_{jitter}$ = 5ps |
| Quantization Noise + Total Jitter | 48% (39%) | 65.2 dB | $F_{in}$ = 25 MHz, TC = 1.05, Input = -3 dBFS, $\sigma_{jitter}$ = 5ps |
| DAC Mismatch Error + Quantization Noise | 21% (12%)<br>13% (4%) | 68.7 dB @ 90%<br>70.9 dB @ 50% | $F_{in}$ = 2.44 MHz, TC = 1.05, Input = -3 dBFS, $\sigma_{DAC}$ = 0.1% |
| Thermal Noise | 20% | | |
| Others | 10% | | |

* The numbers outside the parenthesis in the second column refer to the total noise
TC refers to the normalized RC time constant

## 5.4. System Level Simulation

To see the whole effect of those non-idealities which were analyzed in the previous sections, a system level simulation was performed on the prototype CT ΔΣ modulator. Fig. 5.7 shows the output spectrum in this system level simulation of the modulator, which includes all the non-idealities except the thermal noise. As a comparison, the ideal noise transfer function is also plotted in this figure.

From this output spectrum, it can be seen that the total in-band noise and distortion power is a little lower than the summation of those individual noise sources given in Table 5.2, which is about 70% the total noise. This difference is caused by the signal-related component of the jitter-induced noise which is proportional to the input signal frequency.

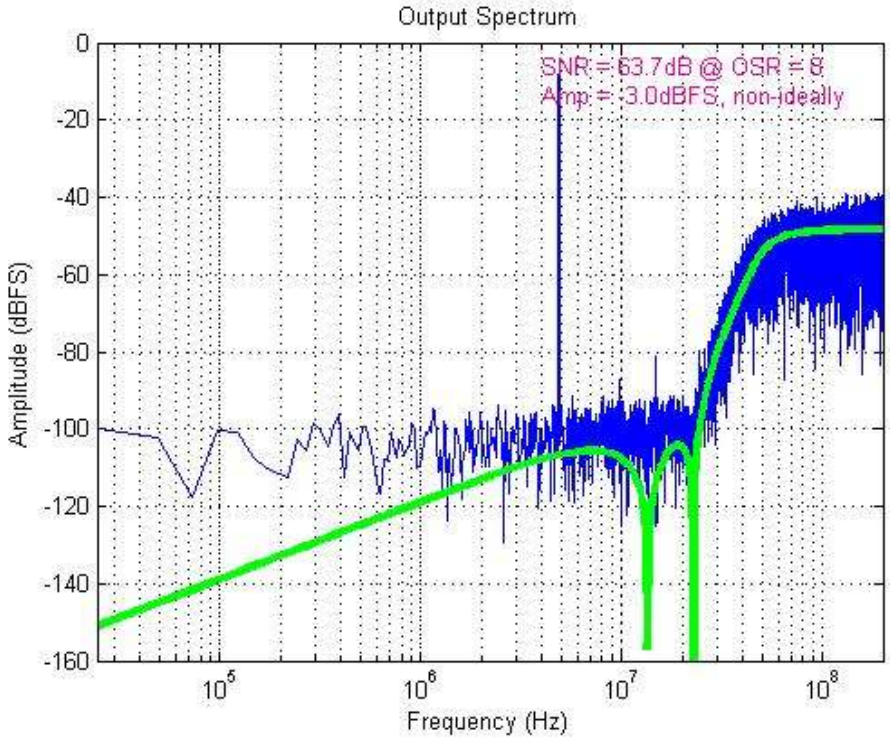



Figure 5.7: Output spectrum of the system level simulation

# CHAPTER 6. CIRCUIT AND LAYOUT LEVEL DESIGN

In this chapter, the design of the circuit blocks which are used in this wideband CT ΔΣ modulator is presented in detail. After that, some layout techniques which are suitable for high speed circuits are described, and the modulator is realized with a 0.18 $\mu$m CMOS technology.

## 6.1. Loop Filter

In chapter 5, the architecture and those branch coefficients of the modulator were determined. Now, it is necessary to translate these coefficients into the real values of the resistors and capacitors. As mentioned in section 4.1, the RC integrators have better linearity and larger signal swing than the $G_mC$ counterparts. In addition, in our modulator, several extra feed-in branches are added to cancel the out-of-band peaking in the STF so if $G_mC$ integrators are used, more active components ($G_m$ cells) are needed to realize those branches. On the other hand, if the RC integrators are used, those branches can be as simple as just resistors, and hence the power consumption is expected to be lower.

Fig. 6.1 shows the top level circuit diagram of the modulator whose loop filter is composed of active RC integrators.

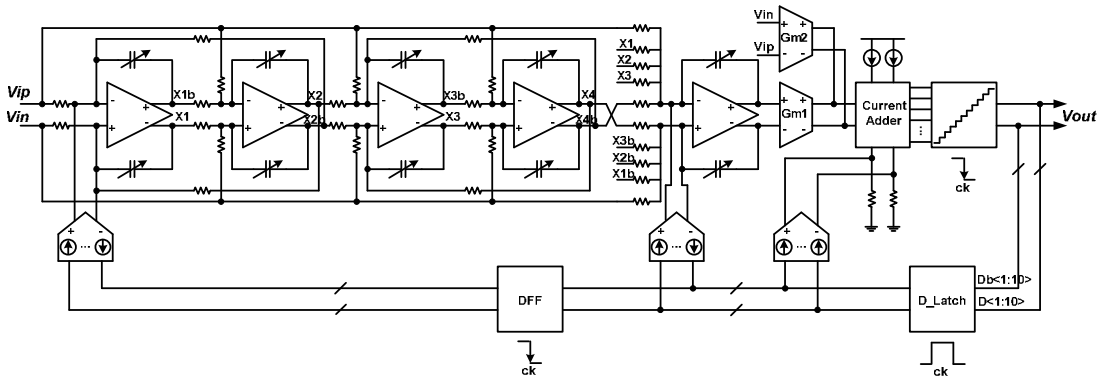



Figure 6.1: Top level circuit diagram of the CT ΔΣ modulator

From the above diagram, it can be seen that the integration capacitor in each stage is actually a capacitor array whose capacitance is tunable. In order to improve the speed of the fifth integrator, it was not used to compose the second resonator as in a traditional 5$^{th}$-order loop filter, so the first stage had to be a resonator instead of an integrator. The output of the loop filter is added to the direct feed-in and feedback signals through a fast current adder whose outputs are the differences between the summation signal and the threshold voltages. The quantizer outputs are sampled again by the D latches half clock later than the quantizer sampling instant, which allows the quantizer to make decision in as long as half clock period. The outputs of the D latches are fed back to the DACs in the zero-order and 1$^{st}$-order loops, and also sampled by the D flip-flops which provide the feedback signals to the main DAC.

## 6.2. Front-End Circuits

As mentioned before, the noise performance of the front-end circuits that include the first integrator and the main feedback DAC is the most important to the modulator, because any error introduced by those circuit blocks will appear at the modulator output without noise shaping. The diagram of the front-end circuits is shown in Fig. 6.2.

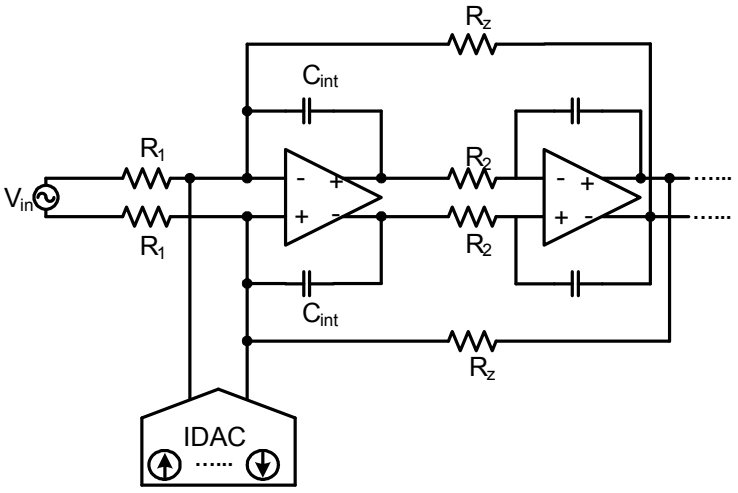



Figure 6.2: Diagram of the front-end circuits

### *6.2.1. Noise Analysis*

The input-referred noise power spectral density (PSD) of $R_1$ is simply expressed as $V_{R_1}^2(f) = 4kTR_1$, but as for $R_z$, the input-referred noise PSD should be calculated as

$$V_{R_z}^2(f) = \frac{4kTR_z \cdot \left| \frac{1}{j \cdot 2\pi f \cdot R_z C_{\text{int}}} \right|^2}{\left| \frac{1}{j \cdot 2\pi f \cdot R_1 C_{\text{int}}} \right|^2} = 4kTR_z \left( \frac{R_1}{R_z} \right)^2 = 4kTR_1 \left( \frac{R_1}{R_z} \right) \tag{6.1}$$

The total input-inferred noise PSD of those two resistors in the differential circuit can be approximated as

$$V_R^2(f) = 8kTR_1 \left( 1 + \left( \frac{R_1}{R_z} \right) \right) = 8kTR_1 \left( 1 + \left( \frac{K_{z1}}{K_{u1}} \right) \right) \tag{6.2}$$

where $K_{u1}$ and $K_{z1}$ are the normalized coefficients of the input and resonator branches, defined in Fig. 5.4.

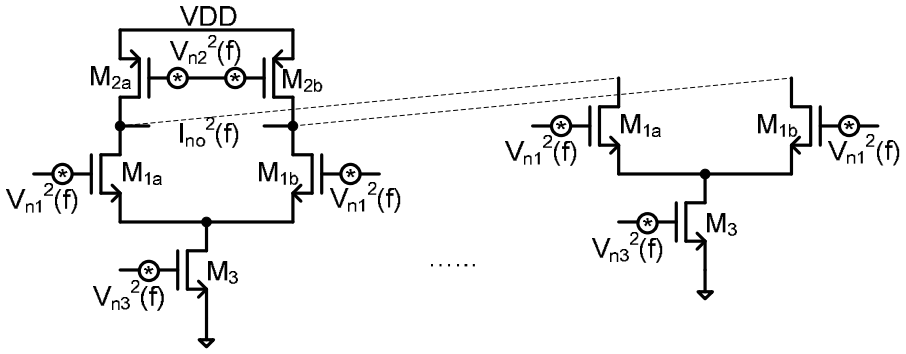



Figure 6.3: Noise sources in the simplified diagram of the current DAC

The second noise source is the current feedback DAC (IDAC). Fig. 6.3 gives out a simplified internal schematic of the IDAC, which consists of ten voltage-to-current (V-I) transformation units and two shared PMOS current sources. All input transistors as well as those transistors whose sources are connected with power or ground supplies should be

considered while calculating the noise PSD at the output of the IDAC. At one moment, one input transistor of the V-I unit is in the active region, and the other is in the cutoff region which does not contribute noise to the output. Because the active input transistor works as a cascode transistor, the noise from this transistor is also negligible. For the active branch which conducts the current, the output noise current PSD is given by:

$$I_{n1}^2(f) = V_{n2}^2(f) \cdot g_{m2}^2 + 10 \cdot V_{n3}^2(f) g_{m3}^2 \tag{6.3}$$

where $g_{m2}$ and $g_{m3}$ are the transconductances of the PMOS and NMOS current sources, respectively. As for the cutoff branch, the output noise current PSD is given by:

$$I_{n2}^2(f) = V_{n2}^2(f) \cdot g_{m2}^2 \tag{6.4}$$

So the total IDAC output noise current PSD is given by:

$$I_{no}^2(f) = 2V_{n2}^2(f) \cdot g_{m2}^2 + 10 \cdot V_{n3}^2(f) \cdot g_{m3}^2 \tag{6.5}$$

where

$$V_{n2}^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_{m2}} + \frac{K_{m2}}{W_{m2}L_{m2}C_{ox}f} \text{ and } V_{n3}^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_{m3}} + \frac{K_{m3}}{W_{m3}L_{m3}C_{ox}f} \tag{6.6}$$

In a broadband application like this design, the thermal noise is usually the dominant component compared with the flicker noise, so to simplify the calculation, the second term of the right side of the above two equations is neglected. After using Eq. 6.6 in Eq. 6.5, the output noise current PSD is given by

$$I_{no}^2(f) = \frac{16kT}{3} g_{m2} + \frac{80kT}{3} g_{m3} \tag{6.7}$$

If $I_t$ is used to represent the tail current of the V-I unit, then the current value of the PMOS current source is equal to $5I_t$. So, $g_{m2}$ and $g_{m3}$ can be expressed as

$$g_{m2} = \frac{2 \cdot (5I_t)}{V_{dsat_{m2}}} \text{ and } g_{m3} = \frac{2 \cdot I_t}{V_{dsat_{m3}}} \tag{6.8}$$

Using Eq. 6.8 in Eq. 6.7, we can get an expression for the output noise current PSD of the IDAC:

$$I_{no}^2(f) = \frac{32 I_{full-scale} kT}{3}\left(\frac{1}{V_{dsat_{m2}}} + \frac{1}{V_{dsat_{m3}}}\right) \tag{6.9}$$

where $I_{full\text{-}scale}$, defined as $I_{full\text{-}scale} = 5I_t$, is the feedback current when the absolute value of the DAC input $V_{DAC}$ is equal to the reference voltage of the quantizer, $V_{ref}$. $I_{full\text{-}scale}$ can be calculated as:

$$I_{full-scale} = \left(\frac{K_{d1}}{K_{u1}}\right)\frac{V_{ref}}{2R_1} \tag{6.10}$$

where $K_{d1}$ is the normalized coefficient of the main feedback branch defined in Fig. 5.4.

Assuming the saturation voltages of the PMOS and NMOS current source transistors are the same, which is $V_{dsatm2} = V_{dsatm3} = V_{dsat}$, the final expression of the noise current PSD at the IDAC output is given by:

$$I_{no}^2(f) = \frac{32kTV_{ref}}{3V_{dsat}R_1}\left(\frac{K_{d1}}{K_{u1}}\right) \tag{6.11}$$

So the input-referred noise voltage PSD of the IDAC is given by:

$$V_{DAC}^2(f) = I_{no}^2(f)\cdot R_1^2 = \frac{32kTV_{ref}R_1}{3V_{dsat}}\left(\frac{K_{d1}}{K_{u1}}\right) \tag{6.12}$$

The third noise source is the operational amplifier (opamp). To simplify the calculation, we only consider the noise from the input stage which is assumed to be realized with the simplest differential-pair (Fig. 6.4).

Due to the symmetry of the circuit, the noise of $M_3$ has little contribution to the output noise. As for the output noise caused by the input transistors and active loads, it can be

calculated with the similar method as that used to calculate the DAC noise, leading to the following equation:

$$V_{no}^2(f) = 2V_{n1}^2(f)\cdot(g_{m1}R_0)^2 + 2V_{n2}^2(f)\cdot(g_{m2}R_0)^2 \tag{6.13}$$

where $R_0$ is the output impedance of the differential-pair. The output noise in Eq. 6.13 can be represented as an equivalent input noise source, $V_{neq}^2(f)$, by dividing it with the square of the opamp gain ,$g_{m1}R_0$, which results in:

$$V_{neq}^2(f) = 2V_{n1}^2(f) + 2V_{n2}^2(f)\left(\frac{g_{m2}}{g_{m1}}\right)^2 \tag{6.14}$$

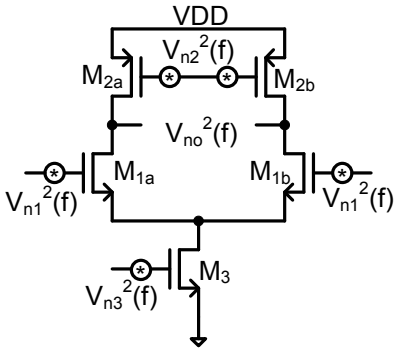



Figure 6.4: Noise sources in the differential-pair

Also, if only thermal noise is considered, which means $V_n^2(f) = 4kT\left(\frac{2}{3}\right)\frac{1}{g_m}$, then the equivalent input noise can be expressed as below:

$$V_{neq}^2(f) = \frac{16kT}{3}\left(\frac{1}{g_{m1}}\right) + \frac{16kT}{3}\left(\frac{g_{m2}}{g_{m1}}\right)^2\left(\frac{1}{g_{m2}}\right) \tag{6.15}$$

After referring this noise to the input of the modulator, we can get following input-referred noise PSD of the opamp:

$$V_{opamp}^2(f) = V_{neq}^2(f)\left|1 + j2\pi fR_1C_{\text{int}}\right|^2 \tag{6.16}$$

If only the band of interest is considered, which means $f \ll f_s$ with a normally high oversampling ratio, then the above equation can be simplified as below:

$$V_{opamp}^2(f) \approx V_{neq}^2(f) = \frac{16kT}{3g_{m1}}\left(1+\left(\frac{g_{m2}}{g_{m1}}\right)\right) \tag{6.17}$$

According to the noise budget shown in Table 5.2, the in-band thermal noise power of the front-end circuits $V^2_{nRMS}$ should be less than -73 dBFS, which leads to the following inequality:

$$10\log_{10}\left(\frac{V_{nRMS}^2}{V_{ref}^2/2}\right) = 10\log_{10}\left(\frac{2\int_0^{f_B}\left(V_R^2(f)+V_{DAC}^2(f)+V_{opamp}^2(f)\right)df}{V_{vef}^2}\right) \le -73 \tag{6.18}$$

Integrating the noise PSD given by Eq. 6.2 across the band of interest, the noise power in dBFS due to the input resistors is given by:

$$V_{nR(rms)}^2(dBFS) = 10\log_{10}\left(\frac{8kTR_1\left(1+\left(\frac{K_{z1}}{K_{u1}}\right)\right)f_B}{V_{ref}^2/2}\right) \tag{6.19}$$

The time constant of the first integrator, $R_1C_{int}$, should be equal to the $T_s/K_{u1}$. If we set the integration capacitor to be 2 pF, then the input resistance is 3.333 kΩ. In addition, using the parameters as $k$ = 1.38 × $10^{-23}$, $T$ = 300, $f_B$ = 25 MHz and $V_{ref}$ = 0.8 $V$, the resulting noise power will be about -80.2 dBFS, which means about 19% total thermal noise of the front-end circuits is introduced by the input and resonator resistors.

As for the thermal noise from the current DAC, we can calculate the noise power based on Eq. 6.12:

$$V_{nDAC(rms)}^2(dBFS) = 10\log_{10}\left(\frac{\int_0^{f_B} V_{DAC}^2(f)df}{V_{ref}^2/2}\right) = 10\log_{10}\left(\left(\frac{K_{d1}}{K_{u1}}\right)\frac{64kTR_1 f_B}{3V_{dsat}V_{ref}}\right) \quad (6.20)$$

If we set $V_{dsat}$ = 0.4 V, then the noise power is about -75.2 dBFS. In other words, about 60% the total thermal noise of the front-end circuits is introduced by the current DAC. The full scale current is about 157 $\mu$A, which leads to a total static current of 314 $\mu$A for the main DAC.

The same method can be used to calculate the noise from opamp based on Eq. 6.17. In our design, the transconductance of the input transistors and PMOS current sources are about 3.4 mS and 3.2 mS respectively, so the noise power in dBFS is given by:

$$V_{nopamp(rms)}^2(dBFS) = 10\log_{10}\left(\frac{16kT(1+(g_{m2}/g_{m1}))f_B}{3g_{m1}V_{ref}^2/2}\right) = -89.9 \text{ dBFS} \quad (6.21)$$

Above result means the thermal noise due to the opamp is only about 2% the total noise of the front-end circuits.

### *6.2.2. Opamp Design*

In a low voltage design, usually two kinds of opamp architectures are popular, two-stage and folded-cascode opamps. However, in a CT loop filter composed of the active RC integrators, the resistive load makes the folded-cascode opamp less efficient in terms of the DC gain than the two-stage opamp. So, in our design, all stages employ the latter one.

The first opamp should be biased such that it is never saturated during normal operation. The calculation in the previous section shows that the full-scale current of the feedback DAC is about 160 $\mu$A. During the start-up, it is conceivable that the DAC is tipped all the way to one side while the input is tipped all the way to the wrong side, so the opamp

should be able to handle 320 $\mu$A slew current without saturation. To give some extra margin, 400 ~ 500 $\mu$A/leg for the output stage should be sufficient. That means that the output stage of the opamp will need about 1 mA. In order to save power, a class-AB output stage may be used to provide such a big output current with much lower biasing current. There are many kinds of class-AB output stages. Due to the low voltage operation, only a class-AB biasing of inverting amplifier output stage can be used. A robust class-AB output stage which has excellent properties in CMOS technology is shown in Fig. 6.5 [45].

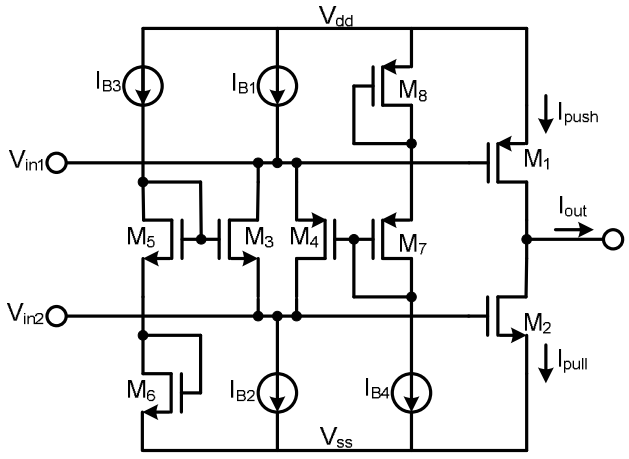



Figure 6.5: A large output swing class-AB CMOS output stage with CM transistor coupling

If we set the ratio of $(W/L)_P$ over $(W/L)_N$ equal to the ratio of the mobilities $\mu_N$ and $\mu_P$, then the transconductances of the NMOS and PMOS transistors are equal with equal currents. For simplicity, we can set all NMOS the same $(W/L)_N$ and all PMOS the same $(W/L)_P$, except for the output transistors which are scaled a factor of $\alpha$. If we choose the quiescent currents through the translinear loop transistors equal, we need the following relation between the biasing currents: $1/2I_{B1} = 1/2I_{B2} = I_{B3} = I_{B4} = I_B$. The quiescent current of the output stage, $I_q$, is equal to $\alpha I_B$. The input can be added through either input ports. When a positive input voltage is added through $V_{in1}$ point, the current through $M_4$ will increase by the same amount as the decrease of the current through $M_3$, which makes the voltages at the gates of the output

transistors increase the same amount. $I_{pull}$ becomes larger while $I_{push}$ becomes smaller. This procedure will continue until all $2I_B$ current flows through $M_4$ and $M_3$ is cut off, at which point $I_{push} = (2-\sqrt{2})^2 I_q$ and $I_{pull} = 4I_q$. After that, the $I_{push}$ will keep the same minimal value while the $I_{pull}$ can further increase far above $4I_q$. When the input is negative, the circuit behavior is the same.

In our design, in order to get a good high frequency performance, we should keep the minimal current at a reasonable large value. We set the quiescent current to be 100 $\mu$A and $\alpha$ to be 10, which reduces the translinear current $I_B$ to 10 $\mu$A. A simulation result of input-output current characteristic of this class-AB output stage is shown in Fig. 6.6. Y-axis of this plot represents the current of the output (orange dots), $I_{push}$ (green dots), $I_{pull}$ (red crosses), current through $M_3$ (blue diamonds) and $M_4$ (magenta dots). Because a 1 Ω resistor is used to sense the current, the unit of Y-axis is $\mu$V instead of $\mu$A. From this simulation result, we can see that when input current is about 240 nA, all biasing current (20 $\mu$A) flows through $M_3$ or $M_4$, and the output current reaches as high as 400 $\mu$A.

As for the whole opamp, a two-stage Miller-compensation opamp with the above class-AB output stages is designed for the first integrator (see Fig. 6.7). An NMOS differential pair is used as the input stage, for two reasons. First, the NMOS transistor is faster than PMOS. Second, the input common mode voltage of the opamp is set to be 1.1 V instead of $V_{dd}/2$ (0.9 V) to increase the $V_{dsat}$ of the current cells in the feedback DAC, and hence to reduce the thermal noise of the DAC, so it is more suitable to use an NMOS input pair. The benefit of using PMOS transistors in the input differential pair is low flicker noise, but in our wideband design, the flicker noise is of less concern.

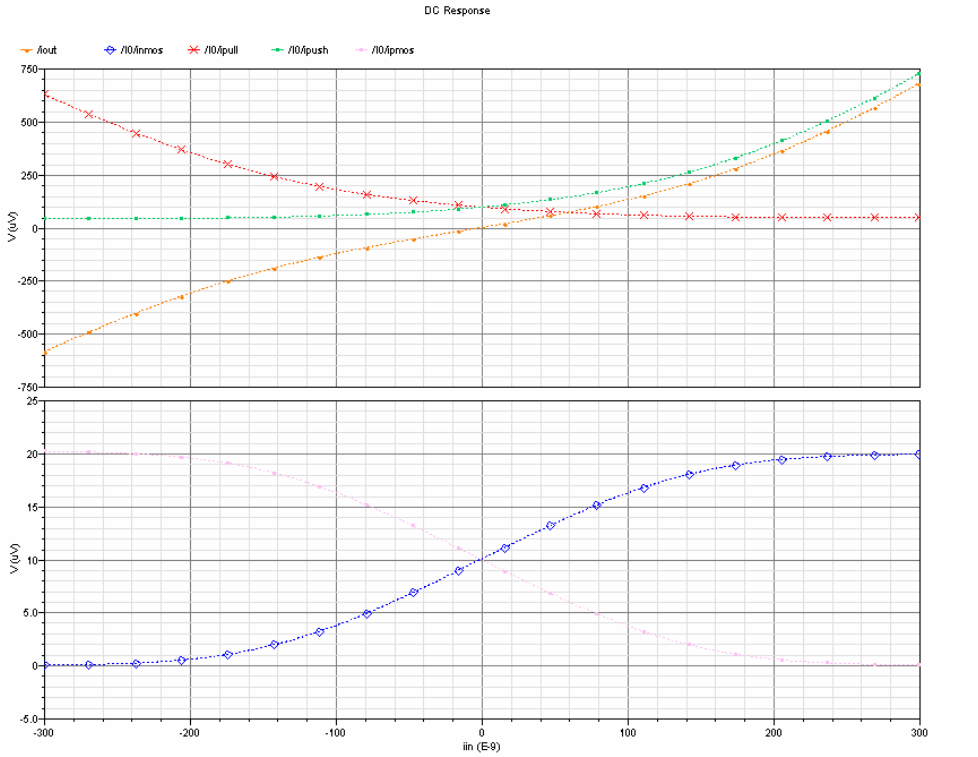



Figure 6.6: Input-output current characteristics of the class-AB output stage

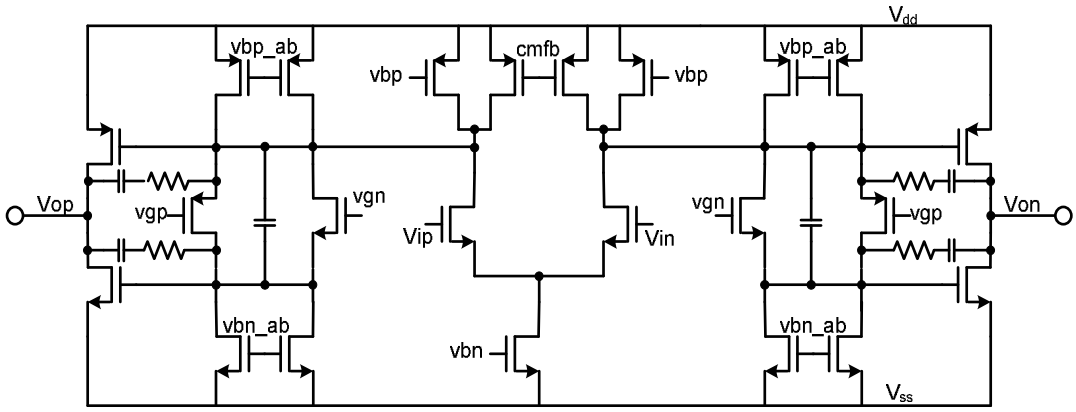



Figure 6.7: Schematic of the two-stage opamp

For a CT ΔΣ modulator, many papers said that the requirement of the opamp gain-bandwidth product (GBW) can be as low as 1 ~ 2 times the clock rate. However, this "Golden Rule" only works under two conditions. First, the OSR of the modulator should be high enough (larger than 16) because this will guarantee for the opamp with such a low GBW to

still provide enough loop gain for the in-band signals to maintain a linear operation. Second, the noise shaping cannot be too aggressive for a given number of the quantizer levels. Otherwise, the high frequency quantization noise will be dominant in the feedback DAC signal, and cause nonlinearity in the integrator operation, because with a GBW of 1 ~ 2 times the clock rate, the opamp cannot handle this large high frequency feedback signal.

In our design, these two conditions are not satisfied very well, so if the opamp GBW is designed according to the "Golden Rule", large swings of the high frequency signals can be seen at the virtual ground of the opamp, which causes an SNR degradation in the modulator. The simulations showed that for the first and fifth stages of the modulator (see Fig. 6.1), the opamp loop GBW should be as high as 3 times the sampling frequency to maintain linear operation. However, for the internal stages, the GBW requirement of the opamp can be determined based on the "Golden Rule" without affecting the modulator performance because the stages don't need to process the high frequency feedback signals.

As for the common-mode feedback (CMFB) circuits (Fig. 6.8), two resistors are used to sense the common-mode voltage of the opamp outputs, $V_{op}$ and $V_{on}$. A simple differential amplifier with diode-connected active loads is employed to compare the common-mode voltage with the reference, and to generate the "cmfb" signal for the opamp. To increase the phase margin of the CMFB loop, only parts of the active load transistors in the opamp first stage are controlled by the "cmfb" signal. However, this scheme will reduce the DC gain of the CMFB loop, so a trade-off should be made between the phase-margin and DC gain.

### *6.2.3. Current DAC Design*

Fig. 6.9 shows the schematic of the unit current cell. The current cell is composed of four transistors which are current source $M_1$, cascode transistor $M_2$ and two switches ($M_{3a}$ and

$M_{3b}$). The cascode transistor is used to increase the output impedance of the current source, and at the same time, to prevent the dynamic glitches at the node *A* from impacting the current in $M_1$. However, adding this cascode transistor reduces the allowable saturation voltage of $M_1$ and hence the noise performance of the current DAC. The gates of the switch transistors are controlled by the complementary digital feedback signals, *D* and *Db*.

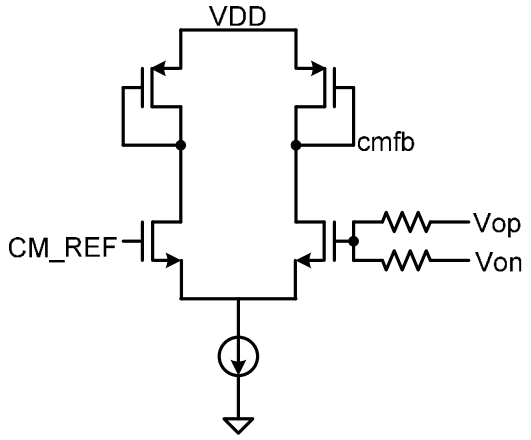



Figure 6.8: Schematic of the CMFB circuit

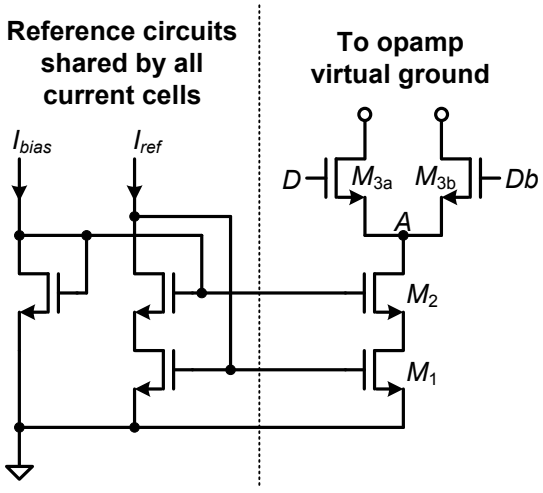



Figure 6.9: Schematic of the unit current cell

In this modulator, in order to reduce the excess loop delay as well as the circuit complexity, no dynamic element matching (DEM) is used to shape the DAC error. So,

according to the noise budget given in Table 5.2, the mismatch error of the unit current cells should be as small as 0.1%.

For two MOS transistors with the same dimension and biasing conditions, the variance of the relative drain current mismatch error $\Delta I/I$ can be expressed as [46]

$$\sigma^2_{\frac{\Delta I}{I}} = \sigma^2_{\frac{\Delta\beta}{\beta}} + \left( \frac{2}{V_{GS} - V_{TH}} \sigma_{\Delta V_{TH}} \right)^2 \tag{6.22}$$

where $\Delta\beta/\beta$ and $\Delta V_{TH}$ are the mismatches of the current factor $\beta$ and the threshold voltage $V_{TH}$ between those two transistors. If the mismatch is caused by the independent random disturbances of physical properties, and the correlation distance of the statistical disturbance is small compared to the active device area, then they can be approximated by

$$\sigma^2_{\frac{\Delta\beta}{\beta}} = \frac{A^2_\beta}{W \cdot L} \text{ and } \sigma^2_{\Delta V_{TH}} = \frac{A^2_{V_{TH}}}{W \cdot L} \tag{6.23}$$

where $A_\beta$ and $A_{VTH}$ are process-dependant constants which is usually provided by the chip manufacturer.

Using these equations, the minimum size of the device which is required to provide a given matching property is given by [47 ~ 48]:

$$(W \cdot L)_{\min} = \frac{\frac{1}{2}\left[ A^2_\beta + \frac{4A^2_{V_{TH}}}{(V_{GS} - V_{TH})^2} \right]}{\sigma^2_{\frac{\Delta I}{I}}} \tag{6.24}$$

where, in our case, $\sigma_{\Delta I/I}$ of 0.1% should be used.

As shown in Fig. 6.1, the complementary digital input signals of the current DAC are generated by the D flip-flops, so the jitter of the clock signal which is used to trigger those D flip-flops will be critical to the modulator performance. As we mentioned in the system level design, the RMS values of the clock jitter sensitivity of this modulator is set to be 5 ps. In

order to achieve such a low jitter value, a low-jitter clock generator is designed on the chip (see Fig. 6.10)

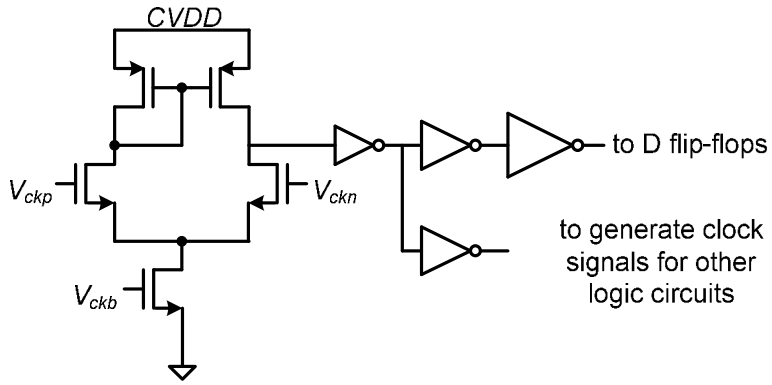



Figure 6.10: Low-jitter clock generation

To reduce the common-mode noise probably coupled to the test board and to obtain the least amount of clock jitter from the external clock source, a pair of sinusoidal differential clock inputs ($V_{ckp}$ and $V_{ckn}$) are generated on the board and fed to the modulator. On the chip, this differential clock signal is transformed to a single-ended one with a simple differential-input single-ended-output amplifier. It is critical to use as few clock driver stages as possible to generate the low-jitter clock with sufficient driving capability, because any extra stages will introduce extra device noise which will increase the clock jitter. So, the clock signal of the D flip-flops is separated from those of other logic circuits. To reduce the supply noise, a dedicated and clean supply *CVDD* is used solely for the low-jitter clock generation circuit.

Usually, in a master-slave static D flip-flop, the complementary outputs are generated by inserting an inverter between the outputs *Q* and *Qb*, which makes the complementary signals asymmetrical. In other words, the open and close time instants of the switches in the DAC current cells are dependent on the input signal value, 0 or 1, which introduces an error similar to that caused by the clock jitter. So, a fully differential D flip-flop in which the signal

paths for the complementary outputs are completely symmetrical is used for each bit of the feedback signal.

## 6.3. Summation Circuit

Before the quantizer, a summation circuit (adder) is needed to add the loop filter output to the direct feed-in signal and the feedback DAC output. The speed of this adder is one of the most critical issues in the modulator design. If a passive adder is used, it will be very sensitive to the parasitic input capacitors of the quantizer. If an active voltage adder is used, an extremely fast opamp is needed, which will cost large power. In our design, a fast and low-power active current adder is used to realize this summation operation [17] (see Fig. 6.11).

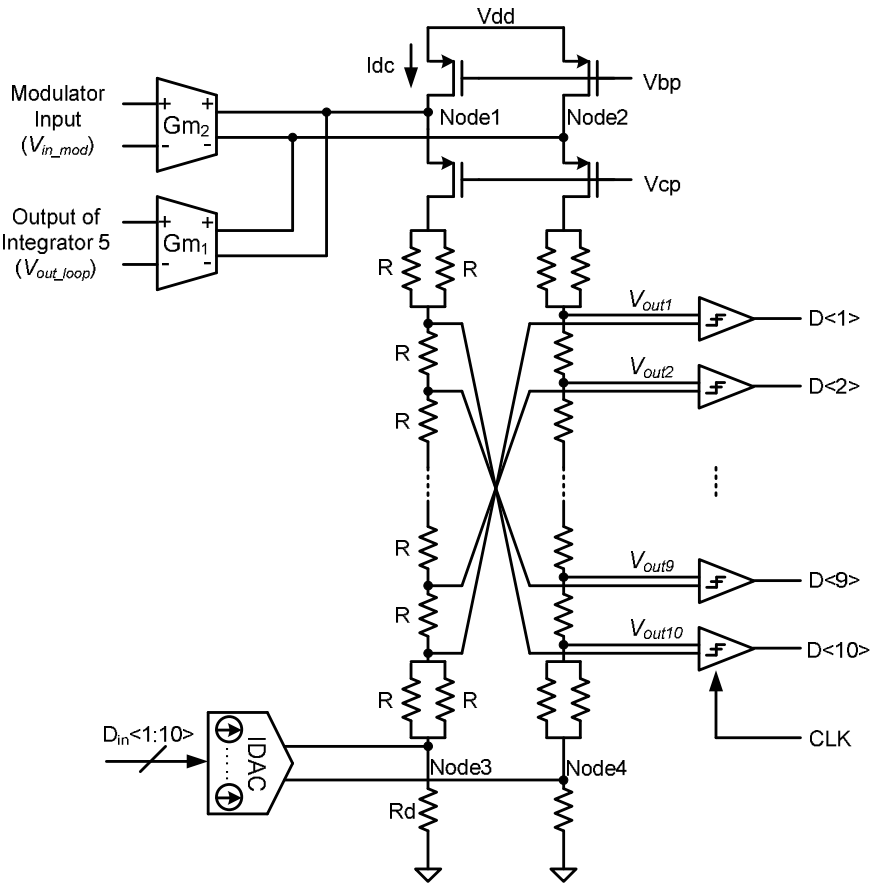



Figure 6.11: Schematic of the summation circuit

In this summation circuit, the loop filter output and the direct feed-in signal are transformed from voltage to current with two transconductor ($G_m$) cells which are shown in Fig. 6.12, and then fed into the resistor ladder at the cascode nodes of the two current sources. Those two cascode nodes are almost kept constant so the linearity of the $G_m$ cells is very high.

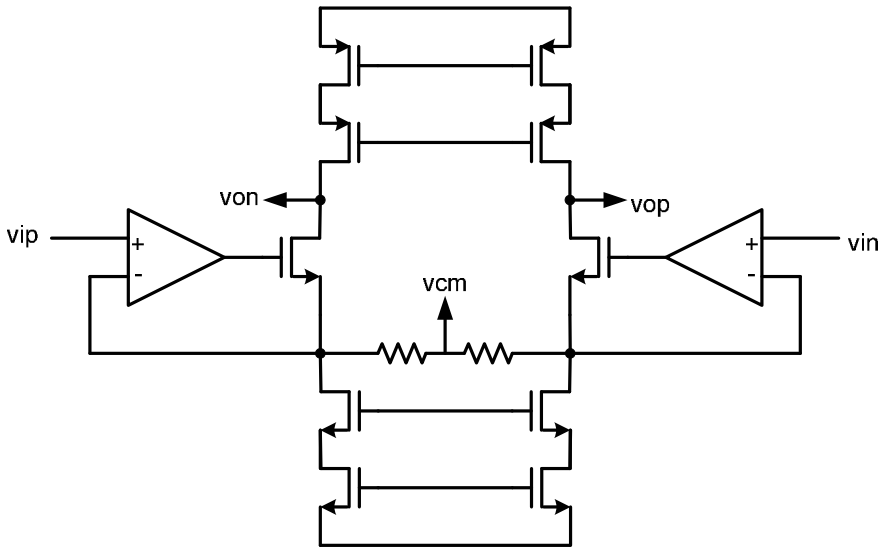



Figure 6.12: Schematic of the $G_m$ cell

In order to increase the input swing and linearity of the $G_m$ cell, the input voltage-current (V-I) conversion is realized by means of a super input $G_m$ stage in combination with two passive resistors [30]. Due to the input local negative feedback and the use of linear resistors, a very linear V-I conversion is obtained without difficult matching requirements for the MOS transistors. Because the voltage at the middle point of the two resistors is just the common-mode voltage of the input differential signals, the $G_{m1}$ is also used to extract the output common-mode voltage of the opamp in the $5^{th}$-stage for the CMFB circuit.

The direct feedback current DAC outputs are fed into the lower points of the resistor ladder. Unlike the current DACs used in the main and first-order loops, this DAC uses PMOS transistors as the current sources, and has a common-mode output (Fig. 6.13).

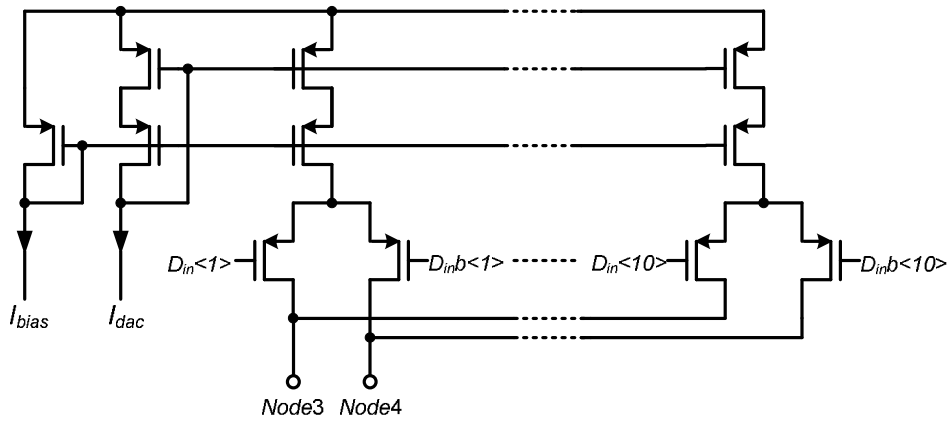



Figure 6.13: Schematic of the direct feedback DAC

The resistor ladder converts all the currents back into voltages and automatically provides the threshold levels needed by the quantizer. It can be shown that the input voltage of the $i^{th}$ comparator ($i$ = 1, 2, …, 10) consists of three components:

$$V_{out_i} = V_{out\_gm} + V_{out\_dac} + V_{out\_th_i} \tag{6.25}$$

The first two components ($V_{out\_gm}$ and $V_{out\_dac}$) do not depend on the comparator index number $i$, and are therefore the same for each comparator in the array. They depend only on the input signals which are the loop filter output $V_{out\_loop}$, the modulator input $V_{in\_mod}$ and the feedback DAC input $D_{in}$<1:10>, synthesizing in this way the summation operation shown in Fig. 5.4. The last component ($V_{out\_thi}$) does not depend on the input signals, but is determined by the comparator number $i$, by the bias current $I_{dc}$, and by the resistance of the ladder, thereby realizing the threshold voltages. These three components are given respectively by

$$\begin{cases} V_{out\_gm} = (10R + 2R_d) \cdot (V_{out\_loop} \cdot G_{m1} + V_{in\_\mathrm{mod}} \cdot G_{m2}) \\ V_{out\_dac} = 2R_d \cdot D_{in} \cdot I_{dac} \\ V_{out\_th_i} = (10 - 2i + 1) \cdot I_{dc} R \end{cases} \tag{6.26}$$

From above equations, it can be seen that the branch gains are realized by the products of the resistance and transconductance or current value. Both the transconductance and current

value are inversely proportional to the resistance, so the accuracy of the branch coefficients relies on that of the resistance ratio which can be made very high in modern semiconductor process.

The speed of the current adder is determined by its poles. The main pole of this current adder is introduced by the resistor ladder and the distributed parasitic capacitance across the ladder. In order to increase this pole frequency, small resistors are used in the ladder and the input capacitance of the comparators is minimized. The second pole resides at the *Node*1 and *Node*2, and is caused by the drain capacitors of the transistors converging to those two nodes as well as the parasitic wiring capacitors.

## 6.4. Quantizer

The quantizer consists of ten latched comparators. Each latched comparator is composed of a single preamplifier stage and a master-slave latch (Fig. 6.14).

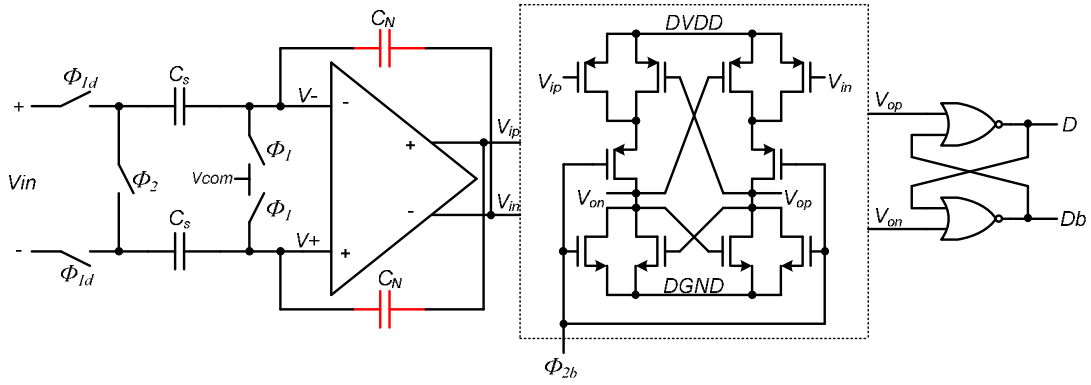



Figure 6.14: Schematic of the comparator

During $\Phi_1$, the outputs of the summation circuit are sampled to the bottom plate of the sampling capacitors $C_s$. At the same time, the regenerative latch (the circuit in the dotted-line box) is in the reset status to reduce the hysteresis, which means the positive feedback loop is broken and its outputs are pulled down to the ground. After that, the sampling switches are

opened and the two terminals of the input signal is shorted together, which makes the voltage difference between the preamplifier input terminals, $V_+$ and $V_-$, equal to the sampled input signal. This voltage difference is amplified by the preamplifier and fed into the regenerative latch. Now, the latch is out of the reset, and the positive feedback loop, which is composed of two back-to-back inverters, will quickly amplify the input difference to the logic levels.

As mentioned in Section 4.2.2, the comparator offset, which consists of the input offset of the preamplifier and the latch offset, will increase the quantization noise. The input-referred offset of the latch is attenuated by the gain of the preamplifier (usually 10 to 20) so it is negligible. As for the input offset of the preamplifier, some offset storage techniques, e.g., the auto-zeroing scheme shown in Fig. 4.11, are often used to reduce it. Unfortunately, these techniques are not suitable for our extremely fast comparators (400 MHz), so the dimension of the input differential-pair transistors of the preamplifier has to be enlarged to minimize this input offset. This large transistor size will cause big parasitic capacitors $C_p$ at the preamplifier input nodes, $V_+$ and $V_-$, whose voltage difference during $\Phi_2$ is now changed to:

$$V_+ - V_- = \frac{C_s}{C_s + C_p} V_{in} \tag{6.27}$$

In Section 6.3, it is mentioned that the main pole of the current adder is determined by the distributed R-C network of the resistor ladder. So, the sampling capacitance, which is the main component of the distributed capacitance, has to be minimized to speed up the current adder. This small sampling capacitance makes the factor in the right side of Eq. 6.27 significantly attenuate the input signal hence reduce the effective gain of the preamplifier. To resolve this issue, two neutralization capacitors (the $C_N$ in Fig. 6.14) are introduced to cancel the parasitic ones, especially the Miller capacitance caused by the gate-drain capacitor [49].

An R-S flip-flop follows the regenerative latch for two reasons. First, this flip-flop can amplify the input difference further to reduce the metastability. Second, the R-S flip-flop will

keep the quantizer output stable when the output of the regenerative latch is pulled down to the ground during $\Phi_1$.

## 6.5. Clock Generator

In our modulator, the clock signals are used in the quantizer and feedback DACs. Fig. 6.15 shows simplified diagram of the comparator and feedback network as well as the timing relationship between the different clock signals.

The sampling point is at the falling edge of $\Phi_1$ which is noted as time 0. The ideal feedback time instant of DAC2 and DAC3 is half clock period later than the sampling point. Due to the very short clock period, the loop delay introduced by speed-limited components, such as the feedback DACs, integrator 5 and current adder, is not negligible. As mentioned in Section 5.2, this delay will make the modulator unstable. So, the feedback time instant in the real circuits should be earlier than the ideal one to compensate for this delay. Under different process conditions, supply voltages and working temperatures (PVT), the required amount of this time advance is different, so we have to make the time distance between the rising edge of $\Phi_{lat}$ and the time point of 0.5 variable. The same situation exists for the feedback timing of the DAC1. The ideal feedback time instant of DAC1 is one clock period later than the sampling instant. In the real circuits, the rising edge of $\Phi_{dff}$ is earlier than the time point of 1.

The simplified schematic of the multi-phase clock generator is shown in Fig. 6.16. The clock signal, *ck*, is the output of the differential-to-single-ended transformation circuit shown in Fig. 6.10. Two variable delay cells are inserted into the clock generator to realize the variable feedback clock signals, $\Phi_{dff}$ and $\Phi_{lat}$. The detailed schematic of this variable delay cell is shown in Fig. 6.17. The delay value can be adjusted by changing the biasing current of the PMOS transistors.

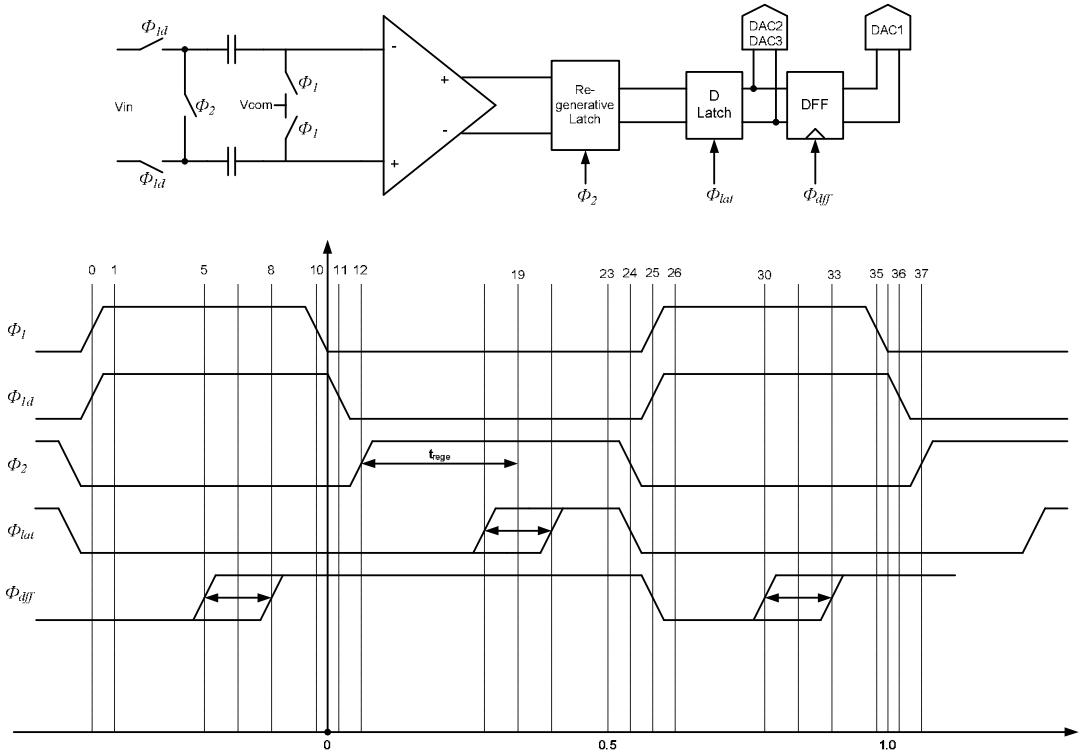



Figure 6.15: Timing relationship between different clock signals

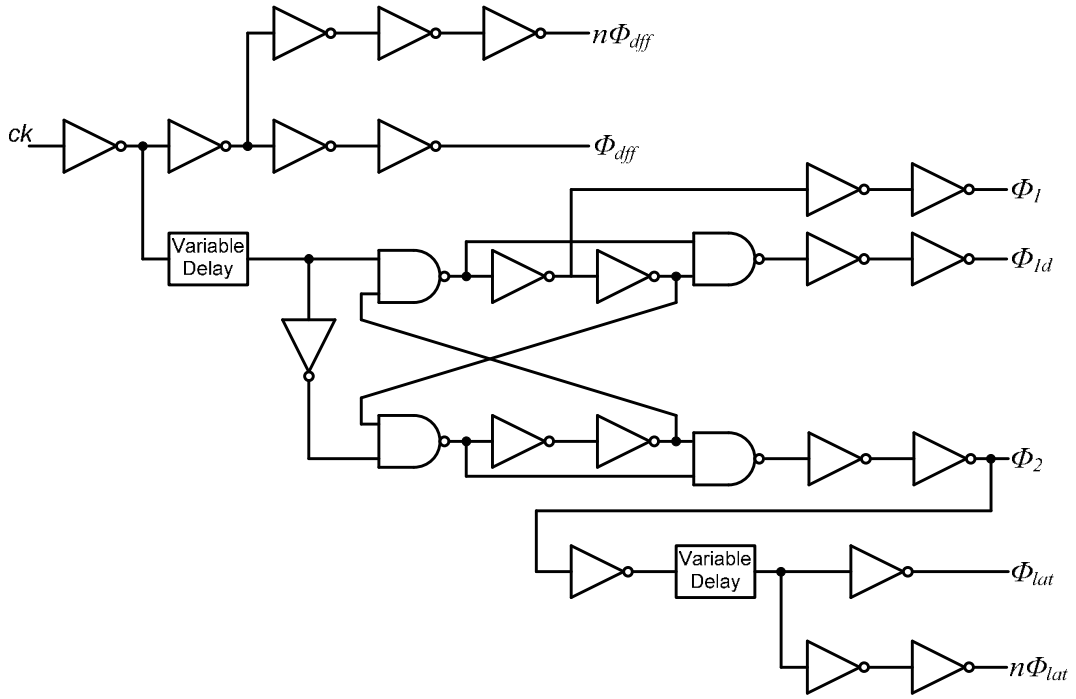



Figure 6.16: Schematic of the multi-phase clock generator

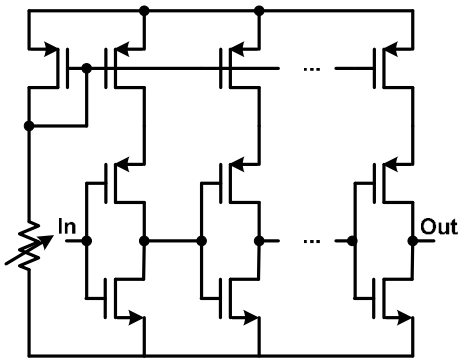



Figure 6.17: Schematic of the variable delay cell

## 6.6. Interface Circuit

The output of the quantizer is a 10-bit thermometer coded signal at the data rate of 400 MHz. In order to ease the chip evaluation, it is necessary to reduce the output data rate with a reasonable data width. An interface circuit, which includes a Wallace-Tree to realize the thermometer-to-binary transformation and a 1:4 DEMUX to reduce the data rate to 100 MHz, is integrated on the chip (see Fig. 6.18).

This Wallace-Tree thermometer-to-binary encoder, shown in Fig. 6.19, counts the number of "1s" in the 10-bit input signal. This encoder is not the fastest solution for thermometer-to-binary conversion, but it is the most hardware efficient one. As long as the worst case conversion time is less than a clock period, this encoder is good enough. It should be mentioned that the Wallace-Tree can effectively "kill" the bubbles which may occur at the output of the flash ADC [33]. For example, if at some instant, the thermometer-code is "0001011111" with one bubble, the Wallace-Tree will generate a binary code as "0110" as if the outputs were "0000111111". Hence, a dedicated bubble-killer circuit after the quantizer as in [50] is not needed in this design.

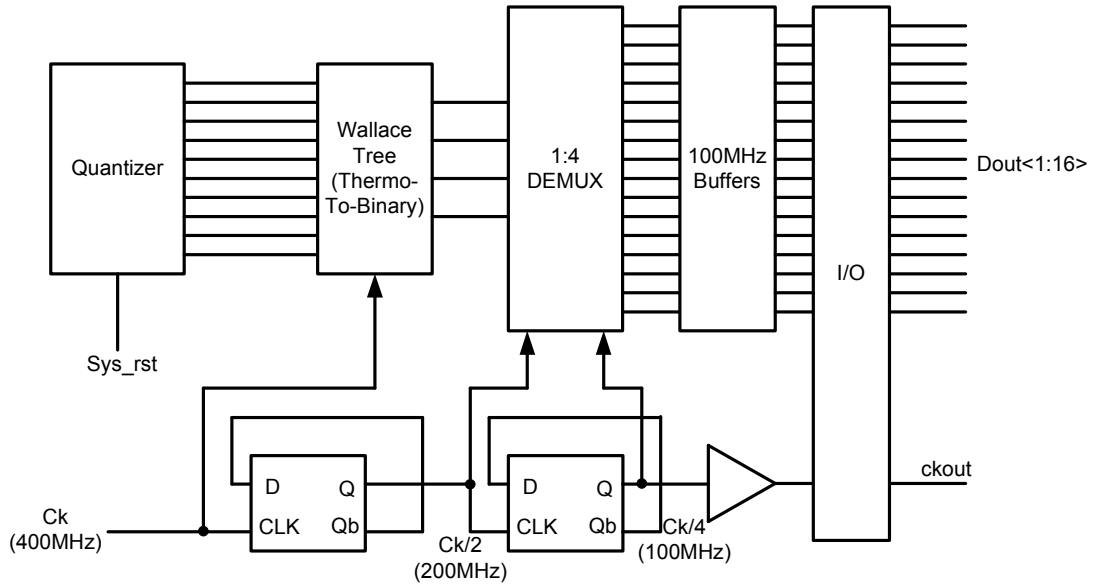



Figure 6.18: Diagram of the interface circuit

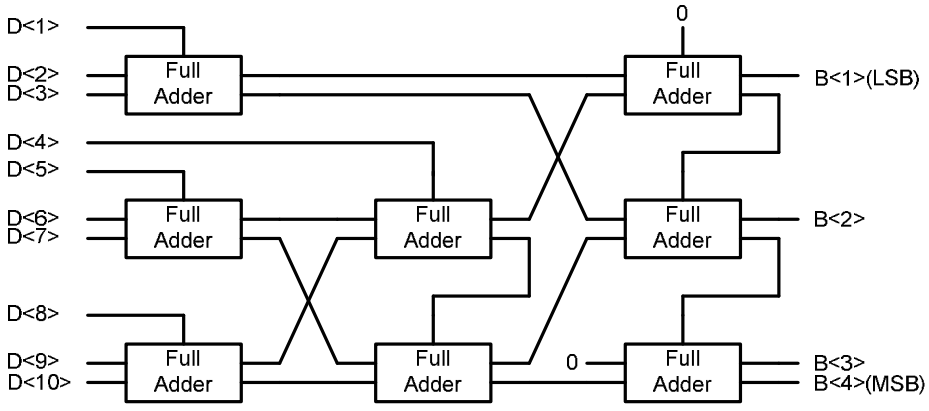



Figure 6.19: Diagram of the Wallace-Tree thermometer-to-binary encoder

The 1:4 DEMUX needs half rate clock signal *ck*/2 and quarter rate clock signal *ck*/4, which are generated by two static D flip-flops whose inputs are connected with their complementary outputs. Each 1:4 cell (Fig. 6.20a) consists of three 1:2 DEMUX cells which are shown in Fig. 6.20b. The input data is sampled at both rising and falling edges of the half-rate clock. The negative level enabled D latch is used to align the output data.

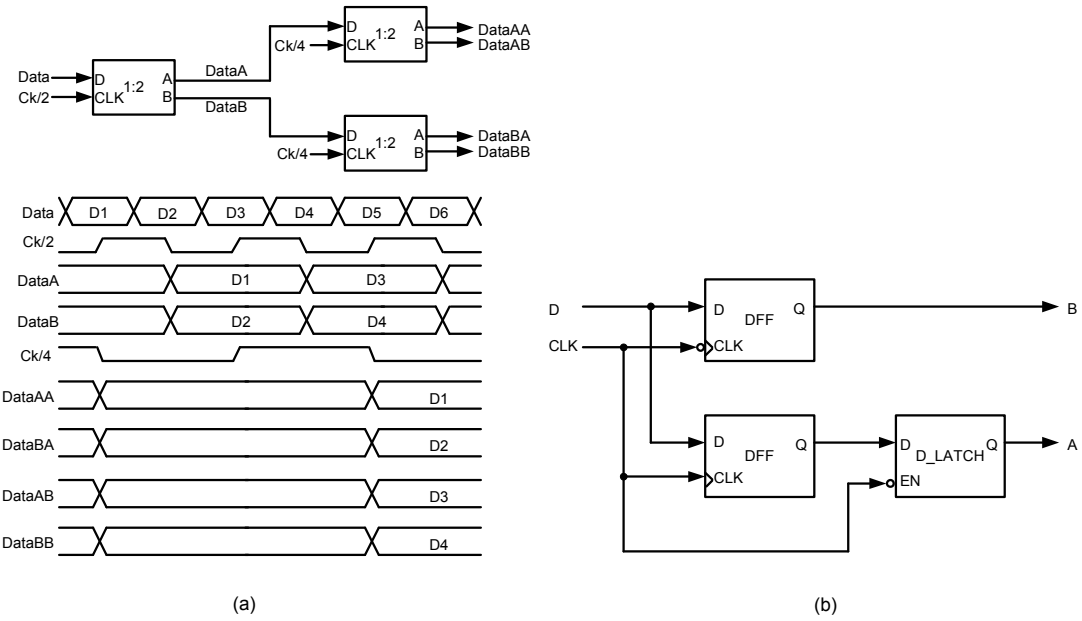



Figure 6.20: (a) 1:4 DEMUX and its timing; (2) 1:2 DEMUX cell

## 6.7. Time Constant Tuning

Due to the PVT variation, the RC time constant of the integrators can vary by as much as ±30%, which will greatly reduce the noise shaping effectiveness and even drive the loop filter unstable. According to the noise budget shown in Table 5.2, the accuracy of the RC time constant in this design needs to be at most ±5%.

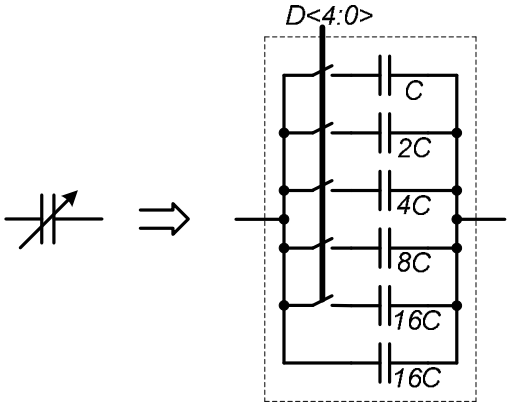



Figure 6.21: Tunable capacitor array

A 5-bit binary-weighted tunable capacitor array is used for the integration capacitor in each integrator. There is an "always-in-use" capacitor which is equal to the most significant bit (MSB) capacitance, 16*C*. So, the total "in-use" capacitance is given by

$$C_{in-use} = 16C + kC \quad (k = 0, 1, \ldots, 31) \tag{6.28}$$

The minimum and maximum available capacitances of the capacitor array are

$$C_{\min} = 16C \text{ and } C_{\max} = 47C \tag{6.29}$$

So, the tuning range of the capacitor array is

$$\text{Tuning Range} = \frac{C_{\max}}{C_{\min}} = 2.94 \tag{6.30}$$

and the tuning resolution is

$$\text{Tuning Resolution} = \frac{C}{32C} = 3.125\% \tag{6.31}$$

where 32*C* is the nominal value of the integration capacitor and *C* is the tuning step.

## 6.8. Layout Considerations for High Speed Circuits

The CT ΔΣ modulator is essentially a mixed-signal system which includes continuous-time blocks (e.g., the loop filter), sampled-data blocks (e.g., the quantizer), and digital blocks (e.g., the D flip-flops). To achieve high resolution and linearity, caution should be taken in the layout design to reduce the effects of mismatch, parasitic and digital noise coupling to analog blocks.

Fig. 6.22 shows the die photo of the whole modulator, in which some important blocks are annotated. Several commonly used layout techniques were employed, such as common-centroid layout for current sources, inter-digitation for transistors, guard ring and

shielding. Between the analog (upper) and digital (lower) areas, a deep n-well was inserted to further reduce the noise coupling.

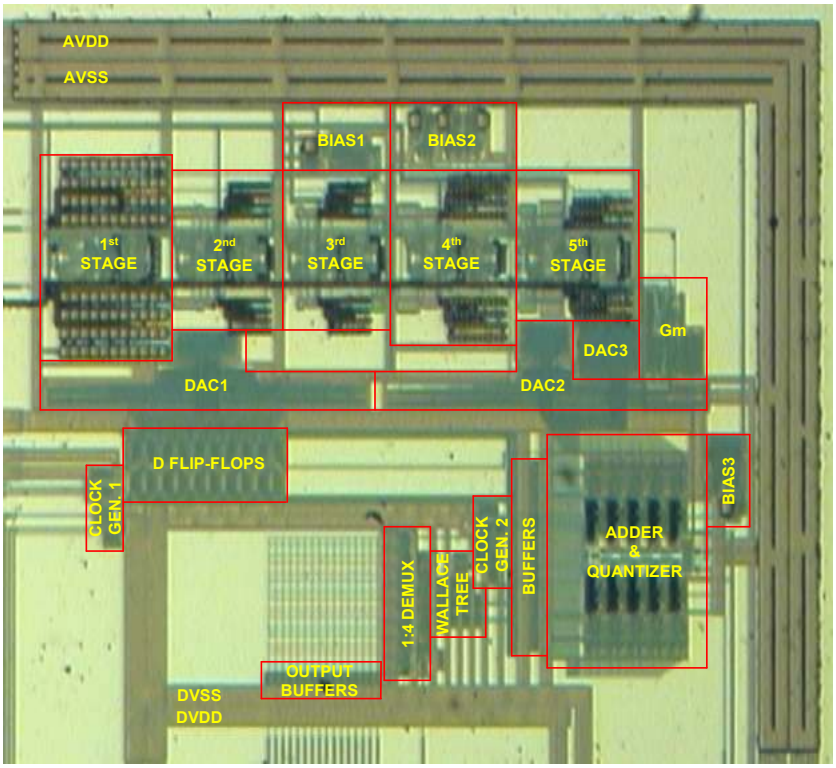



Figure 6.22: Die photo of the CT ΔΣ modulator

In a high speed circuit, such as this modulator, not only the symmetry of the circuit components but also the symmetry of the interconnections should be considered while drawing the layout, because here the parasitic capacitors and resistors of the metal lines are not negligible. So, a fully differential layout was drawn for the loop filter. This layout scheme is illustrated in Fig. 6.23 for the integrator.

From this plot, it can be seen that both the circuit components (e.g., *R*+ and *R*-) and supply and signal lines (e.g., *V*+ and *V*-) are fully symmetrical for the differential paths. Similar methods are used to draw the layout inside the opamp. A detailed fully differential layout of the first integrator is shown in Fig. 6.24. All differential transistor pairs are drawn

with 2-dimensional common-centroid scheme. The differential signals are routed in the middle of the transistor columns which makes the signal paths fully symmetrical. However, the two capacitor arrays are laid out independently, so the matching between them has to depend on the matching property of the MIM capacitors themselves. In order to improve this matching, dummy capacitors are used to make the environments of all unit capacitors the same.

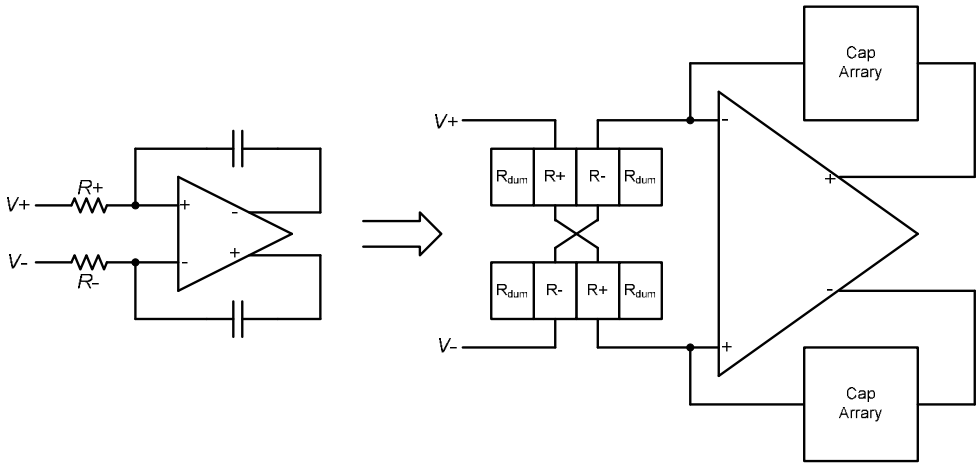



Figure 6.23: The fully differential layout scheme

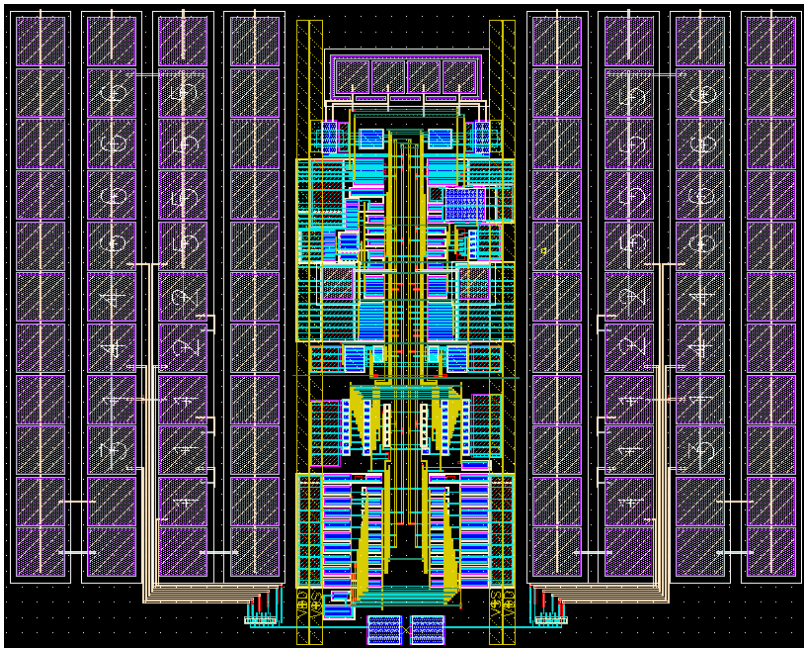


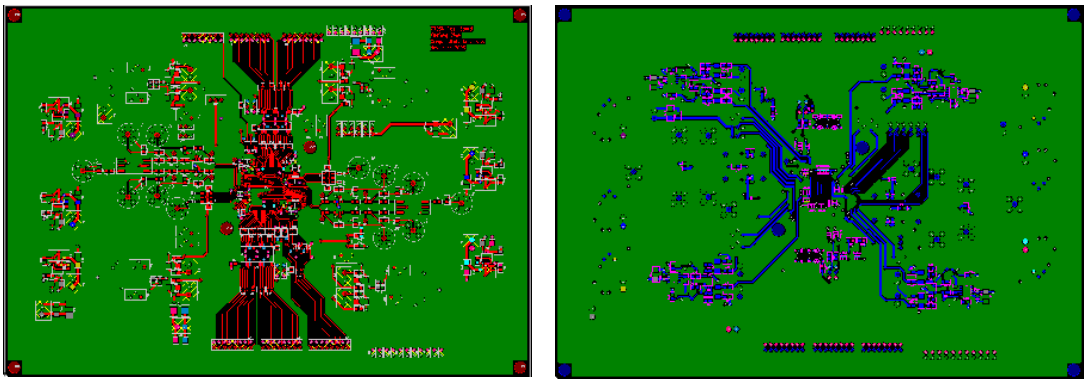
Figure 6.24: Fully differential layout of the 1st integrator

# CHAPTER 7. CHIP EVALUATION

This chapter describes the test setup and experimental results obtained from the prototype chip.

## 7.1. Test Board Design

To achieve the expected performance of the prototype chip, a good test board design is of utmost importance. A four-layer printed circuit board (PCB) was designed, which is shown in Fig. 7.1. The top layer is mainly used to place the components and route signal traces. The second layer is the ground plane which is divided into analog and digital sections. Several jumpers are also included on the board for the optional connection between those two ground sections. The third layer is the power plane. It is also divided into several sub-planes each of which is used to distribute a given power supply. The bottom layer is used to place a few components and route the reference signals.



(a) (b)

Figure 7.1: (a) Top layer and (b) bottom layer of the test board

While designing this test board, several criteria were applied to minimize the noise in the power supplies, the crosstalk between traces, and the parasitic capacitance and resistance.

Each analog power supply is generated by a low noise, low dropout regulator instead of by the DC supply equipment. The output of the regulator is further decoupled by a 10 $\mu$F tantalum capacitor for the low-frequency noise. In addition, at each supply pin of the prototype chip, ceramic capacitors of 0.1 $\mu$F and 0.01 $\mu$F are placed to decouple the high-frequency noise. All reference voltages are also generated by the regulators, which are buffered by high driving capacity opamps. All power supplies are distributed evenly to the chips through the power planes. The power and ground pins are connected to the corresponding planes through the vias and wide traces which were made as short as possible to minimize the wire resistance. All differential signal traces are routed symmetrically. The distances between the signal traces are kept reasonably wide to reduce crosstalk. The circuits which generate sensitive analog signals, e.g., the inputs of the modulator and the clock generator, are placed as close as possible to the prototype chip. The high frequency digital signal traces are also as short as possible to reduce electromagnetic interference (EMI).

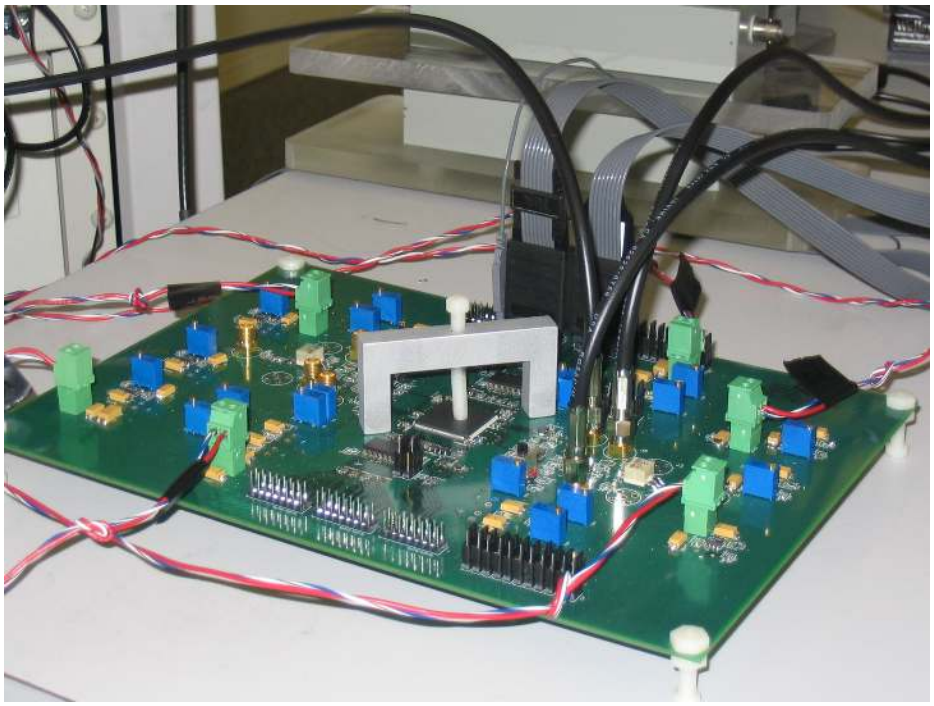


Figure 7.2: Test setup photo

## 7.2. Test Environment

Fig. 7.3 shows the test environment of the prototype chip. For the modulator input, two options are available. One is the low-frequency high-accuracy differential signal from the Audio Precision (AP), and the other is the high-frequency single-ended signal from the radio frequency (RF) signal generator. The latter one needs to be filtered by high performance passive bandpass filters and transformed into the differential signal by the on-board balun before it is fed into the prototype chip. The 400 MHz clock signal is obtained from the RF signal generator, e.g., HP8665A, and transformed to a differential one on the board, which is transformed back to single-ended on the chip. The power supply for the regulators and other commercial analog chips on the board is 5 V, which is provided by the DC supply instrument. The digital power supplies of the device under test (DUT) as well as other commercial digital chips, 3.3 VD and 1.8 VD, are also directly provided by the instrument. The modulator outputs are buffered by the commercial bus driver on the board before they are sampled by the logic analyzer. The data acquired by the logic analyzer is transferred to the computer and analyzed by the commercial software, e.g., spectrum analysis with MATLAB.

## 7.3. Measurement Results

Two modulators were integrated on the chip. They use the same architecture. When we did post-layout simulation with extracted capacitors, the modulator2 (MOD2) became unstable due to the limited loop speed, especially the speed of the first order loop. As mentioned in Section 6.3, the main pole of this loop is introduced by the distributed RC time constant of the current adder, so we decreased the resistance of the unit resistors in the resistor ladder from 100 Ω to 60 Ω to make the loop faster. The new modulator, modulator1 (MOD1), was stable in the post-layout simulation with partial extracted capacitors.

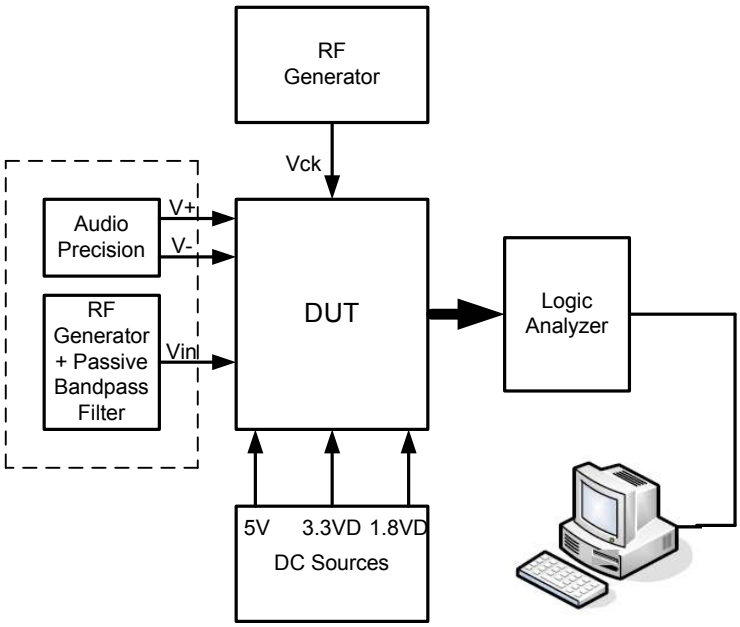



Figure 7.3: Test environment

### *7.3.1. Problem of the Interface Circuits*

In order to ease the interface with off-chip circuits, an interface circuit was designed for the modulator outputs. For convenience, we redraw the diagram of the interface circuit in Fig. 7.4. Because MOD1 is the main modulator that we want to test, we also extracted the thermometer-code outputs of the quantizer to the chip outputs through big digital buffers to guarantee that MOD1 is testable, even if the interface circuit doesn't work. However, due to the limited number of I/O pads, only four LSBs of the thermometer-code were connected to the I/O pads.

When the modulator is in the reset status, which means that the quantizer outputs are constant, the 100 MHz clock signal, *ckout*, is correct and stable. However, the period of the clock signal became inaccurate and varying significantly when the modulator is out of rest. Although both modulators showed the same problem, the clock signal of MOD2 is much more stable than that of MOD1. Because the *ckout* is obtained by dividing the 400MHz clock signal

twice, this wrong signal means that the clock divider and hence the 1:4 DEMUX circuit cannot work correctly.

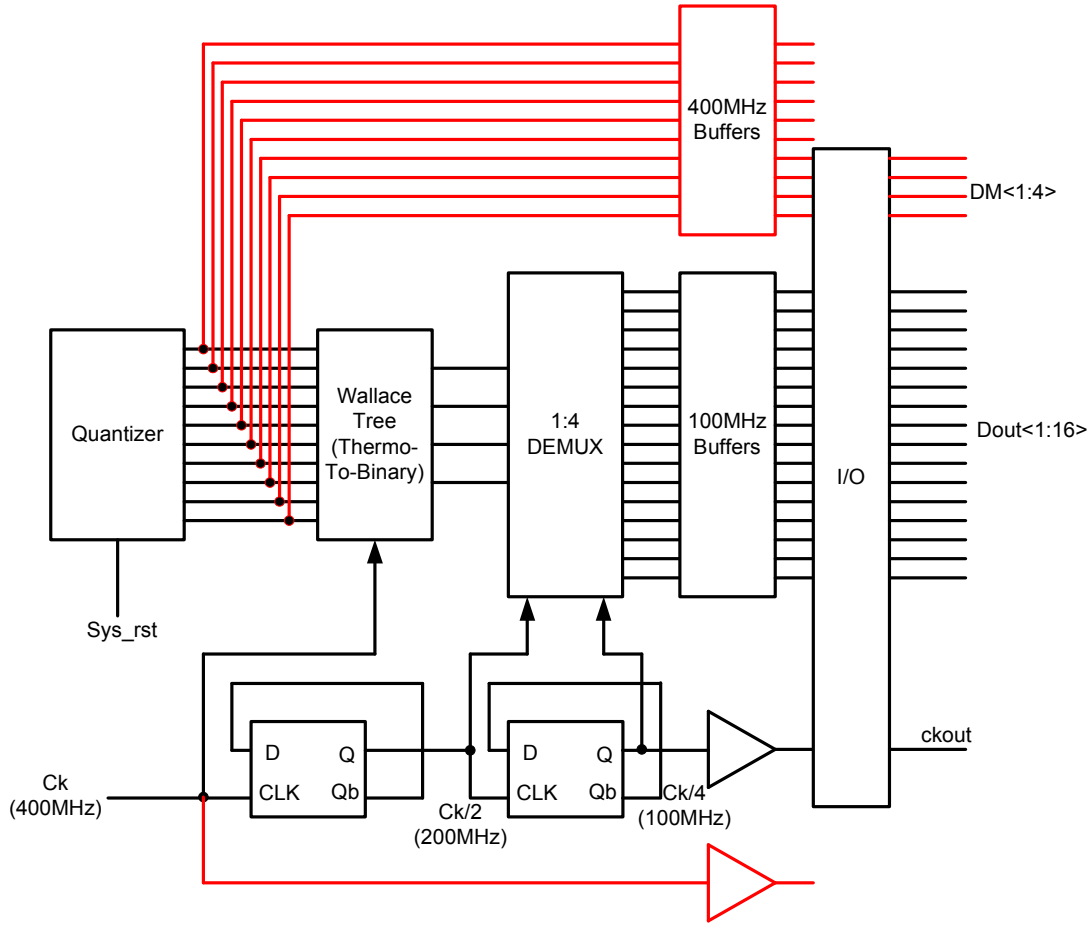


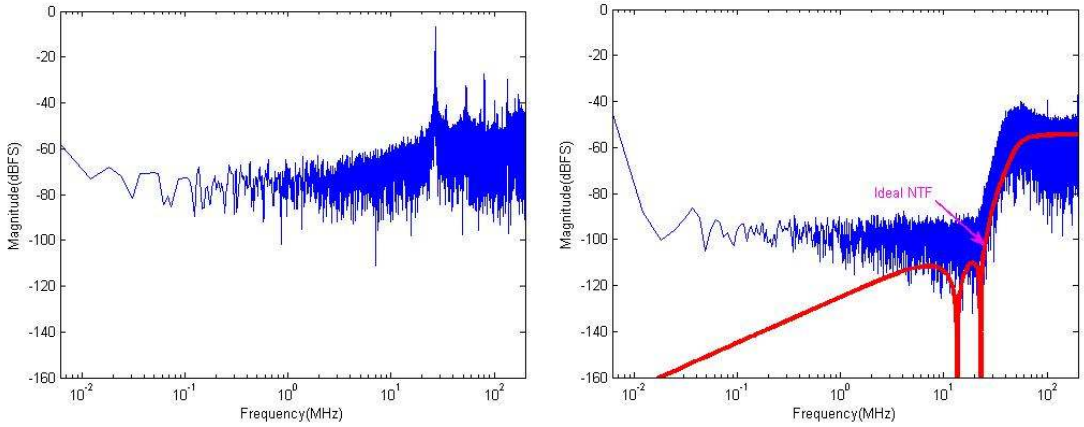

Figure 7.4: Diagram of the interface circuit (the buffers in red are only included in MOD1)

Based on the above test observations, the possible reason for this interface circuit problem is that the working of those digital buffers, which are used to buffer both the 16-bit binary outputs and the 10-bit thermometer-code outputs, affected the working of the interface circuit through the shared power supply bus, *DVDD* and *DGND*. This also can explain why the MOD2 showed better results than MOD1.

We tried to resolve this problem by increasing the digital power supply voltage which can increase the speed of the digital circuit, but this didn't work for MOD1. However, increasing logic supply could make the interface circuit in MOD2 work well.

### *7.3.2. Evaluation of MOD2*

Due to the problem of the interface circuit, we only have two methods to access the outputs of the modulators. As for the MOD2, because the interface circuits can work correctly with the increased logic power supply voltage, for example 1.9 V, we can access this modulator output through the 16-bit, 100 MHz binary code. As for the MOD1, because the interface circuits cannot work, only those four LSBs of the thermometer-code (400 MHz) can be accessed. However, the logic analyzer in our department cannot sample such high speed signals. So, at this moment, we can only test the MOD2.




(a) (b)

Figure 7.5: Output spectrum of the MOD2 with (a) normal and (b) increased RC time constant

Based on the measurement value of the reference resistor, we found that the real resistances of the resistors on the chip are a bit larger than the design values. So, the integration capacitors should be tuned to a smaller value to compensate the RC time constant

variation due to the process variation. Unfortunately, test results showed that MOD2 was unstable with the normal RC time constants (Fig. 7.5a). In order to make the loop stable, the RC time constant was increased by about 10% (Fig. 7.5b). However, due to the deviation of the RC time constant, the noise shaping was shifted a little to the left of the ideal NTF (the bottom plot in the figure), which increased the in-band noise power, especially the power between 20MHz and 25MHz.

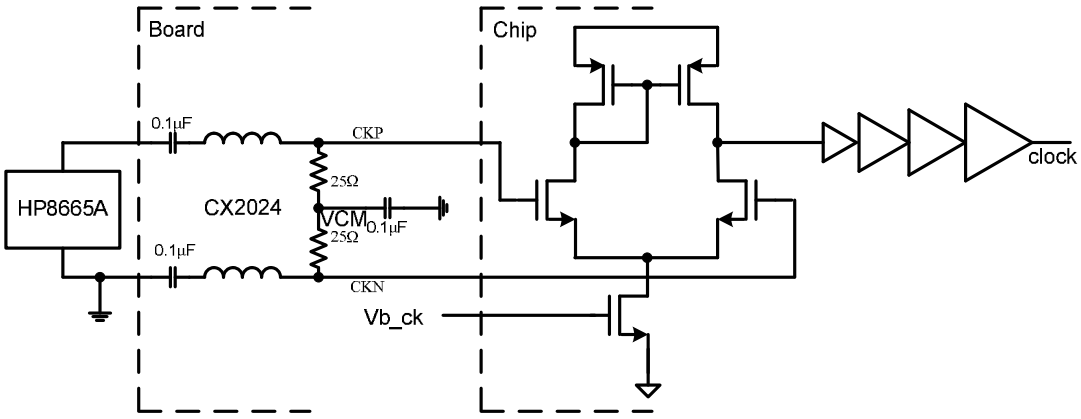



Figure 7.6: Diagram of the clock generator

Besides the noise shaping deviation, another import issue which increased the noise power is DAC clock jitter. In this test, the clock signal was obtained from the synthesized signal generator, HP8665A. This clock signal is transformed to differential signal on the board through a RF balun, and then this differential signal is transformed back to single-ended clock and buffered by the on-chip circuits (Fig 7.6). The design value of the biasing voltage of the differential pair *Vb_ck* is 600 mV, but we found that the in-band noise floor could be lowered significantly while increasing this biasing voltage (Fig 7.7). The bottom spectrum in the figure is obtained with the biasing voltage of 800 mV, whose in-band noise floor is about 12 dB lower than the top one. At this point, it should be mentioned that the RMS clock jitter sensitivity of the modulator was set to be 5ps during the system level design, but the real jitter

value which is caused by HP8665A and other circuit blocks on the clock signal path is indeterminable. What we can do is just to lower the jitter value as much as possible.

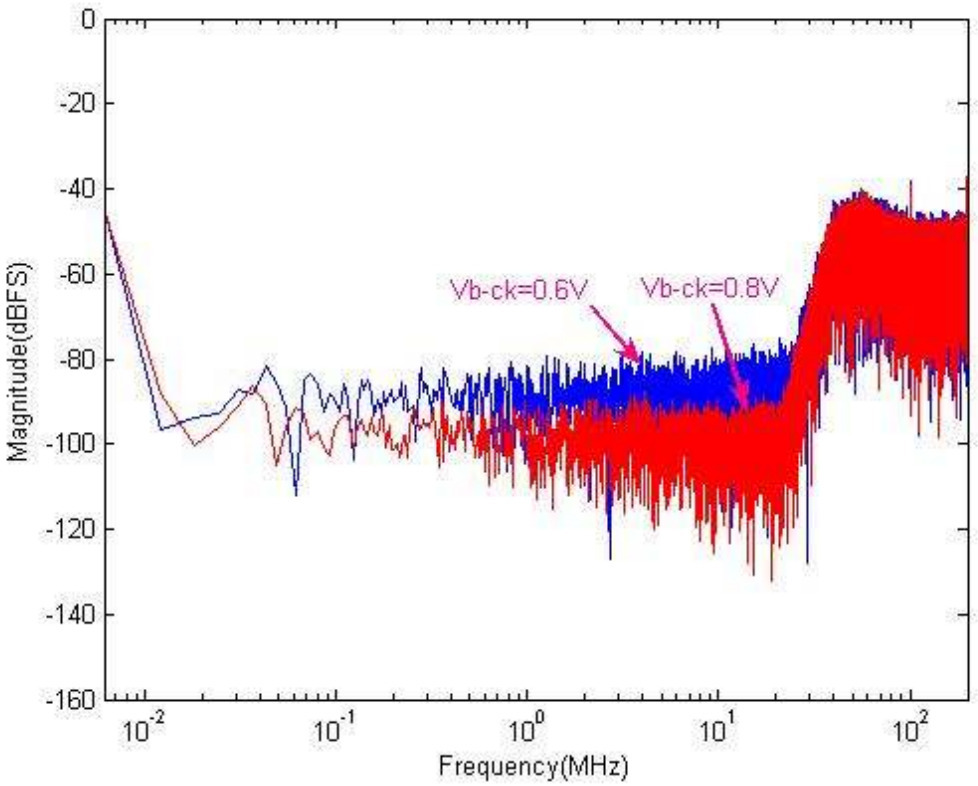



Figure 7.7: The effect of the clock jitter

### *7.3.3. Measurement Results*

The prototype chips have been tested with a 2 MHz input signal and 400 MHz sampling rate. Since the signal bandwidth is 25 MHz, up to the 12$^{th}$ harmonics of the input signal will be included in the calculation of the signal-to-noise-plus-distortion ratio (SNDR). The achieved peak SNDR is 52 dB and peak SNR is 52.5 dB. The dynamic range (DR) is 55dB. Fig. 7.8 shows the relationship between the SNDR/SNR and the input amplitude.

Due to the noise shaping deviation, the noise power between 20 MHz and 25 MHz is dominated by the quantization noise instead of the thermal noise. If we reduce the signal

bandwidth to 20 MHz, this quantization noise can be excluded. In addition, the RC time constant can be increased further to improve the stability and hence the maximum allowable input signal. Now, the achieved peak SNDR and SNR are 56 dB and 58 dB respectively. The dynamic range is increased to 60 dB. Fig. 7.8 also shows the plots of SNDR/SNR versus input amplitude with 20 MHz band of interest.

With the input signal of -6 dBFS and 2 MHz, the output spectra of the MOD2 with 25 MHz and 20 MHz signal bandwidths are shown in Fig. 7.9 and Fig. 7.10, respectively.

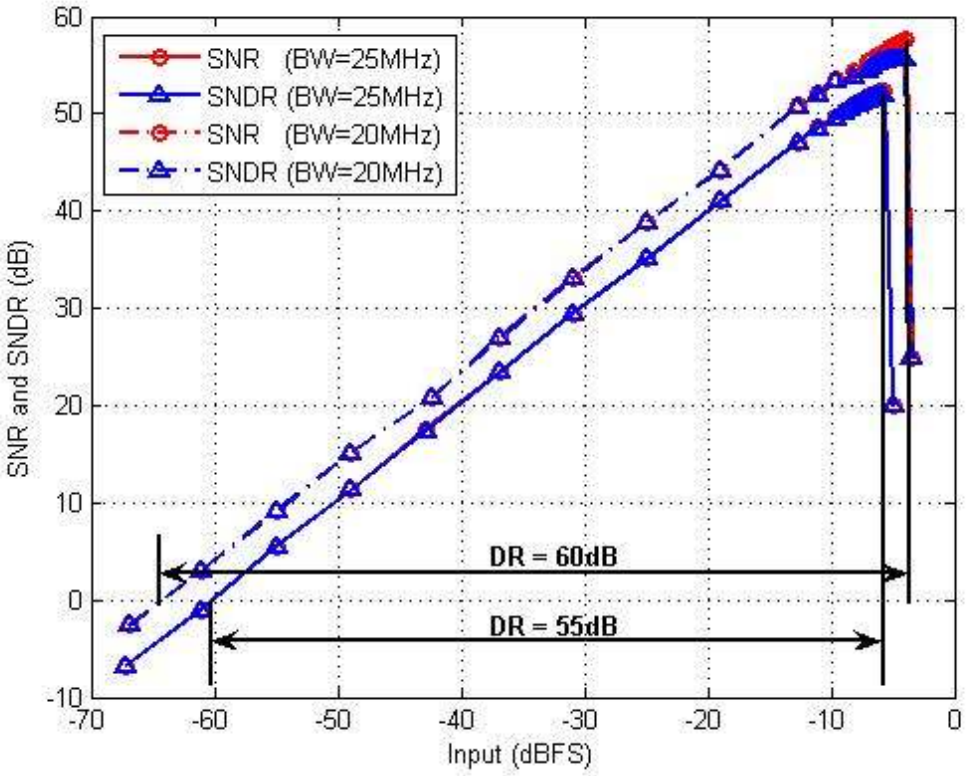



Figure 7.8: SNR and SNDR versus input amplitude with 2 MHz input

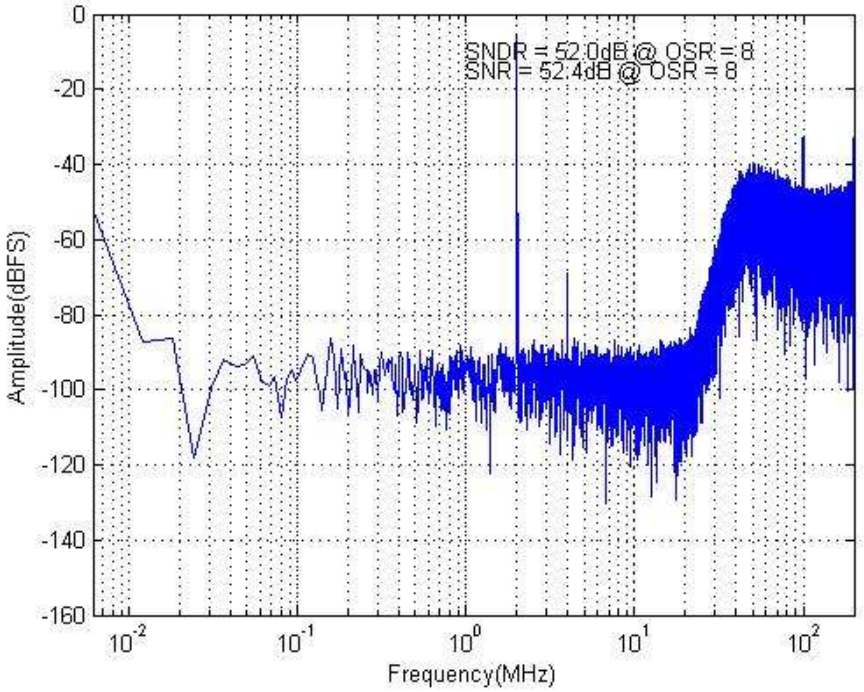



Figure 7.9: Output spectrum of MOD2 (BW = 25 MHz)

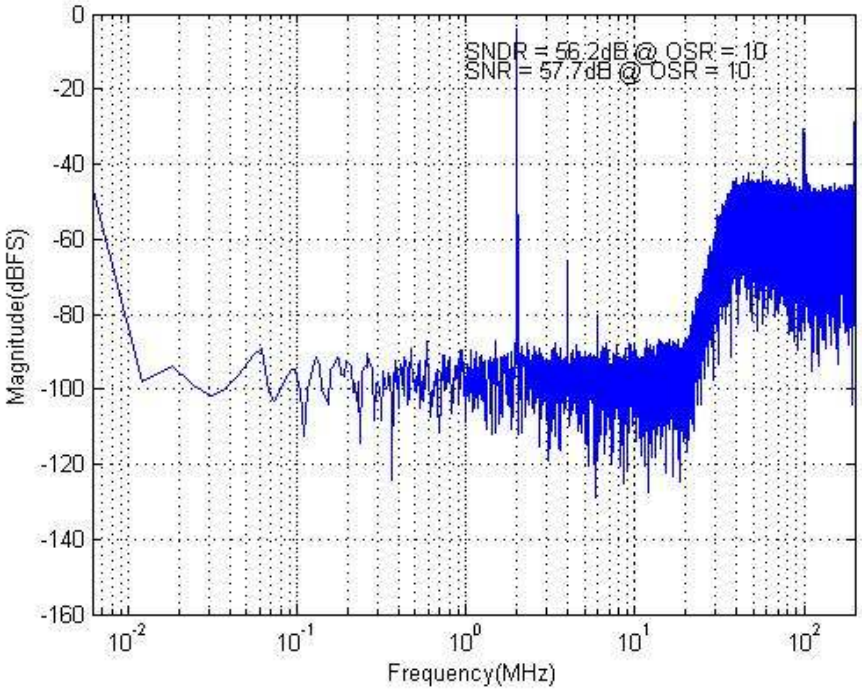



Figure 7.10: Output spectrum of MOD2 (BW = 20 MHz)

From the above output spectrum, it can be seen that big tones reside at the half clock (200 MHz) and quarter clock (100 MHz) frequencies. Those tones are dangerous because they will fold the out-of-band noise into the band of interest and hence increase the in-band noise floor. Those tones come from the clock divider of the logic circuits. A possible path through which they are coupled into the analog part of the modulator is the reference circuits of the feedback DAC. The second harmonic, which increases quickly while the input signal amplitude approaches the peak value, limits the available SFDR.

Input signals with frequencies lower or higher than 2 MHz were also applied to evaluate MOD2. The choices of the frequencies are based on the availability of the passive bandpass filters in our test lab. Table 7.1 lists the peak SNDR and SNR within 25 MHz and 20 MHz band of interest for different input frequencies.

Table 7.1 Test results with different input frequencies

| Input Frequency | BW = 25 MHz | | BW = 20 MHz | |
|---|---|---|---|---|
| | Peak SNDR | Peak SNR | Peak SNDR | Peak SNR |
| 200 kHz | 52.4 | 53.2 | 56.3 | 57.5 |
| 500 kHz | 51.6 | 52.0 | 56.1 | 56.9 |
| 1 MHz | 51.9 | 52.2 | 55.2 | 57.2 |
| 2 MHz | 52.1 | 52.5 | 56.2 | 58.0 |
| 4 MHz | 52.1 | 52.4 | 54.6 | 58.0 |
| 10 MHz | 53.1 | 53.5 | 53.0 | 56.1 |
| 20 MHz | 51.9 | 51.9 | 53.9 | 53.9 |

From above measurement results, it can be seen that for 25 MHz bandwidth, the modulator performance shows little degradation when higher frequency signals are applied. However, for 20 MHz bandwidth, both the distortion and noise floor increase significantly when the input frequency is higher than 10 MHz. Two possible reasons can explain this. First, the linearity of the circuits on the test board as well as the chip itself becomes worse when

high frequency input signals are applied. Second, when the input signal frequency is higher than 10 MHz, the signal harmonics are mostly outside the band of interest. These harmonics will fold the big out-of-band quantization noise into the signal band and hence raise the in-band noise floor.

Table 7.2 shows the summary of the measured chip characteristics while the input signal frequency is 2 MHz.

Table 7.2: Summary of the measured chip results

| Specifications | | Values |
|---|---|---|
| Peak SNDR | BW = 25 MHz | 52 dB |
| | BW = 20 MHz | 56 dB |
| Peak SNR | BW = 25 MHz | 52.5 dB |
| | BW = 20 MHz | 58 dB |
| Dynamic Range | BW = 25 MHz | 55 dB |
| | BW = 20 MHz | 60 dB |
| Clock frequency | | 400 MHz |
| Power supply | | 1.8 V |
| Power consumption | | 18 mW |
| Die area w/o pad | | 1.3 mm × 0.9 mm |
| Fabrication process | | 0.18 $\mu$m 1P6M mixed/RF CMOS |

## 7.4. Comparison Between This Work and Earlier Reported Designs

Table 7.3 lists previously reported wideband (BW ≥ 10 MHz) CT ΔΣ modulators. Compared with them, this work is not the best but still near the top. Because the jitter sensitivity is one of the most important specifications which will affect the design of a CT ΔΣ modulator, it is also listed in the table.

Table 7.3: Performance comparison between reported designs and this work

| Reference | Architecture | SNDR (dB) | BW (MHz) | Jitter Sensi ($ps_{rms}$) | Power (mW) | FOM* (pJ/conv.) |
|---|---|---|---|---|---|---|
| [11] | 2-2 MASH, Real | 56 | 10 | N/A | 122 | 11.83 |
| [12] | $4^{th}$-order, Complex | 68.8 | 23 | 3 | 42.6 | 0.41 |
| [51] | $3^{rd}$-order, Real | 74 | 20 | 0.3 | 20 | 0.12 |
| [52] | MASH, Complex | 69 | 20 | N/A | 56 | 0.61 |
| [53] | $5^{th}$-order, Real | 52 | 10 | N/A | 7 | 1.07 |
| [54] | $4^{th}$-order, Real | 61 | 12 | 20 | 70 | 3.18 |
| [55] | $4^{th}$-order, Real | 61 | 15 | 10 | 70 | 2.54 |
| [56] | $2^{nd}$-order, Complex | 53 | 20 | N/A | 32 | 2.19 |
| [57] | $3^{rd}$-order, Real, time-interleaved | 57/49 | 10/20 | N/A | 87 | 7.5/9.43 |
| My Work | $5^{th}$-order, Real | 52/56 | 25/20 | 5 | 18 | 1.11/0.87 |

* FOM = Power/$(2 \cdot BW \cdot 2^{(SNDR-1.76)/6.02})$. Smaller FOM is better

# CHAPTER 8. CONCLUSIONS

## 8.1. Summary

In this dissertation, the following topics associated with the wideband low-power continuous-time ΔΣ modulator were studied in detail:

- A novel simulation-based synthesis method, used to synthesize a CT ΔΣ modulator from its DT target according to the impulse-invariant transformation.
- A thorough trade-off study was made determining different system-level parameters, based on the considerations of the power consumption, dynamic range requirement and clock jitter sensitivity.
- A traditional feed-forward modulator architecture was modified in several ways to meet our design goals. First, an extra feedback path was introduced to move the first stage out of the $1^{st}$-order loop to reduce the speed requirement, and hence the power consumption of the first opamp. In addition, it also divides the big adder in front of the quantizer into two smaller ones to ease the circuit realization. Second, several direct feed-in branches to the input of each integrator and the adder were added, and optimized to cancel the out-of-band peaking in the signal transfer function, which equivalently increases the dynamic range of the modulator. Third, a direct feedback path was introduced to relax the quantizer delay requirement, addressing the issue of the excess loop delay.
- The effect of the clock jitter in CT ΔΣ modulator was analyzed extensively by modeling the jitter-induced noise with an additive while noise in the feedback

signal. Non-return-to-zero feedback DAC pulse was adopted to reduce the jitter sensitivity.

- Capacitor tuning was integrated to overcome the RC time constant shift due to the variations of the process, supply voltage and working temperature.
- In order to maximize the loop speed, a fast current adder was used, and the sampling capacitor of the comparator minimized.
- A neutralization technique was used to cancel the input capacitor of the comparator, which is introduced by the large-size and hence low-offset input transistors.
- A fully differential layout scheme was used to make the wiring of the differential signals symmetrical to minimize the offset and distortion.

Combining all the above techniques, the modulator achieved 55 dB and 60 dB dynamic range within 25 MHz and 20 MHz bandwidths, respectively. Clocked at 400 MHz, the modulator consumes only 10 mA from a 1.8 V power supply.

## 8.2. Future Work

To improve the performance of this work, e.g., to increase the dynamic range to 12 bits or higher while keeping the bandwidth and power consumption the same, several issues need to be considered:

- Some techniques need to be used to reduce the clock jitter sensitivity further. One possible way to reduce jitter sensitivity is to use non-rectangular, e.g., exponential decaying, feedback DAC waveforms. Another possible way is to use the return-to-zero DAC pulse, while keeping the pulse width very accurate, by using some circuit blocks such as delay locked loop (DLL).

- The number of quantizer levels needs to be increased to improve the dynamic range. However, the power consumption of the quantizer is proportional to the number of quantizer levels. In order to reduce the power consumption, some techniques like tracking-ADC-quantizer [58] should be used to reduce the number of comparators.
- If more advanced semiconductor technologies, e.g., 130 nm, 90 nm or even 65 nm CMOS, are available, the clock rate and the hence the OSR should be increased further, to reduce the aggressiveness of the noise shaping and the number of quantizer levels. An intuitive analysis in this work shows that a high OSR CT $\Delta\Sigma$ modulator is more suitable for low-power design.

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