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A Wideband Sigma-Delta Modulator With Cross-Coupled Two-Paths

Erkan Bilhan, *Member, IEEE*, and Franco Maloberti, *Fellow, IEEE*

***Abstract*—The performance of a sigma-delta analog-to-digital converter (ADC) critically depends on one or more of the main three parameters: over-sampling ratio, the order of the modulators, and the number of bits used. Increasing each one of these parameters presents a degree of challenge (i.e., the increase in the over-sampling ratio is limited by the technology and the power consumption requirement). This paper presents a method to obtain high order noise shaping with N-path architectures that are based on first-order or second-order modulators. The desired noise transfer function (NTF) is obtained by suitable cross-coupling paths. The method was applied to a two-path first-order modulator for obtaining a second-order noise shaping. The performances of the proposed sigma-delta ADC were verified at the behavioral and transistor level implemented in 90-nm CMOS technology.**

***Index Terms*—Analog-to-digital conversion, data conversion, low power, noise shaping, sigma delta.**

I. Introduction

THERE is an increasing demand for low-power data converters because of the portable semiconductor market requests. In addition to low-power, medium resolution and wideband are also required. For a system-on-chip (SoC) solution, the analog sections must work properly in a noisy digital environment and must be designed with digital technologies. Because of these conditions, the sigma-delta method is preferred as it does not need precise components and it consumes less power than the Nyquist rate counterparts.

As it is well known, the resolution of a sigma-delta ADC depends on three design factors: the number of bits of the quantizer, the oversampling-ratio (OSR), and the order of the modulator [1]. A proper choice of these three parameters leads to an optimum power consumption. The number of bits must be limited because of the exponential increase in the area and the power consumption of the ADC, as well as the difficulty in obtaining an effective dynamic linearization of the loop DACs. A high OSR value means using high-sampling frequencies and, in turn, burning more power in the operational amplifiers (op-amp). High-order modulators require an equivalent number of integrators to the order of the modulator and, again, more power. Therefore, a good design strategy, verified by the quantitative study given below, is to use a relatively low order, a low OSR, and the maximum affordable resolution for the quantizer.

Another option, exploited in this paper, is the multipath (N-path) scheme. It reduces the clock frequency in each path at the cost of the replicas of the hardware working in parallel. Reducing the clock frequency by a factor of N reduces the power consumption of the op-amps by a higher factor (close to N^2). Therefore, the duplicated hardware consumes N times more power, but each path consumes much less than $1/N$ and the global power cost is less. In the literature N-path architectures are applied to implement high-speed and -resolution Nyquist rate and sigma-delta converters [2]–[18]. The use of time-interleaved technique in sigma-delta scheme is, however, problematic because each path needs the digital output of previous path that is not immediately available because the modulator is running at $1/N$ speed. Solutions proposed are able to fix the problem only for small N, but methods require additional circuitry and computation effort.

Another feature of the N-path schemes is that they give rise to a $z \rightarrow z^N$ transformation that increases the order of the transfer functions. Therefore, if a single path has p zeros and q poles, the N-path becomes a system with pN zeros and qN poles. The new zeros and poles can be beneficial or detrimental to the operation of the circuit. Indeed, for a plain N-path $\Sigma\Delta$ modulator, the extra zeros of the NTF worsen the signal-to-noise-ratio (SNR). However, as this paper shows, it is possible to suitably move the extra NTF zeros for improving the noise-shaping performances.

This paper first discusses theoretical and practical considerations of N-path $\Sigma\Delta$ modulators and then presents a cross-coupling scheme that increases the order of the modulator without any increase in the number of active components. The proposed cross-coupling scheme is verified by design of a cross-coupled two-path, time-interleaved architecture composed of two first-order modulators, given in Section VI. The two cross-coupled branches bring both zeros of the two path system to $z = 1$ in order to achieve second-order noise shaping. The clock speed in each path is half of the one in a conventional second-order modulator. This leads to using two op-amps that run at half of the clock frequency. The modulator's power efficiency is further improved by using only one time-shared op-amp. The simulations, based on a 90-nm CMOS technology, confirm the expected results and benefits.

II. N-Path Sigma-Delta Architectures

The N-path scheme, shown in Fig. 1(a), has been used in sampled-data filters for transforming a low-pass into a band-pass response. In a typical N-path filter, the input samples are

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E. Bilhan is with the Application Specific Products, Texas Instruments, Dallas, TX 75243 USA (e-mail: ebilhan@ti.com).

F. Maloberti is with the Electronic Department, University of Pavia, 27100 Pavia, Italy (e-mail: franco.maloberti@unipv.it).

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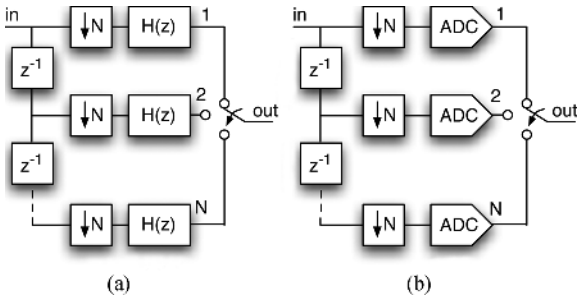

Fig. 1. (a) N-path filter. (b) N-path ADC.

sequentially conveyed to the various paths that run at f_s/N. The outputs of paths are multiplexed to form single data stream path. As mentioned earlier, this scheme realizes the $z \rightarrow z^N$ transformation, resulting in multiplication of zeros and poles. If the single path has zeros or poles around $z = 1$, then the zeros and poles of the N-path architecture are around $z = \sqrt[N]{1}$. For $N = 2$, the transformation generates zeros at $z = \pm 1$. Therefore, in addition to original zeros or poles at $z = 1$ extra zeros at Nyquist change the high-pass response. For $N = 3$ extra zeros or poles are at $\pm 2f_N/3$ giving bandpass feature, and so forth.

The N-path method can be used with data converters [Fig. 1(b)]. For Nyquist-rate architectures this scheme is named as interleaved data converter [2]. The quantization noise affects the output of each path but, because of the multiplexing, each path contributes with only $1/N$ of its power. Therefore, the quantization noise power at the output is equal to the quantization noise power of a single path. The Nyquist-rate data converters give rise to the white quantization noise level, hence the $z \rightarrow z^N$ transformation does not change the noise spectrum. On the contrary, if the N-path architecture is composed of sigma-delta modulators, the quantization noise spectrum of each path is shaped by $\mathrm{NTF}(z)$ and the transformation $z \rightarrow z^N$ yields an output spectrum shaped by $\mathrm{NTF}(z^N)$. If a low-pass nth-order modulator with $\mathrm{NTF} = (1 - z^{-1})^n$ is considered, then the NTF_N of the N-path modulator is

$$\mathrm{NTF}_N(z) = (1 - z^{-N})^n \tag{1}$$

such that, for $N = 2$ and $n = 2$, we have $\mathrm{NTF} = (1 - z^{-2})^2 = (1 - z^{-1})^2(1 + z^{-1})^2$ with two beneficial zeros at $z = 1$, but also two zeros at $z = -1$. These extra zeros are, indeed, a limit to low-pass noise shaping. Their contribution a low frequency gives gain equal to 2. Therefore, a plain two-path second-order scheme experiences a loss in SNR of 12 dB.

The above shows that, for example, a two-path scheme with second-order modulators yields a fourth-order NTF, but two of the zeros are in the wrong positions that degrades performance. Therefore, it would be better to have just two zeros (obtained with a two-path first-order architecture) but placed both at the beneficial place $z = 1$.

A. Moving Zeros in an N-Path Sigma-Delta Architecture

The target of a low-pass sigma-delta modulator is to have all of the zeros at $z = 1$ (or, in some cases, to have pairs of them in complex conjugate places, but close to $z = 1$, inside the signal band). Therefore, the target of an nth-order modulator is to generate

$$\mathrm{NTF} = (1 - z^{-1})^n. \tag{2}$$

Due to the demand on low power and limits imposed by the finite matching between components, the order of the modulator must be low. This limits design choices to a second-, third-, or, rarely, fourth-order modulator architectures. Therefore, target NTF is one of the following:

$$\mathrm{NTF}_2 = 1 - 2z^{-1} + z^{-2} \tag{3}$$

$$\mathrm{NTF}_3 = 1 - 3z^{-1} + 3z^{-2} - z^{-3} \tag{4}$$

$$\mathrm{NTF}_4 = 1 - 4z^{-1} + 6z^{-2} - 4z^{-3} + z^{-4}. \tag{5}$$

Notice that coefficients of intermediate terms increases with the order, and the sign of the highest order term is $+1$ for even paths and -1 for odd orders. Having large coefficients, as we will see shortly, negatively affects the feedback factor of op-amps. Moreover, the sign in the highest order term needs some attention for the N-path realization.

Let us again consider the (1) and focus on the highest order term. A two-path first-order modulator gives rise to $-z^{-2}$. A three-path first-order scheme produces $-z^{-3}$, while a two-path second-order modulator yields $+z^{-4}$. The sign of the highest order term is the correct one for the third- and the fourth-order shaping, but not for the second-order shaping. In order to have the right sign for second-order shaping, it is necessary to use in the parallel paths $\mathrm{NTF} = (1 + z^{-1})$ instead of $\mathrm{NTF} = (1 - z^{-1})$, as it is actually done in the demonstrating design.

The NTF_N expressed by (1) provides only the terms of the type $a_i z^{-N \cdot k}$. Therefore, the missing terms and the different coefficients must be introduced to obtain the desired NTF. Equation (1) can be the basis for building the needed transfer function but additional actions are necessary. The required modification of NTF_N uses one of the following methods:

- modifying the path transfer function by moving pair of zeros out of $z = 1$ onto the unity circle;
- generating extra terms by adding cross-coupled paths to the architecture.

Consider the three basic schemes shown in Fig. 2 that use the basic functions

$$H(z) = \frac{1}{1 - z^{-1}} \quad \text{or} \quad H(z) = \frac{1}{1 + z^{-1}} \tag{6}$$

in the path, depending on the necessity. In these figures, the quantizers are represented by the addition of the quantization noise ϵ_i, i.e., the linear equivalent. The following three observations can be made: 1) the parallel paths operate with some delay in comparison to one another; 2) there are possible extra inputs (the one indicated with arrows in the diagrams; with or without delay) in addition to the main inputs; and 3) the quantization error of each path (i.e., the difference between the integrator output and the digital-to-analog converter (DAC) voltage produced according to the digital code) can be easily generated.

These three observations are the basis of the method used here. The quantization noise of one path can be conveniently injected at the main input or one of the auxiliary inputs of other paths for benefiting of the granted delay [18]. Actually, the extra

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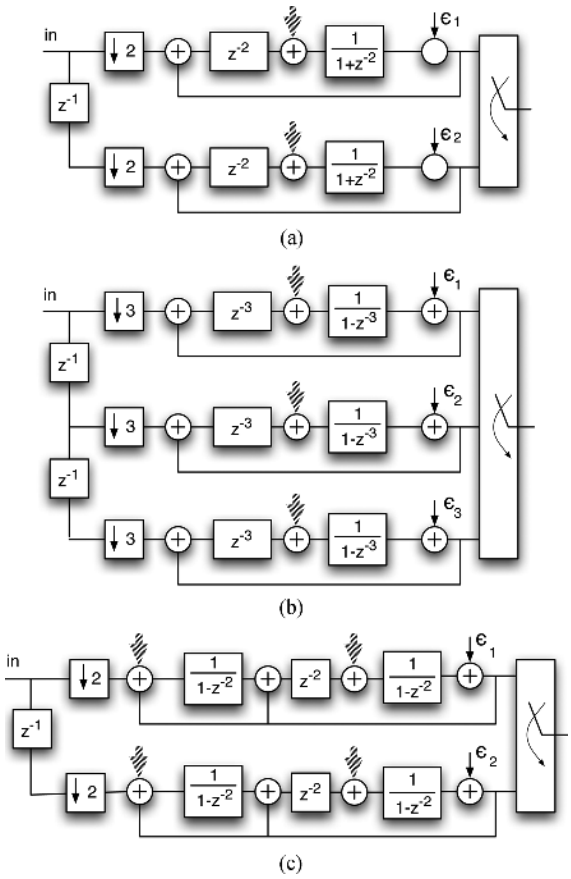

Fig. 2. (a) Two-path of first-order modulators. (b) Three-path of first-order modulators. (c) Two-path of second-order modulators.

injection will show up at the other output, but the multiplexing will properly combine the various terms acting on the same quantization noise.

If the extra noise injection is at the main input of a path, the contributed term will be the relative delay of the path multiplied by its signal transfer function (STF). For the injections at an intermediate point, it is necessary to estimate and use the transfer function from that point to the output. It can be necessary to multiply the quantization noise by an appropriate factor and, eventually, a negative sign obtained by swapping the fully differential signals can be necessary.

III. Power Consumption Minimization

The value of the sampling capacitor of the first switched-capacitor (SC) integrator affects the power consumption of the modulator [21]–[23]. There are two design constraints that set the minimum value for the sampling capacitor: the thermal (kT/C) noise and the matching requirements. For the first constraint, the sampled noise on the input capacitance dominates total thermal noise. Other noise sources are inside the loop, hence their noise contributions are significantly shaped. The thermal noise from the input sampling capacitor is reduced only by the oversampling factor OSR. Since the kT/C contribution of the input capacitance must be less than one half of the least-significant bit (LSB), it is necessary to have

$$C_{\rm in} > \frac{4 \cdot kT}{\Delta^2 \cdot {\rm OSR}} \tag{7}$$

where $\Delta = V_{\rm Ref}/2^{N_{bit}}$ and $V_{\rm Ref}$ is the DAC reference. The thermal noise sets the minimum value of the sampling capacitor for high-resolution modulators, ,but for 60–70-dB SNR, the required capacitance is smaller than allowed minimum capacitance of modern technologies.

The second limit depends on the accuracy required for the feedback capacitance and the unity capacitance of the DAC (that, indeed, can slightly scale down with many elements). The two lower limits $C_{f,\min}$ and $C_{U,\min}$ and the number of bits of the quantizer N_Q determine the minimum input capacitance

$$C_{\rm in,min} = \max[C_{f,\min}; 2^{N_Q} \cdot C_{U,\min}]. \tag{8}$$

The power of an op-amp depends on the transconductance gain whose value is established by needed unity gain frequency and load capacitance $(g_m = 2\pi C_L f_T)$ [24]. Moreover, C_L is proportional to $C_{\rm in}$. Since, for a given feedback factor β the clock frequency $f_{\rm CK}$ must be lower than βf_T, it is necessary to verify

$$g_m = \frac{\alpha \cdot 2\pi f_{\rm CK} C_{\rm in}}{\beta} \tag{9}$$

where α is the margin factor that increases with the desired resolution. A typical value of α for medium resolution is 4. Moreover, remembering that, for MOS transistors in saturation $g_m = 2I_D/V_{\rm ov}$ ($V_{\rm ov}$ = overdrive voltage), the power of the first op-amp can be approximated by

$$\begin{aligned} P_1 &= \gamma V_{\rm DD} I_D \\ &= \gamma V_{\rm DD} \left[\left(\frac{V_{\rm ov}}{2} \right) \left(\frac{\alpha \cdot 2\pi f_{\rm CK} C_{\rm in}}{\beta} \right) \right] \end{aligned} \tag{10}$$

where γ indicates how many I_D's are used in the op-amp (from four to eight for a two-stage or a cascode amplifier).

For a second-order modulator, the power required for the second op-amp is lower than that for the first op-amp because the kT/C noise and the mismatch errors after the first integrator are shaped. Thus, the capacitance of second stage can be scaled down. Typically, the second op-amp uses only half of the power of the first op-amp.

Other components that consume power are the comparators of the quantizer. Their power depends on clock speed and resolution. An equation for the comparator's power can be obtained by curve fitting the Spice simulation results of a pre-amp followed by a latch. A possible approximation is

$$P_c = \eta V_{\rm DD} f_{\rm CK} \left(1 + \frac{\theta}{\Delta} \right) \tag{11}$$

where η and θ are parameters that depend upon the technology used. The above fitting curve can be obtained for a specific technology from simulations with variable input and given accuracy target at different clock frequencies. The parameters η and θ are extracted with best fitting method.

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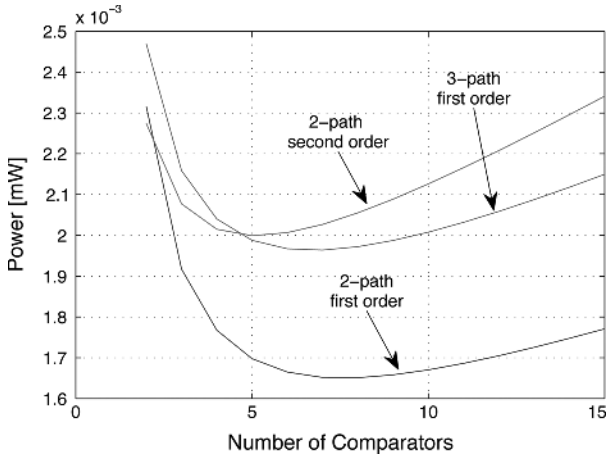

Fig. 3. Power versus the number of comparators for the three multipath schemes of Fig. 2.

The above equations lead to optimum design that can be then obtained with the one of the schemes of Fig. 2. Using typical parameters related to a modern 90-nm CMOS technology gives the plot of Fig. 3. The target SNR is 62 dB. The result is that high-order architectures give a more effective noise shaping and enables a lower OSR, but the less favorable feedback factor increases the requirements of the op-amp. The total power consumption is lower for the two-path first-order modulators. Another significant result is that there is an optimum number of comparators for quantizer. The trade-off comes from the reduction of op-amp power for lower OSR and the need of power for higher number of more demanding comparators. The optimum is in the range of five to ten comparators.

IV. Two-Path Sigma-Delta ADC

Fig. 4 shows two-path scheme with first-order modulators. In the Fig. 4(a), the loop transfer function $z^{-2}/(1+z^{-2})$ is distributed along the loop, as done in Fig. 2(a) for avoiding extra delay in the quantization error paths. The two-paths shown in Fig. 4(a) use the same clock control running at half of the sampling frequency.

The scheme foresees the injection of the quantization error from the bottom path with zero delay to the other path, which can be problematic for real implementations. This limit is eliminated by moving the delay from the output to the input in the upper path for obtaining the diagram of Fig. 4(b). The clock schemes of the paths are delayed with respect to the other, but a full period delay in both cross-coupled paths results. The delay can be conveniently used in the circuit implementation to allow the time needed for the quantization.

Fig. 5 shows the output spectrum obtained by a behavioral simulation of the diagram of Fig. 4(b). The slope at low frequency is the expected 40 dB/dec. With a 3-b quantizer, the peak SNR is 65 dB and occurs at -12 dB$_{\rm FS}$.

The scheme in Fig. 4 uses the transfer function $1/(1+z^{-2})$. This transfer function can be obtained by the $z \longrightarrow -z$ transformation, [19], [20], followed by the $z \rightarrow z^2$ transformation applied over $1/(1-z^{-1})$ to yield

$$\frac{1}{1-z^{-1}} \underset{z \rightarrow -z}{\longrightarrow} \frac{1}{1+z^{-1}} \underset{z \rightarrow z^2}{\longrightarrow} \frac{1}{1+z^{-2}}. \tag{12}$$

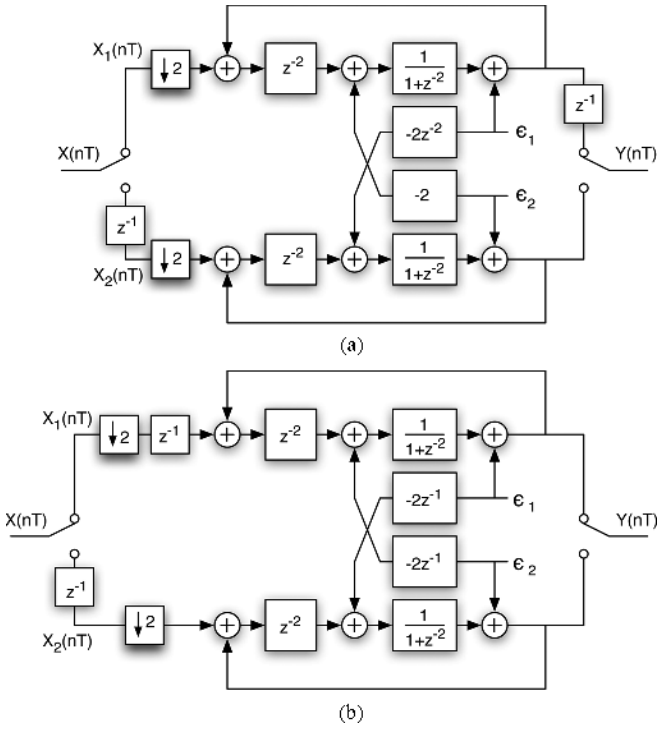

Fig. 4. Two-path cross-coupled scheme with first order modulators. (a) With the two paths running with the same clock and (b) with delayed clocks on the two paths.

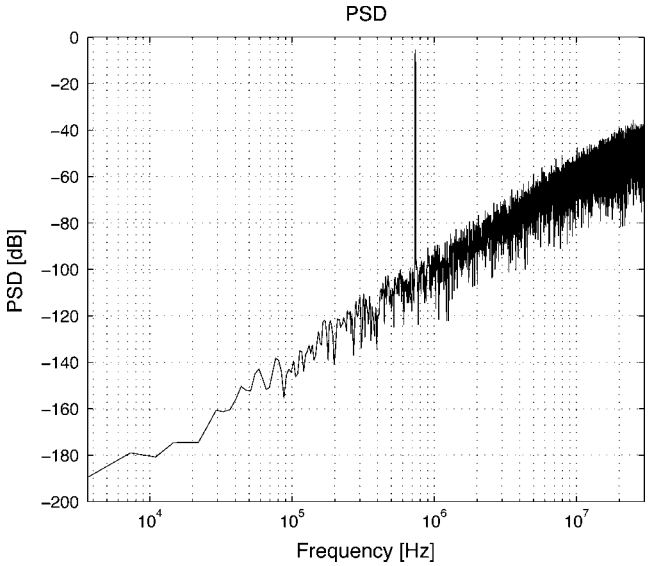

Fig. 5. Output spectrum obtained by a behavioral simulation of the diagram of Fig. 4(b).

Notice that the operator $1/(1+z^{-1})$ realized by the diagram of Fig. 6(a) in the time domain obtains

$$-Y(nT+T) = Y(nT) - X(nT) \tag{13}$$

$$Y(nT+2T) = -Y(nT+T) + X(nT+T) \tag{14}$$

$$-Y(nT+3T) = Y(nT+T) - X(nT+2T) \tag{15}$$

and so forth, indicating that, if the input is multiplied by a square wave signal, the output is the square wave modulation of the expected result. This is obtained with the scheme of Fig. 6(b).

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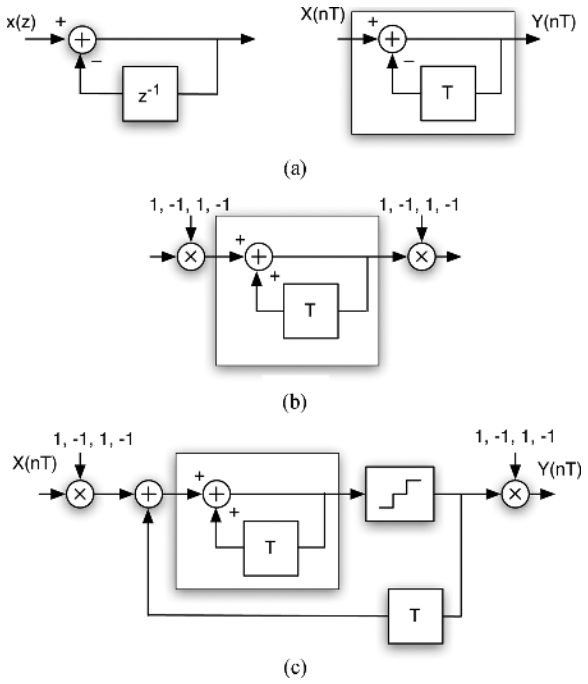

Fig. 6. (a) Scheme that obtains $H(z) = (1+z^{-1})$. (b) Its implementation with a conventional time-domain integrator. (c) Use of the basic block in a first-order sigma-delta modulator.

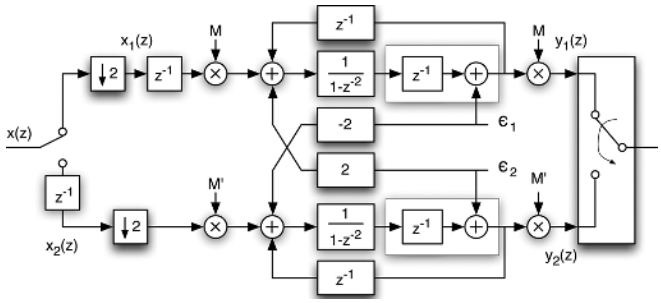

Fig. 7. Two-path cross-coupled scheme based on the scheme of Fig. 6 and the basic block of Fig. 4(b).

When used in the first-order sigma-delta modulator it is placed in feedback loop with a quantizer. However, these two nonlinear modulation blocks can be moved to the both ends, input and output of the sigma-delta modulator, to obtain a linear section. The result is shown in Fig. 6(c) that contains a conventional integrator.

The diagram shown in Fig. 6(c) can be viewed as a double chopper for the input signal and a single chopper for the quantization noise. The effects of choppers on the signal cancel out each other while chopping the noise at half of the clock frequency gives rise to a low-pass to high-pass transformation.

The solution illustrated in Fig. 6(c) is applied to the two-path scheme of Fig. 4(b), and the resulting system is shown in Fig. 7. Notice that one unity delay element is incorporated into the quantizer because in the real circuit the flash and the DAC needs some operational time. One of the cross coupled connections changes its polarity and becomes two because, for ϵ_2, the modulation through the upper and the lower paths have opposite signs.

TABLE I
SIMULINK MODEL PARAMETERS

Signal Bandwidth	2MHz
Output Data Rate	60MHz
OSR	15
Input Amplitude	$-3\,dB$
Input Frequency	$736\,KHz$

The decimation by a factor of two at the input delivers the even input samples to the upper path and the odd samples to the lower path; one is delayed with respect to the other, as shown by

$$x(z) = x_1(z) + x_2(z). \tag{16}$$

The output and quantization noise of the even path shows up at the odd times and the output and quantization noise of the odd path is available at even times. Therefore, there is a delay z^{-1} to consider. For this reason, the quantization noise of the upper and lower paths are denoted as ϵ_o and ϵ_e, respectively. The following results can be obtained by inspecting the block diagram

$$y_1(z) = [x_1(z) - 2\epsilon_2]z^{-1} + \epsilon_2(1 + z^{-2}) \tag{17}$$
$$y_2(z) = [x_2(z) - 2\epsilon_1]z^{-1} + \epsilon_1(1 + z^{-2}). \tag{18}$$

Since the output consists of adding the even and odd components, accounting for the extra delay at the input before the decimation results in

$$y(z) = x(z)z^{-2} + \frac{\epsilon_1 + \epsilon_2}{2}(1 - 2z^{-1} + z^{-2}). \tag{19}$$

This is the expected noise shaping. Note that the division by two of the quantization error contributions accounts for the effect of the interpolator.

V. SYSTEM-LEVEL SIMULATIONS

Accuracy of the proposed two-path sigma-delta architecture depends on the mismatch between paths and limitations caused by the op-amps used. The Simulink simulation uses the op-amp model described in [25], which accounts for the finite gain, bandwidth, and slew-rate. Moreover, a proper injection of white noise models the kT/C limit. We use an ideal modulator model to benchmark the results. The design parameters used for the Simulink simulations for both models are summarized in Table I. Each of the modulator parallel paths is composed of an integrator, a flash ADC with eight comparators as the quantizer, and a nine-level feedback DAC, which is the same as in its conventional counterpart.

The proposed modulator architecture cross couples the quantization noise with a gain of two. Therefore, the number of quantization levels that obtain optimum power consumption is also beneficial to prevent saturation and overloading of integrator and quantizer with large input signals. Behavioral simulations showed that a nine-level quantizer and feedback DAC ensures proper operation for input signals until $-3\,\mathrm{dB_{FS}}$. However, multilevel DAC possibly introduces nonlinearity due to component mismatch errors. Since modern technologies exhibit 10–12-b matching for capacitors, only for high-performance

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TABLE II
SIMULATION RESULTS

GBW [MHz]	Slew-rate [V/μs]	SNR [dB]	Note
60	100	44	large harmonic tones
60	125	63.1	harmonic tone at $-60\,dB_c$
60	150	63.7	
60	175	64.4	
60	200	64.6	
90	100	44.9	large harmonic tones
90	125	63.8	harmonic tone at $-64\,dB_c$
90	150	63.8	
90	175	64.9	
90	200	64.4	

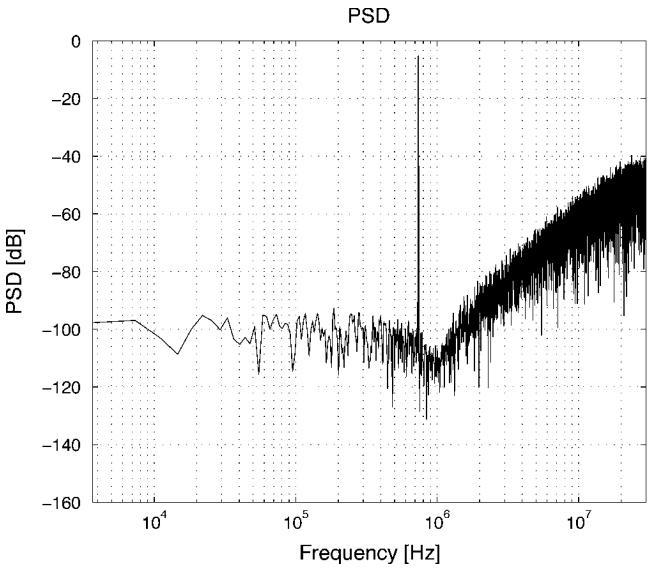

Fig. 8. Output spectrum of the diagram of Fig. 4(b) with a gain of 100 of the used op-amp.

ADCs, it may be necessary to apply DAC linearization methods [26]–[28].

Extensive simulations show that the main performance limitation comes from op-amp's unity gain bandwidth (GBW) and the slew rate. As shown in Table II, it is necessary to ensure a GBW that is about the clock frequency (two times the clock of each path). Increasing the GBW does not give significant benefits. The slew rate must be above $150\ \mathrm{V}/\mu\mathrm{s}$, which is large but affordable. Path mismatch is a significant limit for large SNRs that are obtained with higher OSR and more levels in the quantizer. If the target SNR is around 60 dB, it is required to ensure a matching better than 0.4% for having less than 1 dB loss in the SNR.

The effect of the finite gain is beneficial until a given level because it shifts the zeros to complex conjugate positions. Fig. 8 shows the simulated output spectrum with $GBW = 60$ MHz, $slew-rate = 150\ \mathrm{V}/\mu\mathrm{s}$, and $A_0 = 100$. The combined action of the three parameters shifts the zeros to around 1 MHz; this enhances the SNR to 66 dB, the value of the ideal case with OSR $= 15$.

VI. CIRCUIT DESIGN AND SIMULATIONS

The circuit implementation for the scheme in Fig. 7 requires using two op-amps, one for each path. Fig. 9 shows a possible

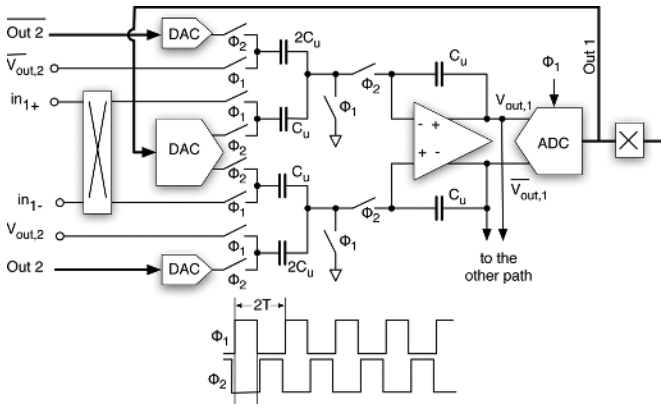

Fig. 9. Circuit schematic of one of the paths of the scheme of Fig. 7 and phase scheme.

SC implementation for one of the two paths. The scheme that indicates the modulation at the input and output schematically uses a fully differential op-amp and feedback capacitors. The minimum value of the capacitors is determined according to the technology's requirements such that to satisfy the kT/C limit and constraint by the OSR and the full-scale voltage. For the target specification, it is necessary to ensure $C_u > 100$ fF. There are two injecting elements at the input of the integrator; the one equals to C_u is for the input and the feedback DAC. The other one equal to $2C_u$ is for the cross-coupled path.

The DAC can be made by a Kelvin divider made by resistors. Alternatively, the input capacitances can be divided into subelements for realizing a capacitor-based DAC. Therefore, for a nine-level DAC and the use of three-level references ($V_{\mathrm{Ref}+},\ V_{CM},\ V_{\mathrm{ref}-}$), the unity element is 1/4 of the value used as in feedback path of the op-amp. For matching reasons, the minimum element cannot be lower than a given value established by the technology. For the 90-nm technology used for the demonstrating design, the recommendation is to use $C_u > 50$ fF. Therefore, the feedback element becomes $C_f > 200$ fF.

The phase scheme depicted in Fig. 9 outlines the decimation by a factor of two. The inputs are sampled during the phase Φ_1, and integration occurs during Φ_2 together with the DAC's operation. The ADC starts the conversion at the beginning of phase Φ_1. Therefore, there is a full period T for the path loop, but the operation of the cross-coupled DAC must be completed during the phase Φ_1. This does not present a problem, because the speed of the flash is much higher than the speed of one of the op-amps.

For the operation described above, the op-amp of one of the paths integrates the input during the even clock periods and the other during the odd ones. Therefore, it is possible to time-share an op-amp between two paths in order to reduce the number of the active components and, consequently, the power consumption [29]. For this, it is necessary to double the feedback elements with a pair of switches that are periodically disconnected from the op-amp to operate as analog memory. For each differential input, as shown in Fig. 10, there are four input structures: two that inject during the phase Φ_1 and the others during the phase Φ_2. The quantizer runs at the full clock speed of the

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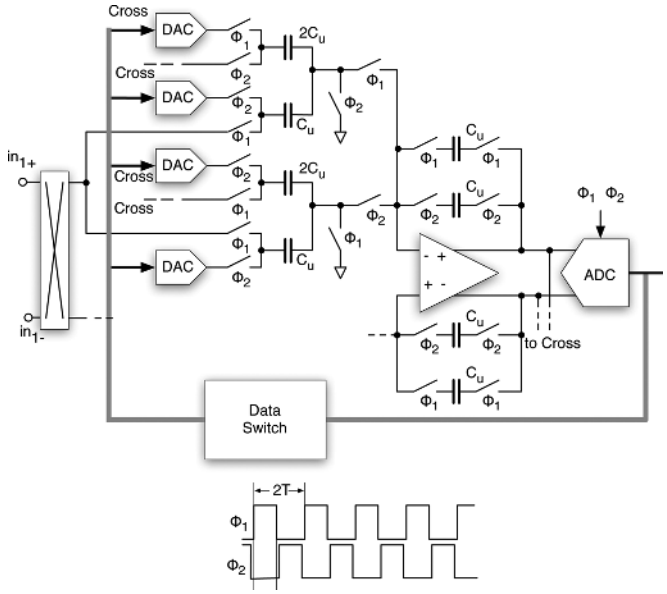

Fig. 10. Circuit schematic for a time-shared implementation.

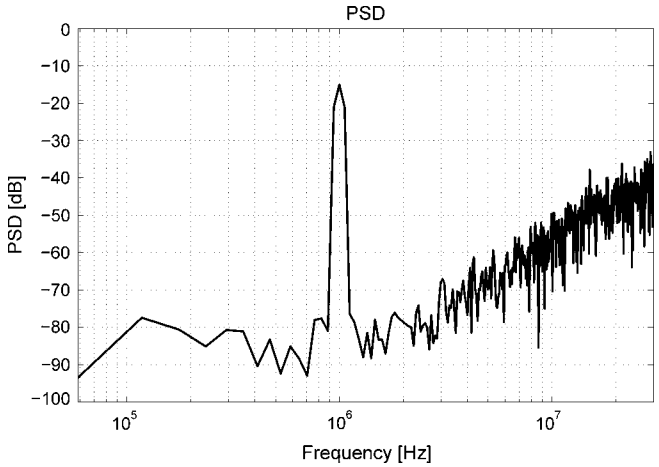

Fig. 11. Spectrum from a transistor-level simulation.

modulator and provides the digital data for signal reconstruction and for the feedback DAC of the paths and the cross-coupled connections.

The scheme in Fig. 10 has been simulated at the transistor level. The integrator is implemented using a fully differential two-stage op-amp with a folded cascode first stage followed by a common-source second stage. The open loop gain is 82 dB, $\mathrm{GBW} = 80$ MHz and 52° phase margin for a feedback factor of -13 dB. The slew rate is $173\ \mathrm{V}/\mu\mathrm{s}$.

The power spectral density presented in Fig. 11 has been obtained after a transient simulation lasting for 2048 clock periods. As expected, the noise shaping is second-order and the SNR is 53 dB. This value closely matches with the result obtained from behavioral simulations for the same input signal level of -12 dB.

The proposed architecture increases the order of a first-order two-path modulator to yield a second-order system. This enables reduction in the OSR and, consequently, the operating speed of the modulator. Compared with a conventional second-order system, the proposed architecture operates at half of the operating speed and provides the same performance. Another advantage comes with the fact that time interleaving makes it easier to time-share the op-amp between the two paths in order to reduce the number of required active components. Therefore, for a conventional second-order modulator, it is necessary to use two op-amps running at full speed. The time-interleaved solution uses two op-amps running at half-clock speed or, alternatively, only one time-interelaved. The circuit implementation of the modulator provides 9 b of resolution while consuming 1.56 mW from a 1.2-V power supply. Power consumption is better than the one foreseen in Fig. 3 because of time-sharing the op-amp. Notice that use of time-sharing is not equivalent to going back to full-speed operation but corresponds to exploiting the clock period during which the op-amp is not working. Time-sharing the op-amp can also be applied in conventional second-order modulators, but, in that case, the clock is full clock. The power-saving benefits of time-sharing the op-amp cannot be fully realized due to the fact that the slew-rate must increase as behavioral model suggested. Therefore, the two-path method reduces power by about 1.6 (the benefit is not 2 because of additional bandwidth requested by extra inputs), the time-sharing adds an additional 1.6 reduction factor, leading to a total $\times 2.5$ power reduction. A summary of this work's results along with some recent works is given in Table III. Notice that the last line of the table reports the FoM (figure of merit) as defined in [30]. As known, comparison depends on technology and safety margin used. However, this conservative design, as required to obtain good yield in industrial products, achieves a FoM well below 1 pJ.

TABLE III
COMPARISON WITH RECENT WORKS

	[18]	[31]	[32]	ThisWork
Fs [MHz]	120	120	153	60
BW [MHz]	2.5	2.5	1.92	2
Order	3rd	3rd	4th	2nd
SNR [dB]	81	77.6	72.02	56
Power [mW]	15	19	14	1.56
FoM [pJ]	0.33	0.66	1.12	0.75

VII. CONCLUSION

Using time-interleaved sigma-delta ADC architecture with cross-coupled quantization noise offers design flexibility and increases the order of the system, the power effectiveness due to reduced OSR, and required active components for a second-order two-path modulator. Depending on the target specifications, it is possible to identify the best tradeoff between the order of the modulator, the number of bits of the quantizer, and the OSR. For medium resolution (10-b) and 2-MHz bandwidth, the optimum is a two-path scheme with first-order modulators. The proposed sigma-delta modulator architecture has been verified, and results are obtained trough the simulations of the complete ADC circuit designed in 90-nm CMOS technology.

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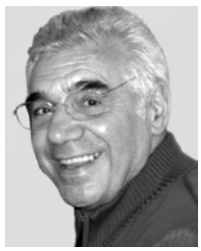
Erkan Bilhan (M'06) received the B.S. degree in electronics and communications engineering from Istanbul Technical University, Istanbul, Turkey, in 1997, the M.S. degree in electrical engineering from Texas A&M University, College Station, in 2001, and the Ph.D. degree in electrical engineering from the University of Texas, Dallas, in 2008.

He joined Texas Instruments, Dallas, in 2001, where he is currently an Analog Mixed-Signal Design Engineer. His research interests involve data converters, phase-locked loops, and power management circuits.



Franco Maloberti (F'96) received the Laurea degree in physics (*summa cum laude*) from the University of Parma, Parma, Italy, in 1968 and the Dr. Honoris Causa Ph.D. degree in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996.

He is a Professor of Microelectronics and Head of the Micro Integrated Systems Group, University of Pavia, Italy. In 1993, he was a Visiting Professor with The Swiss Federal Institute of Technology (ETH-PEL), Zurich, Switzerland and in 2004 a Visiting Professor with EPFL, Lausanne, Switzerland. From 2000 to 2002, he was the TI/J.Kilby Analog Engineering Chair Professor with Texas A&M University and, from 2002 to 2004, the Distinguished Microelectronic Chair Professor with the University of Texas, Dallas. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog–digital applications, mainly in the areas of switched-capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A/D design. He has written more than 380 published papers, four books, and holds 29 patents.

Dr. Maloberti was VP Region 8 of IEEE CAS (1995–1997), the 2002–2003 President of the IEEE Sensor Council, Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II—EXPRESS BRIEFS (TCAS-II), an IEEE Circuits and Systems (CAS) BoG member (2003–2005), VP Publications of the IEEE CAS Society (2007–2008) and President of the IEEE-PRIME Steering Committee. He is a Distinguished Lecturer of the IEEE Solid-States Circuits Society. He was the recipient of the 1999 IEEE CAS Society Meritorious Service Award, the 2000 CAS Society Golden Jubilee Medal, the IEEE Millenium Medal, the 1996 IEE Fleming Premium, the 2007 ESSCIRC Best Paper Award, and the 2007 IEEJ Workshop Best Paper Award.

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