A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS

R. Shrestha[1], R.A.R Van der Zee[1], A.J.M de Graauw[2], and B. Nauta[1]

[1]University of Twente, Enschede, The Netherlands
[2]NXP, Eindhoven, The Netherlands
Email: r.shrestha@utwente.nl

Abstract

A wideband modulator for a 20MHz bandwidth polar modulated PA is presented which achieves a maximum efficiency of 87.5% and a small signal -3dB bandwidth of 285MHz. Realized in 65nm CMOS, it consists of a cascoded nested Miller compensated linear amplifier and a class D switching amplifier. It can deliver 22.7dBm output power to a 5.3Ω load. With a switching frequency of 118MHz, the output switching ripple is 4.3mVrms.

Keywords: supply modulator, power amplifier, CMOS and cascoded nested Miller.

Introduction

The rapid increase in demand for high data-rates has led modern wireless standards to use spectrally efficient complex modulation schemes that contain information both in amplitude and phase. Amplifying those signals using a conventional linear Power Amplifier (PA) does preserve modulation accuracy and limits spectral regrowth but suffers from poor efficiency due to the high peak to average power ratio of the signal. Polar modulation transmitter architectures, where a phase modulated signal with constant envelope is amplified by a non-linear PA and the amplitude information is restored via its power supply, have the potential to enhance the efficiency. However, switching modulators used in such architectures must have high bandwidth, several times higher than the signal bandwidth, and low switching ripple while achieving high efficiency even at large power back-off. As a result, state-of-the-art implementations [1,2,3] of supply modulators are reported either only for standards with at most a few MHz of signal bandwidth or for envelope tracking systems [4] where the accuracy of the modulator is less important.

This paper presents a modulator for a 20MHz signal bandwidth polar modulated PA. Fabricated in a 65nm CMOS process, it achieves a peak efficiency of 87.5% and a small signal -3dB bandwidth of 285MHz.

Overview of the operation

Fig. 1 shows the architecture of a polar transmitter with the modulator comprising of a self oscillating parallel linear and switching amplifier [5]. The linear amplifier (AB) takes care of the linearity while the switching amplifier (D) supplies most of the current ensuring high efficiency. The amplifier AB is used in feedback mode not only to reproduce the input envelope with low distortion but also to attenuate the switching ripple of switching amplifier D. The control signal for the switching part is derived by copying the output current of AB and comparing it with a threshold level using a hysteretic comparator. If the output current of AB exceeds a threshold, D injects a large current via L_1. This way, D supplies most of the current and the

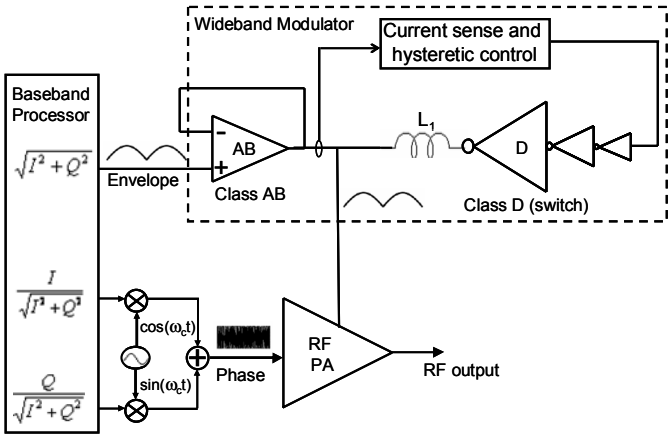


Fig. 1 Polar modulated transmitter architecture.

AB-D system is self-oscillating.

The amount of switching residue generated by the combined amplifier depends on the inductor L_1 and on the output impedance of amplifier AB. AB should have a low output impedance at the switching frequency to suppress the switching noise of amplifier D which could directly affect the output PA spectrum. Also, the bandwidth of the modulator should be several times higher than the signal bandwidth to avoid distortion since the input envelope bandwidth is much higher than the signal bandwidth. To meet these very demanding requirements we used a three-stage cascoded nested Miller compensated amplifier with rail-to-rail input and output as shown in Fig. 2. This configuration is obtained by connecting an outer miller capacitor C_{m2} to the source of the cascode transistor of the first stage [6]. The cascode transistor buffers the Miller capacitor current and feeds it into equivalent capacitor C_g at the gain node, which converts it back to a voltage. So when $C_{m2}>C_g$, the maximum feedback factor can

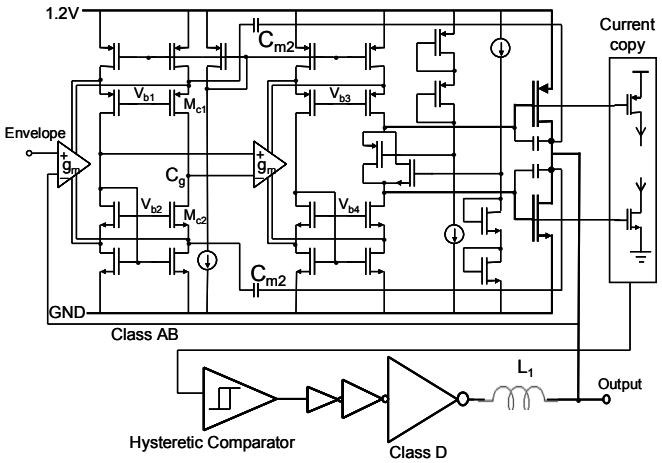


Fig. 2 Detailed circuit diagram of the Supply Modulator.

be larger than 1 by a factor C_{m2}/C_g. This permits a higher unity gain frequency and decreases the output impedance.

The class D amplifier is simply a chain of inverters. The choice of L_1 depends on the envelope bandwidth, power dissipation in AB and the switching frequency. The sum of conduction loss and switching loss are minimized by proper dimensioning of the power- and driver transistors, leading to a switching frequency of 100MHz, and W/L of 9k/0.06 (PMOS) and 3k/0.06 (NMOS) for the power transistors. The driver transistors are 7.5 times smaller.

Measurement results

The output inductor L_1 in fig. 2 is 80nH, off-chip. Fig. 3 shows the measured DC efficiency performance of the supply modulator with respect to its output power with a 5.3Ω load and a supply voltage of 1.2V. It delivers 22.7dBm of output power with a peak efficiency of 87.5%. The efficiency stays above 40% with 10dB of output power back-off. When compared to the measured efficiency of the stand-alone AB amplifier for the same 10dB of output power back-off, the presented modulator shows an efficiency that is almost double as high. The switching ripple is 4.3mVrms at the switching frequency of 118MHz.

Fig. 4(a) shows the measured output impedance of the amplifier AB. The output impedance is below 0.21Ω up to 50MHz frequency. At 100MHz the output impedance is 0.5Ω.

The amplitude of a IEEE 802.11g WLAN signal is applied to the modulator with a 5.3Ω load. Fig. 4(b) shows the superimposed input and output waveforms. The measured small signal (-3dB) bandwidth of the modulator is 285MHz and the power bandwidth, the bandwidth over which an amplifier can deliver at least half of its maximum output power, is 45MHz.

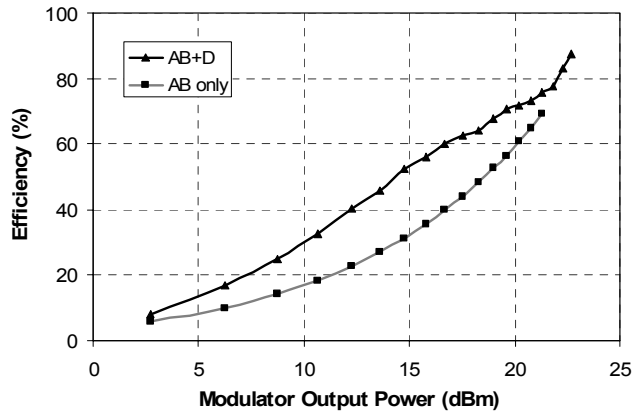
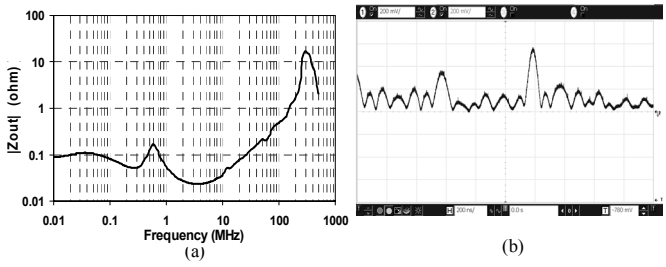


Fig. 3 Measured efficiency performance of the supply modulator.



(a) (b)

Fig. 4 (a) Measured output impedance of AB, (b) Superimposed input and output waveforms of the modulator for the amplitude of the IEEE 802.11g WLAN signal.

These measurements suggest that the modulator is good enough to use for WLAN purposes. However, unlike some existing literature, we think the only way to show that the supply modulator is really good enough is to feed it with the actual WLAN signal, connect it to an RF PA and observe the output spectrum. This is shown in Fig 5. We see that the spectral mask is satisfied, even including all non-idealities of the RF PA. The chip micrograph is shown in Fig. 6.

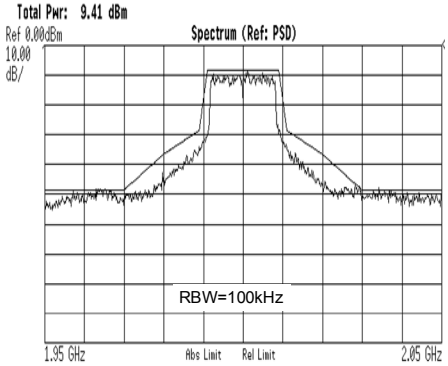


Fig. 5 Measured RF PA output spectrum with the presented modulator for IEEE 802.11g WLAN signal.

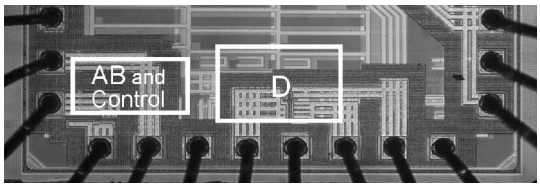


Fig. 6 Chip Micrograph. The active area of the modulator is $0.1043mm^2$.

Conclusions

The presented modulator has a much larger bandwidth than previously reported in literature for polar modulation applications while achieving a peak efficiency of 87.5%. At 10dB back-off the efficiency is more than 40%. The small signal bandwidth is 285MHz and the switching ripple is as low as 4.3mVrms.

Acknowledgement

This work was supported by NXP. We specially like to thank Pieter Lok, Domine Leenaerts and Freek van Straten.

References

[1] T. Kwak et al. "A 2W Hybrid Switching Amplitude Modulator for EDGE Polar Transmitter," *ISSCC Dig. Tech. Papers* pp. 518-519, Feb. 2007.

[2] J. Kitchen, et al. "Combined Linear and Δ-Modulated Switched Mode PA Supply Modulator for Polar Transmitters", *ISSCC Dig. Tech. Papers*, pp. 82-83, Feb. 2007.

[3] P. Reynaert and M. Steyaert, "A 1.75-GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE," *IEEE JSSC*, pp. 2598-2608, Dec., 2005.

[4] F. Wang et al. "A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier" *IEEE JSSC*, pp. 1271-1281, June 2007.

[5] R.A.R. van der Zee and A.J.M. van Tujil "A power-efficient audio amplifier combining switching and linear techniques", *IEEE JSSC*, pp.985-991, July 1999.

[6] Hogervorst et al. "A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries" *IEEE JSSC*, pp.1505-1513, December 1994.