A Wideband W-Band Receiver Front-End in 65-nm CMOS

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***Abstract*—A 75-to-91 GHz receiver front-end, consisting of a three-stage cascode low-noise amplifier (LNA), a double-balanced Gilbert-cell mixer and a differential DC-to-9 GHz IF buffer, is reported in 65-nm general purpose (GP) CMOS technology. The noise and input-impedance matched LNA employs a cascode input stage with shunt-series, transformer feedback. A theoretical and experimental comparison with a conventional inductor-feedback LNA indicates 0.5–1 dB higher gain, 0.3–0.6 dB lower noise figure and better input return loss for the transformer feedback LNA. The receiver has a differential down-conversion gain of 13 dB, an input $P_{1\mathrm{dB}}$ of −16.2 dBm, and a double-sideband noise figure of 8.5 to 10 dB at an IF of 1 GHz. Because of the transformer feedback, the input return loss is better than −20 dB from 80 to 92 GHz and remains below −10 dB from 70 GHz beyond 95 GHz. The circuit occupies an area of 460 μm × 500 μm and consumes 89 mW (47 mW in the LNA and mixer) from a 1.5 V supply. An LO-to-RF isolation of 60 dB was measured for LO signals in the 80-to-85 GHz range. Measurements of the mixer breakout, which includes transformers at the RF and LO ports, show a record $\mathrm{NF}_{\mathrm{DSB}}$ of 8 to 10 dB over the 74-to-91 GHz band. The 50-Ω noise figure of the LNA is 6.4 to 8.4 dB in the 75-to-88.5 GHz range. The LNA can also be employed as a transmitter output stage with a saturated output power of +4 dBm.**

***Index Terms*—Gilbert-cell mixer, low-noise amplifiers (LNAs), millimeter-wave imaging, nanoscale CMOS, noise in circuits with feedback, W-band.**

I. Introduction

During the last four years, CMOS technology has emerged as a strong candidate for low-cost wireless HDMI ICs in the 60 GHz band [1]–[8]. More recently, with the first reports of 80-to-100 GHz amplifiers in 90-nm and 65-nm technologies [9], [10], and with SiGe BiCMOS building blocks and transceivers showing robust performance margin over process and temperature at 80 GHz [11] and even operation at 160 GHz [12], the prospect of SoCs at and beyond 100 GHz no longer appears far-fetched [13]. For example, one of the most interesting applications of CMOS millimeter-wave ICs is in large passive imaging receiver arrays for radiometry [14] night and fog vision cameras, and security applications [15] where very low power, compact size, low-noise (8 dB or lower) and a bandwidth exceeding 8 GHz are critical requirements.

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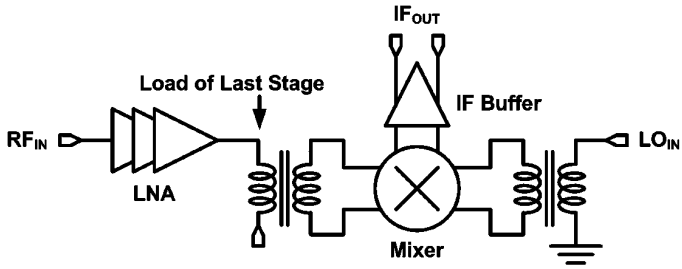

Fig. 1. Receiver block diagram.

We have recently reported two W-band receivers implemented in a 65-nm CMOS technology with a 7-metal "digital" backend [16]. In this paper, we describe in detail the design methodology of the individual building blocks, investigate the merits of series-series and shunt-series reactive feedback in low-noise amplifiers (LNAs), and we demonstrate significantly improved performance from a re-designed version of one of those receivers.

The paper is organized as follows. The receiver design considerations are discussed in Section II. Next, in Section III and in the Appendix, the performance of the new shunt-series, transformer-feedback, cascode LNA stage is analyzed in comparison with that of the classical cascode topology with inductive degeneration. Section IV continues with the low-noise design of the double-balanced Gilbert-cell mixer and IF amplifier. Details of the fabrication technology, along with the measured transistor, inductor and transformer performance in the 55-to-94 GHz range are presented in Section V, and the measured performance of the entire receiver, of the two LNAs and mixer breakouts is summarized in Section VI.

II. Receiver Design Considerations

The block diagram of this receiver is shown in Fig. 1. It features (i) a single-ended three-stage LNA with a shunt-series transformer feedback input stage, (ii) a double-balanced Gilbert-cell mixer with inductive degeneration, inductive broadbanding, and single-ended-to-differential transformers at the LO and RF ports, and (iii) a differential IF buffer which drives 50-Ω loads. In this implementation the LO signal is provided by an external source. However, integration of a fundamental frequency VCO and static frequency divider along with this receiver is also possible [15]. Furthermore, a PA with moderate output power of up to 10 mW can be added to realize the single-chip active imager transceiver architecture proposed in [13] or a 79–81 GHz transceiver for collision avoidance radar. This general purpose receiver topology, also implemented in 90-nm CMOS at 60 GHz [4], in SiGe BiCMOS at 80 GHz [11] and 160 GHz [12], is the

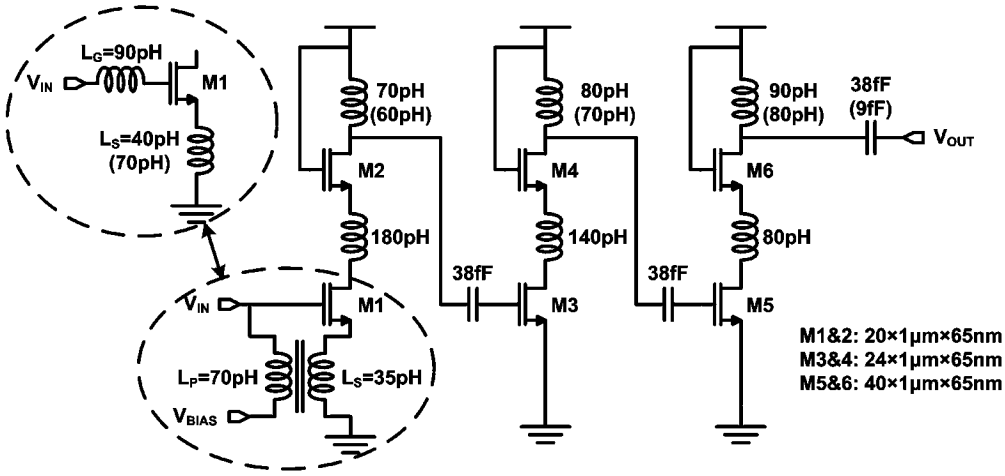

Fig. 2. Inductive (inset) and transformer-feedback LNA schematics. All transistors are minimum gate length. The bias circuitry is not shown.

most generic one that allows high-IF, low-IF and direct conversion radio architectures to be realized. It also features a very broad bandwidth, adequate to cover all radio, radar and imaging applications that could be of interest in the W-band.

Although an entirely differential receiver topology is preferable to improve isolation, a single-ended LNA has been chosen in order to facilitate noise figure and S-parameter testing above 70 GHz.

The rather loosely defined receiver design goals were (i) minimum noise, (ii) largest IF bandwidth, (iii) maximum linearity, (iv) differential 2×50-Ω IF loads, (v) differential down-conversion gain larger than 10 dB, and (vi) lowest power dissipation from 1.5 V supply.

Since measurements of the noise performance of 65-nm CMOS transistors above 60 GHz have not been conducted and published to date, setting a target value for the receiver noise figure was rather haphazard. Indeed, one of the goals of this work is to use this receiver as a test vehicle for characterizing the noise figure and optimal noise figure current density of 65-nm n-MOSFETs in the 75-to-95 GHz range. As a consequence, it was decided to aim for the best possible receiver noise figure by applying a well-established bipolar and CMOS low-noise amplifier design methodology [18], recently adapted to millimeter-wave frequencies [9], [19], [20] and relying on the invariance of the optimal noise figure current density observed in previous generations of CMOS technologies [21]. Furthermore, the double-balanced Gilbert-cell mixer and the inter-stage matching between the LNA and the mixer were also designed for optimal noise performance following the technique first developed in [22].

In passive imagers and radiometers, the temperature gradient than can be resolved is inversely proportional to the square root of the IF bandwidth of the receiver. A very large bandwidth of 10 GHz or higher is needed to achieve sub 1°K imaging resolution [15]. Such a large bandwidth is also useful in multigigabit rate last-mile radio links.

Although interferers are less likely to occur at 80 GHz and their strength is already attenuated by 20 dB as the distance from the originating interference source to the imager exceeds $10\,\lambda = 4$ cm, maximizing linearity remains one of the main receiver design considerations, after noise figure and receiver bandwidth.

The minimum receiver noise figure target imposes the size and bias current in the first stage of the LNA, as discussed in the next section. The maximum linear voltage swing at the output of the IF amplifier, about 0.7 V_{PP} dictates the 28 mA tail current of the differential IF buffer and, along with the downconversion gain, sets the upper bound on the input compression point of the entire receiver to -9 dBm.

III. Low-Noise Amplifier Design

The popularity of the cascode LNA topology with series-series inductive feedback, shown in the inset of Fig. 2, is due to the fact that a unique, optimal solution exists that simultaneously matches the input and noise impedances of the first stage of the LNA to Z_0 (typically 50 Ω). This topology lends itself to an algorithmic design methodology [18], even at mm-waves [3], [9], [19], [20]. Noise impedance matching is accomplished by sizing the input stage transistors, i.e., changing $g_{m\text{eff}}$ in (1) at the minimum noise figure current density bias [19]

$$R_{\text{SOPT}} \approx R_s + R_g + \frac{k_2}{\omega(C_{gs}+C_{gd})} \approx R_s + R_g + \frac{k_2 f_{T\text{eff}}}{f \times g_{m\text{eff}}} \quad (1)$$

while input resistance matching is realized, roughly independent of frequency, by choosing the appropriate value for L_S [18] such that

$$Z_0 = R_{\text{in}} \approx R_s + R_g + \omega_{T\text{eff}} L_s \quad (2)$$

In (1) and (2) $f_{T\text{eff}}$ and $g_{m\text{eff}}$ describe the effective cutoff frequency and transconductance, respectively, of the entire stage. Both depend on the drain current density, can be obtained from transistor measurements or from device simulations, and include the impact of the parasitic source resistance R_s. Parameter k_2, approximately 0.5, characterizes the noise of the MOSFET.

Common-source and cascode topologies without feedback i.e., with $L_s = 0$ in (2), as well as common-gate ones, cannot achieve simultaneous noise and impedance matching, except by accident, at a single frequency.

As discussed in [9], at mm-wave frequencies the pad capacitance introduces an additional parallel resonant circuit at the

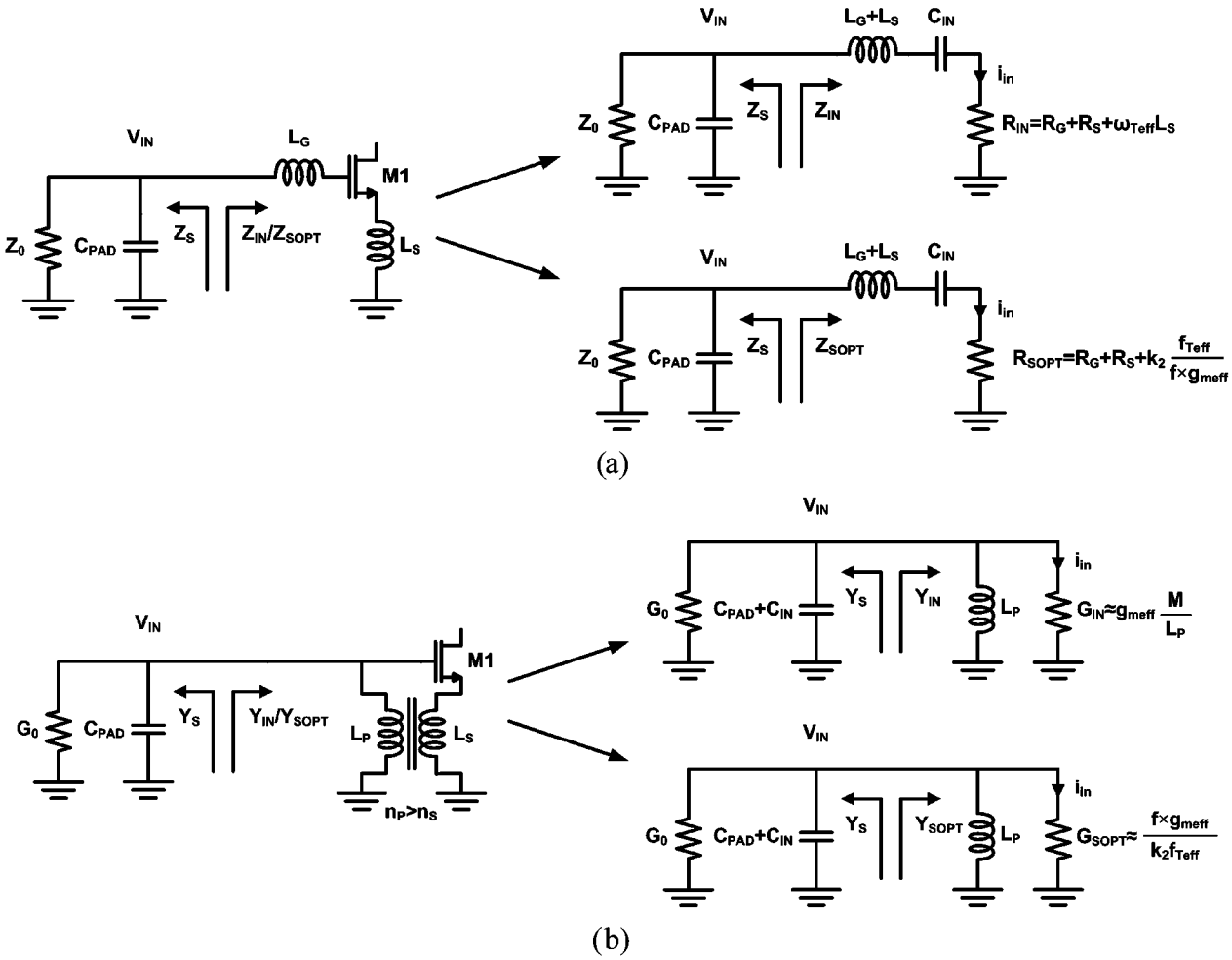

Fig. 3. Equivalent circuits describing the input and noise impedance of the a) series-series inductor-feedback LNA and b) shunt-series transformer feedback LNA, in the presence of the pad capacitance.

input of the series-series feedback LNA. This is illustrated in Fig. 3(a) for both the input and the noise impedance of the series-series inductive feedback LNA stage. Matching the input and noise impedance over a broad bandwidth becomes more problematic. Ideally, a shunt-series reactive feedback that would simultaneously compensate the pad capacitance and the input capacitance of the transistor over a broader bandwidth at mm-wave frequencies should be employed instead.

Such a wideband LNA with shunt-series feedback was recently proposed [23] for applications in the 2-to-12 GHz range. It uses transformer feedback in the first CS stage, while the second stage is formed by a transimpedance amplifier. An alternate, lossless shunt-series feedback topology, that retains the broadband input admittance and noise admittance matching, employs a cascode. Its schematic is illustrated by the first stage of the LNA shown in Fig. 2. The matching of the input and noise admittance of this LNA to the signal source admittance in the presence of the pad capacitance is conceptually illustrated in Fig. 3(b). Intuitively, this feedback scheme is expected to yield broader band input and noise impedance matching since, in a first order approximation which ignores R_g, R_s and assumes $k = 1$, only a single parallel-resonance occurs at its input. The noise and signal performance of the two LNA topologies is analyzed in more detail next.

A. Inductive-Feedback LNA

The expressions of the optimal noise impedance and of the minimum noise figure of this amplifier can be derived using the noise impedance formalism and Z-matrices [24], [25] shown in (3) and (4) at the bottom of the page, where subscript "a" denotes the parameters of the amplifier network (i.e., of the MOS

$$Z_{\rm SOPT} = \sqrt{R_{{\rm sopt}a}^2 + \frac{R_{uf}}{G_{na}} + 2R_{cora}\Re(Z_{11f}) + \Re^2(Z_{11f}) + \frac{|Z_{corf} - Z_{11f}|^2 G_{nf}}{G_{na}}} + j[X_{{\rm sopt}a} - \Im(Z_{11f})] \tag{3}$$

$$F_{\rm MIN} = 1 + 2G_{na}[R_{cora} + R_{\rm sopt} + \Re(Z_{11f})] \tag{4}$$

cascode) and subscript "f" describes the parameters of the feedback network formed by L_G and L_S. For the feedback network consisting of lossy inductors L_G and L_S with loss resistors R_{LG} and R_{LS}, respectively, $G_{nf}=0, R_{uf}=R_{LG}+R_{LS}, Z_{corf}=0, Z_{11f}=R_{LG}+R_{LS}+j\omega(L_S+L_G), Z_{12a}=0$. If L_S and L_G are ideal, i.e., their Q is infinite, then

$$\begin{aligned} &G_{nf}=0, R_{uf}=0, Z_{corf}=0,\\ &Z_{11f}=j\omega(L_S+L_G),\\ &Z_{12f}=j\omega L_S, \text{ and } Z_{12a}=0. \end{aligned} \tag{5}$$

As a consequence, the noise figure of the noise-matched LNA is identical to the minimum noise-figure of the MOS cascode. At the same time, by inserting (5) into (3), the real part of the optimal noise impedance becomes equal to that of the main amplifier. Only the imaginary part changes due to the presence of L_S and L_G. The implication is that the lossless feedback network does not change the optimum noise resistance $R_{\rm SOPT}$ and cannot provide noise impedance matching. It is the transistor sizing alone that ensures that.

B. Transformer-Feedback LNA

This circuit can be analyzed using g-network parameters, the noise admittance formalism, and the theory of noise in networks with shunt-series feedback [25]. The g-matrix entries of the transformer-feedback network can be expressed as

$$\begin{aligned} &g_{11f}=\frac{-j}{\omega L_P}+G_P, g_{12f}=\frac{M}{L_P},\\ &g_{21f}=\frac{-M}{L_P}, g_{22f}=j\omega L_S(1-k^2)+R_{\rm SEC} \end{aligned} \tag{6}$$

where L_P, L_S, k, and M are the inductance of the primary, the inductance of the secondary, the coupling factor, and the mutual inductance of the transformer, respectively. G_P is the loss conductance of the primary and $R_{\rm SEC}$ is the loss resistance of the secondary coil of the transformer. As derived in the Appendix, if the imaginary part is tuned out by the parallel inductance of the transformer primary, the input conductance of the amplifier with feedback can be cast as

$$G_{\rm IN}=g_{m\rm eff}\frac{M}{L_P}+G_P. \tag{7}$$

Similarly to the input resistance of the LNA with inductive degeneration, it does not vary with frequency and is a function of the feedback network (transformer) parameters M, L_P, G_P, and, unlike (2), of the MOSFET transconductance, $g_{m\rm eff}$.

The expressions of the optimal noise admittance of the amplifier with feedback and of its minimum noise figure are derived in the Appendix and shown in (8) and (9) at the bottom of the page. If the transformer is lossless, i.e., $G_P=0$ and $R_{\rm SEC}=0$, then

$$R_{nf}=0, G_{uf}=0, Y_{corf}=0, \Re(g_{11f})=0 \tag{10}$$

and $G_{\rm sopt}$ (8) and $\rm NF_{MIN}$ (9) of the amplifier with feedback become identical to those of the MOSFET cascode

$$R_n\approx R_{na}, G_u=G_{ua}, Y_{cor}=Y_{cora} \tag{11}$$

$$Y_{\rm sopt}=G_{{\rm sopt}a}+j\left(B_{{\rm sopt}a}+\frac{1}{\omega L_P}\right) \tag{12}$$

$$F_{\rm MIN}=1+2R_{na}[G_{cora}+G_{{\rm sopt}a}]=F_{{\rm MIN}a}. \tag{13}$$

Therefore, despite the different topologies employed for their input stage, the two LNAs in Fig. 2 exhibit similar flexibility in adjusting the optimal noise resistance (conductance), from $g_{m\rm eff}$, and the input resistance (conductance), from L_S and L_p/M, respectively.

Although (12) and (13) ignore the resistive parasitics of the MOSFET and the finite Q of the transformer, they can be accounted for in an analytical manner, as shown in the Appendix.

As indicated in the schematics of Fig. 2 and as shown in the high-resolution die photos of Fig. 4, the two LNAs have identical bias currents and component values except for the feedback network in the input stage. The transistors in the first stage are biased at 0.25 mA/μm, a value which was experimentally found to lead to the best overall receiver noise figure [16], while those in the second and third stages are biased for maximum linearity at 0.3 mA/μm [3]. In an effort to maximize gain, inductive degeneration is not employed in the second and third stages. All LNA transistors have 1-μm finger width, contacted on one side of the gate, and have minimum gate length. The gate resistance and the source resistance are approximately 200 Ω per finger and the effective transconductance is about 1.1 mS/μm at a drain current density of 0.25 mA/μm. The $f_{T\rm eff}$ of the cascode with inductive broadbanding is 115 GHz and, according to (1), results in an optimal noise resistance of 50 Ω at 85 to 90 GHz for a 20-μm width cascode stage.

C. LNA Design Methodology

A step-by-step algorithmic LNA design methodology can be derived for the transformer-feedback LNA, similar to the one developed for the series-series inductor feedback one [19].

$$\begin{aligned} Y_{\rm SOPT}=&\sqrt{G_{{\rm sopt}a}^2+\frac{G_{uf}}{R_{na}}+2G_{cora}\Re(g_{11f})+\Re^2(g_{11f})+\frac{|Y_{corf}-g_{11f}|^2R_{nf}}{R_{na}}}\\ &+j|B_{{\rm sopt}a}-\Im(g_{11f})| \end{aligned} \tag{8}$$

$$F_{\rm MIN}=1+2R_{na}[G_{cora}+G_{\rm sopt}+\Re(g_{11f})] \tag{9}$$

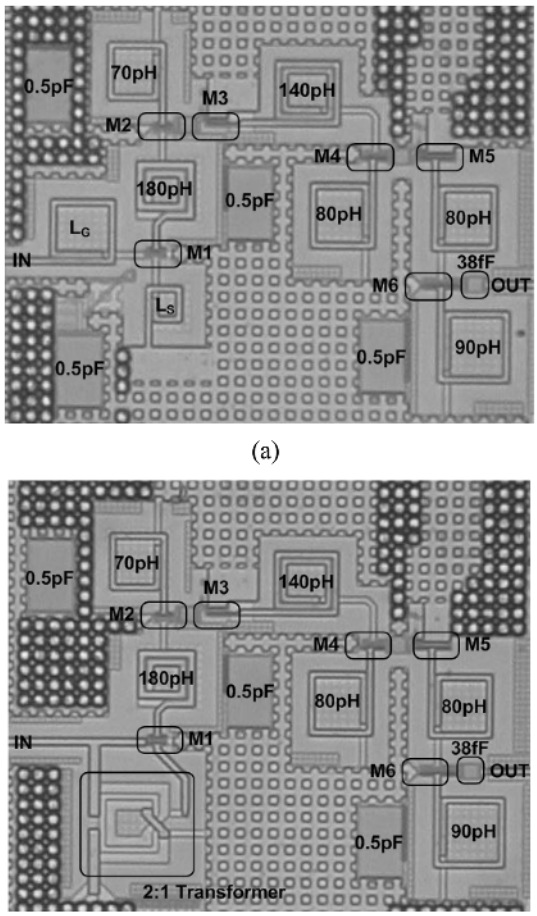

Fig. 4. Die photos of (a) inductor-feedback and (b) transformer-feedback LNAs.

Step 1: Transistor sizing using (1) for $R_{\text{sopt}} = 50\Omega$ and assuming 1 μm wide gate fingers

$$N_f = \frac{1}{Z_0}\left[R_g(W_f) + \frac{R_s^{'}}{W_f} + \frac{k_1 f_{T\text{eff}}}{f \times g_{m\text{eff}}^{'} W_f}\right] = \frac{1}{50}\left[200 + \frac{200}{1} + \frac{0.5 \times 115\ \text{GHz}}{85\ \text{GHz} \times 1.1\ \text{mS} \times 1}\right] = 20.3 \approx 20$$

where $R_S^{'}$ is the source resistance per unit gate width.

Step 2: Cascode bias current calculation assuming $J_{\text{opt}} = 0.25$ mA/μm

$$I_{DS} = J_{\text{OPT}} W_G = 0.25 \frac{\text{mA}}{\mu\text{m}} \times 20\ \mu\text{m} = 5\ \text{mA}.$$

Step 3: Determine L_P for input susceptance cancellation from (A.16)

$$L_P = \frac{1}{\omega^2\left(C_{\text{PAD}} + \frac{g_{m\text{eff}}}{\omega_{T\text{eff}}}\right)} = \frac{1}{(2\pi \times 85 \times 10^9)^2 \times \left(20fF + \frac{22\text{mS}}{2\pi \times 115 \times 10^9}\right)} = 69.5\ \text{pH} \approx 70\ \text{pH}.$$

Step 4: Find M/L_P for input conductance matching from (7), assuming a Q of 4 for the primary and a pad capacitance of 20 fF.

$$G_P = \frac{1}{\omega L_P Q} = \frac{1}{2\pi \times 85 \times 10^9 \times 69.5 \times 10^{-12} \times 4} = 6.73\ \text{mS}$$
$$\frac{M}{L_P} = \frac{\frac{1}{Z_0} - G_P}{g_{m\text{eff}}} = \frac{20\ \text{mS} - 6.73\ \text{mS}}{22\ \text{mS}} = 0.6.$$

In the case of the series-series inductor feedback LNA, steps 1–2 remain the same while steps 3 and 4 are modified, as follows.

Step 3: Find L_S for input resistance matching from (2)

$$L_s = \frac{Z_0 - R_g - R_s}{2\pi f_{T\text{eff}}} = \frac{50 - (200/20) - (200/20)}{2\pi \times 115 \times 10^9} = 41.5\ \text{pH} \approx 42\ \text{pH}.$$

Step 4: Calculate L_G to cancel the imaginary part of the input and noise impedance using (5) in [19]

$$L_G + L_S = \frac{\omega_{T\text{eff}}}{(2\pi f)^2 W_G g_{m\text{eff}}^{'}} = \frac{2\,\pi \times 115 \times 10^9}{(2\,\pi \times 85 \times 10^9)^2 \times 20\ \mu\text{m} \times 1.1 \frac{\text{mS}}{\mu m}} = 115\ \text{pH}, L_G = 73\ \text{pH}.$$

With the exception of M/L_P, all component values are very close to those finally arrived at by simulation in Fig. 2, indicating that a fairly accurate initial hand-design is possible even at 85 GHz. We note that the transformer-feedback LNA has an extra element of freedom through L_S or k, making its design more complicated than that of the inductor-feedback LNA. By choosing a smaller inductance for the secondary, the (current) gain of the amplifier stage is increased. However, the lowest value of L_S is limited by the power gain and current gain of the transistor itself at 80–90 GHz, and is also constrained by the inductance value of the primary, the coupling coefficient k, and layout realizability. The power gain and the peak gain of both the inductor-feedback and transformer-feedback stages is set by the Q and inductance, respectively, of the drain inductor of M_2.

The 2:1 vertically stacked transformer employed in the shunt-series feedback was designed using ASITIC to achieve $k = 0.56$, $L_P = 70$ pH, and $L_S = 35$ pH. The transformer primary has two windings in the top metal with 3 μm width and 2 μm spacing. Its diameter is 24 μm. The secondary has a single 2-μm wide winding with a diameter of 18 μm and is realized in the second metal from the top. The 2-π equivalent circuit employed in circuit simulations is shown in Fig. 5.

Although the hand analysis provides good initial values, the design methodology described earlier is most effectively conducted by simulation. To avoid iterations in the design of

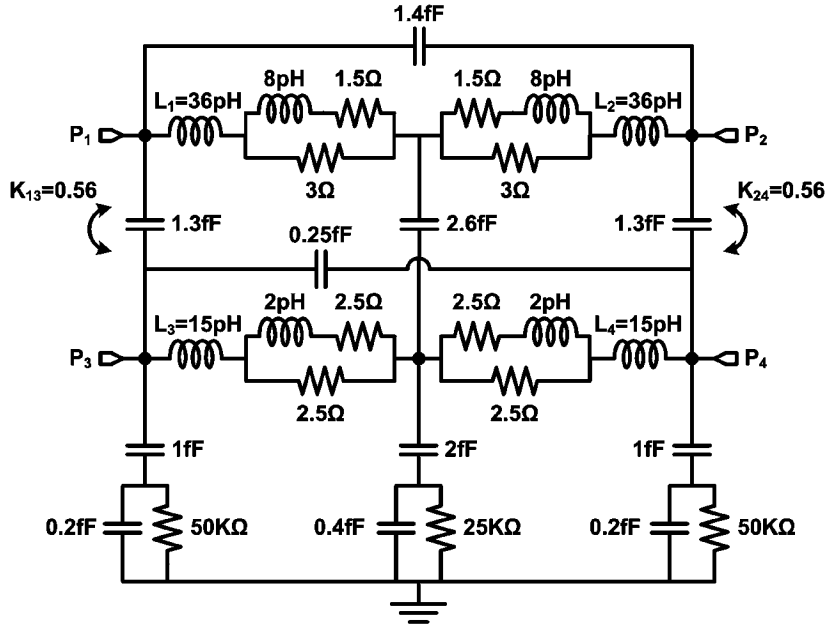

Fig. 5. Equivalent 2-π circuit of the $2:1$ LNA-feedback transformer.

the transformer, after the first step, as in [19], the transistor (cascode) should be replaced by its extracted layout with *RC* parasitics.

The component values from the first design spin [16] are shown in brackets in Fig. 2. In the present fabrication spin, the load inductors in the drains of M2, M4 and M6 were increased by about 10% in order to reduce the LNA center frequency from 86 GHz [14] to 78 GHz. The size and bias current of the third LNA stage are 40 μm and 12 mA, respectively, large enough to operate it as a transmitter output stage with $+4$ dBm saturated power.

The S-parameters, noise figure, and optimum source reflection coefficient $\Gamma_{\rm OPT}$ were simulated after extraction of layout RC-parasitics. They confirmed that the input impedance and noise impedance of the transformer-feedback LNA can be matched over a wider bandwidth, with the added benefit of slightly improved noise figure. The peak gain and $\rm NF_{50}$ are 16 dB and 5 to 6 dB, respectively, for a supply of 1.5 V.

IV. Mixer and If Amplifier Design

The mixer employs a double-balanced Gilbert-cell topology with inductive degeneration, common-mode inductor [22], and broad-banding [4], as illustrated in Fig. 6. The MOSFETs in the transconductor and switching quad are biased for fast switching [21] and low-noise operation at 0.18 mA/μm. The input linear voltage swing of the mixer, 0.4 Vpp, is dictated by the bias current density in the transconductor pair and by the AC-voltage drop on the 30 pH source degeneration inductors. It limits the overall receiver $P_{\rm 1dB}$ to -16 dBm. The differential input and noise impedance of the mixer is matched to the 75 Ω output impedance of the LNA at the 1:1 transformer output. The 140-pH inductors form an artificial transmission line, with the input capacitance in the mixing quad $(C_{gs}+2C_{sb})$ and the output capacitance of the transconductor $(C_{db}+C_{gd})$ as in the LNA stages. This maximizes the bandwidth of the mixer, as required in imaging receivers, and reduces its noise figure [4]. The 100-pH common-mode inductor suppresses even-mode harmonics.

Dual-coil, vertically stacked transformers are used at the LO and RF ports for single-ended to differential conversion and to provide bias to the mixer through the center taps. The IF-buffer is terminated on-die with 50-Ω loads and is biased at 0.3 mA/μm, for maximum linearity. The mixer and IF amplifier layout is shown in the high-resolution receiver die photo of Fig. 7. Symmetry was an important goal in the design of the layout to ensure good isolation between the LO and RF ports. The 0.5 pF bias de-coupling capacitors are strategically placed throughout the bias distribution mesh and close to the center-taps of the two transformers.

V. Fabrication and Technology Performance

The circuits were fabricated in STM's digital 65-nm CMOS process with standard 7-layer Cu back-end. The f_T and $f_{\rm MAX}$ of LP and GP n-MOSFETs with 80 gate fingers and 1 μm finger width, contacted on one side of the gate, were measured on the same die as the receiver. The maximum stable gain of GP n-MOSFETs is 8.4 dB at 94 GHz. Because GP transistors exhibit 30% higher g_m (1.1 mS/μm) and f_T (165 GHz at $V_{DS}=0.7$ V), 15% higher $f_{\rm MAX}$ (240 GHz), and 0.3 V lower V_{GS} at peak f_T bias [13], they were used exclusively in all circuits. The receiver occupies 460 μm $\times$ 500 μm, including all pads. The three transformers (i) at the LNA input on the left side, (ii) between the LNA and mixer in the center, and (iii) at the LO-port of the mixer on the right, are clearly visible in the die photo shown in Fig. 7. The differential IF output is located at the top of the die, with 50-Ω lines leading off to the pads which are partially covered by the metal dummy fill.

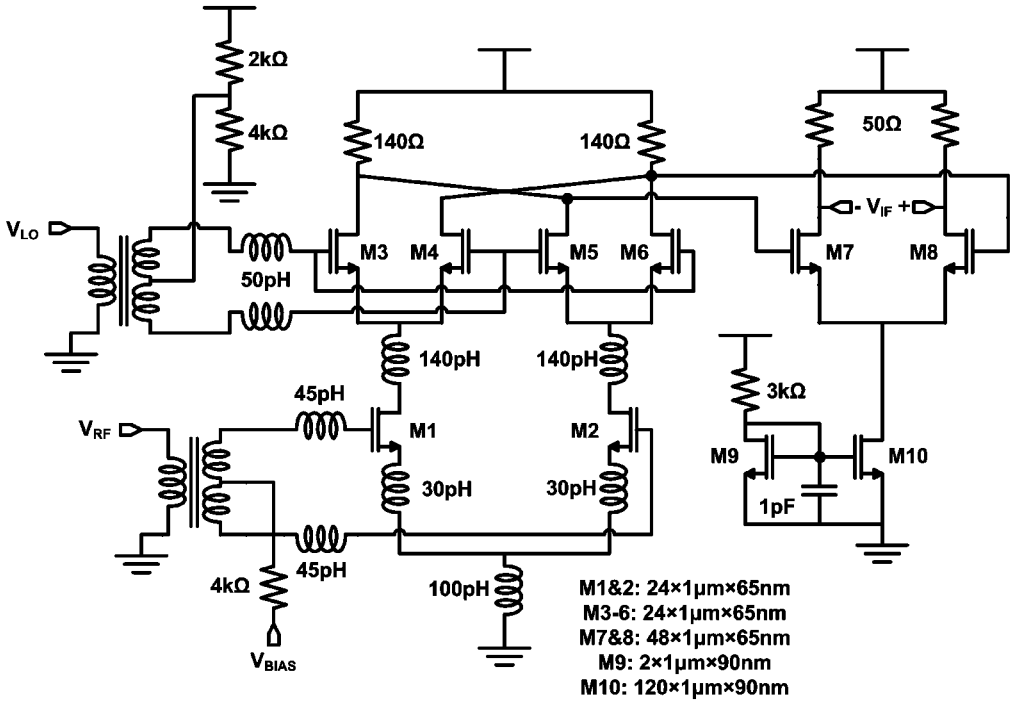

Fig. 6. Mixer and IF buffer schematics.

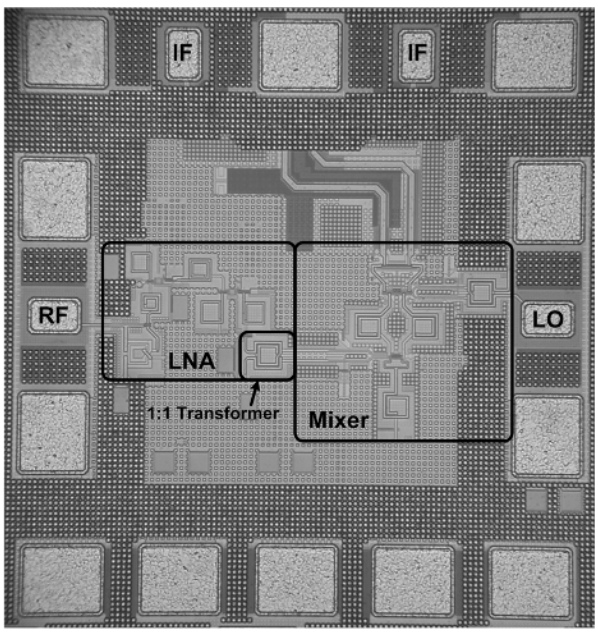

Fig. 7. Receiver die photo showing the RF input on the left, the LO port on the right, and the differential IF outputs at the top.

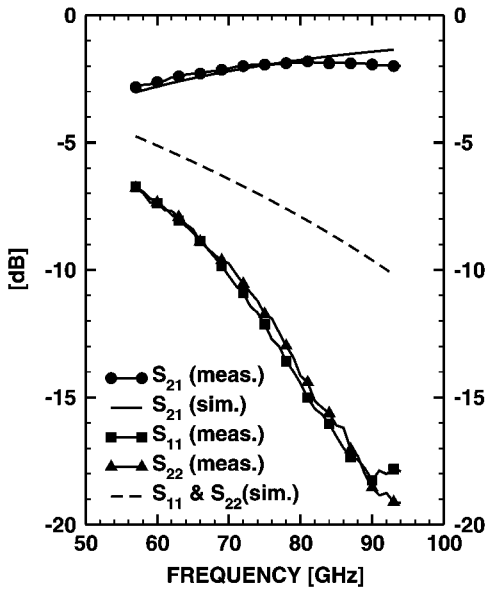

Fig. 8. Measured versus simulated transformer S-parameters.

Fig. 8 compares the measured and simulated S-parameters of the 1:1 transformer employed at the RF and LO ports of the mixer. S_{21} peaks at -2 dB in the 74–94 GHz range. The simulated and measured effective inductance and Q of one of the 80-pH LNA inductors are depicted in Fig. 9. There is less than 3 pH discrepancy between simulation and measurements. It is important to note that the inductor and transformer models were extracted prior to fabrication from ASITIC simulations and that no attempt was made to fit the model parameters to measured data. In fact it is not clear whether the small differences between simulations and measurements are due to model inaccuracy or to measurement and de-embedding errors on pH-range inductance and fF-range capacitance. The excellent Q values of 15 to 20, provide compelling evidence that a digital CMOS backend is acceptable in the W-band.

VI. Circuit Measurements

The two LNAs, the mixer and the receiver were tested on wafer using a 94 GHz Wiltron 360 VNA, 50-to-75 GHz and 75-to-100 GHz Millitech multipliers, an Agilent E4448A PSA

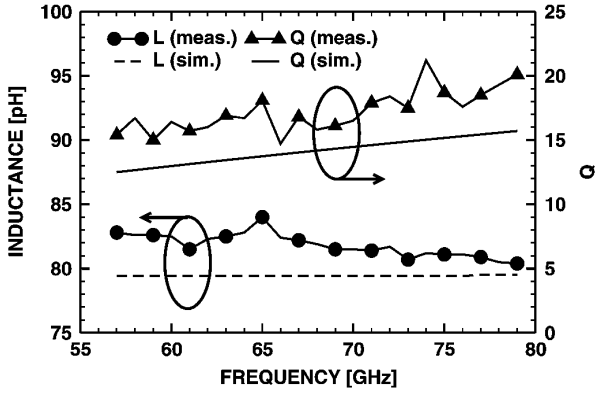

Fig. 9. Simulated and measured inductor Q and inductance.

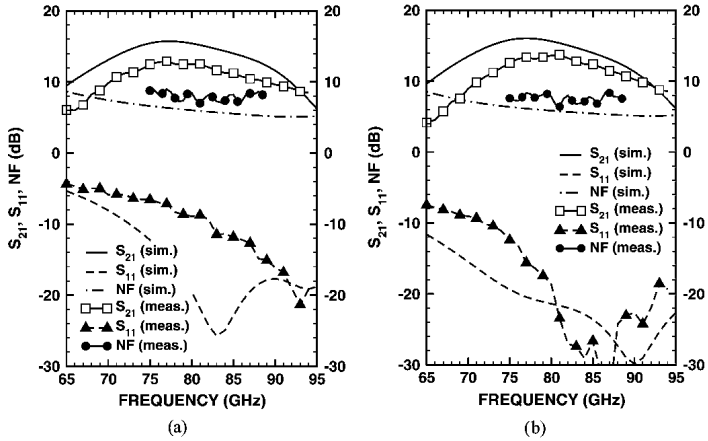

Fig. 10. LNA simulations versus measurements Left: inductor-feedback LNA. Right: Transformer-feedback LNA. $V_{\rm DD} = 1.5$ V.

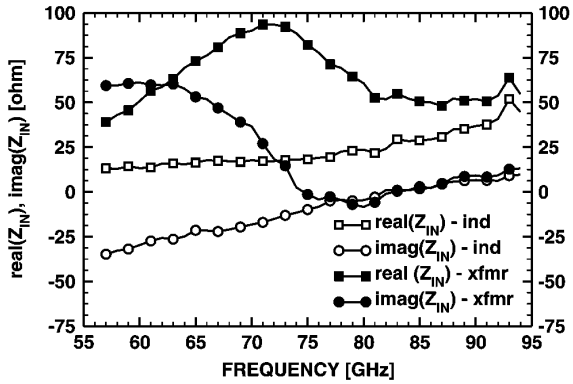

Fig. 11. Measured $R_{\rm IN}$ and $X_{\rm IN}$ versus frequency for the inductor-feedback and transformer-feedback LNAs.

spectrum analyzer, an Agilent W8486A 75-to-110 GHz power sensor, an ELVA-1 75-110 GHz noise source with an Agilent N8975 A noise figure analyzer, an Agilent N8975A K88 SSB image reject downconverter, and a 0-to-30 dB, W-band waveguide attenuator. The 20-fF pad capacitance has not been de-embedded in any of the circuit measurements.

The measured and simulated S_{21}, S_{11} and $\rm NF_{50}$ for the two LNA breakouts are plotted in Fig. 10 at the nominal supply of 1.5 V. The simulation results include the pad capacitance and the *RC* parasitics of the extracted layout at the cell level. The inductors, transformers and all interconnect lines longer than 5 μm are modelled separately as sub-circuits, and were excluded from post-layout extraction. The inductor-feedback and the transformer-feedback LNAs have 13 dB and 13.5 dB gain, respectively, centred at 80 GHz. The measured noise figure is systematically 0.3–0.6 dB lower for the transformer feedback LNA and varies between 6.4 dB and 8.4 dB across the band. This 2 dB ripple in the measured noise figure is due to the variation of the noise source reflection coefficient between cold and hot states. The peaks and troughs occur at exactly the same frequency for both LNAs. The S_{11} of the transformer-feedback LNA is as low as -30 dB at 87 GHz and remains below -20 dB from 80 to 92 GHz. The agreement between measurements and simulations is reasonably good. The measured peak gain and noise figure are about 2 dB below, and 2.5 dB above simulation, respectively. The center frequency is well predicted by simulation and occurs at the desired frequency of 80 GHz. The measured S_{21} is somewhat pessimistic because the VNA source power drives the LNA into soft compression and could not be further attenuated without increasing the noise floor of the VNA during calibration. Part of the 2 dB difference between measurements and simulations could also be attributed to the fact that self-heating and the temperature dependence of the inductor Q, are not captured in simulation and that a full extraction with *RC* parasitics is only performed at the circuit cell level, not at the circuit breakout level. Nevertheless, the lower peak gain and higher noise figure observed in measurements are symptomatic of the inability of MOSFET models to accurately predict gain and noise figure.

Fig. 11 compiles the measured real and imaginary parts of the input impedance of the two LNAs. The superior matching provided by the transformer feedback is immediately apparent. S_{21} measurements were also carried out across 5 dies, with less than 0.5 dB variation, indicating excellent repeatability from die to die, as shown in Fig. 12. The measured dependence of the gain, noise figure and input return loss of both LNAs versus the supply voltage from 1.2 V to 1.8 V is illustrated in Fig. 13. Overall, both LNAs perform quite well with a 3-dB bandwidth extending from 72 to 92 GHz. Fig. 14 compares the variation of the measured noise figure at 81 GHz for the two LNAs as a function of the drain current density of the input transistor and as a function of $V_{\rm DD}$. The minimum noise figure current density changes from 0.15 mA/μm for $V_{\rm DD} = 1$ V ($V_{DS} = 0.5$ V) to 0.28 mA/μm for $V_{\rm DD} = 1.8$ V ($V_{DS} = 0.9$ V) and the 50-Ω noise figure of the transformer-feedback LNA improves from 8 dB to 6 dB. These results confirm those in [19] indicating that, at scaled V_{DS}, the optimum noise figure current density of MOSFETs does not change with frequency and does not change across technology nodes.

The linearity plot of the transformer-feedback LNA, reproduced in Fig. 15, completes the series of tests conducted on the LNA breakouts. The LNA has an input-referred 1 dB compression point of -15.1 dBm and a saturated output power of $+4$ dBm.

The gain and noise figure of the mixer and IF amplifier breakout were measured from 74 to 98 GHz. Fig. 16 shows the

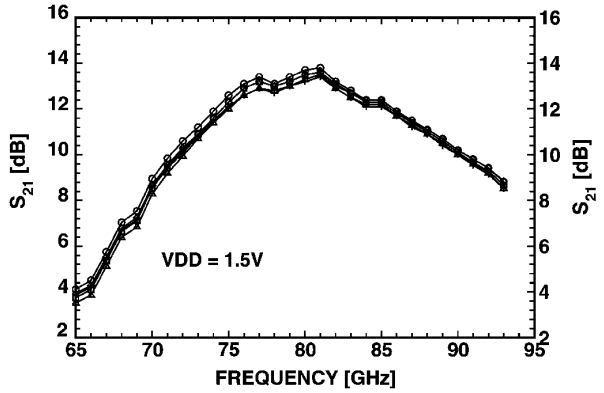

Fig. 12. S_{21} versus frequency characteristics of the transformer-feedback LNA measured across five dies.

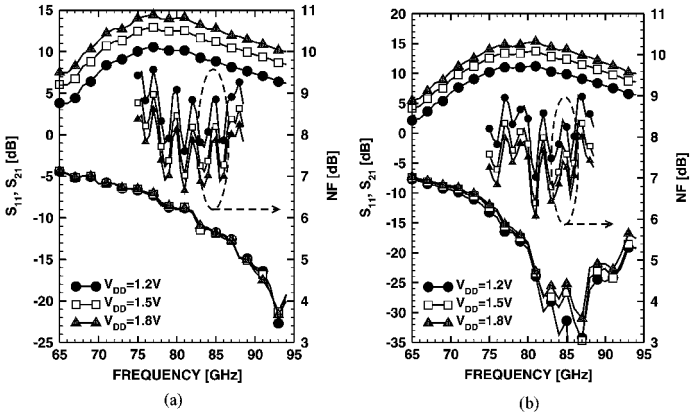

Fig. 13. Measured S-parameters and noise figure as a function of $V_{\rm DD}$. Left: inductor-feedback LNA. Right: transformer-feedback LNA.

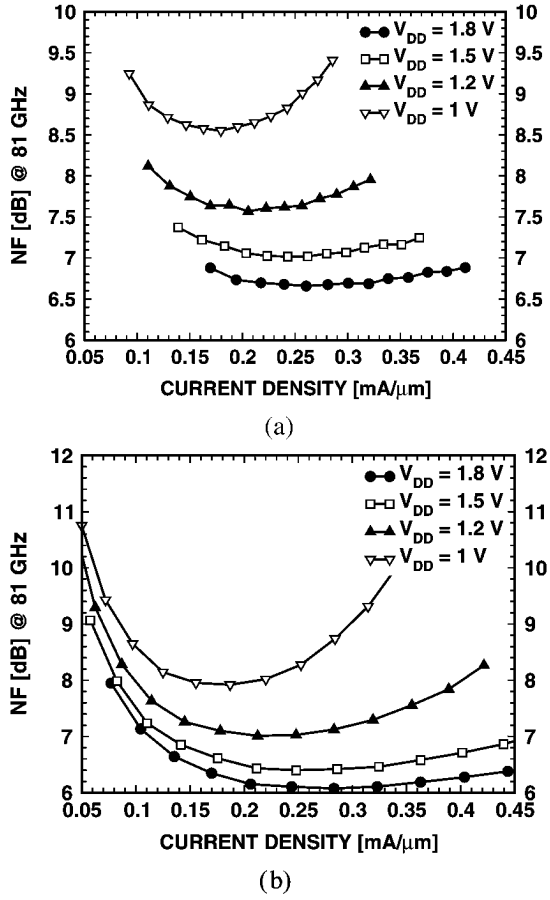

Fig. 14. LNA NF at 81 GHz measured as a function of $V_{\rm DD}$ and I_{DS}/W. Top: inductor-feedback LNA. Bottom: transformer-feedback LNA.

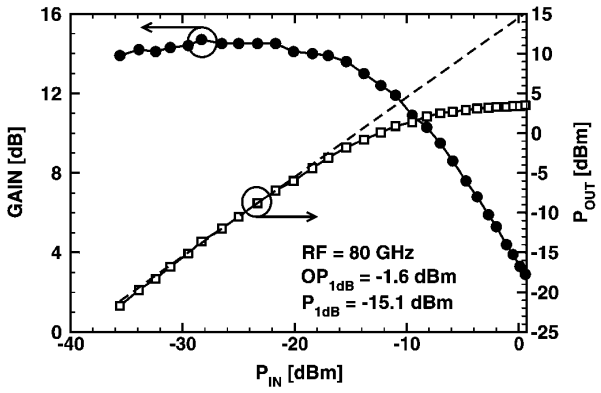

Fig. 15. Measured input/output compression point of the transformer-feedback LNA.

excellent agreement between measurements and simulation. The gain of the mixer is higher than 4 dB from 75 to 90 GHz, while the DSB noise figure remains below 10 dB in the same frequency range.

Fig. 17 reproduces the measured differential down-conversion gain and the DSB noise figure of the entire receiver along with the S_{11} of the transformer-feedback LNA as a function of the RF frequency. The receiver has a peak gain of 13 dB centred at 80 GHz, with the 3 dB bandwidth extending from below 75 to 91 GHz. The DSB noise figure of the receiver is 8.5 to 10 dB at 1 GHz IF over the entire bandwidth of the receiver.

Figs. 18 and 19 reproduce the down-conversion gain and DSB noise figure of the receiver front-end as a function of the IF frequency when the LO signal is fixed at 89 GHz. The maximum available LO power of $+5$ dBm is provided by the multiplier and the IF is swept from 1 to 18 GHz. The differential down-conversion gain reaches 12 dB while the DSB noise figure remains at 7 to 9 dB in the entire range. The 3 dB IF bandwidth exceeds 9 GHz (Fig. 18) and the noise figure improves for higher IF frequencies (Fig. 19), partly due to the waveguide cutoff of the noise source when the lower RF sideband reaches 75 GHz. The excellent linearity of the receiver is demonstrated in Fig. 20 for an RF input of 80 GHz and an LO signal at 75 GHz. The input-referred 1 dB compression point is -16.2 dBm, and is limited by the mixer transconductor, as predicted in the design section, while the saturated power at the IF output is 0 dBm, corresponding to 0.4 Vpp swing per side.

Finally, the LO-to-RF leakage of the receiver was measured with the spectrum analyzer connected to the RF port and applying a $+5$ dBm signal at the LO port. The isolation remains better than -60 dB for the measurement range of 80 to 85 GHz. Most of it, -42 dB, is provided by the LNA whose isolation was obtained from S-parameter measurements between 55 GHz and

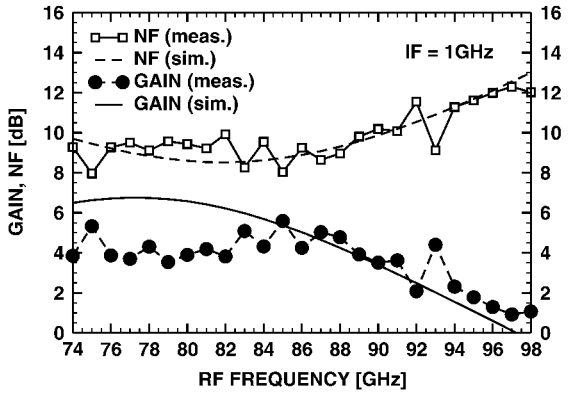

Fig. 16. Comparison of the simulated and measured gain and DSB noise figure of the mixer breakout.

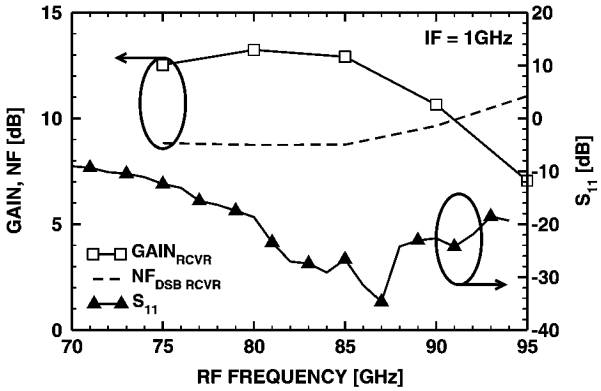

Fig. 17. Measured input return loss, noise figure, and downconversion gain of the receiver as a function of RF frequency for a constant IF of 1 GHz.

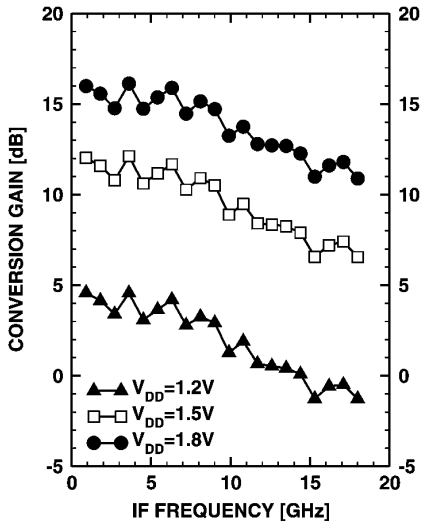

Fig. 18. Measured receiver downconversion gain as a function of IF frequency for a fixed LO frequency of 89 GHz.

94 GHz. Table I compares the performance of this receiver with other CMOS and W-band SiGe BiCMOS receivers and transceivers [26], [27] employing the same architecture.

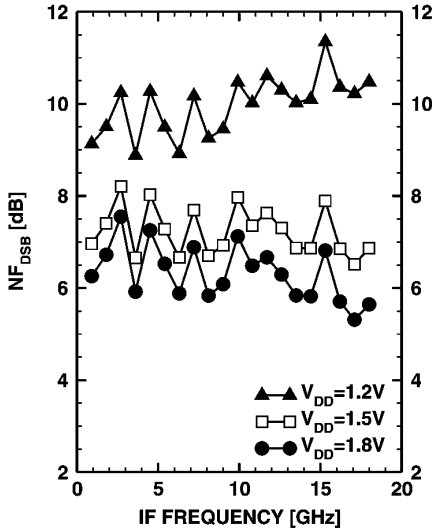

Fig. 19. Measured receiver DSB noise figure as a function of IF frequency for a fixed LO frequency of 89 GHz.

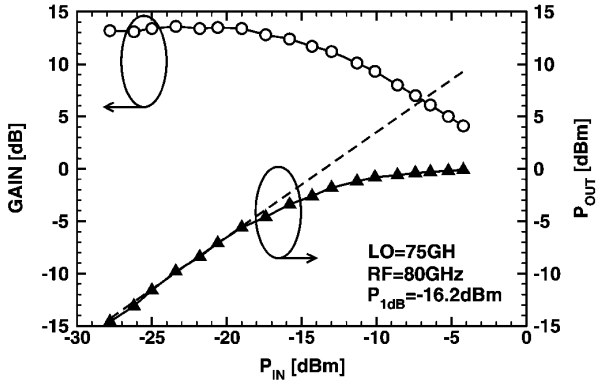

Fig. 20. Measured receiver linearity for 80 GHz RF and 75 GHz LO signals.

VII. Conclusion

The first W-band receiver in CMOS has been reported. The receiver employs a shunt-series, transformer-feedback LNA with improved gain and input matching when compared to a traditional cascode topology with inductive degeneration. The measured performance of the circuit breakouts and of the entire receiver is in fair agreement with simulation and with back-of the-envelope calculations based on measured transistor characteristics. However, there was no need to fit models to measured transistor, inductor and transformer data, indicating that radio receiver design at 90 GHz is predictable and reliable and that the circuit performance is repeatable across dies. The gain, S_{11} and noise figure measurements of the two LNA breakouts confirm the theoretical analysis which predicted better performance for the transformer-feedback version. The measured LNA, mixer and receiver noise figures are 6.4 to 8.4 dB, 8 to 10 dB, and 8.5 to 10 dB, respectively. Because lumped inductors and transformers are used for matching, the whole receiver die occupies only 0.23 mm^2. The large IF-bandwidth, exceeding 9 GHz, the small area, and the low power dissipation of 47 mW (excluding the 50 Ω IF buffer) recommend this receiver for imaging and remote sensing arrays.

TABLE I
W-BAND RECEIVERS AND TRANSCEIVERS FABRICATED IN 65-NM CMOS AND SIGE BICMOS TECHNOLOGIES

RX Gain	3dB BW	IP1dB	NF (dB)	Integration	P_{DC} (mW)	Area (mm^2)	Technology	Ref
13 (dB)	75–91 G 19%	-16 (dBm)	7.5	LNA+mix+IF	89	0.23	RX 65nm CMOS	This work
12 (dB)	75–95 G 22.2%	-18 (dBm)	7	+VCO+div2	206	0.66	RX 65nm CMOS	[17]
24 (dB)	68–76 G 10.3%	-22 (dBm)	4.8	+VCO	123	0.23	RX SiGe BiCMOS f_{MAX} = 240GHz.	[26]
25.6 (dB)	76–81 G 6.5%	-24 (dBm)	9	VCO+PA+div	740	1.17	TX/RX SiGe HBT f_{MAX} = 200GHz.	[11]
40 (dB)	77–85 G 9.8%	-38 (dBm)	3.85	VCO+PA+div	780	1.17	TX/RX SiGe HBT f_{MAX} = 300GHz.	[27]
31 (dB)	85–96 G 11.4%	-30 (dBm)	5.2	VCO+div64	700	1.02	RX SiGe HBT f_{MAX} = 300GHz.	[27]

APPENDIX

To analyze circuits consisting of two-ports connected in shunt at the input and in series at the output, as illustrated in Fig. 21, one can use g-parameters and the noise impedance formalism $i_n = i_u + Y_{cor}v_n$ to derive the expressions of the equivalent input noise sources

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} = \begin{bmatrix} g_{11f} & g_{12f} \\ g_{21f} & g_{22f} \end{bmatrix} + \begin{bmatrix} g_{11a} & g_{12a} \\ g_{21a} & g_{22a} \end{bmatrix} \quad \text{(A.1)}$$

$$v_n = f(v_{nf}, i_{nf}, v_{na}, i_{na}) \quad \text{(A.2)}$$

$$i_n = g(v_{nf}, i_{nf}, v_{na}, i_{na}) \quad \text{(A.3)}$$

The input equivalent noise sources can be calculated in two steps.

Step 1: The input noise voltage is obtained by short-circuiting the outputs and inputs of the two circuits in Fig. 21 and forcing the short circuit output currents to be equal

$$v_n = \frac{g_{21f}v_{nf} + g_{21a}v_{na}}{g_{21}} \quad \text{(A.4)}$$

Step 2: The expression of the input noise current is derived by leaving the inputs and outputs of the two circuits open and forcing the output voltages to be equal

$$i_n = i_{nf} + i_{na} + \frac{g_{11a}g_{21f} - g_{21a}g_{11f}}{g_{21}}v_{nf} + \frac{g_{11f}g_{21a} - g_{21f}g_{11a}}{g_{21}}v_{na}. \quad \text{(A.5)}$$

If the unilateral amplifier approximation holds, as in the case of a transistor at $f \ll f_T$

$$g_{21} \approx g_{21a}, g_{12} \approx g_{12f} \quad \text{(A.6)}$$

one obtains (A.7)–(A.10), shown at the bottom of the page. We note that the noise voltage of the amplifier with shunt-series feedback is equal to that of main amplifier. The noise currents of the amplifier and feedback networks add while Z_{in} and Z_{sopt} decrease. One can conclude that shunt-series transformer feedback can be used for noise matching in situations where the noise impedance of the original two-port is higher than that of the source impedance. The g -parameters of the transformer (with the loss of the primary described by G_P and that of the secondary by R_{SEC}) can be expressed as

$$g_{11f} = \frac{-j}{\omega L_P} + G_P, g_{12f} = \frac{M}{L_P},$$
$$g_{21f} = \frac{-M}{L_P}, g_{22f} = j\omega L_S(1-k^2) + R_{\text{SEC}}. \quad \text{(A.11)}$$

The g-parameters of the cascode stage are

$$g_{11a} = y_{11a} - \frac{y_{12a}y_{21a}}{y_{22a}} \approx j\omega(2C_{gd} + C_{gs}) \approx j\frac{fg_m}{f_{Ta}} \quad \text{(A.12)}$$

$$g_{22a} = \frac{1}{y_{22a}} = \frac{\frac{g_0^2}{g_m} + G_L - j\omega(C_{gd} + C_{db})}{\left(\frac{g_0^2}{g_m} + G_L\right)^2 + \omega^2(C_{gd} + C_{db})^2} \quad \text{(A.13)}$$

$$v_n \approx v_{na}, i_n = i_{nf} + i_{na} + g_{11f}(v_{na} - v_{nf}) \quad \text{(A.7)}$$

$$R_n \approx R_{na}, G_u = G_{uf} + G_{ua} + |Y_{corf} - g_{11f}|^2 R_{nf}, Y_{cor} = Y_{cora} + g_{11f} \quad \text{(A.8)}$$

$$Y_{\text{SOPT}} = \sqrt{G_{\text{sopta}}^2 + \frac{G_{uf}}{R_{na}} + 2G_{cora}\Re(g_{11f}) + \Re^2(g_{11f}) + \frac{|Y_{corf} - g_{11f}|^2 R_{nf}}{R_{na}}} + j[B_{\text{sopta}} - \Im(g_{11f})] \quad \text{(A.9)}$$

$$F_{\text{MIN}} = 1 + 2R_{na}[G_{cora} + G_{\text{sopt}} + \Re(g_{11f})] \quad \text{(A.10)}$$

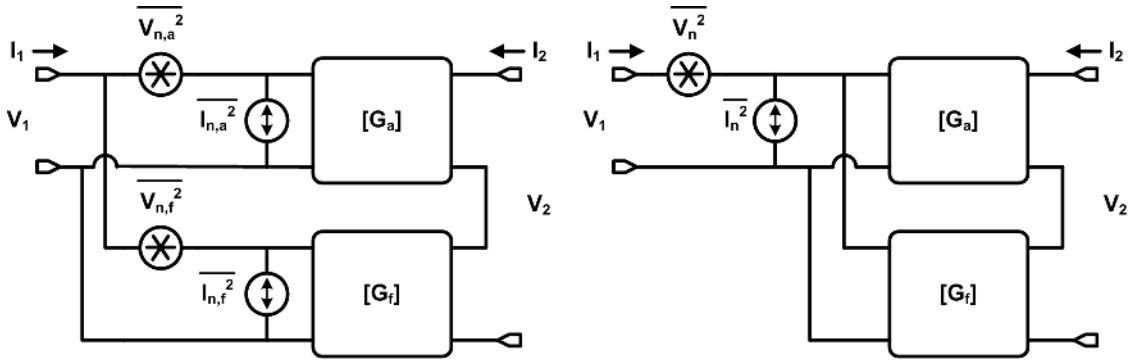

Fig. 21. (a) Two noisy two-ports connected in parallel at the input and series at the output. (b) Noise equivalent circuit representation of the two shunt-series connected two-ports.

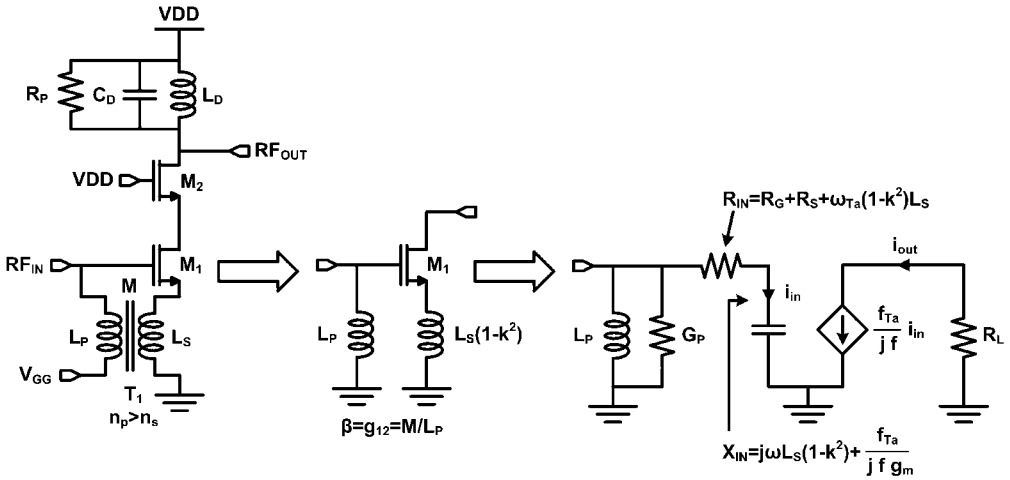

Fig. 22. (a) CS MOSFET LNA with shunt-series feedback using transformer T1. (b) Open loop amplifier with loading from feedback network. (c) Simplified equivalent circuit of the open loop amplifier showing the conductance loss G_P of the transformer primary and the parasitic resistances R_S and R_G of the transistor and of the transformer secondary.

$$g_{12a} = \frac{y_{12a}}{y_{22a}} \approx 0 \tag{A.14}$$

$$g_{21a} = \frac{-y_{21a}}{y_{22a}} \approx \frac{g_m G_L + g_0^2 - j\omega g_m (C_{gd} + C_{db})}{\left(\frac{g_0^2}{g_m} + G_L\right)^2 + \omega^2 (C_{gd} + C_{db})^2} \tag{A.15}$$

where f_{Ta} is the cutoff frequency of the cascode stage and accounts for the Miller capacitance C_{gd}.

The g-parameters of the entire amplifier with feedback shown in Fig. 22 are obtained by adding the g-parameters of the amplifier and those of the feedback network. We take into account that the cascode stage is loaded by G_L which describes the loss conductance of the load inductor L_D.

$$g_{11} = g_{11f} + g_{11a} \approx G_P - \frac{j}{\omega L_P} + j\frac{f \times g_m}{f_{Ta}} \tag{A.16}$$

$$\begin{aligned} g_{22} &= g_{22f} + g_{22a} \\ &= \frac{\frac{g_0^2}{g_m} + G_L - j\omega(C_{gd} + C_{db})}{\left(\frac{g_0^2}{g_m} + G_L\right)^2 + \omega^2 (C_{gd} + C_{db})^2} \\ &\quad + j\omega L_S (1 - k^2) + R_{\mathrm{SEC}} \end{aligned} \tag{A.17}$$

$$g_{12} = g_{12f} + g_{12a} \approx \frac{M}{L_P} \tag{A.18}$$

$$\begin{aligned} g_{21} &= g_{21a} + g_{21f} \approx \frac{-M}{L_P} \\ &\quad + \frac{g_m G_L + g_0^2 - j\omega g_m (C_{gd} + C_{db})}{\left(\frac{g_0^2}{g_m} + G_L\right)^2 + \omega^2 (C_{gd} + C_{db})^2} \\ &\approx \frac{g_m G_L + g_0^2 - j\omega g_m (C_{gd} + C_{db})}{\left(\frac{g_0^2}{g_m} + G_L\right)^2 + \omega^2 (C_{gd} + C_{db})^2}. \end{aligned} \tag{A.19}$$

Finally, the input admittance of the amplifier with feedback becomes

$$\begin{aligned} Y_{\mathrm{IN}} &= g_{11} - \frac{g_{12} g_{21}}{g_{22}} \\ &\approx \frac{-j}{\omega L_P} + j\frac{f \times g_m}{f_{Ta}} + g_m \frac{M}{L_P} + G_P. \end{aligned} \tag{A.20}$$

Equation (A.20) indicates that the feedback can be used to match the real part of the input admittance to 20 mS over a broad bandwidth and to tune out the input capacitance of the cascode stage and the pad capacitance.

$$R_n \approx R_{na}, G_u = G_P + G_{ua} + \left(\frac{1}{\omega^2 L_P^2} + G_P^2\right)\frac{M^2}{L_S^2}R_{\rm SEC},$$
$$Y_{cor} = Y_{cora} + G_P - \frac{j}{\omega L_P} \tag{A.23}$$
$$Y_{\rm SOPT} = \sqrt{G_{{\rm sopt}a}^2 + \frac{G_P}{R_{na}} + 2G_{cora}G_P + G_P^2 + \left(\frac{1}{\omega^2 L_P^2} + G_P^2\right)\frac{M^2}{L_S^2}\frac{R_{\rm SEC}}{R_{na}}} + j\left[B_{{\rm sopt}a} + \frac{1}{\omega L_P}\right] > G_{{\rm sopt}a} \tag{A.24}$$
$$F_{\rm MIN} = 1 + 2R_{na}[G_{cora} + G_{\rm sopt} + G_P] > F_{{\rm MIN}a} \tag{A.25}$$

The noise sources at the input of the transformer feedback network are given by

$$v_{nf}^2 = 4kT\Delta f\frac{M^2}{L_S^2}R_{\rm SEC}, i_{nf}^2 = 4kT\Delta f G_P. \tag{A.21}$$

From them, the noise parameters of the feedback network can be derived:

$$R_{nf} = \frac{M^2}{L_S^2}R_{\rm SEC},$$
$$G_{uf} = G_P, Y_{corf} = 0, \Re(g_{11f}) = G_P. \tag{A.22}$$

The noise parameters of the amplifier with lossy transformer feedback then become (A.23)–(A.25), shown at the top of the page. The optimal noise admittance and the minimum noise figure increase due to the lossy feedback network. Note that if the transformer is lossless, $G_P = 0, R_{\rm SEC} = 0$, and the feedback is purely reactive and does not degrade the noise figure. Unfortunately, in this case, it also does not change the real part of the optimum noise impedance from that of the transistor alone. As a result, the optimal transistor size and bias current for noise matching are still as large as in the case without feedback.

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