A Wireless Implantable Multichannel Digital Neural Recording System for a Micromachined Sieve Electrode

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***Abstract*— This paper reports the development of an implantable, fully integrated, multichannel peripheral neural recording system, which is powered and controlled using an RF telemetry link. The system allows recording of ± 500 μV neural signals from axons regenerated through a micromachined silicon sieve electrode. These signals are amplified using on-chip 100 Hz to 3.1 kHz bandlimited amplifiers, multiplexed, and digitized with a low-power (<2 mW), moderate speed (8 μs/b) current-mode 8-b analog-to-digital converter (ADC). The digitized signal is transmitted to the outside world using a passive RF telemetry link. The circuit is implemented using a bipolar CMOS process. The signal processing CMOS circuitry dissipates only 10 mW of power from a 5-V supply while operating at 2 MHz and consumes 4×4 mm^2 of area. The overall circuit including the RF interface circuitry contains over 5000 transistors, dissipates 90 mW of power, and consumes 4×6 mm^2 of area.**

***Index Terms*—Biomedical sensor, interface circuit, RF circuit.**

I. Introduction

MULTICHANNEL recording of neural activity from the central and peripheral nervous systems has long been pursued by physiologists as a means to understand the operation of individual neurons, to decipher the organization and signal processing techniques of biological neural networks, and to control a variety of prosthetic devices. Silicon micromachining and integrated circuit fabrication techniques have been used recently to produce the recording probes needed to interface with the complex structure of the nervous system. One of the most advanced devices developed to date combines a micromachined silicon microprobe with on-chip CMOS analog circuitry to amplify, multiplex, and transmit analog intracortical neural activity recorded acutely from a number of neurons in the central nervous system (CNS), while using a total of three leads for power and bidirectional data transfer [1]. However, for many future systems, recorded signals should be digitized before transmission to the outside world. On-chip analog-digital conversion is required for enhancing signal-to-noise ratio, for simplifying wireless data transfer, and for allowing limited on-chip digital signal processing for data compression and higher bandwidth. Furthermore, data and power transfer between the implantable unit and the outside world should be achieved without interconnect wires, as these can potentially cause infection at the points where they break the skin. Therefore, hard-wired systems are not suitable for chronic (long-term) recording applications.

A solution to this problem is to use totally implantable units which utilize batteries for power and RF telemetry for transmission of control signals [2], [3]. This method avoids the problems associated with hard-wired systems, but it suffers from the fast discharging of the batteries, especially in chronic applications or in applications where large levels of power are required. This problem can be overcome in some applications either by using rechargeable batteries which are charged using inductively coupled RF telemetry links or by disconnecting the batteries from circuits to limit the power consumption whenever it is not necessary. However, batteries are still not a good power supply in implanted circuits since they are usually big and can potentially leak, posing a hazard to the tissue.

Another solution is to use inductively coupled RF telemetry for both power and data transfer. There exists extensive work in applying this technique successfully [4]–[6]. The major shortcoming of most previous designs has been the large size of the implantable unit. In some designs, this is due to the construction of the implanted unit using discrete electronic devices assembled on medium-size boards through different hybrid techniques. Although this is overcome in other designs by the use of IC techniques, the overall size of the implanted units are still limited by the very large size (in the range of a few centimeters) of the receiver antenna (coil) that is required for the reception of sufficient power. In summary, previous systems are undesirably large for many implantable applications, and there is a need to develop fully integrated low-power miniature electronics systems capable of interfacing with the outside world using RF telemetry.

Over the past few years, we have been developing a totally implantable system [7] with a silicon sieve electrode to be used for multichannel chronic neural recording from individual axons and fibers in the peripheral nervous system (PNS) utilizing the nerve regeneration principle of the PNS. We have previously reported on the fabrication and development of a micromachined passive silicon sieve electrode [8]. In

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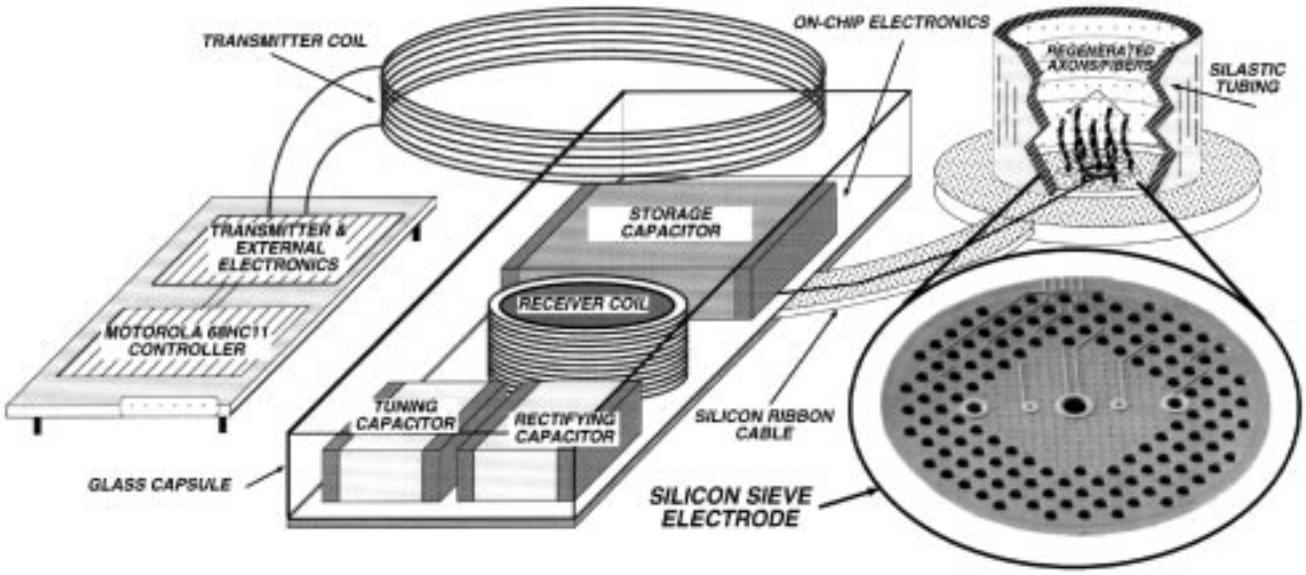


Fig. 1. Overall structure and architecture of the micromachined silicon sieve electrode recording system.

addition, we have reported the development of an efficient transmitter to deliver sufficient power to small implanted coils [9]. This paper presents the development of on-chip circuitry for a telemetrically operated digital neural recording system for chronic neural recording applications. The system is designed for obtaining recordings using sieve electrodes, but it can be used in a number of other neural recording applications by simply replacing the sieve electrodes with other types of electrodes. This system is implemented in a single monolithic chip which combines signal amplification and filtering, low-power A/D conversion, bidirectional user interface, and RF telemetry units for power and data transfer.

II. System Overview

Fig. 1 shows the application and structure of the "sieve" electrode recording system. It consists of a micromachined silicon sieve electrode, a silicon interconnecting cable, on-chip signal processing and RF telemetry interface circuitry, and an external transmitter. The silicon sieve electrode supports a large number of small ($\geq$1 μm in diameter) holes through which individual axons and fibers of a severed nerve can regenerate. The recording sites located around these through-holes are connected to the signal processing circuitry using an integrated 4 μm-thick flexible multilead silicon ribbon cable. Any 2-of-32 recording sites can be selected by a user through address switches at the external controller. The controller generates serial data to modulate a high-efficiency Class-E transmitter/amplifier which drives a circular transmitter coil. The magnetic field set up by the transmitter coil induces an ac voltage across a receiver coil in the implanted unit. The AM RF signal is used to generate both the dc voltage and control data necessary for operating the on-chip electronics. Neural signals from two channels are amplified, time-multiplexed, digitized using a low-power analog-to-digital converter (ADC), and transmitted to the outside world using passive telemetry.

Fig. 2(a) shows the block diagram of the on-chip circuitry, which can operate either with a hard-wired five-lead interface or with a leadless telemetry link. Fig. 2(b) shows the communication protocol of the amplitude-modulated RF telemetry link. The communication protocol supports two modes of operation: write address and read data. The serial digital signals 1 and 0 are encoded by long and short pulse durations, respectively. Following the start signal, a write command (digital 1) is sent, followed by the 10-b address (5 b per channel) of the two channels to be selected. Once the channel selection information is transmitted to the on-chip electronics, it waits for the read command (digital 0) to start analog-to-digital conversion of the two channels consecutively and transmits back a total of 16 data bits (8 b per channel). Then, the on-chip circuitry waits for the next command, and depending on the mode, it either selects the new channels to be recorded from or starts another conversion and transmission cycle. This protocol allows easy synchronization, gives the user control over sampling rate, and is compatible with the RF telemetry system that uses amplitude modulation and passive reverse telemetry for bidirectional signal transmission.

III. Design Considerations and Implementation

The implementation of this system should consider several requirements, dictated by the sampling rate, resolution of the converter, transmission frequency, bandpass characteristic of the preamplifiers, and the fabrication process.

In order to determine the sampling rate required for reliable neural recordings, the major frequency components of the actual recorded signals from an axon were determined to be in the 100 Hz to 3.1 kHz range. Therefore, these signals should be sampled at least every 160 μs to have a minimum Nyquist rate of 6.2 kHz. In addition, signals should be passed through a low-pass filter with a cutoff frequency of $\sim$3.1 kHz to prevent high-frequency aliasing.

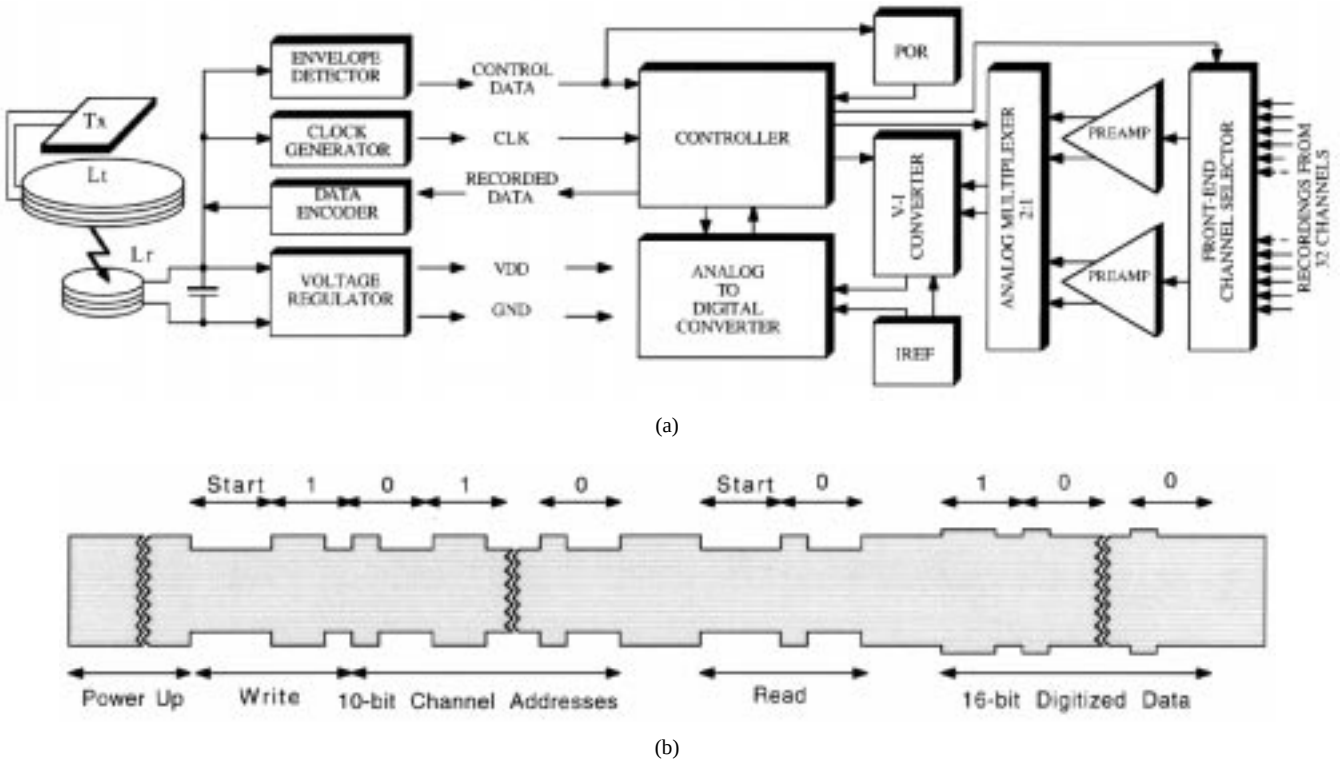


Fig. 2. (a) Block diagram of the on-chip circuitry and (b) the communication protocol of the system.

Another design consideration is the required resolution of the ADC, which can be determined by the amplitude of the signals and the noise levels of the preamplifiers and the electrodes. Since recorded axon potentials are generally in the ± 500 μV range, and the input noise of the amplifiers and the noise of the electrodes are in the 5–10 μV range [1], [17], an 8-b ADC is adequate for this application.

The RF transmission frequency is determined by the required data transmission rate, which is dependent on the sampling rate, and power loss due to tissue absorption. Since the system has to operate inside the body, and the power loss due to tissue absorption increases with the frequency, the transmission frequency should be low. However, it should still be high enough to allow fast data transmission required by the high bandwidth of the recorded neural signals. The data transmission rate depends also on data modulation and encoding techniques. Data is modulated onto an RF carrier using amplitude modulation, and it is encoded using a variable pulse-width modulation technique. These techniques enable the implementation of simple demodulation and decoding circuitry in CMOS with small size and low power consumption.

The data transmission rate in this modulation scheme is limited by the minimum pulse width that can be used to modulate the RF signal. This pulse should be long enough for the RF signal to reach its steady state value during amplitude transitions from high-to-low and low-to-high, which is determined by the time constants of the transmitter and receiver RLC networks. The time constant for an RLC network can be given as $Q/\pi f$, where Q is the quality factor of the RLC network, and f is the transmission frequency. Since at least three time constants are required to reach steady state, the number of cycles required during amplitude transitions will be approximately equal to Q. The pulse width can be decreased, i.e., the data transmission rate can be increased, either by increasing the transmission frequency or by decreasing the Q values of the RLC networks; both decrease the power received by the receiver coil. The transmission frequency and the Q values of the two RLC networks were chosen to be 4 MHz and four, respectively. These values provide a minimum pulse width of 2 μs, i.e., one bit can be transmitted in 8 μs.

The fabrication of the RF telemetry interface and mixed-mode signal processing electronics is achieved using a bipolar CMOS technology [10]. In addition to the standard CMOS devices, this technology provides high performance, junction-isolated vertical bipolar transistors, and a variety of junction and Zener diodes.

A. Bipolar CMOS Process

A bipolar CMOS technology has been developed to fabricate neural probes with on-chip CMOS circuitry [1]. The technology combines a standard 3-μm p-well CMOS process with a deep boron diffusion, while using an n-epi on p-substrate silicon wafer. The deep boron diffusion, which is also used for p-well drive-in, penetrates through the n-epi region to reach the p-substrate. This allows the realization of a number of bipolar devices in isolated n-epi regions for the design of analog circuitry, especially isolated diodes for the voltage regulator circuitry [10]. The lateral npn and pnp transistors, which are inherent in any CMOS process [11]–[13], are fabricated in p-well and n-epi regions, respectively. Current gains of lateral npn and pnp transistors in this process are measured to be about 50 and 15, respectively. Vertical npn

transistors in isolated n-epi regions have current gains in the range of 150–270 with collector–emitter breakdown voltages of more than 60 V. It is also possible to fabricate a number of junction and Zener diodes with different breakdown voltages. In addition, the fabrication process uses two polysilicon layers, which can be utilized to form on-chip capacitors with breakdown voltages higher than 20 V.

An important device in the telemetric sieve recording system is the isolated diode necessary for the voltage regulator circuitry and is fabricated using p-well/n^+ junctions in isolated n-epi regions. Although these diodes form parasitic devices which result in leakage current to substrate from the p-well, this can be minimized with careful layout techniques.

Fig. 3(a) shows the cross section of a p-well/n^+ diode and its associated parasitic bipolar devices, and Fig. 3(b) shows the interconnection of these devices. Here, n-epi is shorted to p-well to prevent the parasitic npn transistor from turning on. However, there is a resistive path ($R_{\rm epi}$) between the epi contact and the area under the p-well. In addition, there is also a resistive path, represented by $R_{\rm well}$, between the p-well contact and the n^+ region. When current is passed from p-well to n^+, the parasitic npn transistor can turn on, which in turn increases the voltage drop across $R_{\rm epi}$ to the point where the pnp transistor will turn on, resulting in current leakage from p-well to substrate. In order to minimize this effect, $R_{\rm epi}$ resistance should be decreased as much as possible. In a standard bipolar process, $R_{\rm epi}$ resistance is kept low with the use of a buried n^+ layer. Since there is no buried layer in this process, special care was taken in the layout of these diodes to decrease $R_{\rm epi}$ resistance. It should be noted here that this leakage current is not a problem in the CMOS circuitry since there is no current flow from p-well to n^+ region.

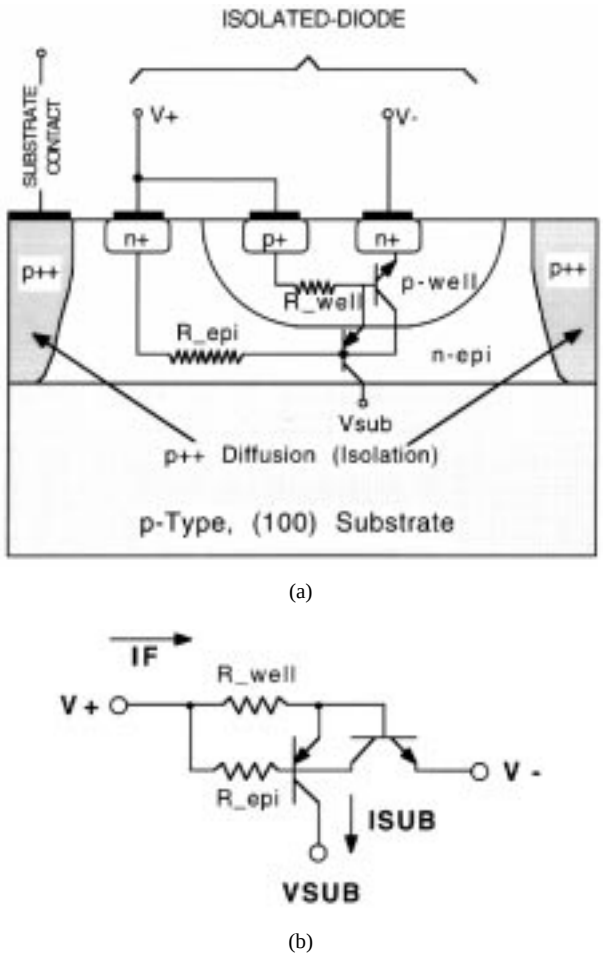


Fig. 3. P-well/n^+ diode and its associated parasitic bipolar structures: (a) cross-sectional view and (b) circuit connection.

B. RF Telemetry Interface

The RF telemetry interface consists of a voltage regulator to generate the voltage supply necessary for the implanted electronics, an envelopedetector to receive data from external electronics, a clock generator, and a circuit block for passive reverse telemetry of the digitized recorded data to the outside world.

1) Voltage Regulator: The voltage regulator should generate a 5-V supply from the RF signal for the on-chip electronics, with a regulation consistent with the required accuracy of the A/D converter. It also should include the circuitry necessary for reverse passive telemetry. Fig. 4 shows the voltage regulator designed for this purpose. The RF signal induced across the receiver coil, which is about 20-V peak, is first rectified by the full-wave rectifier. The rectifier diodes, $D1$–$D8$, are implemented using p-well/n^+ junctions. Although p-well/n^+ diodes have a breakdown voltage of about 23 V, two of them are used in series, as a safety measure, to prevent breakdown in case the received RF signal is unexpectedly high.

The rectified signal is regulated with a new voltage regulator designed for this application. Good voltage regulation is achieved by forcing a constant current in diode strings $D16$–$D25$ through transistors $M8$, $M9$, and diodes $D13$–$D15$. The npn transistor $Q2$ supplies power to the on-chip circuit while its base is driven by $Q1$ to decrease the current draw from the diode string, thus improving the voltage regulation. Transistors $M10$–$M13$ and diodes $D26$–$D29$ keep the supply voltage regulated against load current variations. Transistor $M14$ prevents the drain-to-source voltage of $M11$ from becoming very high, and therefore, the breakdown of $M11$, which may occur due to an excessive current draw from the circuit. In order to improve voltage regulation further (necessary for achieving the 8-b accuracy needed for the ADC) and to save area, capacitors $C1$, $C2$, and $C3$ are chosen to be hybrid capacitors, with capacitances of 220 pF, 470 pF, and 1 μF. Simulation results show that the maximum peak-to-peak ripple on top of the 5-V supply is less than 0.02 V, i.e., the voltage regulator provides a regulation better than 8 b. This regulation is maintained even during the loading of the receiver coil by passive telemetry circuitry.

The voltage regulator shown in Fig. 4 also includes a circuit for reverse passive telemetry to transmit the recorded data to the outside world. Reverse passive telemetry is achieved using the circuit made of transistors $M1$–$M7$ and diodes $D9$–$D12$. This circuit uses current loading to load down the receiver coil, which in turn results in a current change in the transmitter coil that can be sensed and recovered by external electronics. This method eliminates the need for an active transmitter in the

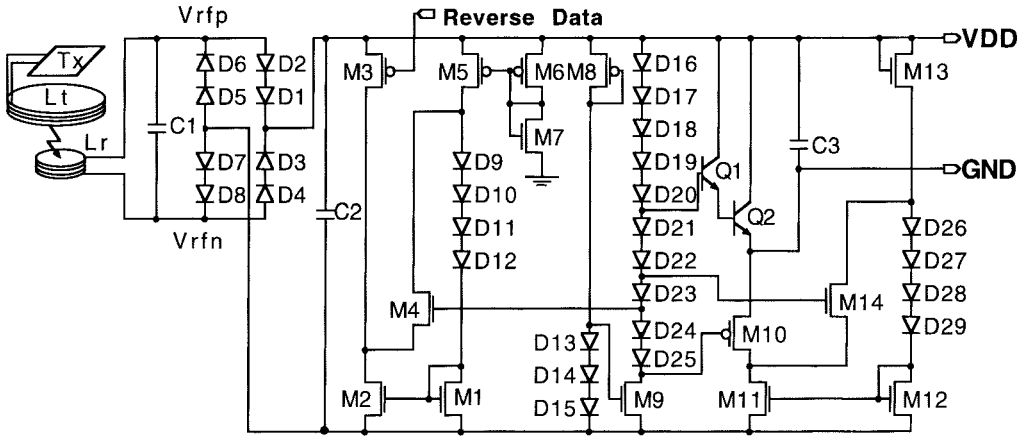


Fig. 4. The voltage regulator with passive telemetry circuitry.

implanted unit, thus reducing power consumption and size of the implanted unit.

The voltage regulator circuitry together with the passive telemetry portion occupies an area of 2 mm^2 and dissipates $\approx$77 mW of power while providing a voltage regulation of better than 99.8% (i.e., less than 0.2% noise).

2) Envelope Detector: A new envelope detector has been designed to prevent problems associated with the implementation of a conventional detector in CMOS technology. Fig. 5(a) shows the current-mode envelope detector developed for this application. The currents through $M1$ and $M5$ have the same amplitude under steady state conditions, but are different during an amplitude change, due to different capacitor values used for $C1$ and $C2$. Therefore, any amplitude change in the RF signal will result in a current change in $M1$ and $M5$, which is mirrored to $M4$ and $M6$, so that they can be compared to define if the change is due to a high-to-low amplitude transition or vice versa. Transistors $M7$ and $M8$ are used to generate hysteresis to prevent any state change due to any ripple on the current signals. The envelope detector occupies an area of 1 mm^2 and consumes a power of only 2 mW.

3) Clock Generator: In order to synchronize the on-chip circuitry with the external electronics during data transmission, the clock for the control circuit is also generated from the RF carrier using the circuit in Fig. 5(b). To prevent a possible breakdown of the MOS transistors due to the high RF voltages, the circuit first divides the RF voltage amplitude by an order of magnitude using on-chip capacitors $C1$ and $C2$. This reduced voltage is then used to drive the three-stage oscillator circuit with a weak final inverter. This oscillator circuit generates an output at a frequency twice the RF signal, i.e., 8 MHz for this application. This signal is then divided down using two frequency dividers to generate the 2-MHz clock signal necessary for the controller. The clock generator together with two frequency dividers occupies an area of 1 mm^2 and consumes 1 mW of power.

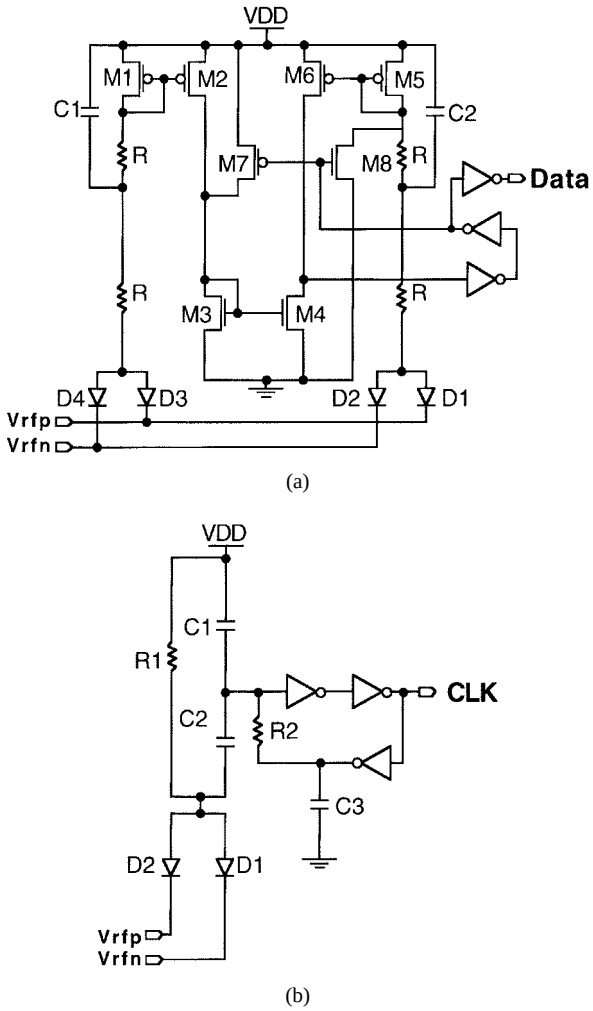


Fig. 5. (a) The current-mode envelope detector and (b) the clock generator circuitry.

C. Signal Processing Circuitry

The signal processing circuitry is designed such that it can either operate with a hard-wired five-lead interface or with the wireless RF telemetry interface. It includes both digital and analog CMOS circuits to implement the controller, neural preamplifiers, analog-to-digital converter, current and voltage reference, and voltage-to-current converter for the current mode ADC.

1) Controller: The controller circuit is used to decode the information modulated on the RF carrier and to generate con-

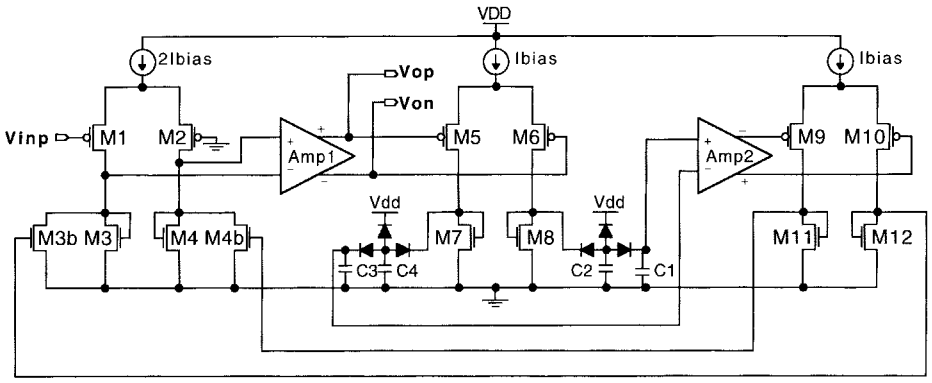


Fig. 6. A simplified schematic of the neural preamplifier.

trol signals for the overall operation of the on-chip electronics. It is first reset during charge up with the power-on-reset (POR) circuit, and then it waits for the command data. If the command data is a write address command, then the controller receives and decodes the 10-b information for the two channels to be selected. If the command data is a read data command, then it feeds a start signal to the ADC for conversion and transmission of two 8-b data words.

The controller uses counters to identify the length of the active low and high signals for decoding the encoded serial digital control information. If the signals are longer or shorter than a specified window, the controller goes to the initial state waiting for another command cycle. This improves the reliability of the system since the controller does not get stuck if there is an interruption in the RF link.

The controller has been designed and implemented using the delay-element method to simplify the design and layout process and ensure its functionality. The delay elements are implemented using master-slave flip-flops with two-phase nonoverlapping clocks to prevent clock skew problems and minimize the effects of critical paths in the control circuit. The transistors in the flip-flops are sized carefully for low power operation at the expense of larger die area. The controller circuit together with the counters consumes an area of 3.6 mm^2.

2) Front-End Analog Multiplexers: The front-end multiplexers are used to select any two out of 32 channels for recording. Two 5-b channel addresses stored in two 5-b registers are decoded with two 5-to-32 decoders, which are used to drive the multiplexers to connect the selected channels to the preamplifiers. Special attention is paid to the design of this multiplexer to prevent any charge injection during address changes and to achieve high isolation between channels. The simulations of the multiplexer shows that 85-dB isolation can be achieved between channels at the expense of the overall increased area.

3) Neural Preamplifier with DC Feedback: Neural signals, with ± 500 μV amplitude range, are amplified with two preamplifiers as shown in Fig. 6. Each preamplifier has an in-band ac gain of 40 dB with a 3-dB bandwidth of 100 Hz to 3.1 kHz. A special feature of the preamplifier is that it has a dc gain of -40 dB which is critical in preventing amplifier saturation due to input offset and dc drift caused by the electrode-electrolyte

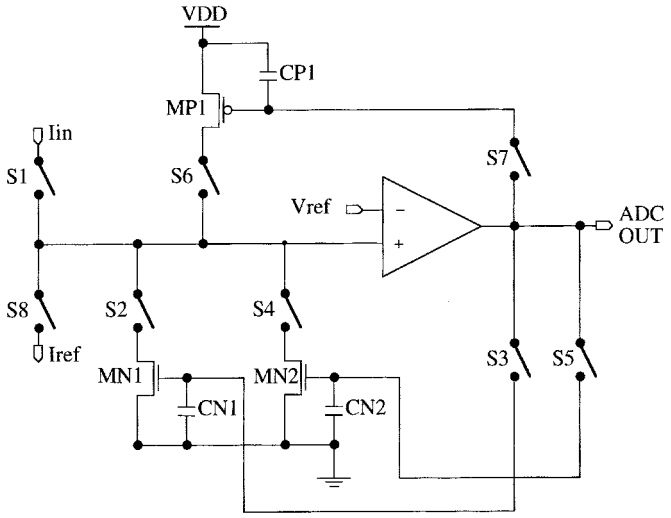


Fig. 7. The current-mode algorithmic analog-to-digital converter.

half-cell. The low cutoff frequency required for dc suppression is achieved using a diode-capacitor filter which avoids the use of chopping or off-chip hybrid components [1] and allows the preamplifier to accommodate a ± 500 μV signal superimposed on ± 160 mV dc or low frequency noise. Each amplifier dissipates only 0.3 mW, occupies 0.2 mm^2, generates the differential signal necessary for the linear voltage-to-current (V–I) converter, and incorporates feedback to prevent output saturation even in the face of gross process variations.

4) Analog-to-Digital Converter: Considering the requirements of the sieve electrode recording system and the features of the various analog-to-digital conversion techniques, an 8-b low-power ADC was designed and implemented using the current-mode algorithmic AD conversion approach [14]. The current-mode design provides a larger dynamic range even with very small current levels, decreasing the power consumption [15].

The algorithmic current-mode converter is implemented using a small number of transistors and switches, as shown in Fig. 7. Conversion is achieved algorithmically by multiplying the input current ($I_{\rm in}$) by two and then comparing it with the reference current ($I_{\rm ref}$). If $2I_{\rm in}$ is larger than $I_{\rm ref}$, then the bit output is "1" and the current, $2I_{\rm in} - I_{\rm ref}$, is fed back to the circuit to determine the next bit, otherwise the bit output is

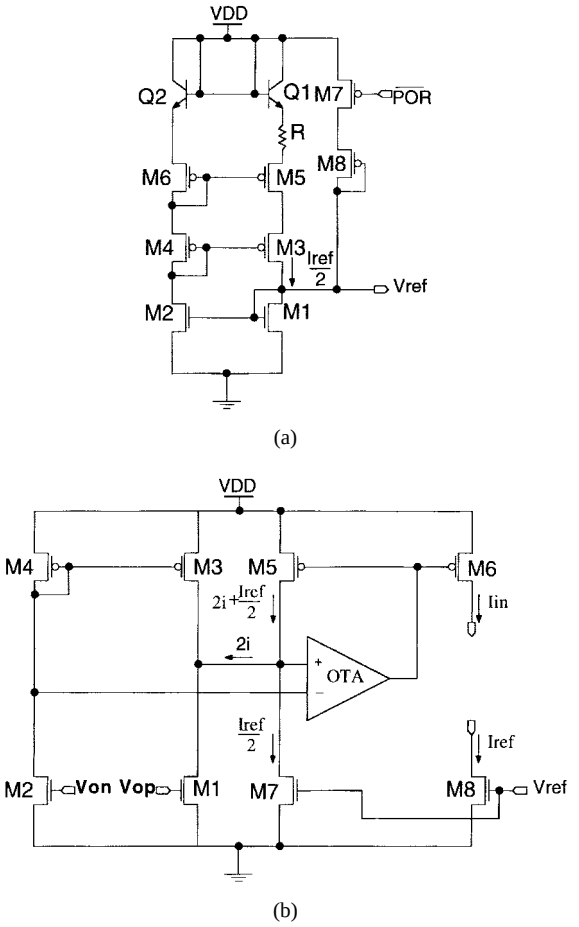


Fig. 8. (a) Current and voltage reference circuitry and (b) the voltage-to-current converter with current shift circuitry.

"0," and $2I_{\text{in}}$ is fed back to the circuit to determine the next bit. This continues until the required bits are all acquired. The reference current is set at 102.4 μA, i.e., a maximum current of only 204.8 μA circulates through the circuit at a time.

The converter combines the amplifier and the current comparator circuitry and consumes only 2 mW, while achieving a conversion accuracy of better than 8 b with a conversion time of 8 μs per bit. The analog portion of the converter occupies only 0.13 mm^2, while the digital portion occupies 1.1 mm^2 in a 3-μm one-metal two-poly CMOS process.

5) Current and Voltage Reference: The current and voltage reference circuit necessary for the ADC is shown in Fig. 8(a). The reference current is set to $V_T \ln(8)/R$ (51.2 μA for this application) by forcing the same bias current in transistors $Q1$ and $Q2$, where the area of $Q2$ is eight times that of $Q1$. These transistors are implemented in the layout by using a 3×3 matrix of minimum size bipolar transistors, where the middle transistor is selected to be $Q1$ and eight peripheral transistors are connected in parallel to implement $Q2$. Transistors $M7$ and $M8$ are used as a start-up circuit during power-on-reset. The resistor is implemented in polysilicon and can be laser trimmed to set the desired reference current. The reference circuit dissipates a power of only 0.5 mW and occupies an area of 0.04 mm^2.

6) Voltage-to-Current Converter: The voltage-to-current (V–I) converter circuit shown in Fig. 8(b) is used to generate the current necessary for the ADC. The converter is designed to provide a transconductance of 1024 μA/V so that a maximum of $\pm$50 mV amplifier output creates a maximum $2i$ current of $\pm$51.2 μA. This current is shifted to 0–102.4 μA range and mirrored to the ADC by using a circuitry with a compensated operational transconductance amplifier (OTA) in order to accommodate negative currents while preventing degradation of the accuracy of the converter due to channel-length modulation, especially for low currents. Simulation results show that the converter provides a nonlinearity of less than 0.08% (an accuracy $>$9 b). The V–I converter has a settling time $\approx$2 μs even for an output current of 0.1 μA, occupies an area of 0.05 mm^2, and dissipates $\approx$2.8 mW.

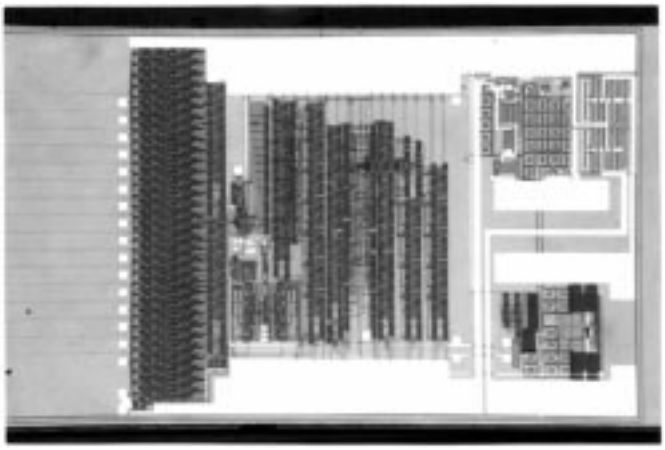


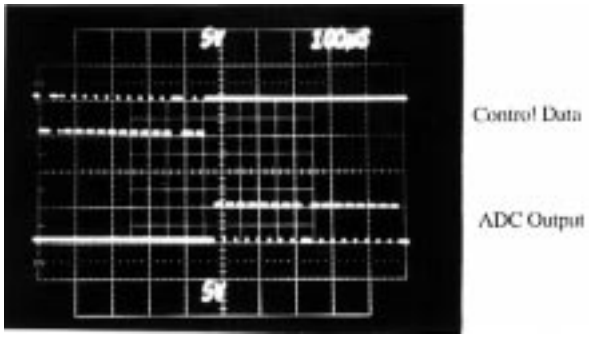
Fig. 9. Photograph of the chip fabricated using the 3-μm, p-well, single-metal, double-poly CMOS process at the University of Michigan. The chip measures 4 $\times$ 6 mm^2 and contains more than 5000 transistors.

IV. Experimental Results

The circuit has been designed and fabricated using a custom 3-μm p-well bipolar-CMOS process, and its full functionality has been verified. Fig. 9 shows a photograph of the chip, which measures 4 $\times$ 6 mm^2 and contains $\approx$5000 transistors.

In order to test the circuit, external electronics were designed and implemented using a Motorola 68HC11 controller board to generate the serial encoded data, based on the address channel information and the mode of the operation set by the user. The external electronics also includes circuitry to recover the recorded and digitized analog signal coming from the implanted on-chip circuit. The functionality of all of the circuit blocks were verified, including the control circuit, the current reference circuit, the front-end analog multiplexers, the V–I converter, and the ADC.

Fig. 10 shows the function of the control circuit in write and read modes. The upper trace shows the control data coming from the external electronics, and the bottom trace shows the output of the ADC. After the write data signal, two 5-b address data are loaded to the address register serially, and the read data command is sent to the on-chip electronics; after recognizing the read data command, the on-chip controller starts the AD conversion, and two 8-b data words are computed algorithmically, generating a serial data output. Once address channels are set, only read data commands can be sent,



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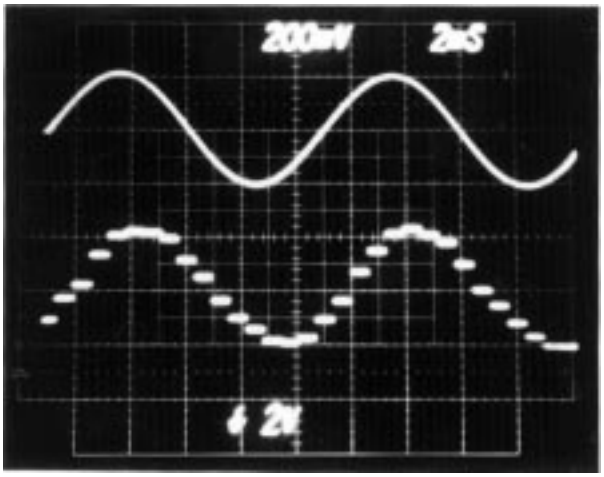

Fig. 11. The input signal to the preamplifier (before being attenuated 500 times) and the recovered digitized output signal, verifying the functionality of the signal processing circuitry.

increasing the sampling rate. This serial data is decoded and converted to analog form with an external DAC to recover the recorded and digitized signals. Fig. 11 shows a $\pm$400 μV input signal to the preamplifier produced by an external signal generator (biological signals are not used for testing of this system) and the output signal recovered by the external electronics, verifying the functionality of the on-chip signal processing circuitry. The on-chip signal processing circuitry dissipates only 10 mW of power when operating at 1 MHz. As stated before, since recorded neural signals are generally in the $\pm$500 μV range, and the input noise of the amplifiers and recording electrodes is in the 5–10 μV range [1], it is expected that the on-chip signal processing circuitry will operate properly in the intended application. It should be noted that conducting biological experiments to verify the functionality of the system *in vivo* is complicated and beyond the scope of this paper; these tests are underway and their results will be presented in the future.

The testing of the RF interface part of the circuitry was performed using an inductively coupled RF telemetry link operating at 1 MHz. This link employs a circular transmitter coil which has a diameter of 10 mm and a height of 2 mm with 60 turns, resulting in an inductance value of $\approx$55 μH and a Q of 26 at 1 MHz. The receiver coil measures 4.7 mm in

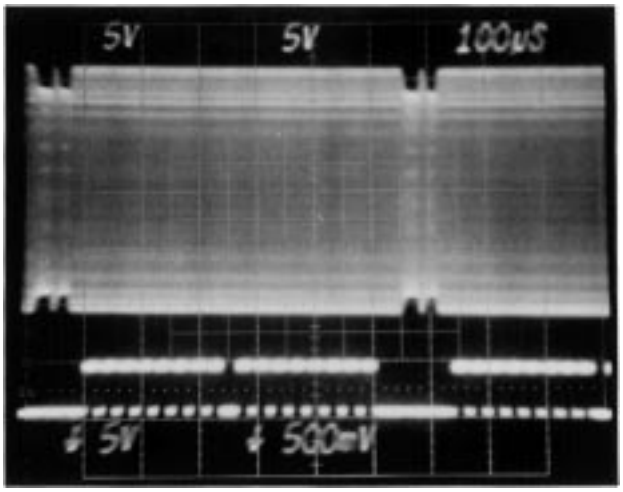

Fig. 12. The received RF signal which has the read data signal modulated on it and the two 8-b output coming from the ADC.

diameter and 2.5 mm in height with 120 turns, resulting in an inductance value of $\approx$65 μH and a Q of 22 at 1 MHz. When the transmitter and receiver coils are placed face-to-face with a distance of 5 mm, they result in an inductive link with a coupling coefficient of 0.082 and a mutual inductance of $\approx$4.9 μH, providing enough voltage gain to test the RF telemetry interface. It should be noted here that the usable working distance between the transmitter and receiver is $\approx$5 mm with 20% tolerance for this design. This distance is more than that required for proper operation in the actual biological environment. With proper design, the mutual inductance, and therefore the received power in the implanted unit, can be maintained relatively constant in the face of small lateral and vertical misalignments in coil positions [16], [17].

This link was first used to verify the functionality of the individual blocks of the RF interface circuitry, including the clock generator, envelope detector, and voltage regulator. After verifying the functionality of the RF interface circuitry, the functionality of the controller circuitry was tested together with the on-chip RF telemetry interface. Fig. 12 shows the received RF signal which has the read data signal modulated on it and the two 8-b output coming from the ADC. Here, the read data signal is extracted from the envelope by the on-chip circuit; with this information, the controller starts the ADC which generates two 8-b serial data, as shown on the bottom trace. It should be noted here that the entire on-chip circuitry, including the envelope detector and the clock generator circuits, in these tests is supplied by 5 V generated by the on-chip voltage regulator circuitry, verifying that the on-chip circuitry can be powered and controlled using an inductively coupled RF telemetry link.

When conducting the test shown in Fig. 12, the output of the ADC was disconnected from the passive telemetry circuitry which modulates the current of the voltage regulator. Therefore, the amplitude of the received RF signal does not change with the ADC output signal. When the ADC output is connected to the passive telemetry circuitry, the received RF signal amplitude changes, as shown in Fig. 13. The upper trace in Fig. 13 shows the amplitude of the received RF signal which

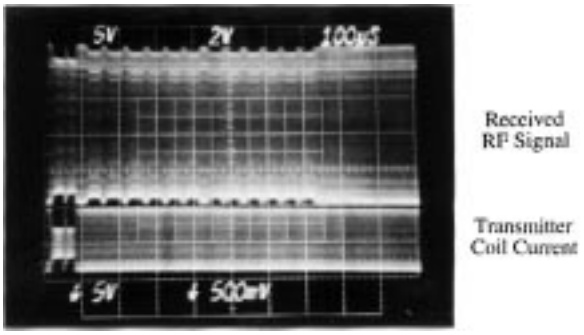

Fig. 13. The received RF signal and the current flowing through the transmitter coil. It can be seen that the amplitude of the received voltage is also modulated due to the controlled loading of the receiver coil to achieve passive telemetry.

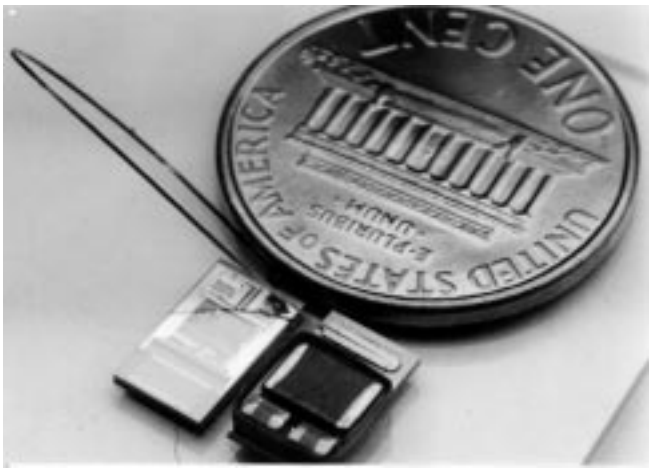

Fig. 14. Photograph of a complete sieve electrode telemetry module with silicon cable interconnects next to a penny. An IC chip without the capacitors and coil is also shown.

has an AM modulated signal containing read data command. After the read data command is received, the controller starts the AD conversion, and the output of the ADC loads the receiver coil, resulting in the AM modulation of the carrier by the on-chip circuitry. This verifies that the passive telemetry portion of the on-chip circuitry functions as designed. The bottom trace in Fig. 13 shows the current flowing through the transmitter coil, which changes $\approx$1% with the controlled current loading of the receiver coil. The envelope of this signal is demodulated using external electronics to obtain the recorded digital signal.

The fabricated chip and the hybrid components are assembled as shown in Fig. 14. Note that the electrode is connected to the electronics using a silicon ribbon cable, which carries the 32 signals from the recording sites. The size of the total implantable unit, including three hybrid capacitors and the receiver coil, is $5 \times 8 \times 2$ mm^3. Table I summarizes features of the sieve electrode telemetrically powered and controlled neural recording system. The entire electronics and components need to be protected by a glass capsule before implanting the unit into an animal, which can be achieved using a hermetic packaging technique based on glass-to-silicon electrostatic bonding [9], [18].

TABLE I
SUMMARY OF THE IMPLANTABLE SIEVE ELECTRODE NEURAL RECORDING SYSTEM FEATURES

Circuit Block	*Area mm²*	*Power Dissp., mW*	*Other Features of the Individual Circuit Blocks*
Preamplifiers	0.22/ea.	0.3/ea.	AC Gain=100, DC Gain=0.01, BW=3.2kHz
V-I Converter	0.05	2.8	Accuracy: 9-10 Bits, Settling Time: 2μsec
ADC	1.23	2	Accuracy: >8 Bits, Conversion Time: 8μsec
Current Reference	0.04	0.5	Provides both current and voltage reference
Control Circuitry	3.6	Low	Operates at 2MHz
Multiplexer	3.6	≈0	Provides Better than 85dB Isolation
Voltage Regulator	2	77	Output Voltage = 5.2V
Clock Generator	1	1	Frequency: 2MHz
Envelope Detector	1	2	Works in current mode
TOTAL	≈24	<90	Implemented Using a 3μm CMOS Technology

V. CONCLUSIONS

This paper presents a telemetrically powered and controlled digital neural recording system with on-chip analog and digital circuitry for use in chronic recording applications. The system allows recording of $\pm$500 μV neural signals from axons regenerated through a micromachined silicon sieve electrode. These signals are amplified using on-chip 100 Hz to 3.1 kHz bandlimited amplifiers, multiplexed, and digitized with a low-power (<2 mW), moderate speed (8 μs/b) current-mode 8-b ADC. The digitized signal is transmitted to the outside world using a passive RF telemetry link. The circuit is implemented using a bipolar-CMOS process. The signal processing CMOS circuitry dissipates only 10 mW of power from a 5-V supply while operating at 2 MHz, and consumes 4×4 mm^2 of area. The overall circuit contains over 5000 transistors, dissipates 90 mW of power, and consumes 4×6 mm^2 of area. This is one of the few complete telemetry systems developed for neurophysiological applications which combines signal amplification and filtering, low-power A/D conversion, bidirectional user interface, and RF telemetry units for power and data transfer all integrated monolithically on a single chip. The system is designed for obtaining recordings using sieve electrodes, but it can be used in a number of other neural recording applications by simply replacing the sieve electrodes with other types of electrodes. The complete system is now being implanted in appropriate animal models and will be used to acquire long-term neural data.

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REFERENCES

[1] J. Ji and K. D. Wise, "An implantable CMOS circuit interface for multiplexed multielectrode recording arrays," *IEEE J. Solid-State Circuits*, vol. 27, pp. 433–443, Mar. 1992.
[2] A. M. Leung, W. H. Ko, T. M. Spear, and J. A. Bettice, "Intracranial pressure telemetry system using semicustom integrated circuits," *IEEE Trans. Biomed. Eng.*, vol. BME-33, pp. 386–395, Apr. 1986.
[3] M. G. Dorman, M. A. Prisbe, and J. D. Meindl, "A monolithic signal processor for a neurophysiological telemetry system," *IEEE. J. Solid-State Circuits*, vol. SC-20, pp. 1185–1193, Dec. 1985.
[4] B. Smith, P. H. Peckham, M. W. Keith, and D. D. Roscoe, "An externally powered, multichannel, implantable stimulator for versatile control of paralyzed muscle," *IEEE Trans. Biomed. Eng.*, vol. BME-34, pp. 499–508, July 1987.

[5] H. V. Allen, J. W. Knutti, and J. D. Meindl, "Integrated power controllers and RF data transmitters for totally implantable telemetry," *Biotelemetry Patient Monit.*, vol. 6, pp. 147–159, 1979.
[6] D. C. Galbraith, "An implantable multichannel neural stimulator," Ph.D. dissertation, Stanford Univ., Stanford, CA, Dec. 1984.
[7] T. Akin, K. Najafi, and R. Bradley, "An implantable multichannel digital neural recording system for a micromachined sieve electrode," in *Tech. Dig., 8th Int. Conf. Solid-State Sensors and Actuators (Transducers'95)*, Stockholm, Sweden, June 1995, pp. 51–54.
[8] T. Akin, K. Najafi, R. Smoke, and R. Bradley, "A micromachined silicon sieve electrode for nerve regeneration applications," *IEEE Trans. Biomed. Eng.*, vol. BME-41, pp. 305–313, Apr. 1994.
[9] T. Akin, B. Ziaie, and K. Najafi, "RF telemetry powering and control of hermetically-sealed integrated sensors and actuators," in *Dig., Solid-State Sensors and Actuators Workshop*, Hilton Head, SC, June 1990, pp. 145–148.
[10] B. Ziaie, Y. Gianchandani, and K. Najafi, "A high-current IrOx thin-film neuromuscular microstimulator," in *Tech. Dig., IEEE Int. Solid-State Sensors and Actuators Conf.*, San Francisco, CA, June 1991, pp. 124–127.
[11] E. A. Vittoz, "MOS transistors operated in the lateral bipolar mode and their applications in CMOS technology," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 273–279, June 1983.
[12] C. A. Laber, C. F. Rahim, S. F. Dreyer, G. T. Uehara, P. T. Kwok, and P. R. Gray, "Design considerations for a high-performance 3-μm CMOS analog standard-cell library," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 181–189, Apr. 1987.
[13] T.-W. Pan and A. A. Abidi, "A 50-dB variable gain amplifier using parasitic bipolar transistors in CMOS," *IEEE J. Solid-State Circuits*, vol. 24, pp. 951–961, Aug. 1989.
[14] D. G. Nairn and A. T. Salama, "A ratio-independent algorithmic analog-to-digital converter combining current mode and dynamic techniques," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 319–325, Mar. 1990.
[15] C. Toumazuo, F. J. Lidgey, and D. G. Haigh, Eds., *Analogue IC Design: The Current-Mode Approach.* London: Peregrinus, 1990.
[16] F. C. Flack, E. D. James, and D. M. Schlapp, "Mutual inductance of air-cored coils: Effect on design of radio-frequency coupled implants," *Med. & Biol. Eng.*, vol. 9, pp. 79–85, 1971.
[17] M. Soma, D. C. Galbraith, and R. L. White, "Radio-frequency coils in implantable devices: Misalignment analysis and design procedure," *IEEE Trans. Biomed. Eng.*, vol. BME-34, pp. 276–282, Apr. 1987.
[18] B. Ziaie, J. Von Arx, M. Nardin, and K. Najafi, "A hermetic packaging technology with multiple feedthroughs for integrated sensors and actuators," in *Tech. Dig., 7th Int. Conf. Solid-State Sensors and Actuators (Transducers'93)*, Yokohama, Japan, June 1993, pp. 266–269.

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Robert M. Bradley, photograph and biography not available at the time of publication.