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Summary

In this work, a data-dependent feedback-cutting–based bit-interleaved 12T static random access memory (SRAM) cell is proposed, which enhances the write margin in terms of write trip point (WTP) and write static noise margin (WSNM) by 2.14× and 8.99× whereas read stability in terms of dynamic read noise margin (DRNM) and read static noise margin (RSNM) by 1.06× and 2.6 ×, respectively, for 0.4 V when compared with a conventional 6T SRAM cell. The standby power has also been reduced to 0.93× with an area overhead of 1.49× as that of 6T. Monte Carlo simulation results show that the proposed cell offers a robust write margin when compared with the state-of-the-art memory cells available in the literature. An analytical model of WSNM for 12T operating in subthreshold region is also proposed, which has been verified using the simulation results. Finally, a small SRAM macro along with its independent memory controller has been designed.

KEYWORDS

circuit design, low-power, SRAM, stability, write ability

1 | INTRODUCTION

With the aggressive growth of semiconductor market, the usage of on-site static random access memory (SRAM) is also increasing. The key design parameters for SRAM, which needs to be improved, vary according to its applications. For example, Internet of Things (IoTs), body sensor nodes (BSNs), wearable electronics, and image processing applications demand robustness and energy efficiency[1]; while for recent artificial neural networks (ANNs) applications, graphics (GPU) processors, servers, and other high end applications, the energy is traded off to achieve high performance.[2] Moreover, in case of wearable IoT applications (such as Google Glass, Fitbit, and Pebble), detecting and reacting to the mobile and ambient context (like speech, occupancy, and motion) from the wireless IoT sensor data has been the key enabler of research. All of these sensors capture and analyze the run time data by temporarily storing it into a memory, and thus, SRAM has been the repetitive architecture of this data storage and occupies the major portion of the system area.[3] Therefore, the power consumed by SRAM plays the crucial role in overall power consumed by the system.

Various methods have been implemented in the literature for minimizing the power consumption in which the voltage scaling has always been the preferred choice to reduce both the switching and leakage power for CMOS VLSI.[4] However, designing a resilient SRAM operating in near-threshold or subthreshold region is extremely challenging due to the

increased effect of process, voltage, and temperature (PVT) variations.[5] Therefore, the use of conventional 6T SRAM cell at a low-supply voltage ($< 2V_{TH}$) operation is not preferable due to the reduced noise margin, which leads towards a higher probability of the cell malfunctioning.[6] Read disturb, half-select destruction, and read-write conflict are other major issues of conventional 6T cell at low-supply voltage.

Moreover, in order to implement a large on-chip functionality, the designs are migrating towards the advanced technology nodes. However, with these decreasing technology nodes, the memory failure probability is increasing.[7] To address these issues, various bit cells have been proposed. Verma and Chandrakasan[8] and Kim et al[9] proposed an approach to remove read disturbance and thus to improve the read static noise margin (RSNM) of SRAM cells by decoupling the storage nodes from the bit lines, which is termed as read decoupling. However, any effective strategy to improve the write ability was absent in this solution. Static random access memory cells in Chang et al[10] and Kushwah and Vishvakarma[11] proposed the feedback-cutting–based methodology for the inverter pair used in SRAM to enhance the write margin and dynamic read decoupling to reduce the read disturb. A provision to reduce the leakage power was also incorporated whereby the stacking devices in each of the inverter. However, feedback cutting through NMOS devices causes the storage nodes to be floating. Hence, the cells become prone towards the leakage current and noise occurrence.[5] In addition, these implementations also demand for additional circuitry to generate the data-dependent control signals. A PPN10T cell designed in Lo and Huang[12] uses a latch formed by a cross coupled P-P-N inverter pair for ultralow cell leakage and high immunity to data-dependent bit-line leakage. However, the cell has lower write ability. Saeidi et al[13] proposed a differential 8T cell by cutting off the feedback loop of the cell during read operation and thus to expand the read margin. But it required the use of wider access devices for improved write ability, and therefore, results in the area overhead. In Moghaddam et al,[14] a 9T cell was proposed that is based on the threshold voltage variation technique, where the dynamic threshold voltage (V_{TH}) effect and drain-induced barrier lowering (DIBL) concepts were implemented to suppress the leakage issues. Wang et al[15] proposed a method for energy efficient SRAM cell by the strategic use of multi-V_{TH} devices. But it demands for an additional boosted supply and also involved extra processing steps during fabrication. In Maroof et al,[16] a 10T cell using the charge sharing mechanism between the bit lines has been proposed, which avoids the need of bit line to be precharged up to complete V_{DD} voltage. It results in the improved low-power memory cell, but there is no specific strategy incorporated to improve the write stability. The half-select issues are also not addressed by the work. Therefore, all of the aforementioned discussed cells either contributed to improve the read stability or to control the leakage power. In practice, along with the leakage reduction and read data stability, write ability of SRAM is equally important for the present wearable and mobile IoT systems to record and process the data successfully. Figure 1 shows different published cells, which have been considered in this work.

The work published in Chiu et al[5] proposed a 12T SRAM cell, which has incorporated the data-aware power-cutoff scheme to improve the write operation at low-supply voltage. But the use of two data-dependent word line signal of the cell demands an additional signal generating circuitry, which has resulted into the area and power overhead for the overall memory array. Another single write port bit cell based on cutting off the supply voltage to improve the write ability was proposed in Jain et al.[17] But the power cutoff is recovered back once the current write clock cycle is completed, and hence, the written data may be disturbed by the noise interference during the next clock transition. In Kim and Mazumder,[18] another 12T memory cell has been proposed for write margin improvement. However, no consideration for the impact of memory half-select issues has been made.

In this work, we propose a new cross-point selection based 12T SRAM memory cell. The contributions of this work can be summarized as follows:

1) Stacked combination incorporated with the pull down networks of inverter pair, controlled by the bit lines, supports to enhance the write ability, and thus enlarges the write noise margin.
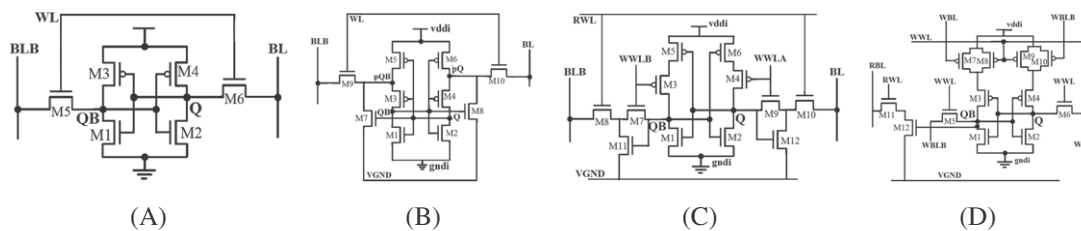

FIGURE 1 Published SRAM bitcell structures from literature. A, conventional 6T; B, PPN10T[12]; C, DAWA12T[5]; and D, 12T J.Kim.[18] RWL, read word line; SRAM, static random access memory; WL, word line; WWL, write word line

2) Isolated read path of proposed cell removes the probability of any noise occurrence and thus produces the read stability in terms of RSNM equivalent to that of hold SNM (HSNM).

3) Column-wise selection through additional NMOS in the write access path enables bit-interleaving structure and completely solves the half-select issues during write operation.

4) Stacking effect in cross-coupled inverters reduces the leakage power.

5) The proposed cell demonstrates its robustness towards the PVT variations.

6) A small size (256 bits) memory with its independent controller has been designed and implemented in a standard 180-nm technology.

Rest of this paper is organized as follows: In section 2, we discuss the proposed 12T SRAM cell and its operation comparing the post-layout simulation results with the state-of-the-art memory cells. Also, we propose an analytical modeling for the write static noise margin (WSNM) of the proposed cell when operating in subthreshold region. Then after, the design and analysis of memory array is discussed in section 3. Section 4 concludes the paper.

2 | ROBUST LOW-POWER HALF-SELECT FREE 12T SRAM

The circuit structure and layout design of the proposed 12T SRAM cell are shown in Figure 2. The cell consists of two cross-coupled inverters with one additional NMOS in each inverter. Lower NMOSFETs (M1, M2) are controlled by the bit line and thus facilitates the data-dependent feedback cutting (DDFC). Therefore, this mechanism improves the write ability of the proposed cell. The stacking effect, which is formed by the use of two series connected NMOS devices in write access path and also in the inverter pair, increases the equivalent resistance of the paths and therefore helps to control the overall leakage power of the proposed cell. Moreover, the cell has an isolated read path to remove the trade-off between read and write operation. It offers the increased read stability equivalent to that of hold stability. The read stability can also be enhanced by increasing the device sizes used in read path, without any degradation in write ability. As the proposed 12T cell has no sizing conflict for its read and write operation, hence, all the transistors for this cell were chosen of minimum size (see Figure 2). However, we have enlarged the width of NMOS (M1-M4) and M12 by 2× to provide the efficient write 0 path from storage node (Q/QB) to ground and improved read stability, respectively. The status of the control signals used for the proposed cell is shown in Table 1.

(A)   (B)
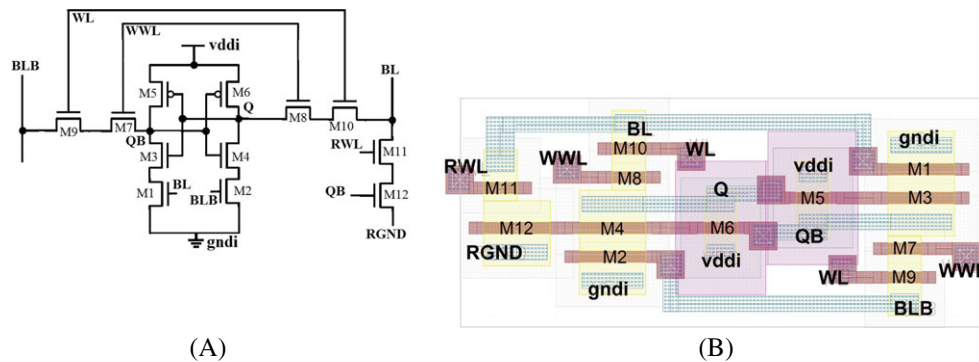
FIGURE 2   Proposed 12T SRAM cell. A, Schematic and B, layout design. RGND, read ground; RWL, read word line; SRAM, static random access memory; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 1   Status of control signals

	Write	Read	Hold
WL	1	0	0
WWL	1	1	0
RWL	0	1	0
RGND	1	0	1

Abbreviations: RGND, read ground; RWL, read word line; WL, word line; WWL, write word line.

To evaluate the performance of proposed 12T SRAM cell, we have chosen state-of-the-art SRAM cells from the literature those that share the similar implementation strategy and compared the proposed 12T with those cells. All the state-of–the-art SRAM cells considered in this work have been redesigned as per the information provided in the related research papers.[5,12,18] Table 2 provides the structural comparison of different SRAM cells.
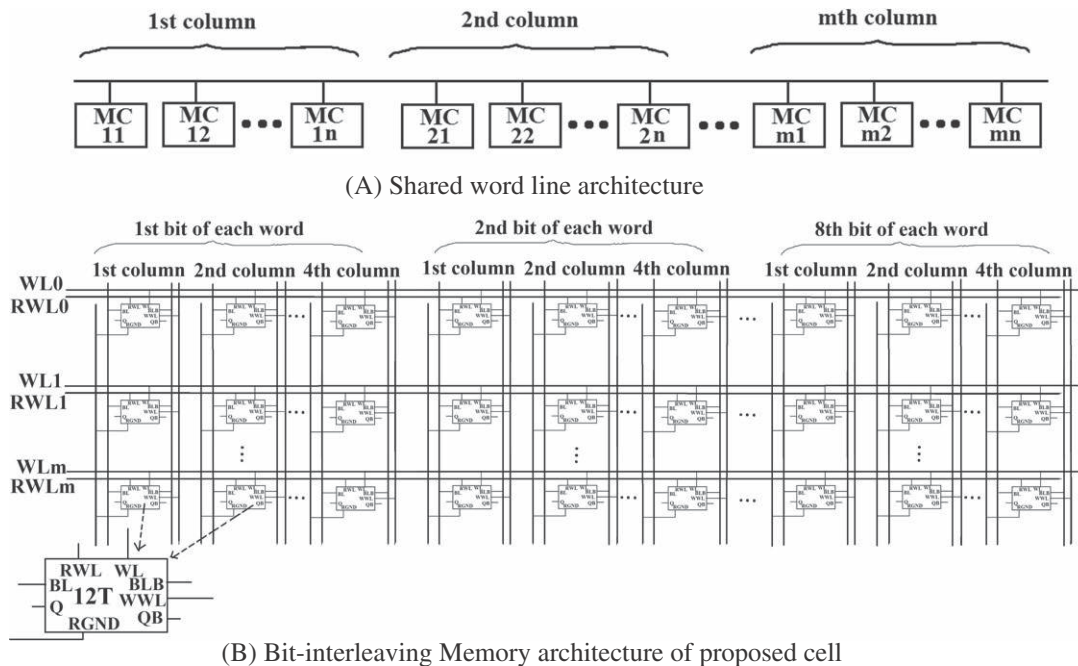
2.1 | Bit-interleaving architecture

In practice, the SRAM cells are arranged in a memory block by using either shared word line (WL) architecture or bit-interleaving architecture,[19] as shown in Figure 3. In shared WL architecture, all the memory bit cells of a common word are arranged one after another. For example, Figure 3A shows a memory block having m × n bits where m is number of columns and n is number of bits per word arranged in shared WL architecture. When the decoder output activates WL signal of a particular row x, all the memory cells connected to that WLx line become activated. Since all the bits of a word are adjacent to each other in this architecture, and WL line for all these bits is activated; therefore, there is high probability for multibit soft-error occurrence especially for ultralow-supply voltage.

Probability of multibit error can be minimized effectively by using the bit-interleaving architecture for a memory array. In this arrangement, nth bit of each word is placed adjacent to each other, as shown in Figure 3B for the proposed 12T

TABLE 2 SRAM cell features comparison

Cell Feature	6T	PPN10T[12]	DAWA12T[5]	12T J.Kim[18]	12T (This work)
Reading/Writing	Diff./Diff.	Diff./Diff.	Diff./Diff.	SE/Diff.	SE/Diff
Bit lines	2	2	2	3	2
Control Signals	1-WL	1-WL,	1-RWL, 1-VGND,	1-RWL, 1-WWL,	1-WL, 1-WWL,
		1-VGND	1-WWLA, 1-WWLB	1-VGND	1-RWL, 1-RGND
Read Decoupling	No	Yes	Yes	Yes	Yes
No. of NMOS in read path	2	2	2	2	2
Stacking effect in write path	No	Yes	Yes	Yes	Yes
Feedback cutting	No	No	Yes	Yes	Yes

Abbreviations: Diff., differential; RWL, read word line; SE, single ended; WL, word line; WWL, write word line; VGND, virtual ground signal.

(A) Shared word line architecture

(B) Bit-interleaving Memory architecture of proposed cell

FIGURE 3 Memory array architecture. A, Shared word line architecture and B, bit-interleaving memory architecture of proposed cell. RGND, read ground; RWL, read word line; WL, word line; WWL, write word line
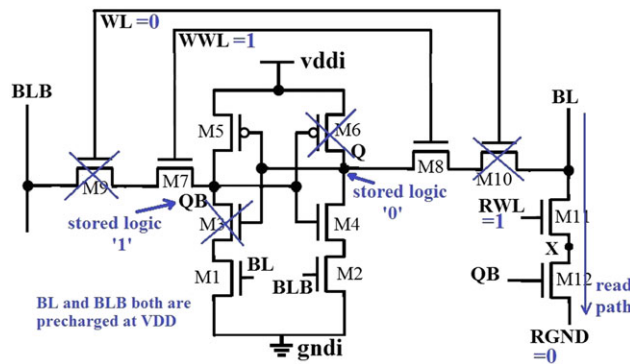
FIGURE 4 Proposed 12T cell during read operation. RGND, read ground; RWL, read word line; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

memory cell. For such kind of architecture, if a single bit soft error occurs, then it can be corrected with the help of simple error correction code (ECC).

2.2 | Read operation with read buffer

The read operation for the selected 12T SRAM is shown in Figure 4 where to perform the read operation, both the bit lines (BL and BLB) are precharged at logic high; read word line (RWL) is enabled high; and the read ground (RGND) signal is made low, while the signals word line (WL) and write word line (WWL) remain at logic low and high, respectively. When RWL is activated using row decoder and RGND is made low using a read buffer driven by column decoder, the proposed cell facilitates a cross point (individual row and column-wise selection) read structure. Hence, there is no issue of half-selected cell for the read operation.

For the read operation when nodes Q and QB store logic low and high, respectively, device M12 is turned ON through the node QB, and therefore, initially precharged BL gets a quick discharge through the path M11 to M12. In this implementation, a differential sense amplifier is used to read the voltage difference of BL and BLB. The discharged bit line BL produces logic low at the output of sense amplifier and therefore results in successful read 0 operation. For the logic high stored at node Q, device NMOS M12 gets turned off and does not allow the discharge path for the bit line. Therefore, BL preserves its precharged value and is read out as logic high by the sense amplifier.

The standard 6T SRAM is most prone to noise during its read operation due to the voltage divider formation in the read path (between the access and pull down devices). Since the storage nodes are directly connected to the read path, therefore, an unwanted noise accumulated at the storage node due to the voltage divider formation in the read path may disturb the stored data. On the contrary, proposed 12T cell prevents any noise involvement at the storage nodes by isolating them from the read path as well as from the bit lines, with low WL value. This approach results in reduced failure probability under interdie/intradie variations and exhibits the enlarged read SNM, which is equivalent to that of hold mode value.[20]

The read current (I_{Read}) for the proposed 12T and 6T SRAM cells have been estimated using standard 65-nm technology node, and the comparative result is illustrated in Figure 5. As the minimum-sized access read transistor (M11) is used in 12T, the read current of this cell is 1.14× less than that of 6T SRAM cell. However, the bit-line leakage of unselected 12T cell is 6× less than that of 6T SRAM cell, due to logic high at RGND signal of proposed 12T, as shown in Figure 5. The read current (and therefore the read speed) of proposed cell can also be increased, if required, independent of its stability by increasing the width of read devices because the read path is decoupled from the cross-coupled inverter pair of the cell and does not affect the stability.

2.3 | Write operation with DDFC

Static random access memory cells proposed in Chang et al[10] and Kushwah and Vishvakarma[11] use the exclusive control signals for feedback cutting, which are generated through the additional circuitry. It results in area and power overhead. Proposed 12T cell removes this overhead by cutting the inverter's feedback path dependent on the data being written on the cell. Figure 6 illustrates the write operation of proposed 12T cell with DDFC approach. For write 0 operation, WL and WWL are enabled; RWL remains disabled; RGND is high while BL and BLB are forced to logic low and high, respectively.
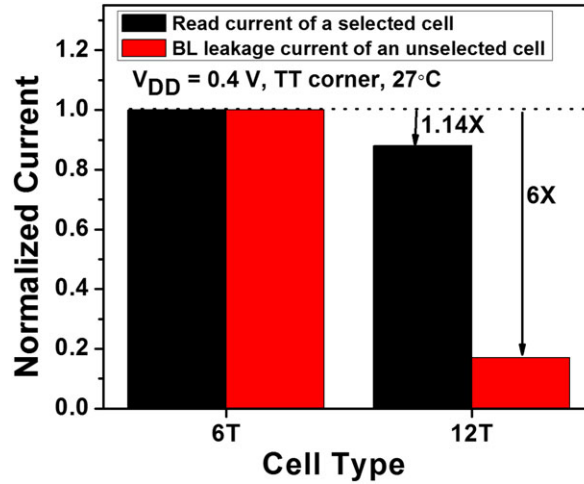
FIGURE 5 BL read current and leakage comparison [Colour figure can be viewed at wileyonlinelibrary.com]
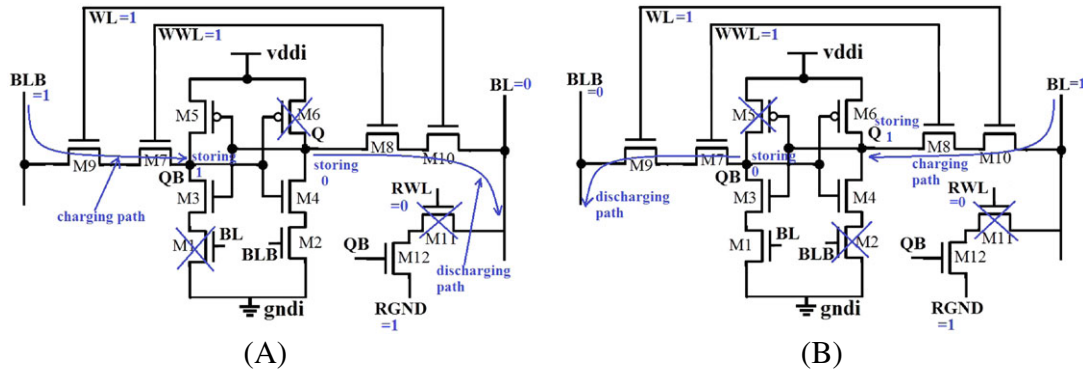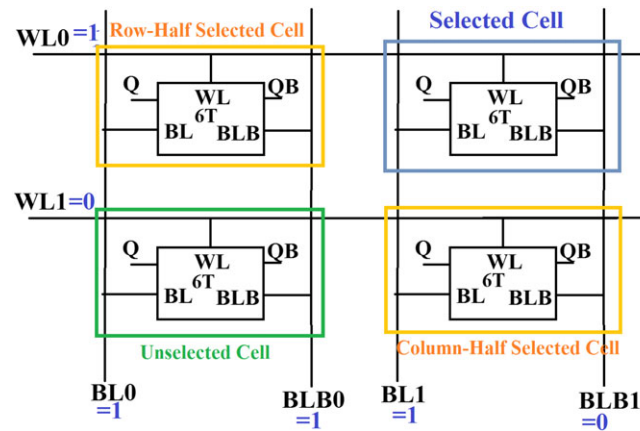

FIGURE 6 Proposed 12T cell during A, write 0 and B, write 1 operation. RGND, read ground; RWL, read word line; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

As M1 is cut off in this condition, QB gets disconnected from the ground, and therefore, BLB successfully charges up the node QB to logic high through M7 and M9. Then logic high stored at QB completely turns off M6 and thus helps to discharge the node Q to zero through the paths M8/M10 and M4/M2 to successfully write 0 into the selected cell. For the proposed cell implementation, a symmetric write structure has been used; therefore, a similar operation is performed for write 1 with the feedback path cutting through M2, as depicted in Figure 6B.

2.4 | Write half select with cross-point selection

As illustrated in Figure 7, while writings 1 and 0 on storage nodes (Q and QB, respectively) of selected 6T cell arranged in the memory array, the corresponding bit lines BL and BLB are activated with 1 and 0, and WL signal of that particular row is enabled. But the cells connected in the same column with low WL values may get affected by the leakage currents through these bit-line voltages, and it may cause to flip the stored data of these cells. This issue is referred as column half-select issue. Similarly, V_{DD} at WL signal activates an entire row of a 6T memory array; however, the bit lines of unintended cells in that particular row might still be clamped at logic high. This may potentially disturb the stored data of those unintended cells, referred as row-half-select issue.

On the contrary to the 6T SRAM array, write operation of proposed 12T SRAM cell is performed by activating the row-based signal WL and column-based signal WWL as shown in Figure 8. Therefore, a row- and column-based selection enables a cross-point write structure. In addition to this, cascaded NMOS devices (M7, M9, M8, and M10) that increases the resistance of write path reduces the write current of half-selected/unselected cells. Therefore, it can be stated that half-select issue is absent in the proposed 12T cell. The performance evaluation of the proposed design using the Monte Carlo simulations for the selected, row-half-selected, and column-half-selected SRAM cell during write 1 mode is shown

FIGURE 7 A 2 × 2 array composed of 6T SRAM cell during write operation. SRAM, static random access memory; WL, word line [Colour figure can be viewed at wileyonlinelibrary.com]
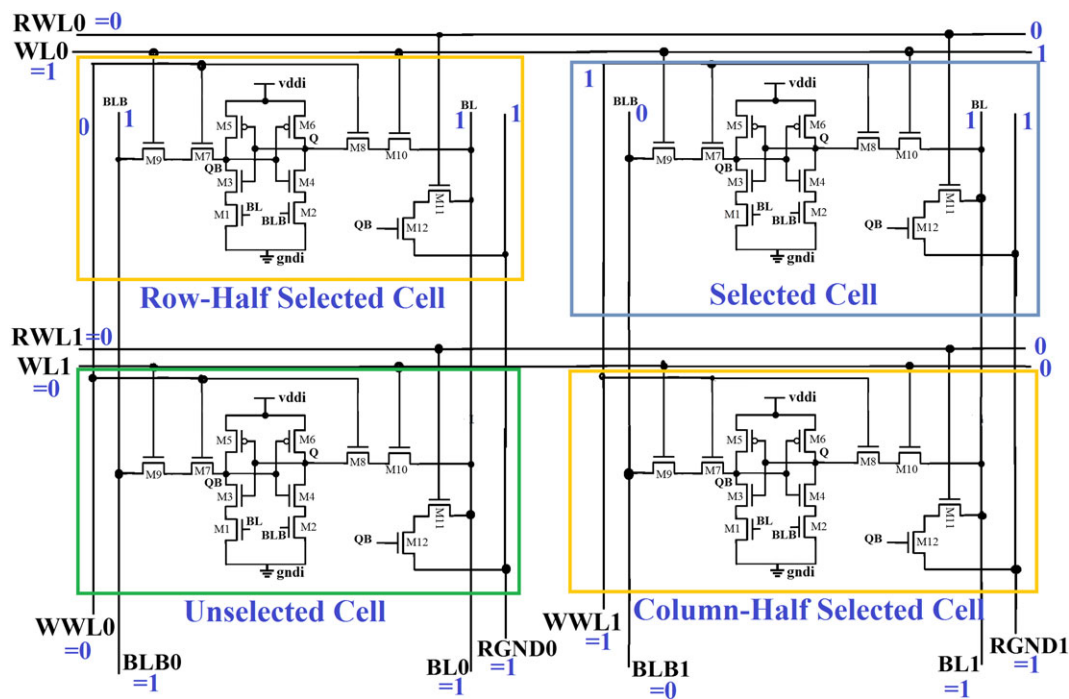

FIGURE 8 A 2 × 2 array composed of proposed 12 SRAM cell during write operation. RGND, read ground; RWL, read word line; SRAM, static random access memory; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

in Figure 9. It is shown in Figure 9 that the proposed cell remains unaffected from the half-select issues and can effectively tolerate the noise occurrence without any change in its stored data.

2.5 | Read stability

Read static noise margin is most common parameter to determine the read stability of a memory cell, which is measured as the side length of the largest square that can be inscribed into the smaller lobe of butterfly curve.[21] The RSNM butterfly curves of 12T and 6T memory cells obtained through the Monte Carlo simulations with 2000 samples are shown in Figure 10. The figure shows a noticeable enhancement in read stability of 12T cell as compared with that of 6T even at the worst process corner FS (fast NMOS and slow PMOS) while working in subthreshold region of operation (0.4-V supply). The RSNM value of proposed 12T has also been compared with state-of–the-art SRAM cells at worst process corner (FS) for both subthreshold as well as superthreshold region of operation (see Table 3).
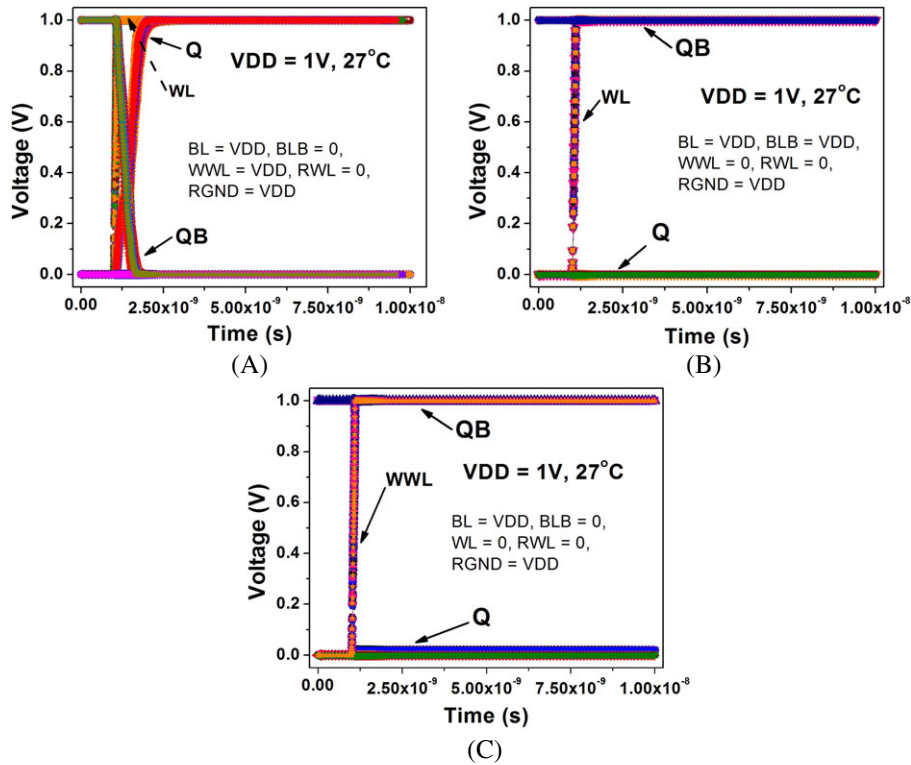
FIGURE 9 Transient simulation results of proposed 12T write operation at 65-nm technology node with 2000 Monte Carlo samples, 1-V supply and 27°C temperature at 65-nm node for A, selected; B, row-half-selected cell; and C, column-half-selected cell. RGND, read ground; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]
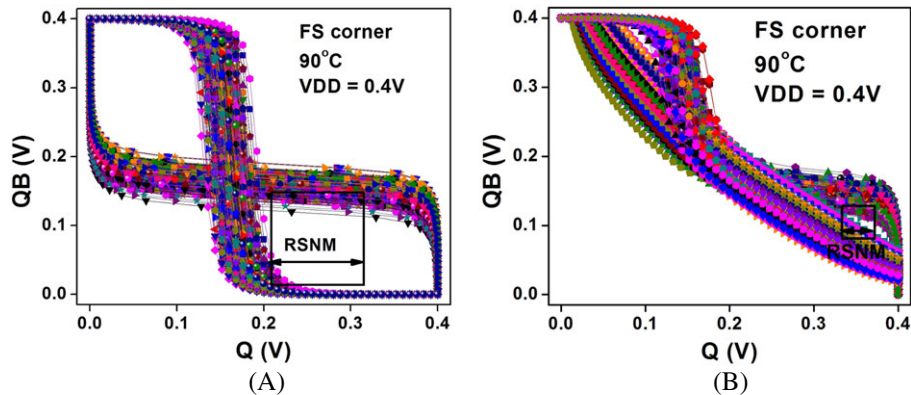

FIGURE 10 Worst case (FS) corner read butterfly curve for 2000 Monte Carlo samples at 0.4-V supply and 90°C temperature with 65-nm technology node for A, proposed 12T and B, 6T static random access memory (SRAM) cell [Colour figure can be viewed at wileyonlinelibrary.com]

Read static noise margin value reflects the read stability of SRAM cell only for its static condition, which is measured by the DC analysis of SRAM cell. Therefore, to obtain the cell read stability during transient state, the dynamic read noise margin (DRNM) is calculated, which is the minimum difference between the storage nodes (Q and QB) during the read operation as shown in Figure 11A. The statistical analysis of dynamic read stability has been performed at FS corner by using 2000 Monte Carlo cycles. Accordingly, a comparison of DRNM mean (μ) values obtained for 12T cell with the published cells is shown in Figure 11B. It can be seen that the proposed 12T cell has higher DRNM value ($1.058\times$ and $1.072\times$ at 0.4 V and 1 V, respectively) than that of 6T, while the DRNM mean (μ) value of proposed cell is equivalent to other SRAM cells under consideration. The reason is that except to 6T cell, all other SRAM cells have employed the read decoupling strategy to improve the cell read stability.

TABLE 3 RSNM comparisons of SRAM cells at FS corner, 27°C for subthreshold and superthreshold operation

	Subthreshold (0.4 V)	Superthreshold (1 V)
12T	110.4 mV	321.7 mV
6T	42.4 mV	144.9 mV
12T J.Kim[18]	122.9 mV	344.2 mV
DAWA12T[5]	119.4 mV	344.2 mV
PPN10T[12]	100.6 mV	309.9 mV

Abbreviations: RSNM, read static noise margin; SRAM, static random access memory.
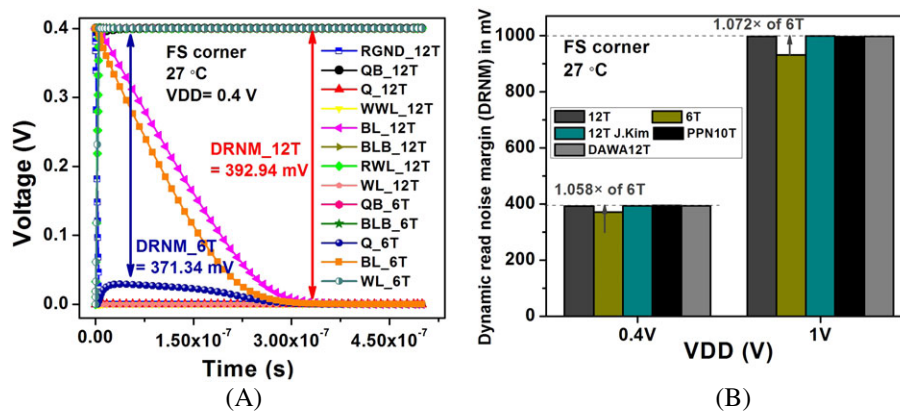

FIGURE 11 Dynamic read noise margin (DRNM) at FS corner. A, Read timing diagram to determine DRNM value at 0.4 V and B, DRNM mean value (μ) comparison using 2000 Monte Carlo samples at 65-nm node [Colour figure can be viewed at wileyonlinelibrary.com]

According to Table 3, RSNM value of proposed 12T cell is significantly higher (2.6×) than that of 6T cell. It can further be enhanced by widening the read devices of the proposed cell without affecting its write performance. Additionally, higher dynamic RNM mean (μ) value of 12T than that of 6T and similar to that of 12T J.Kim,[18] PPN10T,[12] and DAWA12T,[5] as shown in Figure 11B, proves the effective read stability of the proposed 12T cell.

2.6 | Write ability with DDFC

Write ability of an SRAM cell is evaluated in terms of WSNM, which is the ability of memory cell to pull down the node, storing 1, to a value below the switching threshold voltage of another inverter storing 0 so that it can successfully flip the cell stored data.[22] Write static noise margin is determined from the write butterfly curve, which is the side length of the smallest square inscribed in write butterfly curve.[21] A comparison of write butterfly curves for different SRAM cells at the worst process (SF) corner is given in Figure 12, where it can be seen that the proposed 12T cell has the highest WSNM value. It is 9×, 1.2×, 1.7×, and 1.94× higher when compared with the WSNM value of 6T, 12T J.Kim,[18] DAWA12T,[5] and PPN10T,[12] respectively, at 0.4-V V_{DD}. This improvement in write stability of the proposed 12T cell is because of the interrupted feedback path of cross-coupled inverters by turning off either M1 or M2 depending on the writing data. The feedback cutting of inverter pair creates a high-resistance path between the storage node (Q/QB) and ground and therefore prevents the functioning of cross coupled inverters. This enhances the write ability of proposed cell without any additional write assist circuit and therefore makes it robust against any noise occurrence at the stored data. The Monte Carlo simulation (2000 samples) results of proposed 12T and 6T cell at a temperature of 90°C using the worst case (SF corner) for the write butterfly curves are shown in Figure 13. From Figure 13, a significant enhancement can be seen in write stability (in terms of the side of square fitted inside the butterfly curves) of proposed cell against the interdie and intradie variations.

In the recent studies, write trip point (WTP) has also been mentioned as a common factor to define the write ability of a memory cell. It is defined as the difference between V_{DD} and WL value at which stored data of SRAM cell flips, when the bit lines holds the data which is to be written, and WL is swept from 0 to V_{DD}.[23] We have also analyzed the write ability in terms of WTP as shown in Figure 14A where it can be seen that the proposed cell exhibits a significantly higher WTP value
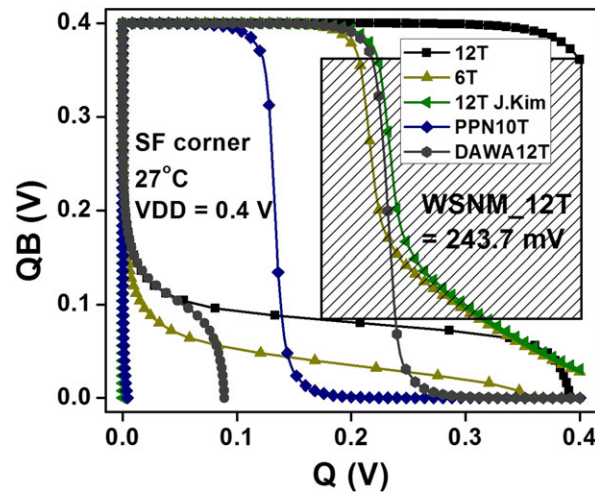
FIGURE 12 Write static noise margin (WSNM) at worst (SF) corner with 0.4-V supply [Colour figure can be viewed at wileyonlinelibrary.com]
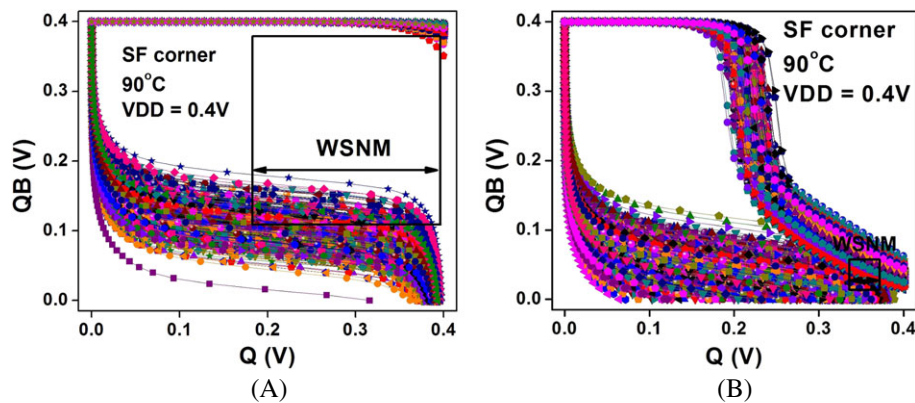

FIGURE 13 Worst (SF) corner write butterfly curve for 2000 Monte Carlo samples at 0.4-V supply and 90°C temperature with 65-nm technology node for A, proposed 12T and B, 6T SRAM cell. SRAM, static random access memory; WSNM, write static noise margin [Colour figure can be viewed at wileyonlinelibrary.com]
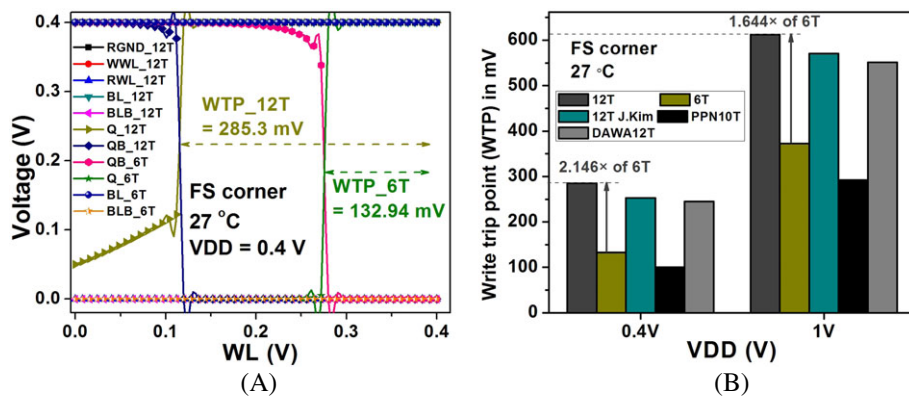
FIGURE 14 A, Write trip point (WTP) determination for 12T and 6T at 0.4 V and B, WTP comparison of different cells for V_{DD} variation at 65-nm technology node [Colour figure can be viewed at wileyonlinelibrary.com]

(ie, higher write ability) for the proposed 12T SRAM cell, which is 2.146× higher than that of 6T. Write ability of proposed cell has also been compared with the other published cells from the literature for subthreshold and superthreshold region as shown in Figure 14B, which shows that the proposed cell has the highest write ability, which is 1.13×, 1.17×, and 2.83× higher than that of 12T J.Kim,[18] DAWA12T,[5] and PPN10T,[12] respectively.
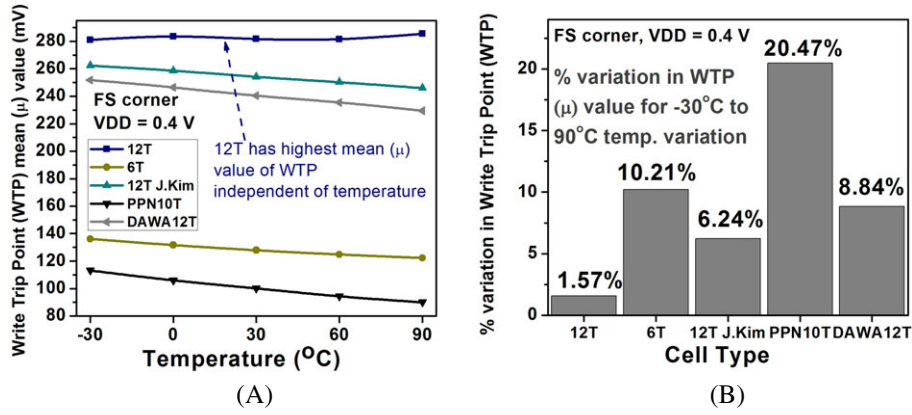
FIGURE 15 2000 Monte Carlo simulation results at 65-nm node for A, write trip point (WTP) mean (μ) value comparison for temperature variations and B, % variation in WTP mean (μ) value for temperature varying from $-30°C$ to $90°C$ [Colour figure can be viewed at wileyonlinelibrary.com]

Figure 15 provides the statistical analysis of write ability using 2000 Monte Carlo simulation including the interdie and intradie variation effects. In Figure 15A, the mean (μ) WTP value is compared with all other SRAM cells under consideration to observe the temperature variation effects for the range of $-30°C$ to $90°C$, and it provides the highest WTP value for the proposed cell at all the temperatures. Figure 15B shows the maximum percentage variation in WTP mean value for the temperature range of $-30°C$ to $90°C$, which illustrates that the proposed 12T SRAM cell has the least WTP sensitivity to temperature variation which is 6.5×, 3.97×, 5.63×, and 13.04× smaller when compared with 6T, 12T J.Kim,[18] DAWA12T,[5] and PPN10T,[12] respectively.

2.7 | Standby power

The basic subthreshold current modeling for a MOSFET is given as[24]:

$$I_{sub} = I_0 exp \left[\frac{V_{GS} - V_{TH} + \lambda_{BS}V_{BS} + \lambda_{DS}V_{DS}}{\eta V_T} \right]$$
$$\left[1 - exp \left(\frac{-V_{DS}}{V_T} \right) \right], \tag{1}$$

where I_0 is the subthreshold current when $V_{GS} = V_{TH}$; η is the subthreshold swing factor; V_T is thermal voltage, which is equal to KT/q; $\lambda_{BS} > 0$ is the body bias coefficient; and $\lambda_{DS} > 0$ is the DIBL coefficient.

Threshold voltage of a short channel device related to its V_{DS} voltage due to DIBL effect and V_{BS} voltage due to the body biasing can be given[25] by Equation 2:

$$V_{TH} = V_{TH0} - \lambda_{BS}V_{BS} - \lambda_{DS}V_{DS}. \tag{2}$$

Standby condition of proposed 12T SRAM is shown in Figure 16 with logics 0 and 1 stored at nodes Q and QB, respectively. In this condition, the source terminal of M3 maintains a nonzero value and therefore leads to its reduced V_{DS} and V_{BS} voltages. Consequently, it results to increased value of V_{TH} for M3, according to Equation 2, and hence provides an exponential reduction in subthreshold leakage current according to Equation 1. Moreover, stacking of NMOS devices (M1/M3 and M2/M4) leads to increased resistance of pull down path and therefore helps to reduce the overall leakage power of the cell.[23]

Figure 17A depicts the standby power comparison of different SRAM cells in which the power is normalized with respect to that of 12T cell. It shows that 12T attends the minimum power consumption among the comparison except to that of PPN10T.[12] However, the stronger write ability (2.83× WTP and 1.93× WSNM as that of PPN10T[12] at worst corner), equivalent read stability and better half-select behavior of proposed 12T makes it a preferable choice over PPN10T.[12] The Monte Carlo simulation with 2000 samples was performed for all the memory cells to determine the leakage power behavior over the temperature variations ranging from $-30°C$ to $90°C$, as shown in Figure 17B, and it shows that the leakage power performance of proposed 12T SRAM cell is the most robust among the compared cells for temperature variation.
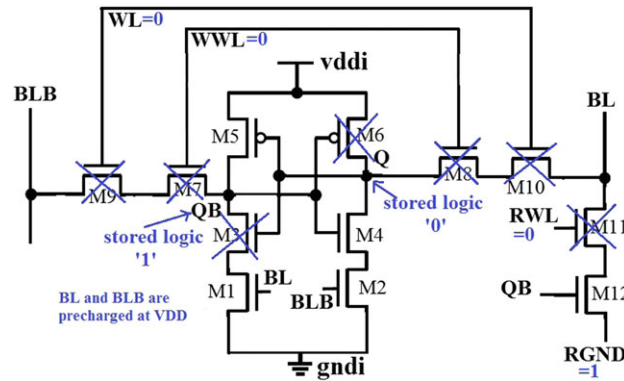
FIGURE 16 Standby condition of proposed 12T SRAM cell for Hold '0'. RGND, read ground; RWL, read word line; SRAM, static random access memory; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]
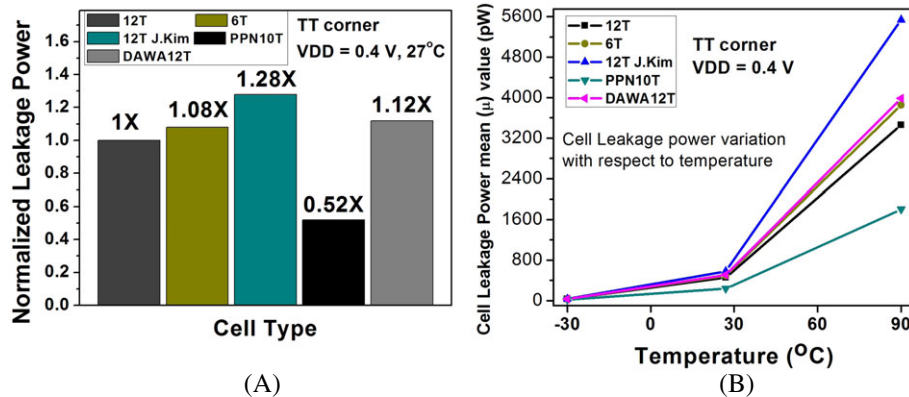
FIGURE 17 Standby power comparison. A, Normalized standby power at 0.4 V and B, standby power mean (μ) value with temperature variations for 2000 Monte Carlo simulations at 0.4 V [Colour figure can be viewed at wileyonlinelibrary.com]

**TABLE 4** Comparison of design metrics among proposed 12T, 6T, PPN10T,[12] 12T J.Kim,[18] and DAWA12T[5]

65-nm Technology Node, VDD = 0.4 V, 27°C	WTP, mV	DRNM, mV	Leakage Power, pW	WSNM, mV	RSNM, mV	HSNM, mV
Conv. 6T	132.94	371.34	482.2	27.1	42.4	110.7
PPN10T	100.74	395.5	234	125.7	100.6	103.4
12T J.Kim	252.96	393.5	578.59	201.9	122.9	122.9
DAWA12T	244.78	393.5	507.1	143.7	119.4	119.4
Proposed 12T	285.30	392.94	451.6	243.7	110.4	110.4

Abbreviations: DRNM, dynamic read noise margin; HSNM, hold static noise margin; RSNM, read static noise margin; WSNM, write static noise margin; WTP, write trip point.

An overall comparison among all the considered SRAM cells for this work, in terms of different design metrics, is presented in Table 4.

2.8 | Simulation results

All the simulation results discussed so far have been determined using the postlayout simulations with a standard 65-nm technology node. However, the final memory array has been designed at a standard 180-nm CMOS technology node and 1.8-V supply voltage as per the requirement of project work (see Acknowledgment). Therefore, to justify the effectiveness of proposed cell among the comparison, all the cells have also been implemented at 180-nm node with the consideration of device sizing while changing the technology node. Layout design of all the state-of-the-art SRAM cells, which are considered in this work, are shown in Figure 18, and a normalized layout area comparison of proposed 12T cell with these
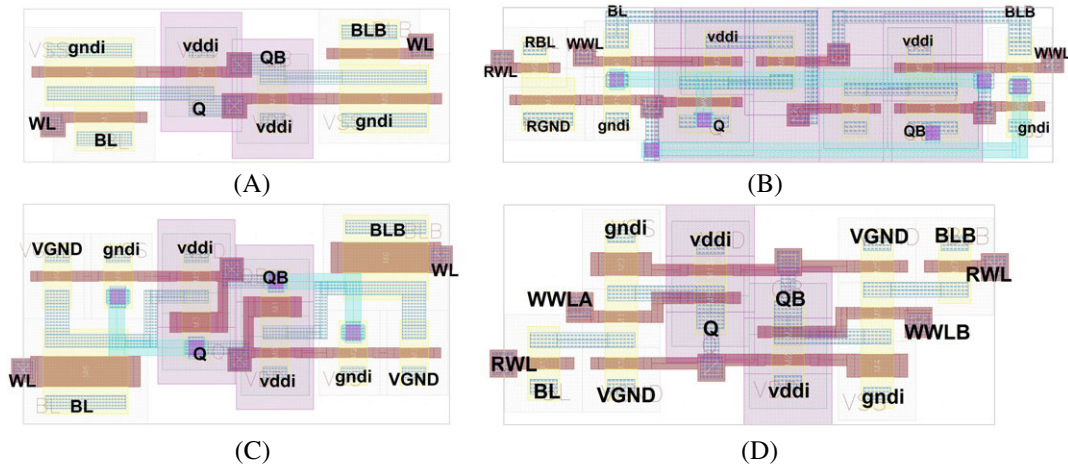
FIGURE 18 Layout design of A, 6T; B, 12T J.Kim[18]; C, PPN10T[12]; and D, DAWA12T[5] using standard 180-nm technology node. RGND, read ground; RWL, read word line; VGND, virtual ground signal; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

TABLE 5 Cell layout area comparison using standard 180-nm technology node

| SRAM Cell	No. of Transistors Used	Layout Area
6T	6 (2 PMOS, 4 NMOS)	1×
PPN10T[12]	10 (4 PMOS, 6 NMOS)	1.57×
DAWA12T[5]	12 (4 PMOS, 8 NMOS)	1.45×
12T J.Kim[18]	12 (6 PMOS, 6 NMOS)	1.46×
12T (this work)	12 (2 PMOS, 10 NMOS)	1.49×
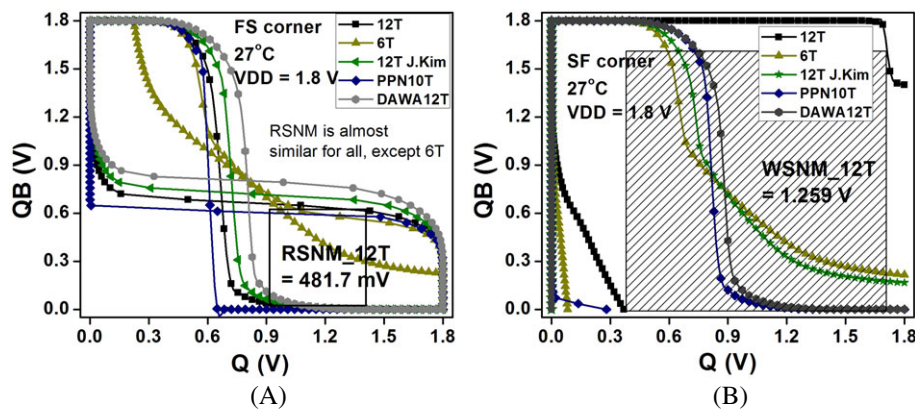
FIGURE 19 Butterfly curves of SRAM cells for A, read and B, write mode at worst process corner and 1.8-V supply with 180-nm node. RSNM, read static noise margin; SRAM, static random access memory [Colour figure can be viewed at wileyonlinelibrary.com]

memory cells is provided in Table 5. The postlayout simulations have been performed for all the memory cells. Figure 19 illustrates the comparison of proposed 12T with the other memory cells for RSNM and WSNM values, respectively. It shows that the read stability of the proposed cell is 2.74× higher than 6T and equivalent to that of other state-of-the-art SRAM cells. Moreover, write stability of our cell is the highest one among all the cells under comparison as shown in 19B.

Figures 20 and 21 show the worst corner RSNM and WSNM analysis, respectively, for the temperature and V_{DD} variations. The RSNM value of proposed 12T cell has lower (7.29%) variation from its maximum value for the temperature variations ranging from −30°C to 90°C while the conventional 6T cell has 11% variation in RSNM. The RSNM variation of proposed cell at different V_{DD} is approximately similar to that of 6T cell as shown in Figure 20. The proposed cell is highly robust for its write stability against the temperature and V_{DD} variations. From Figure 21, it can be seen that the WSNM
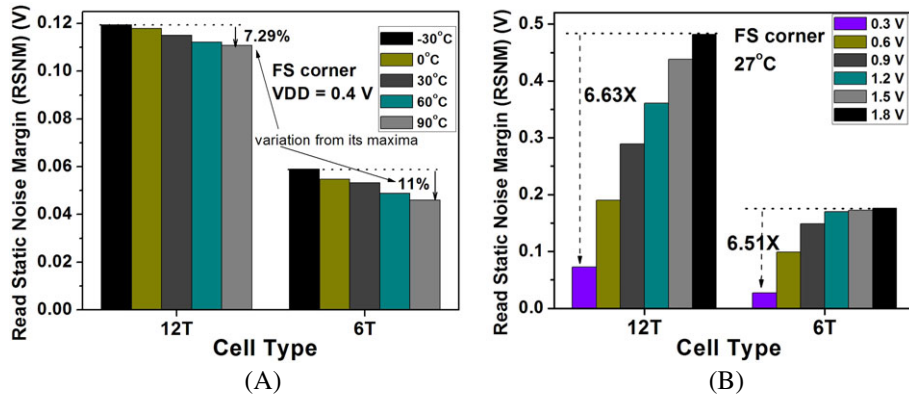
FIGURE 20 Worst case (FS) corner read static noise margin (RSNM) variation A, for different temperatures at 0.4-V supply and B, for V_{DD} variation at 27°C with 180-nm node [Colour figure can be viewed at wileyonlinelibrary.com]
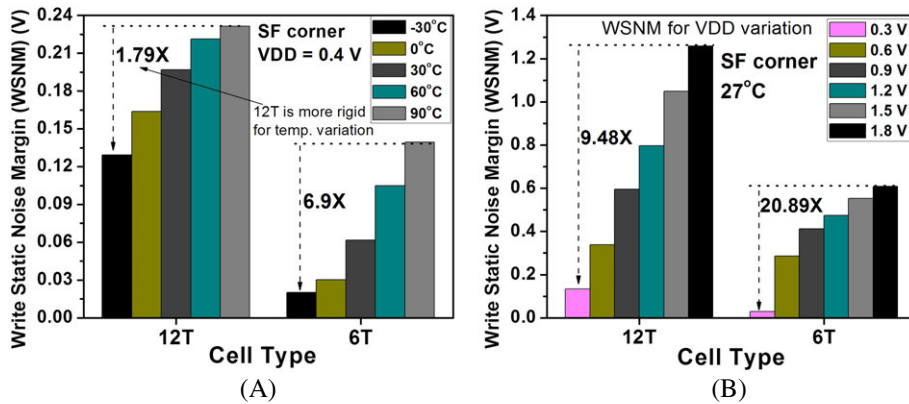
FIGURE 21 Worst case (SF) corner write static noise margin (WSNM) variation A, for different temperatures at 0.4-V supply and B, for V_{DD} variation at 27°C with 180-nm node [Colour figure can be viewed at wileyonlinelibrary.com]
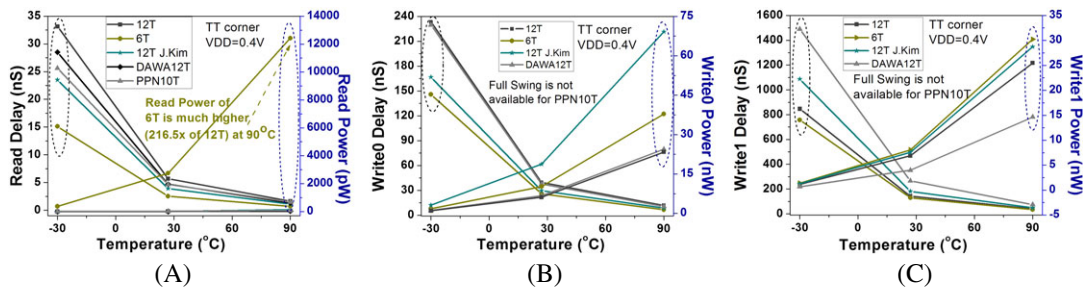

FIGURE 22 Delay and power comparisons at different temperature values during A, read; B, write 0; and C, write 1 operation at 27°C temperature and 0.4-V supply with 180-nm node [Colour figure can be viewed at wileyonlinelibrary.com]

variations for 12T cell from its maximum values are only 1.79× and 9.48×, while the same for 6T are 6.9× and 20.89× for −30°C to 90°C temperature variation and 0.3- to 1.8-V supply voltage variations, respectively, at the worst process corner.

The read/write performance of the cell has also been analyzed and compared with state-of-the-art SRAM cells. The simulation results are given in Figure 22 and Table 6. From Figure 22A, it can be seen that the proposed cell sacrifices in terms of the read speed as the read delay is 2.23×, 1.45×, 1.22×, and 1.2× higher than that of 6T, 12T J.Kim,[18] PPN10T,[12] and DAWA12T,[5] respectively, at 0.4-V V_{DD}. It is because of the increased bit line (BL) capacitance due to the gate capacitance of NMOS M1 and diffusion capacitances of NMOS (M10 and M11). However, the read power consumption is improved for the proposed 12T cell (see Figure 22). It consumes 225×, 1.35×, and 1.86× less read power as compared with 6T, 12T

TABLE 6 Power delay product (PDP) comparison during read, write 0, and write 1 operation

180-nm technology node, VDD = 0.4 V, 27°C	12T	6T	12T J.Kim[18]	PPN10T[12]	DAWA12T[5]
Write 0 PDP (10^{-18})	242.946	263.934	558.154	Full swing is not available	254.37
Write 1 PDP (10^{-18})	981.274	1047.08	1378.79	Full swing is not available	1057.34
Read PDP (10^{-21})	69.34	6992.62	64.52	106.08	61.41
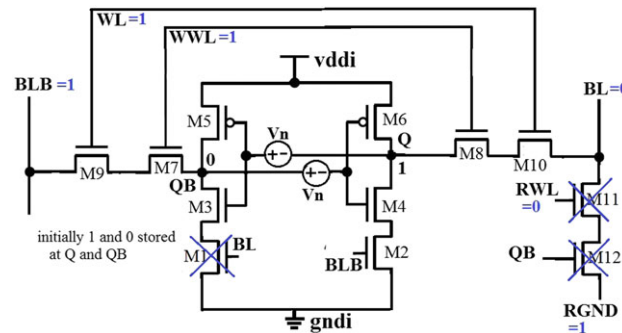
FIGURE 23 12T SRAM write operation with static noise source V_n injected for WSNM determination. RGND, read ground; RWL, read word line; SRAM, static random access memory; WL, word line; WWL, write word line [Colour figure can be viewed at wileyonlinelibrary.com]

J.Kim,[18] and PPN10T,[12] respectively but 2.69× higher than that of DAWA12T[5] at 0.4-V supply voltage. The overall read performance is commonly estimated using the read energy in terms of the read power and delay product (PDP). It can be seen from Table 6 that the read PDP of proposed 12T cell is comparable with the 12T J.Kim[18] and DAWA12T[5] due to the similar read structure, and it is significantly higher as compared with the 6T and also less than that of PPN10T.[12] In this work, the read delay has been estimated as the time between the activation of RWL and the discharging of bit line by 100 mV from its initial value.

Figure 22B,C illustrates the write performance analysis of proposed 12T cell at different temperature values with 0.4-V V_{DD}. Here, the write 1 delay has been estimated as the time between the activation of WWLs (WL/WWL) and the storage node Q reaching up to 0.9 V_{DD}. Similarly, write 0 delay is the time between the activation of WWLs and the time instant for the storage node Q discharging down to 0.1 V_{DD}. Although the proposed cell suffers by the slower write speed due to the increased bit line capacitances, it provides the improved write power that can be seen in Figure 22B,C. Therefore, it offers the overall improvement in its write energy, which can be observed from Table 6. The improved write 1 energies (write 1 PDP) of proposed 12T are 0.94×, 0.71×, and 0.93× while the improved write 0 PDPs are 0.92×, 0.44×, and 0.95× as that of 6T, 12T J.Kim,[18] and DAWA12T,[5] respectively, at 0.4-V supply voltage. The PPN10T[12] cell has not been considered for the write performance comparison in Figure 22B and 22C, as the cell is not capable to provide the full swing at its storage nodes during the write operation.

2.9 | Subthreshold analytical modeling WSNM

Write static noise margin estimation is based on the Voltage Transfer Characteristic (VTC) curves of back-to-back inverters.[21,26] For the write operation, two static noise sources are injected in the feedback loop of inverters in such a manner to prevent the bit cell from being written, as depicted in Figure 23. In that case, the minimum voltage of noise source that forces the bit cell to hold its previous stored data, during the write operation, can be defined as WSNM.[18]

With the assumption that logics 1 and 0 are initially stored at node Q and QB, BL and BLB lines are forced to logics 0 and 1, respectively; WL and WWL are enabled for the write operation; RGND remains connected to 1; and RWL is disabled, which is illustrated in Figure 23. In this condition, logic 0 at BL turns off the device M1 and cuts the path from QB node to ground. Thus, it weakens the node QB to maintain its stored 0 value and starts to charging it up to V_{DD} by BLB through the path M7 and M9. Since the node QB is at logic 1 now, writing logic 0 at Q would be the completion of write operation. Therefore, the voltage value of V_n at which the drain current of M4 and M6 are equal (which is the inverter's switching condition) can be the WSNM.[18] Based on this condition, an analytical model of WSNM value for subthreshold SRAM cell is proposed here.

By equating the subthreshold drain current of M4 and M6 to estimate the WSNM value,

$$I_{SD_{M6}} = I_{DS_{M4}}. \tag{3}$$

After substituting the values of $I_{SD_{M6}}$ and $I_{DS_{M4}}$ and then solving the equation (the detailed derivation is given in the Appendix A), finally, we get the WSNM analytical model as follows:

$$WSNM_{sub} = V_n = \frac{1}{2} \left[V_{DD} - V_{THn} + V_{THp} \right.$$
$$\left. + \eta V_T log_e \left[\frac{\mu_n \, (\frac{W}{L})_{M4}}{\mu_p \, (\frac{W}{L})_{M6}} \right] \right]. \tag{4}$$

Write static noise margin analytical model given in Equation 4 has been verified with the help of simulation results as shown in Figure 24, using the standard 180-nm technology node. The maximum error of our proposed analytical model is 11.4% when compared with the simulated data.
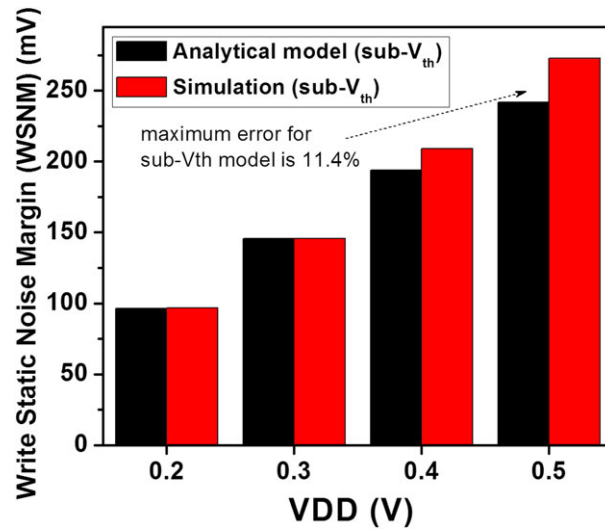

FIGURE 24 Comparison of analytical model with simulated write static noise margin (WSNM) value at different V_{DD} for 180-nm node [Colour figure can be viewed at wileyonlinelibrary.com]
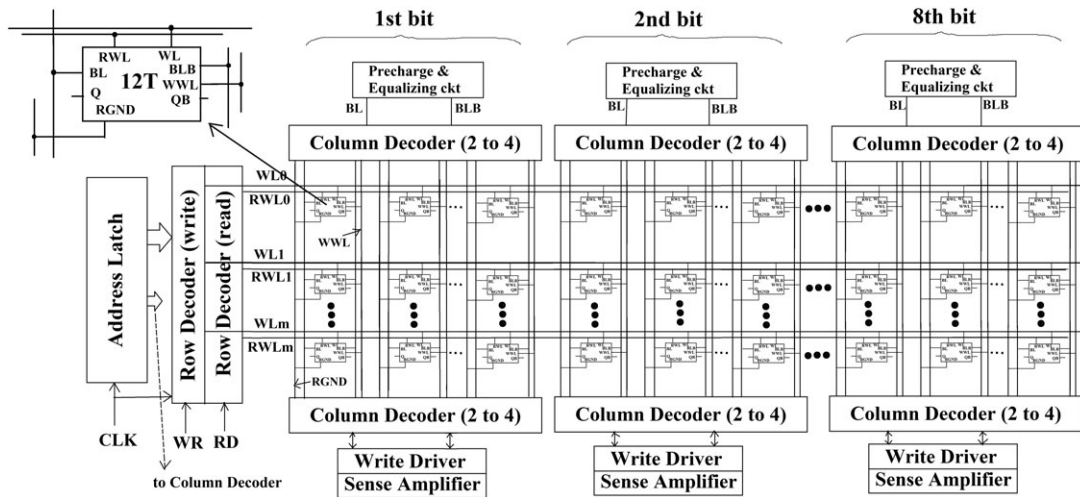
FIGURE 25 Complete bit-interleaved memory architecture of proposed cell. RGND, read ground; RWL, read word line; WL, word line; WWL, write word line
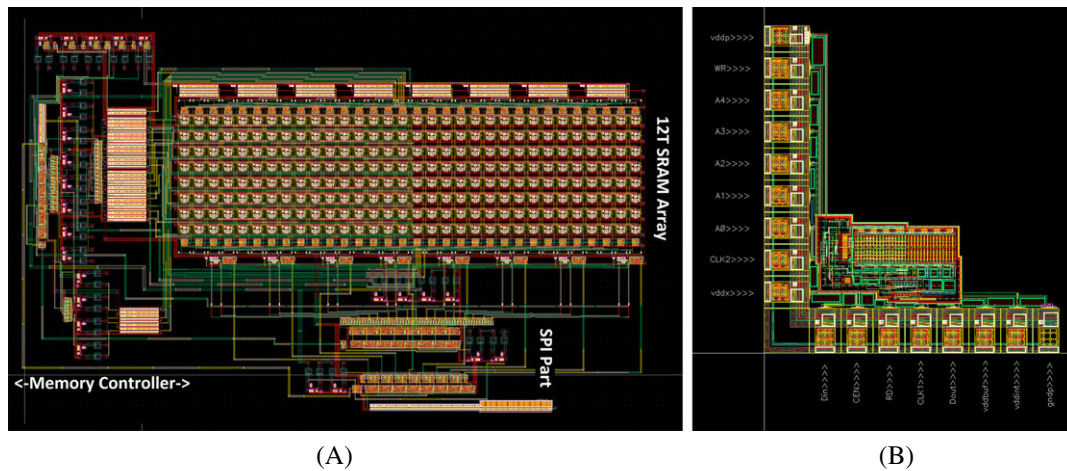
FIGURE 26 A, Custom layout design of 256-bits memory array with its independent memory controller and B, memory placed in the ring. SRAM, static random access memory [Colour figure can be viewed at wileyonlinelibrary.com]
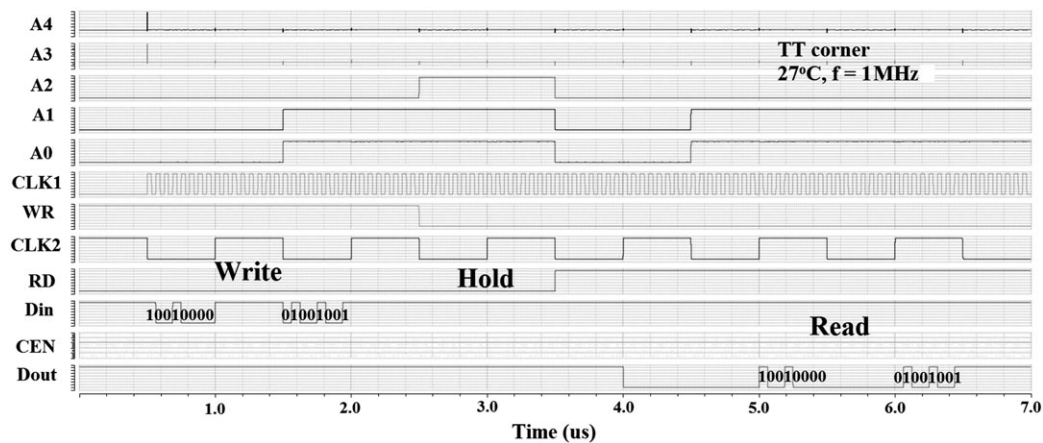
FIGURE 27 Transient simulation results of memory array

3 | MEMORY ARRAY DESIGN

An SRAM macro with 256-bits 12T cell has been designed as illustrated in Figure 25. The 256-bits SRAM macro consists of eight rows by 32 columns, where the word size is 8-bits wide. It employs the 4 bits interleaving architecture that can reduce the soft error by using single bit ECC in contrast to the nonbit-interleaving architecture.[27] The custom layout design of this memory array associated with its memory controller (including data and address latches, address row and column decoders, drivers, address transition detector, precharge and equalizing circuits, and sense amplifiers) is shown in Figure 26A. Figure 26B illustrates the memory layout with standard I/O pads available in the technology when placed inside the ring of an standard IC package. For the system level implementation of this array, due to the limited numbers of available I/O pads, a serial to parallel (SPI) module has been included. SPI is controlled by an additional clock signal, the frequency of which is 16 times higher than that of the memory to support the serial-parallel data conversion. Figure 27 provides the simulation results of the memory array, operating at 1.8-V supply voltage with 1-MHz internal frequency (CLK2) and 16-MHz SPI frequency (CLK1), showing the successful write, hold, and read operation.

4 | CONCLUSION

A DDFC-based bit-interleaving 12T SRAM cell has been proposed in this work. It improves the write ability of SRAM memory. The proposed cell eliminates the read disturb and write half-select issues and significantly improves the write ability by cutting its feedback path during the write operation. The cell shows its robustness against the PVT variations for

both subthreshold and superthreshold operating region, which has been verified by using the Monte Carlo simulations. The leakage power and read stability of proposed cell is also improved as compared with that of standard 6T cell. Moreover, an analytical model of WSNM for subthreshold 12T SRAM is proposed, and it fits within the maximum error of 11.4% at 180-nm technology node. Furthermore, a 256-bits SRAM macro has been designed for 32-kHz operating frequency and 1.8-V supply, considering all the factors required for its fabrication using a standard IC package. The simulated power consumption of the macro during its standby, read, and write mode at above specified V_{DD} and frequency is 24.44, 28.62, and 35.09 nW, respectively. The above-mentioned characteristics make the proposed SRAM cell useful to be deployed as a part of memory in BSNs, on-chip computations, and movable IoT applications.

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APPENDIX A: DERIVATION OF SUBTHRESHOLD ANALYTICAL MODEL OF WSNM

The subthreshold drain current for a MOS device is given as[4,24]:

$$I_{DS} = I_0 exp\left[\frac{V_{GS} - V_{TH}}{\eta V_T}\right]\left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right],$$

where $I_0 = \mu C_{ox}(W/L)(\eta - 1)V_T^2$.

For this analysis, we have not considered the drain-induced barrier lowering (DIBL) and body bias effect for the simplicity. Moreover, since $1 >> exp\left(\frac{-V_{DS}}{V_T}\right)$, the term $exp\left(\frac{-V_{DS}}{V_T}\right)$ can be ignored. Hence, the subthreshold drain current of NMOS M4 and M6 in the proposed cell can be written as

$$I_{DS_{M4}} = I_{0_{M4}} exp\left[\frac{V_{GS_{M4}} - V_{THn}}{\eta V_T}\right],$$

$$I_{SD_{M6}} = I_{0_{M6}} exp\left[\frac{V_{SG_{M6}} - V_{THp}}{\eta V_T}\right].$$

By equating these current ($I_{DS_{M4}}$ and $I_{SD_{M6}}$) to determine the write static noise margin (WSNM) value we get

$$\mu_n\left(\frac{W}{L}\right)_{M4} exp\left[\frac{V_{GS_{M4}} - V_{THn}}{\eta V_T}\right] =$$
$$\mu_p\left(\frac{W}{L}\right)_{M6} exp\left[\frac{V_{SG_{M6}} - V_{THp}}{\eta V_T}\right]. \tag{A1}$$

Figure 23 shows that BLB is connected to logic 1 for the write 0 operation, so M2 is on, and hence, the drain of M2 is 0. Therefore, $V_{SG_{M6}} = (V_{DD} + V_n - V_{QB})$, $V_{GS_{M4}} = (V_{QB} - V_n)$, and $V_{QB} = V_{DD}$. By putting these values in Equation A1 and then solving, we get

$$\mu_n\left(\frac{W}{L}\right)_{M4} exp\left[\frac{V_{DD} - V_n - V_{THn}}{\eta V_T}\right] =$$
$$\mu_p\left(\frac{W}{L}\right)_{M6} exp\left[\frac{V_n - V_{THp}}{\eta V_T}\right]. \tag{A2}$$

Now using this Equation A2, the value of V_n that is equal to the WSNM value can be written as

$$WSNM_{sub} = V_n = \frac{1}{2} \left[V_{DD} - V_{THn} + V_{THp} \right.$$

$$\left. + \eta V_T log_e \left[\frac{\mu_n}{\mu_p} \frac{(\frac{W}{L})_{M4}}{(\frac{W}{L})_{M6}} \right] \right] .$$

(A3)