A Zero-IF 60 GHz 65 nm CMOS Transceiver With Direct BPSK Modulation Demonstrating up to 6 Gb/s Data Rates Over a 2 m Wireless Link

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***Abstract*—This paper presents a directly modulated, 60 GHz zero-IF transceiver architecture suitable for single-carrier, low-power, multi-gigabit wireless links in nanoscale CMOS technologies. This mm-wave front end architecture requires no upconversion of the baseband signals in the transmitter and no analog-to-digital conversion in the receiver, thus minimizing system complexity and power consumption. All circuit blocks are realized using sub-1.0 V topologies, that feature only a single high-frequency transistor between the supply and ground, and which are scalable to future 45 nm, 32 nm, and 22 nm CMOS nodes. The transceiver is fabricated in a 65 nm CMOS process with a digital back-end. It includes a receiver with 14.7 dB gain and 5.6 dB noise figure, a 60 GHz LO distribution tree, a 69 GHz static frequency divider, and a direct BPSK modulator operating over the 55–65 GHz band at data rates exceeding 6 Gb/s. With both the transmitter and the receiver turned on, the chip consumes 374 mW from 1.2 V which reduces to 232 mW for a 1.0 V supply. It occupies 1.28×0.81 mm^2. The transceiver and its building blocks were characterized over temperature up to 85°C and for power supplies down to 1 V. A manufacturability study of 60 GHz radio circuits is presented with measurements of transistors, the low-noise amplifier, and the receiver on slow, typical, and fast process splits. The transceiver architecture and performance were validated in a 1–6 Gb/s 2-meter wireless transmit-receive link over the 55–64 GHz range.**

***Index Terms*—Millimeter-wave, nanoscale CMOS, 60 GHz, wireless transceiver, process variation.**

I. Introduction

THE mass market proliferation of mm-wave circuits is rapidly approaching as multiple industry groups are now working to complete standards for the adoption of the 9 GHz of bandwidth available worldwide between 57 GHz and 66 GHz. The standards are devised to address numerous high-bandwidth applications, ranging from the streaming of uncompressed high-definition video to the wireless replacement of next-generation wired interconnects, such as serial ATA and USB 3.0. With such a wide-range of target markets, the standards will have to be flexible enough to address the various, and sometimes conflicting, performance specifications that these applications will demand.

It has become clear that one of the benefits that 60 GHz radio will present when compared to competing technologies, such as IEEE 802.11 and ultra wideband radios, is that the system-level complexity, and the amount of digital signal processing required to achieve equivalent data rates will be greatly reduced. Single-carrier systems with simple modulation schemes can be utilized and still achieve data rates in the multi-Gb/s range without the need for ADCs and DACs, all of which will consume as much or higher power in a 60 GHz system than in GHz-range radios. However, to take advantage of the potential complexity and power saving opportunities, appropriate transceiver architectures and circuit topologies must be selected.

This paper presents a system which has been tailored to accommodate a simple modulation scheme that is appropriate for rapid file-transfer applications, thus simplifying its design and allowing for a robust implementation, even in CMOS. This architecture differs from other 60 GHz radio chip-sets reported in SiGe BiCMOS [1] or CMOS [2]–[9], because it integrates a fundamental frequency zero-IF transceiver, with a direct modulation transmitter. The system utilizes direct BPSK modulation at 60 GHz, precluding the need for a power amplifier, a fundamental frequency static divider, and operates without requiring image rejection or ADCs in the receiver. The transmitter input accepts baseband digital non-return-to-zero (NRZ) data at rates beyond 6 Gb/s, and the receiver outputs the same digital data stream in NRZ format in a true, single chip bits-in/bits-out radio transceiver.

The paper is organized as follows. Section II presents the system design considerations and the transceiver architecture, and Section III describes the design of the various circuit building blocks. The measured system characteristics are summarized in Section IV, and the results of a wireless link demonstration are shown in Section V.

II. Transceiver Design Considerations

A block diagram of the proposed transceiver is presented in Fig. 1. NRZ data, produced off-chip, is applied to a large-power BPSK modulator which directly modulates the 60 GHz LO signal and drives 50 Ω loads differentially at the transmitter

Manuscript received December 01, 2008; revised March 10, 2009. Current version published July 22, 2009. This work was supported by Fujitsu Limited. Test equipment was provided under grants from CFI, OIT, and NSERC, and by the ECTI facility at the University of Toronto.

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Digital Object Identifier 10.1109/JSSC.2009.2022918

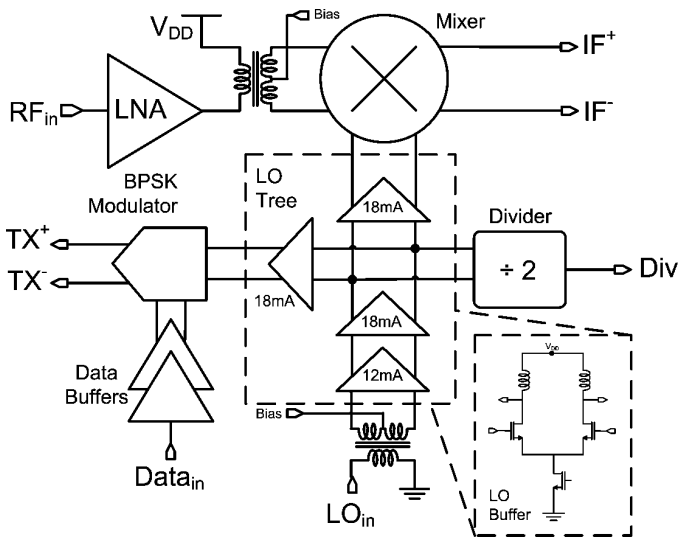

Fig. 1. 60 GHz direct modulation BPSK transceiver architecture.

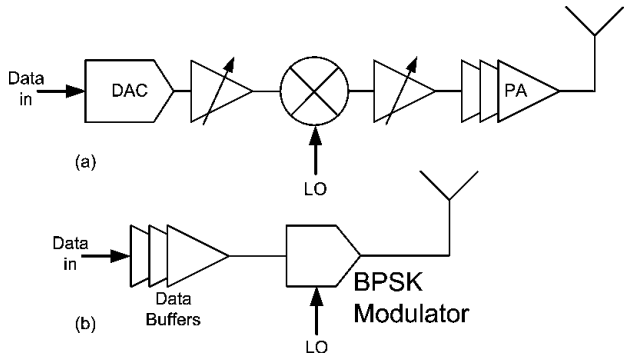

Fig. 2. (a) Conventional up-conversion transmitter. (b) Direct digital modulation transmitter.

output. The use of a single-phase modulation scheme in lieu of a multi-phase or quadrature technique reduces the system complexity and power-consumption required to distribute phase and amplitude matched quadrature signals throughout the chip.

To demonstrate the feasibility of integrating a fundamental frequency PLL, the first stage of the pre-scaler, a novel quasi-static frequency divider, is integrated. The receiver consists of a high-gain, low-noise amplifier that drives a double-balanced Gilbert cell down-convert mixer. Because quadrature modulation was not employed in this system, the receive mixer is single-phase. As well, the system transmitter generates a double sideband signal, negating any benefit of using an image reject mixer. No IF amplifier was included, so it is important to note that all the receive-path gain is at 60 GHz. The baseband NRZ data is provided from off-chip to the transmitter and is recovered at the IF output of the receiver, without any digital signal processing or analog-to-digital conversion.

It is worthwhile to examine the benefits and disadvantages of using a direct digital modulation architecture [10] as opposed to a more conventional direct-conversion transmitter consisting of an up-converter followed by a power amplifier. The latter architecture, shown in Fig. 2(a), has numerous analog blocks, each having to satisfy stringent linearity requirements. In particular, the design of a 60 GHz power amplifier, which simultaneously delivers the high output power, high gain, and high linearity that the various applications demand, represents one of the most serious challenges in mm-wave circuit design. The system-level linearity requirements are typically addressed by operating the power amplifier backed-off several dB from the saturated output power level and much below its peak operating efficiency point. To achieve the required output power levels with these restrictions in 90 nm CMOS, ever more complex designs have been considered, including distributed power-combining with a 1.8 V supply [11] and beam forming using as many as 36 individual transmitters on a single die [12].

A direct digital modulator/PA, Fig. 2(b), addresses this significant limitation by allowing the system to operate in saturated mode, with maximum efficiency, and with the output signal swing constrained only by the reliability limit of the transistors. It also simplifies the baseband circuitry, which can be implemented entirely digitally.

Unfortunately, this purely digital control also limits the type of baseband pulse-shaping that can be performed to digital filtering [13] or delta-sigma oversampling [14] techniques, both of which have been recently demonstrated in 2 GHz and 5 GHz RF-DAC transmitters. Although this paper discusses direct BPSK modulators only, ultimately any type of m-ary QAM, and even direct OFDM modulation, can be implemented using 2-6 binary-weighted unit cells, constructed from the BPSK modulator presented here, connected in parallel, in a manner similar to the digital-RF modulators in [13]–[15], with each BPSK modulator unit acting as a 1-bit 60 GHz DAC.

In discussing potential modulation schemes, it is worth departing briefly from the coherent receiver architectures, and consider that a low-power, low-cost option for the receiver is a direct detection architecture (as in OOK systems [16] or remote sensing). However, if the same receiver sensitivity is to be achieved, the RF filtering, and much higher gain and linearity needed from the LNA to offset the high noise figure of the detector, more than make up for the power savings obtained by removing the down-convert mixer. Incidentally, a PLL is still ultimately required in the transmitter.

A link budget analysis for the short-range, file-transfer application, employing a low-power transceiver with BPSK modulation, provides guidance on the tradeoff between antenna gain and the transmitter output power. Assuming a 2 m wireless link, 25 dBi transmit and receive horn antennas, 0 dBm transmitter output power, 6 dB receiver noise figure and 4 GHz bandwidth with an SNR of 12 dB, provides a link margin (with all the values in dB or dBm):

$$\begin{aligned}&\text{Link margin (dB)}\\&\quad = P_{\text{out}} + G_{\text{TX}} - \text{FSPL} + G_{\text{RX}} - S_i\\&\quad = 36\ \text{dB}\end{aligned} \tag{1}$$

where S_i is the receiver sensitivity and G_{TX} and G_{RX} are the gains of the transmit and receive antennas. The free-space path loss (FSPL) is given by the classical formula:

$$\text{FSPL} = \left(\frac{4\pi d}{\lambda}\right)^2 \tag{2}$$

which, for a 60 GHz signal with $\lambda = 5$ mm, results in a path loss of 74 dB over 2 m.

The relatively large 36 dB link margin can be used to increase the link distance or can be consumed by the various setup losses in an on-wafer wireless experiment, as in this paper. Alternatively, it can be traded off for low cost and lower gain (10–12 dB) PCB antennas, as demanded by a commercial, small form factor 60 GHz radio. This analysis shows that the presence of the high directivity antennas relaxes the transceiver specification sufficiently that only moderate transmit power and good noise figure are necessary. Both requirements are easily satisfied by 65 nm CMOS technology.

When the linearity of this transceiver was specified in March 2007, we considered the presence of an interferer $I = -30$ dBm at the receiver input. This corresponds to a transmitter with $+10$ dBm output power located 10 cm away from the receiver. Assuming a receiver sensitivity S_i of -60 dBm, an SNR of 12 dB, and using the well-known formula

$$\mathrm{IIP}_n = \frac{n \cdot I - (S_i - \mathrm{SNR})}{n - 1} \tag{3}$$

the required receiver IIP_3 becomes -9 dBm. The current release of the IEEE802.15.3c 60 GHz draft sets an even tougher specification on receiver linearity by mandating operation at the nominal BER for a -10 dBm input signal. The latter pushes the minimum required receiver $\mathrm{IP}_{1\mathrm{dB}}$ to at least -10 dBm and IIP_3 to 0 dBm. These linearity figures are difficult to achieve without consuming significant power in the LNA and in the receive mixer which drives 50 Ohm loads directly off chip.

III. Circuit Building Blocks

A principal design consideration for every block was to ensure that they were robust to power-supply and process variation. Stacked transistor topologies that place two or more high-speed transistors between V_{DD} and ground are particularly susceptible to power-supply and process variation, and have thus been avoided. As the measured characteristics in Fig. 3 illustrate, for large V_{DS} (0.8 V to 1.2 V), the performance of a transistor in terms of g_m, f_T and f_{MAX}, is relatively constant over V_{DS} variations. However, as the transistor V_{DS} drops to 0.5 V or below, rapid performance degradation can be seen. Thus, biasing transistors far from this sensitive area will ensure a more robust operation.

Cascode topologies, which have at least two high-speed transistors stacked between V_{DD} and ground are vulnerable to power-supply and process variation due to the low V_{DS} of each transistor and the impact of the V_T variation of the common-gate MOSFET. Even when biased with the constant current density biasing technique [17], which reduces circuit sensitivity to V_T and bias current variations, threshold voltage variations in the common-gate transistor will still result in V_{DS} variation for the common-source MOSFET.

Looking beyond the immediate issue of susceptibility to power-supply and process variation, similar design considerations will become more critical in future process nodes. Scaled 32 nm and 22 nm nodes will require power supplies to be reduced from the levels in 65 nm CMOS, as dictated by constant field scaling rules and device reliability requirements. Using

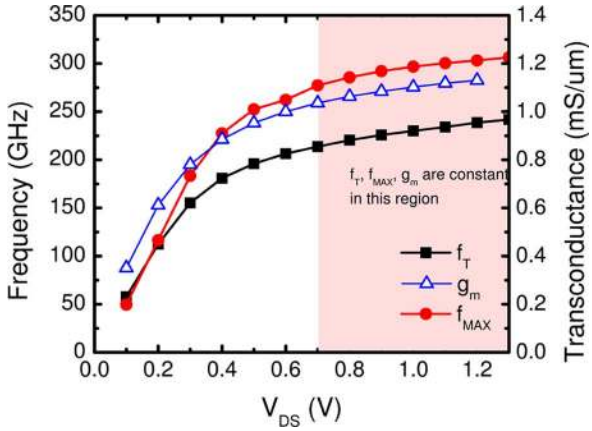

Fig. 3. Measured NFET transistor performance for constant $\mathrm{V}_{GS} = 0.65$ V.

topologies that place only one high-speed transistor between V_{DD} and ground is the only way to maximize the power gain as well as minimize the noise figure of the transistor in future CMOS nodes.

All circuits employed in this system forego stacked transistor topologies in favour of either transformer or capacitively coupled cascode topologies that have no more than a single high-speed transistor stacked above a current source. These topologies ensure operation from 1.2 or 1.0 V supplies, and work equally well in LP, GP, or HP flavors of a 65 nm CMOS process. LP, GP, and HP correspond to low-power, general-purpose, and high-performance process variants of a CMOS node, as described in [18]. These options are typically distinguished from each other based on the effective gate length and oxide thickness, with HP having the thinnest oxide, and the shortest gate length.

The penalty for using AC-coupled cascodes is a doubling of current consumption compared to the traditional telescopic cascode [19], which is only partially compensated by the potential reduction in power supply voltage.

A. Low-Noise Amplifier

The LNA schematic is shown in Fig. 4. It consists of three cascaded CS-CG stages, with the minimum gate length transistors and with increasing gate width from stage to stage. The most important design goals were a power gain of at least 20 dB, a noise figure below 6 dB, and an $\mathrm{IP}_{1\ \mathrm{dB}}$ of -15 dBm which sets the $\mathrm{OP}_{1\mathrm{dB}}$ to at least $+4$ dBm. The gate width and bias current of the MOSFET in the last stage is determined by the output compression point, while the gate width and bias current of the first stage MOSFET is calculated to minimize noise figure and to satisfy the simultaneous noise and input impedance match condition [19].

The design of the LNA proceeds according to the methodology described in [19] for telescopic cascodes, with modifications to accommodate the AC-coupled cascode topology. The load inductance of the CS stage and the source inductance of the CG stage are determined from the condition that, in parallel, they resonate with the total capacitance at the common node of this cascode at the center frequency of the amplifier. Device capacitances at the drain node of the CS transistor and at the source

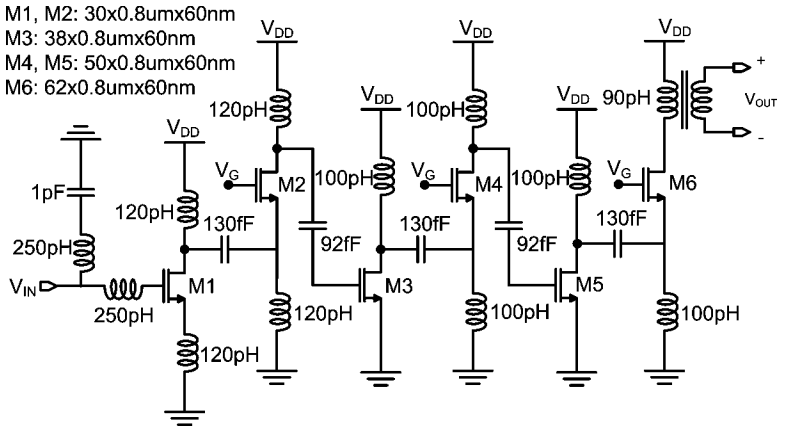

Fig. 4. 1.2 V, three-stage cascaded CS-CG, 60 GHz low-noise amplifier schematic.

of the CG transistor, the parasitic capacitance of the inductor, as well as the bottom-plate capacitance of the AC-coupling MiM capacitor, all contribute to the total node capacitance. For initial hand-derived parameters, a center frequency of 66 GHz, 10% above the desired operating frequency was used in anticipation of the various layout parasitics that are not accounted for. The calculated inductance is equally split into two parallel inductances that are placed at the drain and source nodes respectively. For example, the drain inductance of the first stage, and the source inductance of the second stage are calculated to resonate with the parasitic capacitance of transistors M1 and M2, given by $C_{\rm TOT} = C_{\rm DB1} + C_{GD1} + C_{\rm SB2} + C_{\rm GS2}$. Using the measured transistor capacitances: $C'_{\rm DB} = 0.6$ fF/μm, $C'_{\rm GD} = 0.35$ fF/μm, $C'_{\rm GS} = 0.7$ fF/μm, and $C'_{\rm SB} = 0.6$ fF/μ m, we obtain

$$\frac{L_1}{2} = \frac{L_2}{2} = \frac{1}{4\pi^2 f^2 C_{\rm TOT}} = \frac{1}{4\pi^2 f^2 \cdot 108\ \text{fF}} = 65\ \text{pH}. \quad (4)$$

This corresponds to an effective inductor value of 130 pH, and allowing for an approximate 10% shift in center frequency due to un-modeled parasitic capacitances, 120 pH inductors were implemented. For later stages, in which the MOSFET gate width is larger, the inductor sizing was not scaled down at an equal rate, creating a slight staggering in the center frequency of each stage and thus broadening the frequency response of the entire amplifier.

The input stage is noise and impedance matched to 50 Ω, as in a telescopic cascode stage [19], and is biased at the minimum noise figure current density, which corresponds to 0.3 mA/μm for a transistor V_{DS} of 1.2 V. All transistor layouts feature minimum gate length nMOSFETs with 0.8 μm finger width and double-sided gate contacts. The last stage of the LNA is loaded with a transformer which acts as single-ended to differential converter between the LNA and the double-balanced mixer. The LNA, which can also be operated as a low-noise, moderate power amplifier, consumes 80 mA (60 mA) from a 1.2 V (1.0 V) power supply. It should be noted that the power consumption of the LNA could be reduced by scaling down the size and bias currents in the last four stages without affecting the overall noise figure and gain. However, as discussed in Section II, the input compression point would be negatively affected.

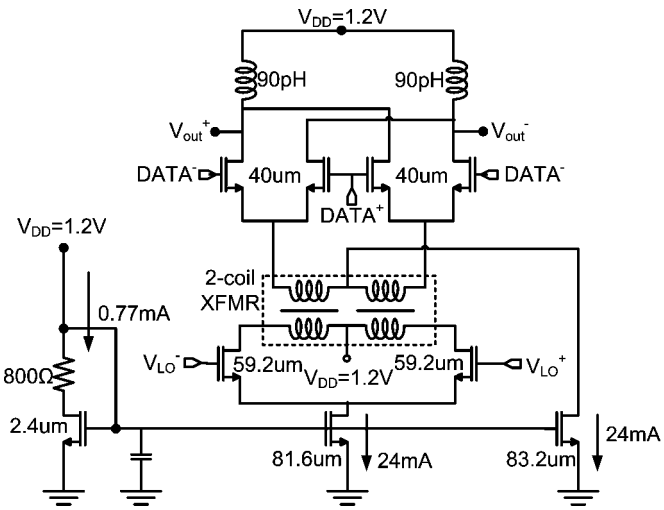

Fig. 5. BPSK modulator schematic.

Finally, it is worth noting the reasons for implementing an AC-coupled cascode topology rather than a simple cascade of common-source (CS) stages. The CS topology with inductive load is known for its potential instability and propensity to oscillate. Furthermore, its poor isolation at mm-waves makes it difficult to design a multistage amplifier, or an entire receiver, when models are inaccurate or process variation is a concern, as in this case. The AC-coupled cascode avoids all of these problems due to its excellent isolation (similar to that of a telescopic cascode) while operating, like the CS stage, with a low-voltage supply.

B. BPSK Modulator

Fig. 5 illustrates the schematic of the BPSK modulator. All transistors have minimum gate length. This topology allows for the direct modulation of the 60 GHz carrier by a large-swing data signal with no concern for signal linearity at the LO port. Historically, the first direct BPSK modulators featured balanced switches realized with PIN or Schottky diodes and diode bridges, but implementations in GaAs MESFET [20], CMOS or SiGe BiCMOS technologies permit the use of the active Gilbert cell. The data signal is applied to the gate of the mixing quad transistors, while the carrier (LO) signal is injected as

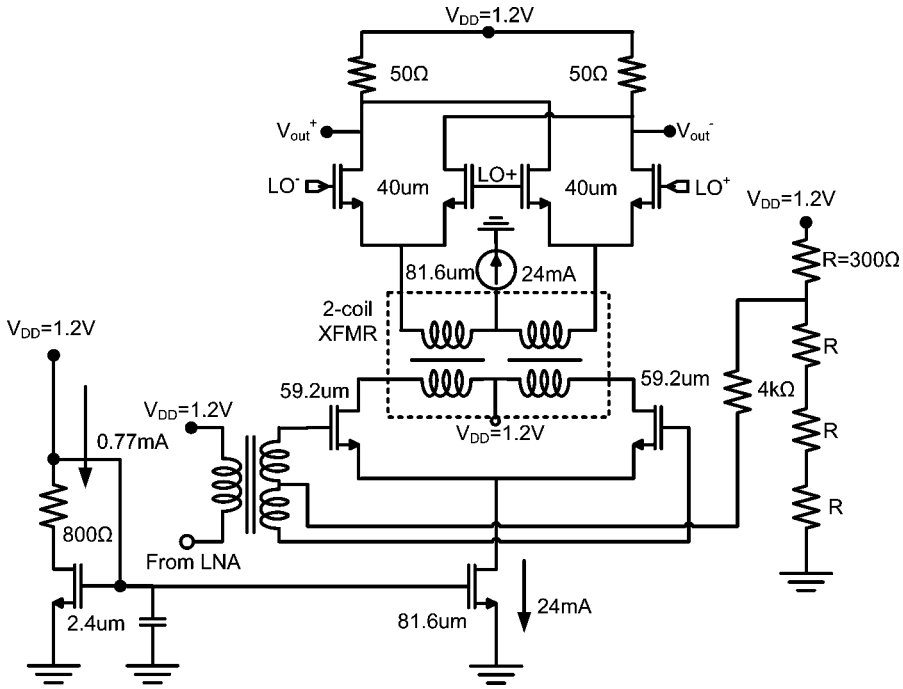

Fig. 6. Mixer schematic.

current, differentially, to the sources of the Gilbert-cell quad. The mixing-quad transistors act like switches, directing the LO current either to the positive or to the negative output node thus introducing the 0–180° phase modulation. Direct mm-wave BPSK modulators based on this topology have been reported at 65 GHz [21] and 77 GHz [22] in SiGe HBT technology, aand similar topologies have been applied recently in direct-digital RF modulators in the 1–5 GHz range [13], [14].

Transformer coupling has been employed to AC-couple the LO signal from the transconductor pair into the Gilbert cell, thus maximizing the V_{DS} (approximately 0.9 V) of the mixing quad transistors and the output power. Since the output transistors act as large power switches, the modulator can be viewed as a switching PA. As long as the LO signal applied to the modulator maintains 50% duty cycle and does not exceed the input compression point of the switch, the EVM of the output spectrum is insensitive to the LO amplitude, temperature, and LO frequency.

The differential modulator output features 90 pH inductors which tune out the transistor and output pad capacitance. The gate width of the MOSFETs in the BPSK modulator is chosen such that the real part of the output impedance at resonance is approximately 60 Ω while $R_{\rm opt}$ is 75 Ω. This simple, relatively wideband, matching is provided by the DC output resistance of the MOSFETs [19].

As in CML gates, the current density through the modulating switches changes from 0 to 0.3 mA/μm [17]. If we consider that all transistors are biased at 6 mA each, or 0.15 mA/μm, we can estimate the output power of this modulator. Assuming a 0.3 V drop across the tail current source, and a minimum of 0.15 V across a fully on transistor, we can expect a maximum theoretical amplitude swing of 0.75 V, or 1.5 $V_{\rm pp}$. This corresponds to a maximum differential output power of

$$P_{\rm out} = 2 \cdot \frac{V_{\rm pp} \cdot I_{\rm BIAS}}{4} = 4.5\,{\rm mW} = +6.5\,{\rm dBm}. \quad (5)$$

If we account for a 2 dB loss due to the output matching network, we arrive at a figure of +4.5 dBm. The latter is confirmed by simulations after layout parasitics extraction which show a voltage swing of 0.9 $V_{\rm pp}$ per side corresponding to a differential output power of 2.7 mW or 4.3 dBm.

C. Mixer

The mixer schematic, shown in Fig. 6, is essentially identical to that of the BPSK modulator. Due to lack of time at the design phase, and because it has to drive 50 Ω loads off chip with a large swing of 0.6 $V_{\rm pp}$ per side, the mixer was simply a copy of the BPSK modulator. All components, sizes, and bias currents are identical. The transistors in the mixing quad are biased at 0.15 mA/μm for maximum switching speed while those in the differential transconductor are biased at 0.2 mA/μm. The single-ended signal from the LNA is converted to differential mode by the load transformer in the output stage of the LNA (shown in this figure), and drives the transconductance pair of the mixer. Transformer coupling is again used to convert the RF signal into an AC current that is injected into the sources of the mixing-quad using a 28 μm, two-coil, vertically-stacked transformer. The mixing-quad transistors are driven directly by an 18 mA LO-tree buffer. This topology has been shown to be scalable up to at least 140 GHz in CMOS [23].

No IF amplifiers were implemented in this system.

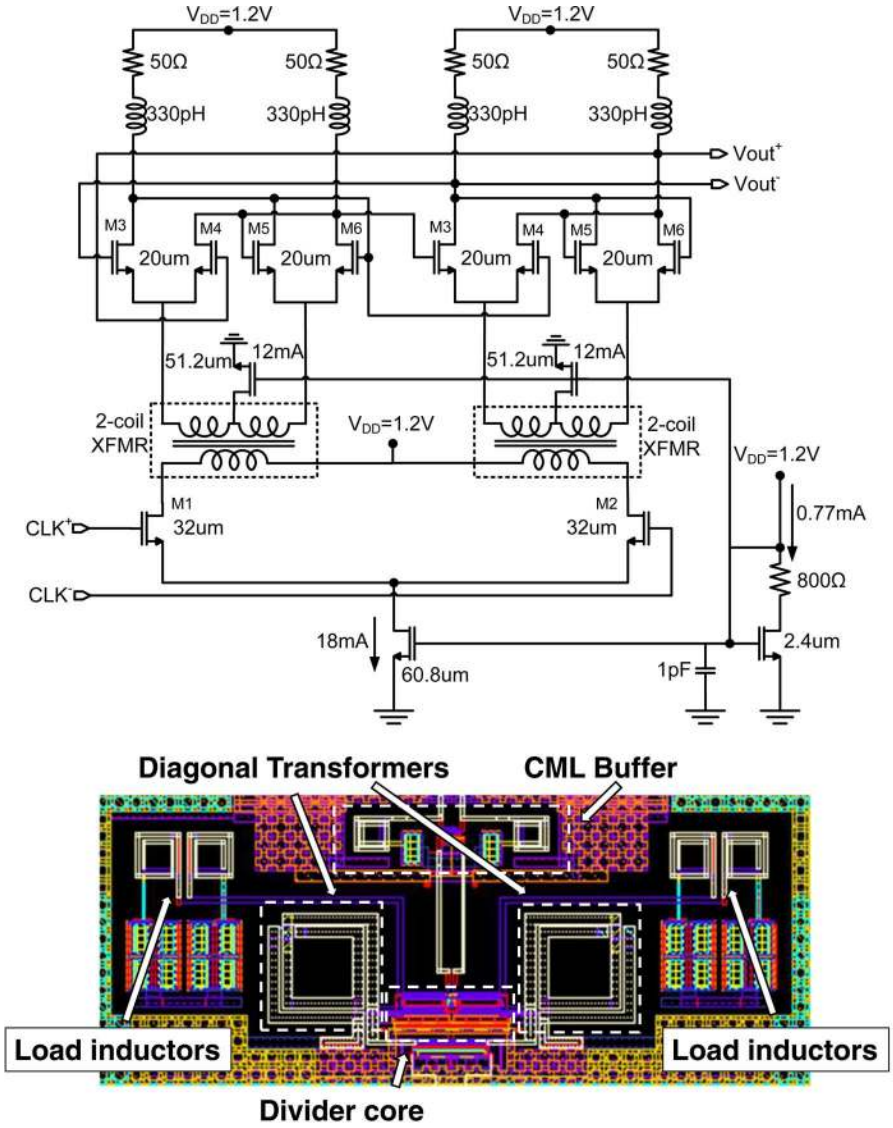

Fig. 7. Static frequency divider schematic (top), and layout details of the divider core (bottom).

D. Quasi-Static Frequency Divider

The fundamental frequency divider represents one of the key blocks required for the successful integration of a fundamental frequency synthesizer. CMOS mm-wave VCOs in the V- and W-band, simultaneously generating >0 dBm output power and exhibiting phase noise values lower than -90 dBc/Hz at 1 MHz offset, have already been demonstrated [24], [25]. While their tuning range is lower than 10%, coverage of the entire 57–66 GHz band can be provided by a bank of frequency-spaced VCOs [26]. A static-like frequency divider guarantees a wide operating frequency range, which is essential in a 60 GHz PLL. A narrowband injection-locked divider, for example, significantly complicates the PLL design where tracking of the VCO and divider over the full frequency band must be ensured over temperature and process variation [26].

Static frequency dividers based on a CML latch topology with stacked high-V_T and low-V_T MOSFETs have been demonstrated at frequencies exceeding 90 GHz [27], [28]. However, their operation range is greatly diminished at 100°C [25] and vanishes at 1.0 V supply. In this paper we propose an alternate static-divider topology that is more suitable for low voltage operation. Its schematic is shown in Fig. 7 (top). It features a single differential pair at the clock input which drives the two latches through two 28 μm $\times$ 28 μm transformers. This effectively eliminates one of the two clock differential pairs resulting in a reduced area and power consumption, while also permitting operation without multiple transistors and V_Ts between V_{DD} and ground. The size and bias current of the eight transistors in the latches, the load resistors, and the load inductor values are identical to those of the 90 GHz CML divider in [27]. The transformers were realized with two vertically stacked coils with inputs and outputs aligned along a diagonal line of symmetry.

Fig. 7 (bottom) illustrates the layout detail including the first of three CML buffers at the divider output.

In order to minimize the layout parasitic capacitances of the latch, which are known to be an important factor in determining the self-oscillation frequency of mm-wave dividers, [27], an

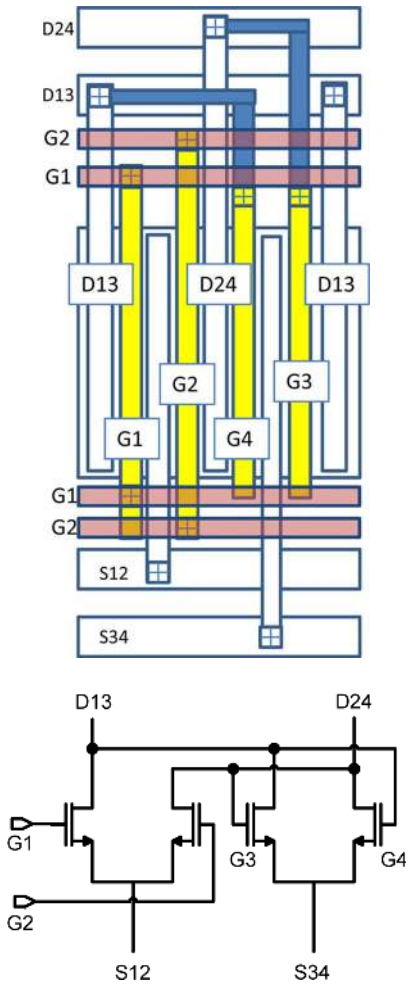

Fig. 8. Illustration of the unit-cell layout of the latch in the divider. Each connection of the latch unit-cell is identified, and the merged, inter-digitated arrangement can be seen.

innovative and compact latch layout was utilized here. Fig. 8 shows a diagram of the layout for the unit-cell that is used to build the entire latch. Each of the unit-cells contains one finger for each of the latch transistors, and all of the required connections. A cascade of these unit-cells is employed to build the entire divider latch. By merging the 4 MOSFETs together and inter-digitating the fingers, the loop-delay time due to long inter-connect, as well as the output differential-mode capacitance are reduced and the maximum frequency of operation is increased. Similarly, by increasing the unit finger width up to 1.6 μm from 0.8 μm, it is possible to cut the number of fingers in half while maintaining the same total gate width. This has the net result of further reducing the parasitic capacitances of the device and thus increasing f_{SOF}.

E. Tuned Clock Tree

The design of the LO tree represents one of the main challenges in achieving large-scale system integration at 60 GHz. While this transceiver is intended to operate with a fundamental-frequency PLL synthesizer, we note that a 60 GHz LO distribution network is needed even if the VCO signal is provided by a multiplier chain or by a second harmonic VCO [29]. In this transceiver, a tuned LO distribution tree with 25% bandwidth was designed. It consists of a cascade of differential buffers with inductive loads and a fanout of two or three, as shown in the inset of Fig. 1. Since the maximum available power gain of a 60 nm nMOSFET is 10–11 dB at 60 GHz, and since the LO buffers are meant to operate with large input and output voltage swings, the voltage gain is about 1 while the current gain cannot exceed 3. Hence, the maximum fanout in the LO tree is limited to 3. Both 12 mA and 18 mA buffers are employed. These relatively large currents are needed to drive the 24 mA BPSK modulator in the transmitter, the 24 mA receiver mixing quad, and the 18 mA divider stage. The MOSFETs in the buffer are biased at 0.3 mA/μm for maximum linearity [19]. An on-chip transformer balun is employed to convert the single-ended external LO signal to differential mode at the input to the first buffer.

A VCO or PLL was not implemented in this transceiver. However, whether the choice is made to design a larger, high-power fundamental frequency VCO [25], a multiplier chain which is able to generate much of the required LO power [1], or a small, low-power oscillator/multiplier that requires significant signal gain in the LO tree in order to provide sufficient power to the critical blocks, the power-consumption burden will still exist, and has simply been shifted between different blocks.

F. Tuned mm-Wave Switch

While not included in the transceiver, a stand-alone 50–70 GHz series-shunt switch, shown in Fig. 9(a), was designed and manufactured on the same dies and characterized separately. Passive switches exhibit excellent linearity without consuming power [30]. They can provide important functions such as on-chip calibration [31] and transmit/receive antenna sharing [32], both critical features facilitating the successful commercialization of mm-wave systems, permitting low-cost at-speed testing and reducing the number of expensive off-chip 60 GHz components.

For a series-shunt switch topology, the trade-offs between the achievable insertion loss and isolation are well known [33], and come as a result of the presence of the various parasitic capacitances, as illustrated in Fig. 9(b). Wider series MOSFETs exhibit smaller ON-resistance and will initially reduce the insertion loss, but the parasitic capacitances will eventually begin to increase the insertion loss while also degrading the isolation. Similarly, the shunt MOSFET ON-resistance increases the effective isolation, but the associated shunt parasitic capacitance will degrade the insertion loss. To minimize the ON-resistance (about 370 $\Omega \cdot \mu$m in 65 nm CMOS [30]) both transistors have minimum gate length. A technique used to mitigate the performance degradation caused by parasitic capacitances, is to use inductors to resonate with the parasitics [34]. Placing a series inductor, $\mathrm{L_{series}}$, across the series MOSFET, and a shunt inductor, $\mathrm{L_{shunt}}$, across the shunt MOSFET, will reduce the insertion loss, and increase the isolation respectively.

These structures can be modeled using the ON and OFF state models shown in Fig. 9(b). The measured MOSFET capacitances at $V_{\mathrm{DS}} = 0$ V are employed to determine $\mathrm{C_{shunt}}$ and

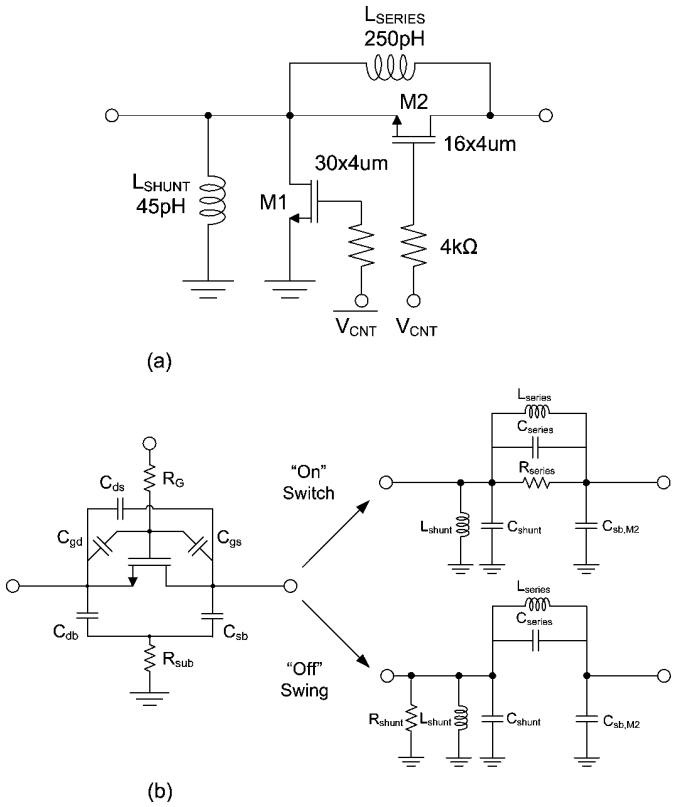

Fig. 9. Schematic of the 60 GHz tuned series-shunt SPST switch (top) and the transistor equivalent models used for hand-design and simulation (bottom).

C_{series}. From the schematic, the parasitic capacitances are given by

$$C_{\text{series}} = \frac{C_{\text{GD,M2}} C_{\text{GS,M2}}}{C_{\text{GD,M2}} + C_{\text{GS,M2}}} + C_{\text{DS,M2}} \tag{6}$$

$$C_{\text{shunt}} = \frac{C_{\text{GD,M1}} C_{\text{GS,M1}}}{C_{\text{GD,M1}} + C_{\text{GS,M1}}} + C_{\text{DS,M1}} + C_{\text{DB,M1}} + C_{\text{DB,M2}} \tag{7}$$

where each parasitic capacitance scales with the device width, W, and $C'_{\text{gd}} = C'_{\text{gs}} = 0.5$ fF/μm, $C'_{\text{ds}} = 0.3$ fF/μm, and $C'_{\text{db}} = C'_{\text{sb}} = 0.6$ fF/μm. The inductors are sized to resonate with the corresponding parasitic capacitances at 60 GHz according to $\omega_{\text{res}} = 1/\sqrt{LC}$. By independently sweeping the device widths of the shunt and series transistors, the trade-off between insertion loss and isolation can be simulated, and device sizing can be selected.

This design aimed for the largest possible isolation while still maintaining less than 3 dB insertion loss. This lead to $W_{\text{series}} = 64$ μm and $W_{\text{shunt}} = 120$ μm, which correspond to $C_{\text{series}} = 35$ fF, $C_{\text{shunt}} = 168$ fF. After layout parasitic extraction and inductor modeling, additional adjustment of the inductors was required to arrive at the final values of $L_{\text{shunt}} = 45$ pH, and $L_{\text{series}} = 250$ pH, as illustrated in Fig. 9(a).

The switch is controlled by complimentary signals that bias the gates through large resistors that prevent oxide breakdown and ensure that the gate acts as an AC-floating node, thus minimizing signal loss through parasitic gate coupling.

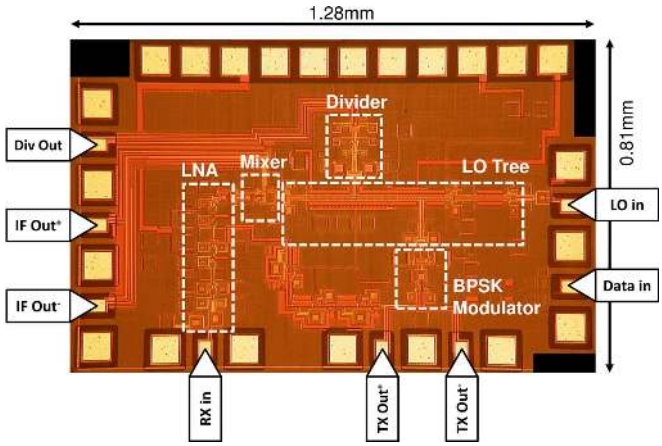

Fig. 10. Die photograph of the transceiver. Total die area is 1.28×0.81 mm^2.

IV. Experimental

A. Chip Implementation and Layout

The transceiver was fabricated in a 65 nm CMOS process with a 7-metal digital back-end and MIM capacitors. Peak f_{MAX} and f_T values of 300 GHz and 220 GHz were measured on 80×60 nm $\times$ 1 μm nMOSFETs with double-sided gate contacts, at current densities of approximately 0.3 and 0.4 mA/μm respectively with a V_{DS} of 1.0 V. The f_T and f_{MAX} values were extracted from the measured H_{21} and the unilateral power gain in the 1 GHz to 67 GHz range using an Agilent 67 GHz PNA. The S-parameters and maximum available gain were also measured in the 55–95 GHz range with a Wiltron 360 B VNA. The input and output parasitics (pad and interconnect) were de-embedded using the T-line procedure described in [35].

A microphotograph of the transceiver is shown in Fig. 10. It occupies 1.28×0.81 mm^2. The LO and RF signals are distributed along μ-strip lines formed in metal 7 over a shunted metal 1 and metal 2 slotted ground plane. A grounded side-wall consisting of p-substrate taps and all metals shunted together forms a Faraday cage-like structure around each transmission line [36] and between circuit blocks, improving isolation.

B. Test Structure and Transceiver Measurements

S-parameter measurements of the LNA breakout, shown in Fig. 11(a) along with simulated results as dashed lines, display a peak gain of 19.2 dB at 60 GHz and a 3 dB bandwidth extending from 54 GHz to 66 GHz. The return loss is better than 10 dB up to 66 GHz. The saturated output power of the LNA, measured in a large-signal measurement setup, is greater than $+7.5$ dBm with a 1.2 V supply and $+5$ dBm with a 1.0 V supply. Fig. 11(b) shows the measured input- and output-referred 1 dB compression points of -14 and $+2.5$ dBm, respectively. The simulations and measurements of the linearity agree within the measurement uncertainty of 1 dB.

The measured S-parameters of the stand-alone mm-wave switch are presented in Fig. 12. The switch achieves a nominal insertion loss of 3.9 dB and an isolation of 28 dB at 60 GHz. The simulated characteristics follow measurements quite well,

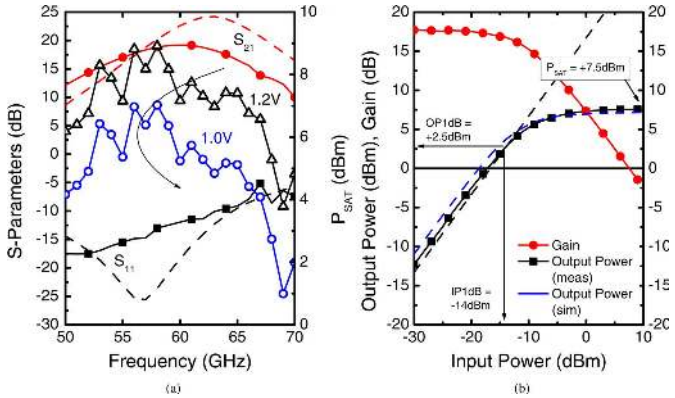

Fig. 11. Measured results of the LNA breakout. (a) S-parameter measurements (with simulated results in dashed lines) and saturated output power results over frequency (b) LNA linearity at 59 GHz with the simulated output power shown as a dashed line.

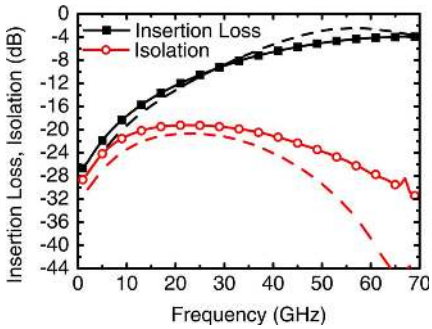

Fig. 12. Measured insertion loss and isolation of the 60 GHz series-shunt SPST switch with simulation results shown as dashed lines.

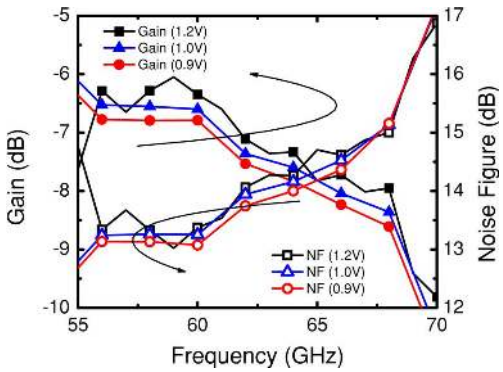

Fig. 13. Measured gain and noise figure of the stand-alone 60 GHz mixer for 1.2, 1.0, and 0.9 V power supplies.

with the largest error observed for isolation. The latter could be due to an optimistic Q value for the modeled inductors.

A breakout of the mixer was tested using an Agilent Noise Figure Analyzer. The gain and 50 Ω noise figure measurements are compiled in Fig. 13. It should be noted that the mixer employs a double balanced topology, requiring differential LO and RF signals. These differential signals were produced on-chip using integrated transformers whose losses degrade both the noise figure and the down-conversion gain. These losses were not de-embedded from the reported measurements.

The static frequency divider sensitivity was measured in the transceiver and includes the effect of the LO distribution net-

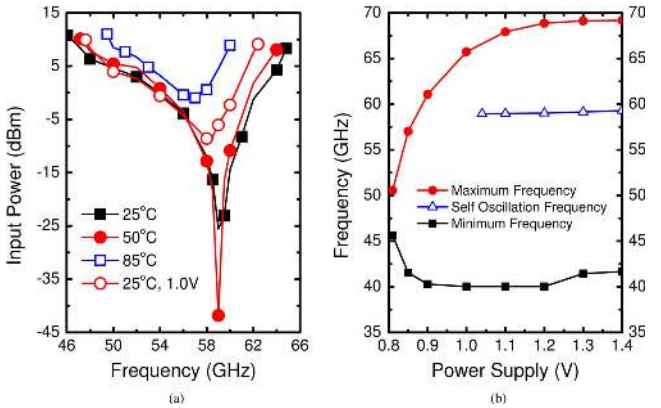

Fig. 14. Measured (a) divider and LO-tree sensitivity, and (b) divider (breakout) frequency range over power supply.

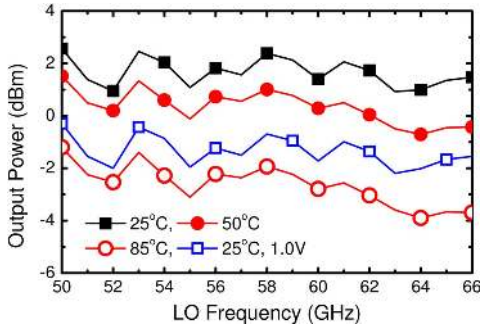

Fig. 15. Measured transmitter output power as a function of LO frequency and over temperature.

work. The self-oscillation frequency is 59.2 GHz at room-temperature with a 1.2 V supply. As illustrated in Fig. 14(a), the divider operates over a frequency range of 46–65 GHz at 1.2 V, and 47–62 GHz at 1.0 V. To remove the impact of the LO tree on the measured performance of the divider, the latter was tested on a breakout version of the divider. Fig. 14(b) shows the maximum, minimum, and self-oscillation frequency of the divider breakout measured as a function of the power supply voltage. When the power supply is reduced to 0.9 V, the divider operates from 40 GHz to 61 GHz. Under nominal conditions (25°C, 1.2 V) the divider operates from 40 GHz to 69 GHz.

The measured total integrated power at the output of the transmitter is plotted in Fig. 15 versus frequency. Measurements are shown over temperature up to 85°C, with a maximum output power above +2.4 dBm at 25°C and 58 GHz.

C. Process Variation

The manufacturability of the 60 GHz transceiver was studied by measuring transistors, the low-noise amplifier, and the stand-alone receiver on 16 dies that were deliberately fabricated on wafer splits representative of the slow, typical, and fast process corners. Results in Fig. 16(a) indicate a 10% drop in transistor peak f_T from the fast to typical corner splits.

It should be noted that, although there is significant V_T variation between corners, the measured peak f_T current density remains essentially constant. The measured LNA gain is plotted in Fig. 16(b) over process corners, along with the simulated performance over the same corners. The LNA gain degradation

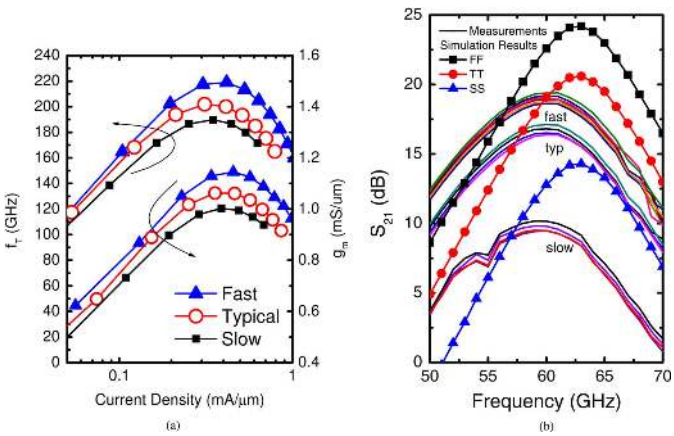

Fig. 16. Measured (a) NFET $80 \times 1\ \mu\text{m} \times 60$ nm f_T and g_m, and (b) LNA S_{21} over fast, typical, and slow process corners. Measured LNA results are shown as lines, with simulated results for the same corners, shown as lines with symbols.

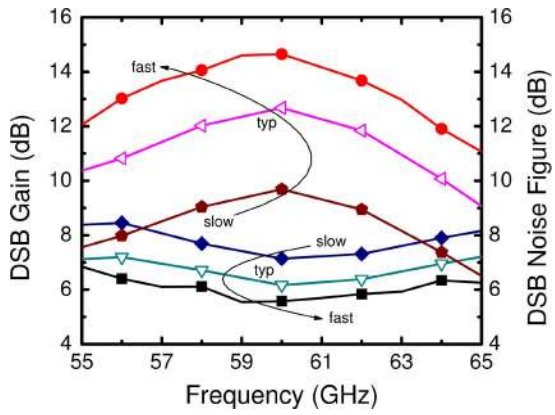

Fig. 17. Measured receiver (breakout) gain and noise figure over fast, typical, and slow process corners.

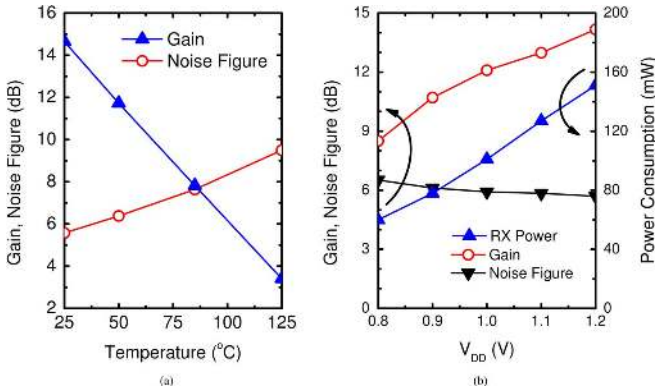

Fig. 18. Measured receiver gain and noise figure over (a) operating temperature, and (b) power supply.

observed from the fast to typical process lots can be seen to track the variation in f_T and g_m, cumulated over 6 gain stages. However, the drop in the slow corner (9–10 dB) exceeds the equivalent decrease observed in the transistor f_T measurement. This increased degradation can be attributed to an error in the biasing of the common-gate transistors in the LNA, which were biased at a fixed V_{GS}, rather than at constant current-density. As the transistor parameters vary over the process corners, the threshold voltage is seen to increase in the slower corners. This ultimately results in a severe under-biasing of the common-gate transistor in the slow process corner, leading to the observed performance degradation.

From the LNA gain measurements, we observe that there is no impact of process variation on the center frequency of the LNA. The latter is determined by the extrinsic device parasitics (metallization capacitance, resistance and inductance) and the discrete tuning elements (inductors, capacitors, etc) which do not vary in these corners lots. This explains why the hand design equations, along with well modeled inductors, are almost as accurate as the transistor models (within 5% of the measured center frequency). The conclusion is that the main impact of the process variation in these tuned circuits is in the peak transconductance value, and hence in the power gain. Although the simulated LNA gain tracks the measurements across process corners, it is optimistic and shifted to higher frequencies by 5–6%. The frequency shift is consistent with the expectations made during the initial design phase. A 5–10% error in the value of the passive components can account for the observed shift. In fact, the main culprit for the reduced gain observed in measurements can only be explained by series resistive and inductive parasitics at the top level layout or by underestimated parasitic capacitance in the extractor or in the inductor models. The latter two are very difficult to measure at 60 GHz. We note that simulation after top level dummy fill and resistive parasitics extraction was not performed due to the large number of circuit elements. A 0.5–0.8 dB gain reduction per LNA stage due to top level layout parasitics is sufficient to account for the discrepancy between the measured and the simulated peak gain of the LNA.

It should be noted that, compared to the standalone receiver breakout measurements, the receiver gain measured in the transceiver was degraded by 3 dB because of insufficient LO power at the mixer LO port. The LO-tree fanout in the transceiver is 3, whereas it is only 1 in the receiver breakout. Performance results for both versions are summarized in Table I at the end of this paper, but the following results are for the receiver only. The receiver gain and noise figure are plotted in Fig. 17 for the fast, typical and slow corners. Measurements were carried out using an Agilent Noise Figure Analyzer with a Noisecom V-Band noise source. A peak receiver conversion gain of 14.7 dB and a 50 Ω noise figure of 5.6 dB are noted, both occurring at 60 GHz. The DSB noise figure remains below 6 dB over an RF bandwidth of 58 to 63 GHz. The receiver measurements indicate that the impact of process variation on the receiver can be, for the majority, attributed to LNA performance decrease due to transistor g_m and f_T degradation. As in the LNA, the peak gain frequency of the receiver and the minimum noise figure frequency are not affected by process variation.

Finally, it should be noted that, despite the significant drop in LNA performance from the fast to the slow process corner (9–10 dB), the receiver noise figure increases by less than 2 dB (from 5.6 to 7.1 dB). This is a direct consequence of the nominally large gain of the LNA. Although additional power consumption was required in order to design an LNA with high nominal gain, it appears to be the only feasible approach to address the large expected process variation of nanoscale mm-wave CMOS circuits.

TABLE I
PERFORMANCE COMPARISON FOR 60 GHz TRANSCEIVER/RECEIVER CHIP-SETS. BRACKETS SHOW MEASURED RESULTS FROM 1.0 V

Gain (dB)	NF (dB)	IP_{1dB} (dBm)	TX Power (dBm)	Modulation, Data Rate	V_{DD} (V)	P_{DC} (mW)	Area (mm^2)	Process and Integration
72	5.5-6.5	-36	17.0	MSK 2.0Gb/s	2.7, 4.0	996	12.2	0.13 SiGe, TX, RX, 20GHz PLL, IQ mod/demod [1]
16-21	5.5-7	-21	n/a	n/a	1.2-1.5	60	0.3	90nm, LNA, mixer, IF buffer, off-chip LO [2]
51	9	-30	8.4	16-QAM 15Gb/s	1.8	362	6.5	90nm, TX, RX, PLL, IQ mod/demod [5]
55.5	6.2	-26	n/a	n/a	1.0	24	1.6	90nm, LNA, mixer, VGA, buffer, off-chip LO [6]
18.3-22	5.7-8.8	-27.5	n/a	n/a	1.2	36	0.2	90nm, LNA, 30GHz LO, RF mixer, IF mixer [7]
19.7	11.7	-17	6.0	QPSK 2.6Gb/s	0.7, 1.0	339	4.5	90nm, TX, RX, IQ mod/demod, off-chip LO [8]
14.7 (12.1)	5.6 (5.7)	-22	n/a	n/a	1.2 (1.0)	151 (101)	0.5	65nm, single-chip RX, off-chip LO, This work (RX)
11.3 (8.9)	5.6 (5.8)	-22	2.4 (-0.7)	BPSK 4Gb/s+	1.2 (1.0)	374 (232)	1.0	65nm, single-chip TXRX, LO tree, divider, off-chip LO, This work (TXRX)

Measurements of the receiver over temperature in Fig. 18(a) show approximately 7 dB gain degradation and 2 dB noise figure increase from 25°C to 85°C. Fig. 18(b) illustrates that the gain and noise figure do not seriously degrade as $V_{\rm DD}$ is reduced to 1.0 V, with a gain drop of 2.5 dB, and a noise figure increase of only 0.3 dB. When operated from 0.8 V supply, the receiver still has 9.8 dB of conversion gain, and a 6.5 dB noise figure, illustrating the relative immunity of this design to power supply variation. While the gain degradation over temperature and supply can be easily compensated for at IF with a VGA, the noise-figure degradation can only be avoided by providing sufficient gain and noise figure margin in the LNA. The measured input return loss of the receiver is less than -10 dB, and the input compression point is -22 dBm.

From these experiments one can conclude that significant variation due to process and temperature in nanoscale CMOS circuits must be expected and accounted for in the design. This observation, first signalled for 90 nm CMOS LNAs [19] has been recently confirmed in the literature by other groups [37], [38], indicating that the insufficient margins offered by 90 nm and even 65 nm CMOS processes will require significant design efforts to ensure robust and reliable 60 GHz systems.

V. WIRELESS LINK DEMONSTRATION

Finally, to validate the functionality and effectiveness of the direct-modulation, zero-IF architecture in CMOS, a transmit-receive link was demonstrated in the 55–64 GHz range by employing one transceiver chip in transmit-mode mounted on a probe station, and another transceiver chip in receive-mode placed on a second probe station, approximately 2 meters away. A schematic of the experimental setup is shown in Fig. 19. The circuits were contacted using 67 GHz signal probes and 67 GHz cables connecting to horn antennas with 25 dBi gain. An external amplifier with 30 dB gain and 4 GHz bandwidth was connected between the IF output of the receiver and a sampling oscilloscope (Agilent 86100C-DCA). The phase and frequency alignment between the two different local oscillator signals of the receiver and the transmitter on the two probe stations was established using an external 10 MHz synchronization signal. However, small periodic drifts in the phase and/or frequency of the LO signals were observed, and manual or automated correction of these phase changes was required. In a commercial transceiver, an LO or IF/baseband phase rotator is needed, similar to those implemented in existing 2–6 GHz WLAN systems employing a direct conversion IQ receiver architecture.

The transmitter output spectrum is shown in Fig. 20(a) (top) for a 4.0 Gb/s $2^7 - 1$ PRBS data signal. Because the output spectra were captured using a harmonic mixer with no image-rejection, only the main lobe of the response can be shown for wideband signals due to the image signals present at all harmonics of the mixer LO signal. The spectra for a narrower-band modulation at 0.5 Gb/s was also captured (bottom) to clearly illustrate the sinc-function response. Note that the system losses have not been de-embedded from the power-levels measured by the PSA. With the transmitter operating at 25°C, Fig. 21b(a), and 50°C, Fig. 21b(b), and with an input data-rate of 4 Gb/s, excellent receive eye diagrams can be seen for both temperatures, with a clearly recovered bit-pattern. To the best of our knowledge, this represents the first demonstration of a 60 GHz transmit/receive link performance over temperature variation in any silicon technology.

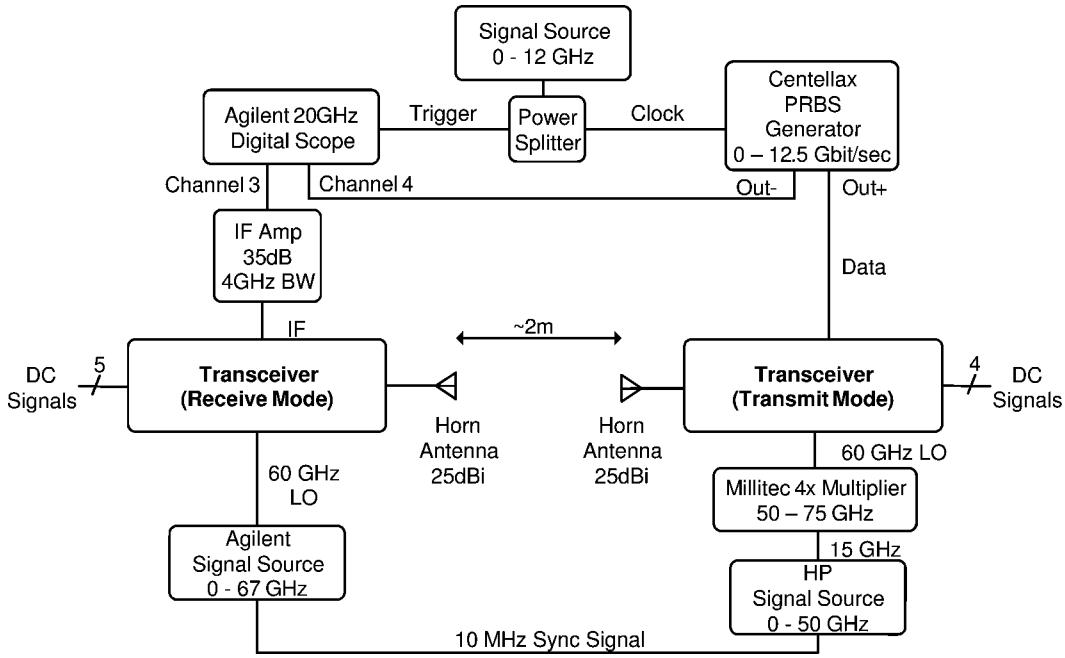

Fig. 19. Diagram of the experimental setup used to demonstrate the wireless link.

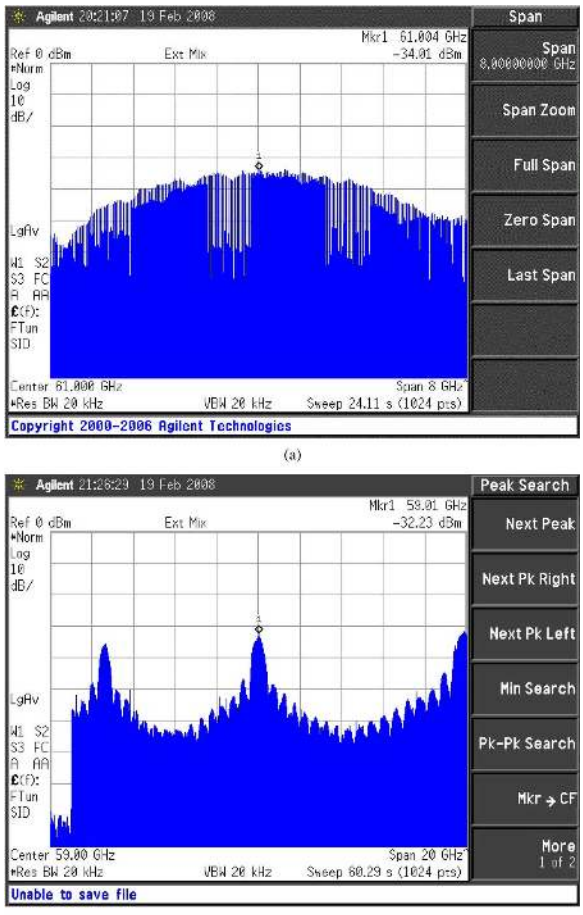

Fig. 20. 4.0 Gb/s PRBS transmitter spectrum at 61 GHz LO (top), and a lower bit-rate (0.5 Gb/s) modulation spectra at 59 GHz (bottom), showing image folding due to the use of a harmonic mixer.

Increasing the input data rate to 6 Gb/s, the bandwidth of the external IF amplifier starts to limit performance, with the eyes and the received bit-pattern in Fig. 22 indicating the onset of bandwidth limitations. These transceiver link experiments demonstrate that the simple, zero-IF, direct-modulation radio architecture, without ADCs or IQ mixer, is adequate for indoor, line-of-sight communication at 60 GHz with data rates up to 6 Gb/s over distances that exceed 2 m.

A performance comparison between this work and that of others is shown in Table I. Due to the general complexities of the systems and the large variation in implementation levels, an equitable comparison is difficult to capture in a single table. While both transceiver and receiver-only half-duplex performance results for this work are shown for the purpose of comparing with other receiver-only work, referenced transceiver publications were not shown in half-duplex mode. It should be emphasized that, although comparable to other transceivers, the power consumption of this circuit was not minimized as a primary design-goal, but rather the operation of the entire system over process, power-supply, and temperature variation was pursued. In the authors' opinion, supported by recent experimental data collected over temperature by other groups [37], [38], achieving the required margin for operating over all corners ultimately results in increased power consumption. With the exception of [1], most published data refer to room temperature operation only and may not be indicative of the expected performance in a real product.

VI. Conclusion

A 1.2 V 60 GHz zero-IF transceiver with direct modulation has been fabricated in a 65 nm CMOS technology. Targeting high-frequency, high-bandwidth data-transfer applications, the system employs direct digital modulation, a 60 GHz LO

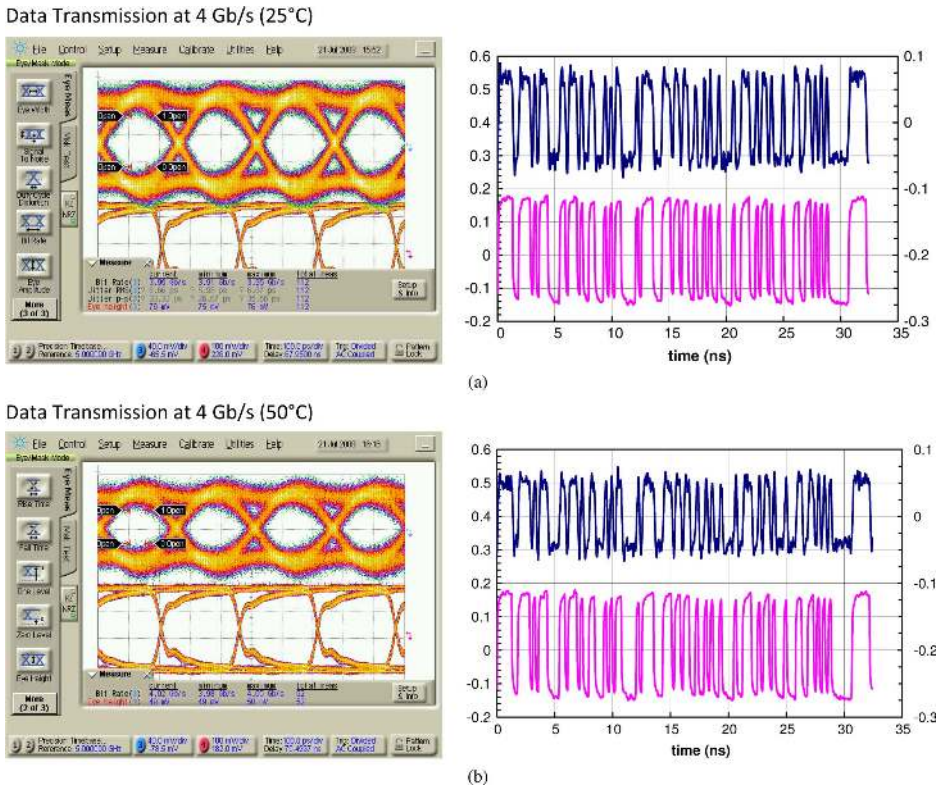

Fig. 21. The received (top) and transmitted (bottom) eyes and bit sequence for (a) 25°C and (b) 50°C at 61 GHz LO. Minimal degradation is observed between temperature points.

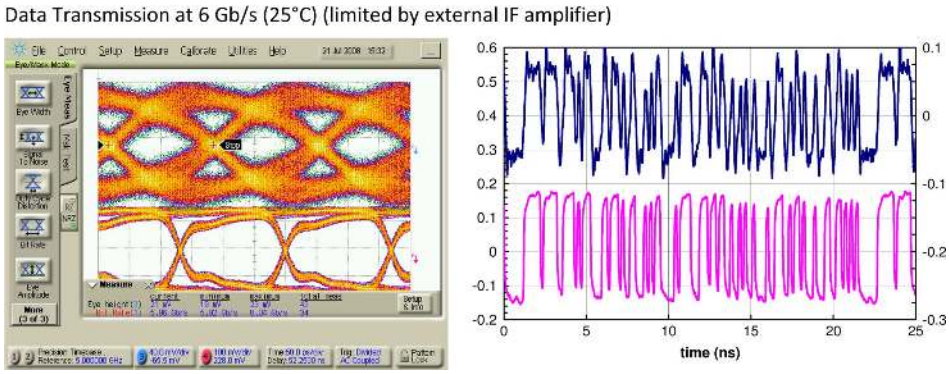

Fig. 22. The received (top) and transmitted (bottom) eyes and bit sequence at 61 GHz LO.

distribution tree, a fundamental frequency static divider, and zero-IF down-conversion. A wireless transmit-receive demonstration over 2 meters between two probe stations acts as a proof-of-concept, achieving data-transfer rates in excess of 4 Gb/s when transmitting at 50 °C. The transceiver occupies only 1.28×0.81 mm^2 and consumes 101 mW and 131 mW from 1 V supply in receive and transmit mode, respectively, raising hopes for the feasibility of a low-power, low-cost multi-gigabit/s radio that could be integrated in cell-phones and other portable devices.

ACKNOWLEDGMENT

The authors would like to thank K. Laskin and I. Sarkas for additional measurement assistance and J. Pristupa and CMC for CAD support. The authors would also like to acknowledge Dr. W. Walker and Dr. M. Wiklund of Fujitsu Laboratories of America Inc. for their support and discussions on digital-rich mm-wave radio transceivers and the IEEE 802.15.3c standard specification.

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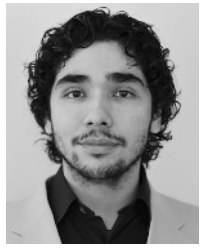

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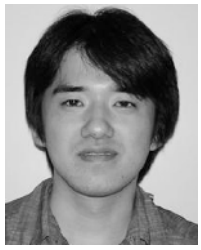

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