

# A Zero-Voltage and Zero-Current Switching Full Bridge DC–DC Converter With Transformer Isolation

Seong-Jeub Jeon, *Member, IEEE* and Gyu-Hyeong Cho, *Member, IEEE*

**Abstract**—A new primary-side-assisted zero-voltage and zero-current switching full bridge dc–dc converter with transformer isolation is proposed. The proposed dc–dc converter uses only one auxiliary transformer and two diodes to obtain ZCS for the leading leg. It has a simple and robust structure, and load current control capability even in short circuit conditions. Possibility of magnetic saturation due to asymmetry of circuits or transient phenomena is greatly reduced, which is a very attractive feature in dc–dc converters with transformer isolation. The power rating of the auxiliary transformer is about 10% of that of the main transformer. Operation of a 12 KW prototype designed for welding application was verified by experiments.

**Index Terms**—DC–DC converter, zero current switching, zero voltage.

## I. INTRODUCTION

IN dc–dc converters with transformer isolation, the size of the isolation transformer is inversely proportional to switching frequency. On the other hand, switching frequency is limited by switching loss that increases proportionally to the frequency. This switching loss can greatly be reduced by using zero voltage switching (ZVS) [1]. However, the ZVS condition is usually too narrow and the conduction loss high. Fig. 1(a) and (b) show ZVS operation waveforms. On the one hand the lagging leg transition is slow and possible under almost all conditions, on the other hand the leading leg transition is abrupt and the ZVS operation is highly dependent on load condition. And the freewheeling periods inserted in to the primary side of the transformer cause conduction loss to the switching devices. To solve these two problems zero-voltage and zero-current switching (ZVZCS) is proposed [2]–[9]. A typical current waveform of ZVZCS converter is shown in Fig. 1(c) and (d). In the ZVZCS full bridge dc–dc converter, one leg (lagging leg) operates in ZVS mode while the other leg (leading leg) operates in ZCS mode. The ZCS condition can be obtained by introducing an auxiliary circuit into the primary or secondary side as shown in Fig. 2. In secondary-side-assisted ZVZCS converters the auxiliary circuit prepares ZCS by suppressing the load current from the isolation transformer, and bypassing the load current through them [2]–[7]. A snubber circuit or an active clamp circuit can be used as an auxiliary circuit [2], [4]–[7]. They have two merits: prolonged on-duty, and unified snubber and auxiliary circuit.

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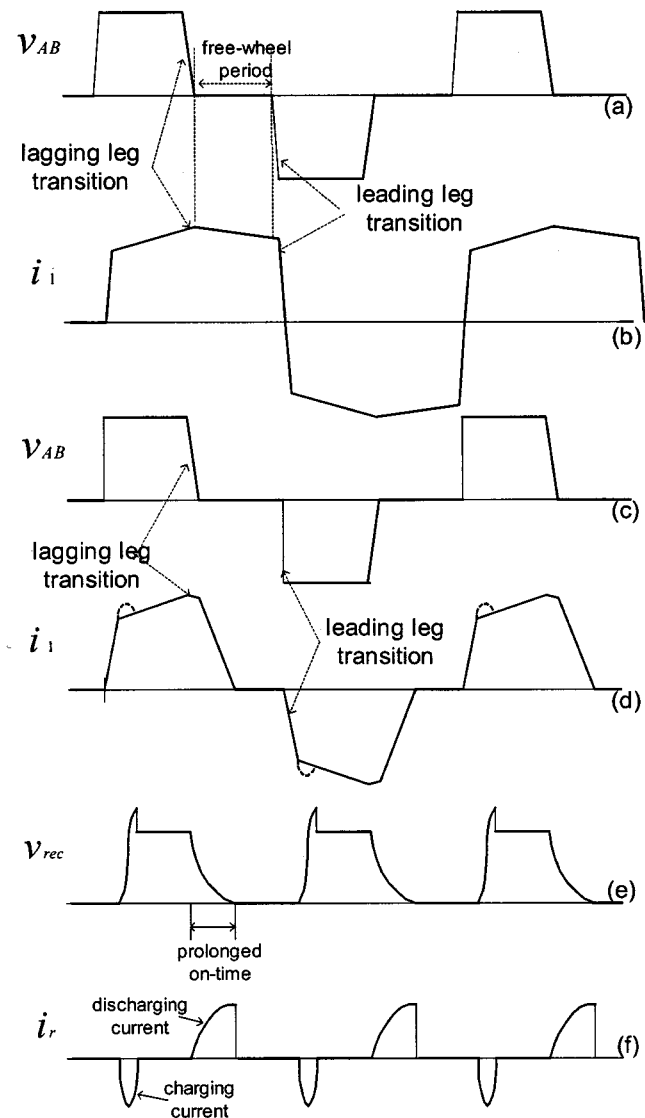


Fig. 1. ZVS and ZVZCS waveforms.

The prolonged on-duty shown in Fig. 1(e) and (f) is a merit when converters operate at high duty ratio, but a serious drawback exists when the system suffers short-circuit condition because it is not controllable. The unified snubber and auxiliary circuit is a great merit, but it is no longer a merit for high power applications because it becomes somewhat bulky. Circuits proposed in [5]–[7] have lower peak rectifier voltage than circuit proposed in [4] by introducing load voltage into auxiliary circuits. However these circuits bypass resonance current into load side at leading

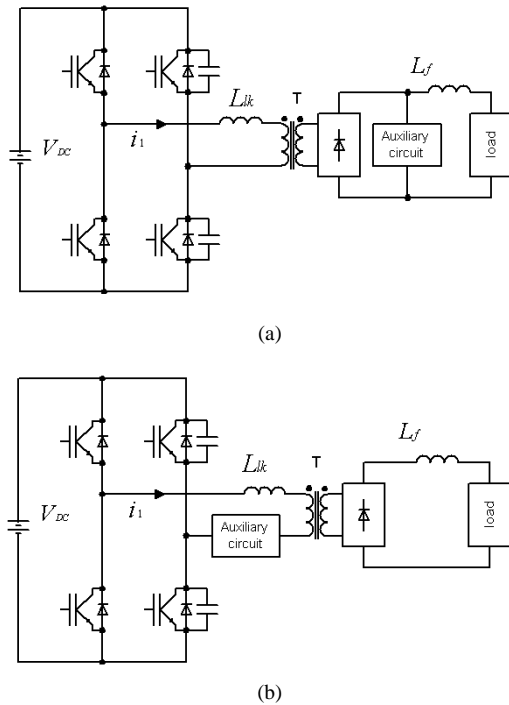


Fig. 2. ZVZCS dc-dc converters (a) Secondary-side-assisted ZVZCS converter (b) Primary-side-assisted ZVZCS converter.

leg transition [5], [7] and have larger resonance or snubber capacitor due to lowered voltage [5]–[7]. Hence the resonance frequency is lowered and the average current of the auxiliary circuit becomes higher. It is reported that the current ratings of the auxiliary diodes are 30% of main rectifier diodes [5], [6]. Furthermore peak rectifier voltage is still  $2V_D/n$  at startup because of zero output voltage [5]–[7]. Accordingly peak and average current of the auxiliary circuit become about four times those of normal states. So startup is a serious problem in these converters. Primary-side-assisted ZVZCS converters provide the ZCS condition by introducing resetting voltage into the primary side, which absorbs reactive energy trapped in leakage inductor [8], [9]. In primary-side-assisted ZVZCS converters, the primary current of the main transformer is reset to zero at every half cycle, hence possibility of magnetic saturation due to asymmetry of circuits or transient phenomena is reduced, which is a very attractive feature in dc-dc converters with transformer isolation. One primary-side-assisted ZVZCS converter uses a capacitor to provide ZCS condition by absorbing reactive energy trapped in leakage inductor, and a saturable core to ensure the ZCS condition [8]. In this type of converter, use of AC capacitor and heating of the saturable core are serious problems. Another type of primary-side-assisted ZVZCS converter uses an auxiliary circuit composed of an auxiliary transformer and two small active switches; it absorbs reactive energy trapped in the leakage inductor by introducing resetting voltage through an auxiliary transformer [9]. Auxiliary transformers or coupled inductors aiding soft switching are found in other applications [10]–[14].

In this paper a new primary-side-assisted ZVZCS dc-dc converter is proposed with an auxiliary circuit consisting of only one auxiliary transformer and two diodes. The power rating of the auxiliary transformer is about 10% of that of the main transformer.

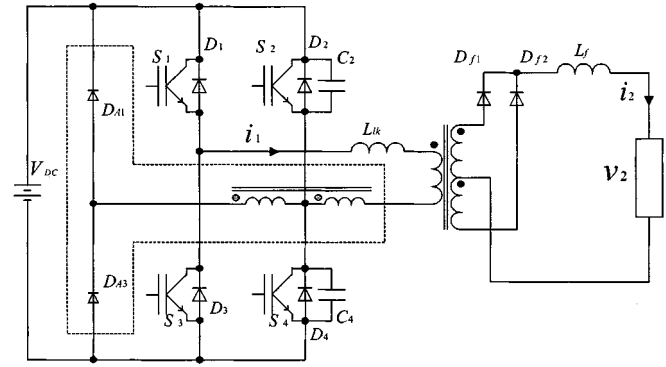


Fig. 3. Circuit diagram of the proposed dc-dc converter.

Because the arc and metal transfer process involves an extreme change in load from short to open circuits, the proposed circuit is well suited for arc welding machines. In some machines welding is started with scratching an electrode on base metal, which means short-circuiting while the load current is controlled to a desired value. The proposed circuit does not lose current control capability even in short circuit conditions, whereas the secondary-side-assisted ZVZCS converters lose control capability and ZVZCS operation.

## II. PROPOSED CIRCUIT

### A. Operation Principle

The proposed dc-dc converter is shown in Fig. 3. The auxiliary circuit, enclosed by the dotted line, consists of only two diodes and a small auxiliary transformer. The primary winding of the auxiliary transformer is connected in series with the primary winding of the main transformer; the secondary winding of the auxiliary transformer is connected between the passive leg and the lagging leg. The output power is controlled by the phase delay between the leading and lagging legs. To obtain appropriate phase delay, phase shift pulse width modulation (PWM) is employed. The lagging leg operates in ZVS condition with assistance of reactive components  $C_2, C_4, L_{lk}$  and  $L_f$ , while the passive leg operates according to the primary current.  $L_{lk}$  is the total leakage inductance of the main transformer and the auxiliary transformer.  $C_2$  and  $C_4$  are the sums of the output capacitance of switches,  $S_2$  and  $S_4$ , and additional capacitors paralleled with them to enhance ZVS effects respectively.  $C_2$  and  $C_4$  provide ZVS-off of switches  $S_2$  and  $S_4$ , when they are turned off.  $L_{lk}$  and  $L_f$  provide ZVS-on by changing the voltage across  $C_2$  and  $C_4$  to the opposite rail voltage and causing the primary current flow through the anti-parallel diode  $D_2$  or  $D_4$  prior to turning on of  $S_2$  or  $S_4$ . The leading leg operates in ZCS conditions with the assistance of the auxiliary circuit, which provides resetting voltage and absorbs reactive energy trapped in the leakage inductor  $L_{lk}$ ; it also resets the primary current prior to switch transition. Resetting is completed prior to switch transitions of the leading leg.

### B. Operation Modes

One cycle operation can be divided into 5 modes as shown in Fig. 4; Fig. 5 shows the operation waveforms. To simplify

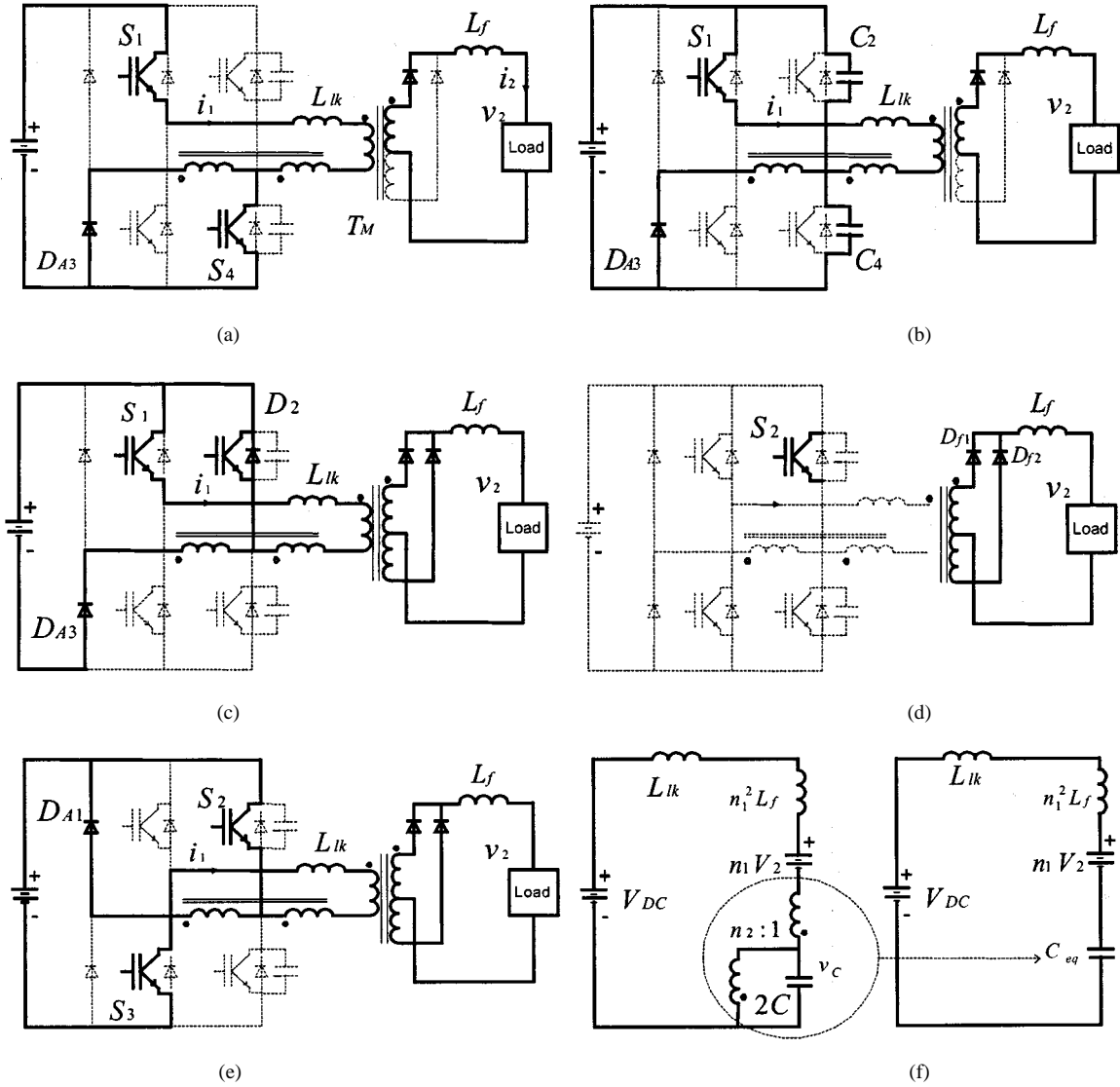


Fig. 4. Operation modes.

analysis, the magnetizing inductance of the main transformer and the auxiliary transformer are ignored.

1) *Mode 1* ( $t_1 < t < t_2$ ): During this mode, switches  $S_1$  and  $S_4$ , are in conduction states and power is transferred through the main transformer and the rectifier diode  $D_{f1}$  to the load. The secondary terminals of the auxiliary transformer are short-circuited by  $D_{A3}$  and  $S_4$ . The current flowing through  $S_4$  is given by

$$i_{S4} = \left(1 + \frac{1}{n_2}\right) i_1. \quad (1)$$

2) *Mode 2* ( $t_2 < t < t_3$ ): Mode 2 is initiated by turning off  $S_4$ . A resonant circuit is constructed with  $C_2$ ,  $C_4$ ,  $L_{lk}$  and  $L_f$ . The equivalent circuit is shown in Fig. 4(f). Voltage across capacitor  $C_4$  is given by

$$v_c = \frac{n_2}{1+n_2} ((V_{DC} - n_1 V_2)(1 - \cos \omega_o(t - t_2)) + I_1(t_2) Z_o \sin \omega_o(t - t_2)) \quad (2)$$

and primary current  $i_1$  is given by

$$i_1 = \frac{(V_{DC} - n_1 V_2)}{Z_o} \sin \omega_o(t - t_2) + I_1(t_2) \cos \omega_o(t - t_2) \quad (3)$$

where

$$\omega_o = \sqrt{\frac{1}{(L_{lk} + n_1^2 L_f) C_{eq}}}, \quad (4)$$

$$Z_o = \sqrt{\frac{L_{lk} + n_1^2 L_f}{C_{eq}}}, \quad (5)$$

$$C_{eq} = 2C \left(\frac{n_2}{1+n_2}\right)^2, \quad (6)$$

$$C = C_2 = C_4. \quad (7)$$

We can consider that current  $i_1$  is constant during this interval, since  $n_1^2 L_f$  is large. The voltage across  $S_4$  increases smoothly to the upper rail voltage, which results in ZVS turn-off of  $S_4$ .

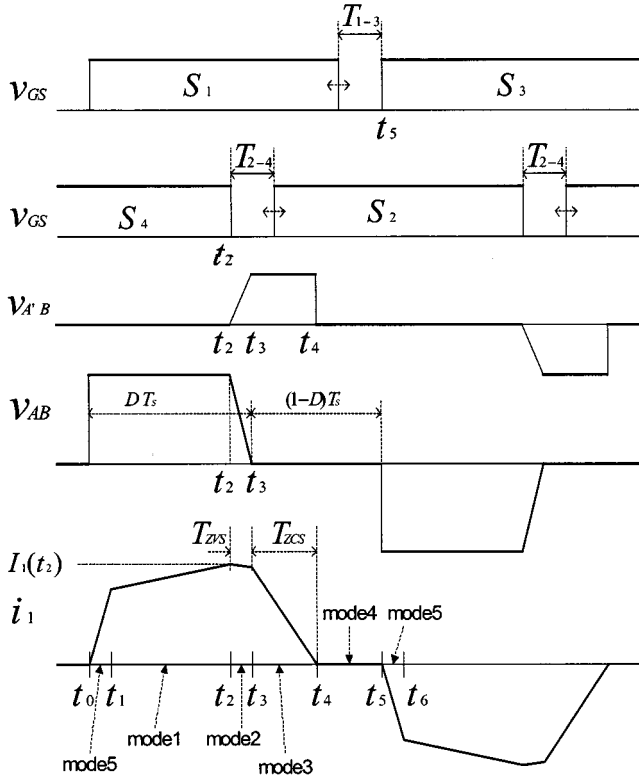


Fig. 5. The operational waveforms of the proposed circuit.

3) *Mode 3* ( $t_3 < t < t_4$ ): After the voltage across  $S_4$  reaches the upper rail voltage, the primary current flows through  $D_2$ , and Mode 3 is initiated. The dc-side voltage is reflected to the primary winding of the auxiliary transformer, as shown in Fig. 4(c). The reactive energy trapped in the inductor is recovered to the dc side. Primary current  $i_1$  decreases to zero as

$$i_1 = I_1(t_3) - \frac{V_{aux}}{L_k} (t - t_3) \quad (8)$$

where  $V_{aux}$  is the reflected voltage of the dc side through the auxiliary transformer, acting to reset the primary current, and given by

$$V_{aux} = \frac{V_{DC}}{n_2}. \quad (9)$$

During this mode, the anti-parallel diode  $D_2$  is in conduction; hence  $S_2$  can be turned on in ZVS conditions.

4) *Mode 4* ( $t_4 < t < t_5$ ): After the primary current becomes zero, Mode 4 is initiated. During this mode the primary current remains at zero, and the load current flows evenly through  $D_{f1}$  and  $D_{f2}$  as in Fig. 4(d). Also in this mode, switch  $S_1$  is turned off with ZCS condition and the load current freewheels through the two secondary windings of the transformer.

5) *Mode 5* ( $t_5 < t < t_6$ ): This mode is initiated by turning on switch  $S_3$  in ZCS conditions. Primary current  $i_1$  begins to flow through switches  $S_2$  and  $S_3$ . The secondary terminals of

the auxiliary transformer are short-circuited by  $D_{A1}$  and  $S_2$ . The primary current  $i_1$  is given by

$$i_1 = -\frac{V_{DC}}{L_k} (t - t_5). \quad (10)$$

Load current flowing through  $D_{f1}$  diverts to  $D_{f2}$  as  $i_1$  increases. This mode ends when the current flowing through  $D_{f1}$  becomes zero.

In this way, one switching cycle is completed. The next switching cycle begins with mode 1 during which switches  $S_2$  and  $S_3$ , are in conduction states.

### C. Consideration on ZVZCS Condition

ZVS-off of switch  $S_4$  is natural, as  $C_{eq}$  is connected in parallel with  $S_4$ . To achieve safe ZVS-on of  $S_2$  the voltage  $v_C$  must reach the upper rail voltage. In general the energy in  $n_1^2 L_f$  is large sufficiently to raise  $v_C$  to the upper rail voltage; therefore ZVS operation is almost always possible. It is usually considered that the current  $i_1$  is constant during Mode 2, since  $n_1^2 L_f$  is large and the time interval is short. The time interval given to switches  $S_2$  and  $S_4$  for ZVS operation is given by (11) and easily designed by selecting the appropriate  $C_{eq}$ .

$$T_{ZVS} = t_3 - t_2 = \frac{C_{eq} V_{DC}}{I_1}. \quad (11)$$

During Mode 3, ZCS-off operation in the leading leg is accomplished by eliminating the primary current prior to removing the gate pulse of  $S_1$ . The approximate time interval required to eliminate the primary current is given by

$$T_{ZCS} = t_4 - t_3 = \frac{L_k I_1}{V_{aux}}. \quad (12)$$

$T_{ZCS}$  is the minimum when current is at its minimum, and the minimum  $T_{ZCS}$  is given by

$$T_{ZCS \min} = \frac{L_k I_{1 \min}}{V_{aux}} \quad (13)$$

where  $I_{1 \min}$  is the minimum current. The minimum current is usually given as magnetizing current of the main transformer.  $T_{ZCS}$  is at its maximum when the current is at maximum, and the maximum  $T_{ZCS}$  is given by

$$T_{ZCS \max} = \frac{L_k I_{1 \max}}{V_{aux}} \quad (14)$$

where  $I_{1 \max}$  is the maximum current allowed.

The condition for safe ZCS operation is given by

$$T_{ZCS \max} < (1 - D_{\max}) T_s \quad (15)$$

where  $D_{\max}$  is the maximum duty cycle and  $T_s$  is the switching period. In general, the duty ratio ranges from 0.6 to 0.9; in special applications such as welding machines, it ranges from 0.3 to 0.6. The ZCS condition can be easily achieved by selecting the appropriate  $V_{aux}$ . In applications with low duty ratios it can be achieved with a low  $V_{aux}$ . The lower the  $V_{aux}$  that is used, the smaller auxiliary transformer required.

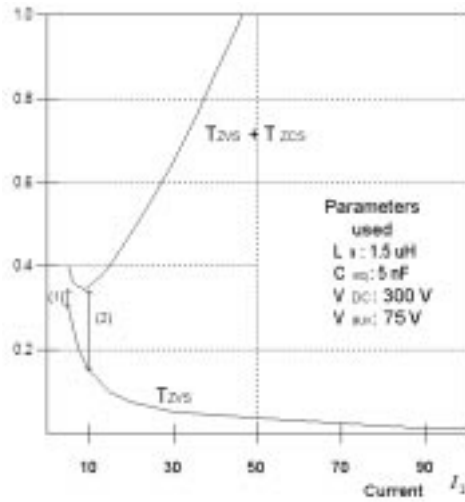


Fig. 6. Safe range of  $T_{d2-4}$  1) when  $I_{1 \min}$  is 5 A, 2) when  $I_{1 \min}$  is 10 A.

#### D. Dead Times for Switch Transitions

1) *Lagging Leg*: The dead time for the lagging leg is denoted as  $T_{d2-4}$ , as shown in Fig. 5, and must satisfy the following condition for safe ZVS transitions of switches.

$$t_3 - t_2 < T_{d2-4} < t_4 - t_2. \quad (16)$$

The left limit is defined as  $T_{ZVS}$  in (11) and is a monotonically decreasing function of  $I_1$ . The right limit is given as the sum of  $T_{ZVS}$  and  $T_{ZCS}$  and is a nearly monotonically increasing function of  $I_1$ . Therefore, if we select  $T_{d2-4}$  according to (17), ZVS transitions of the lagging leg are ensured for all cases.

$$T_{ZVS \max} < T_{d2-4} < T_{ZVS \max} + T_{ZCS \min}. \quad (17)$$

Fig. 6 shows an example for variations of both bounds in (17) and ranges for safe dead time. From Fig. 6 we know it is possible to design a safe dead time with constant value for the lagging leg, even when the minimum current is 5 A, less than one 10th of the rated current.

2) *Leading Leg*: Dead time for the leading leg is denoted by  $T_{d1-3}$ , shown in Fig. 4 and given by (18). The selectable range of a safe dead time is quite wide; hence, the design of dead time for the leading leg is simple:

$$T_{d1-3} < t_5 - t_4. \quad (18)$$

The upper bound  $t_5 - t_4$  is at the minimum when the duty ratio and the current are at their maximums; therefore, if we select dead time according to (19) the switches will be safely switched in all cases:

$$T_{d1-3} < (1 - D_{\max})T_s - T_{ZCS \max}. \quad (19)$$

#### E. Consideration on Designing of Transformers

1) *Main Transformer*: Operation condition of the target system is as follows:

- dc voltage: 280 V–340 V;
- nominal load: 27 V, 450 A;
- open circuit voltage: 65 V;
- sse rate: 60% (forced air cooling).

The operating frequency selected is 42 KHz. To satisfy open circuit output voltage the converter operates at low duty ratio: below 0.6. The core and turns of the main transformer designed are as follows. The measured leakage inductance referred to primary side is 1.5  $\mu$ H. Detailed design will be performed with conventional method.

Core: EI-118 (Isu ceramics)

Primary winding: nineturns

Secondary winding: twoturns (two paralleled and center-tapped).

2) *Auxiliary Transformer*: ZCS is introduced to alleviate conduction loss during freewheeling period, however the auxiliary circuit causes additional conduction loss because current flows through it. The additional conduction loss depends highly on duty ratio and turns ratio of auxiliary transformer. So for high duty application reduction of conduction loss is insignificant. It is also true for the secondary-side-assisted ZVZCS converters, because charging and discharging current flows through the auxiliary circuits. Welding application is the best example where reduction of conduction loss is apparent because low duty ratio is required due to relatively higher open circuit voltage. We can design turns ratio of the auxiliary transformer from appropriate  $T_{ZCS}$ . Setting  $D_{\max}$  to 0.6 and  $T_{d1-3}$  to 1  $\mu$ s, from (19) we get

$$T_{ZCS \max} < (1 - 0.6) \times 11.9 - 1 = 3.76 \mu\text{sec}. \quad (20)$$

From (14) we get resetting voltage

$$V_{aux} > \frac{1.5 \mu \times 110}{3.76 \mu} = 44 \text{ V}. \quad (21)$$

In case of low duty ratio, turns ratio of the auxiliary transformer is decided within the range given in (21) such that the conduction loss might be minimized. Assuming that the primary side switches have the same on voltage we get the loss increased due to the auxiliary circuit as follows:

$$P'_{loss2} = \frac{P_{loss2}}{V_s I_1} = \frac{2D}{n_2} \quad (22)$$

and we get the loss during mode 3 as follows:

$$P'_{loss3} = \frac{P_{loss3}}{V_s I_1} = \frac{1}{2} (1 + n_2) \frac{\%Z_{lk}}{\pi} \quad (23)$$

where

$$\%Z_{lk} = \frac{\omega_s L_{lk} I_1}{V_{DC}} \quad (24)$$

$V_s$  is on voltage of switches and  $\omega_s$  is switching angular frequency.

$P'_{loss2}$  and  $P'_{loss3}$  are depicted in Fig. 7 from which optimum point is obtained when turns ratio  $n_2$  is 4. The power recovered by auxiliary transformer and returned to the source is given by

$$P_{aux} = \frac{1}{2} L_{lk} I_1^2 2f_s = \frac{1}{2} 1.5 \mu \times 110^2 \times 2 \times 42 \text{ K} = 763 \text{ W}. \quad (25)$$

The power rating is about 7% of rated power. The core and turns of the auxiliary transformer are as follows:

core: EI-6044 (TDK);

primary winding: two turns;

secondary winding: eight turns.

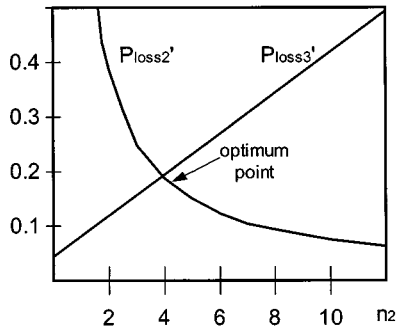
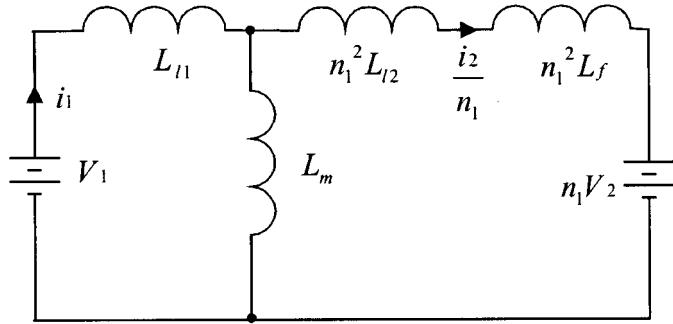
Fig. 7. Loss curve for  $D = 0.4$ .

Fig. 8. Equivalent circuit of the power stage.

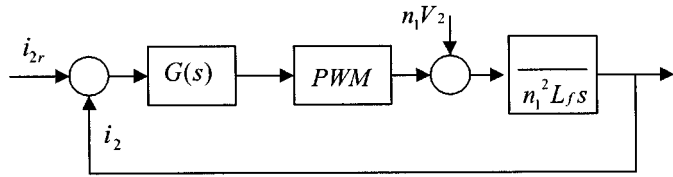


Fig. 9. Control loop for load current.

### F. Control of Load Current

1) *Current Controller*: The equivalent circuit of the power stage is shown in Fig. 8. Assuming that magnetizing inductance is large and leakage inductance is small compared to  $L_f$ , both can be ignored and we obtain the transfer function as

$$\frac{I_1(s)}{V_1(s)} = \frac{1}{n_1^2 L_f s}. \quad (26)$$

The control loop was constructed as in Fig. 9; PI controller is used for  $G(s)$ .

2) *Waveform of the Load Current*: In many cases arc welding requires constant current characteristics as in Fig. 10. Arc voltage is dependent on arc length; for a longer arc, higher voltage is required. The welding current is adjusted according to welding conditions. In some arc welding it is known that better results are obtained when the current pulsates, as in Fig. 11(a). During high current time the metal is molten, and during low current time the metal is solidified. For more comfortable welding it is required that the current has slopes at the start and the end of welding, as in Fig. 11(b). The waveforms are generated by an 87C196KC microcontroller.

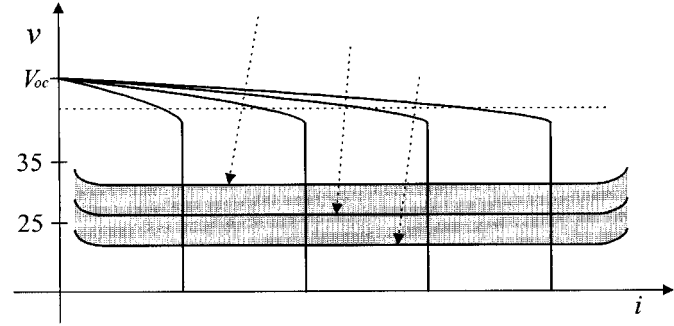


Fig. 10. Constant current characteristics of arc welding.

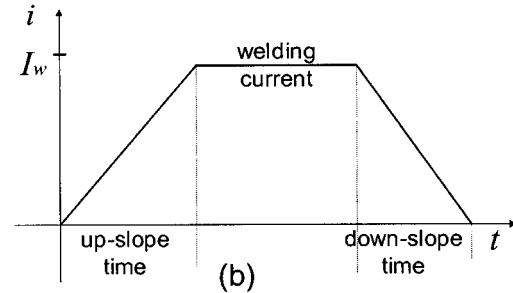
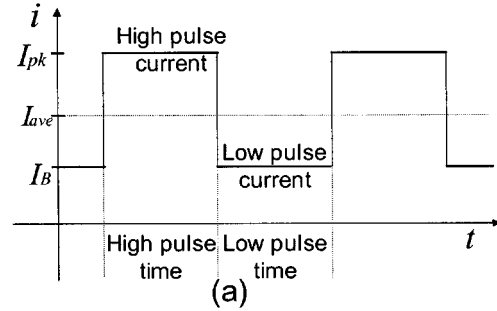


Fig. 11. Current shapes of arc welding.

### III. EXPERIMENTAL RESULTS

A 12KW prototype of the proposed circuit was constructed and tested. It was designed for use in welding applications. Circuit parameters and components used are follows:

$$\begin{aligned} S_1-S_4: & \text{ FM2G200US60} \\ D_{A1}, D_{A3}: & \text{ DSEI2x31-06C} \\ D_{f1}, D_{f2}: & \text{ DSEI2x101-06C *4} \\ C_{eq}: & \text{ 5 nF} \\ L_f: & \text{ 100 uH} \end{aligned}$$

Results are shown in Figs. 12–17. Fig. 12 shows efficiency curve. Although only 27 V output is necessary for welding application, experiment is also performed for 50 V output for comparison with other ZVZCS system. The transformers designed can be operated for 50 V marginally. Maximum efficiency is about 95.5% for 50 V output and about 93.5% for 27 V output. Efficiency for light load is also relatively high. About 80% of efficiency is obtained for 150 W load. No load loss measured is about 50 W. In Figs. 13 and 14, the top trace is the bridge output voltage  $v_{AB}$ ; the middle trace is the primary voltage of the main transformer; the bottom trace is the primary current of the main transformer. Fig. 13 is for 50 V output. The small pulses in the primary voltage are resetting voltage

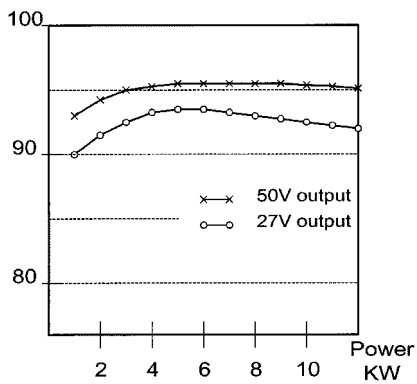


Fig. 12. Efficiency curve.

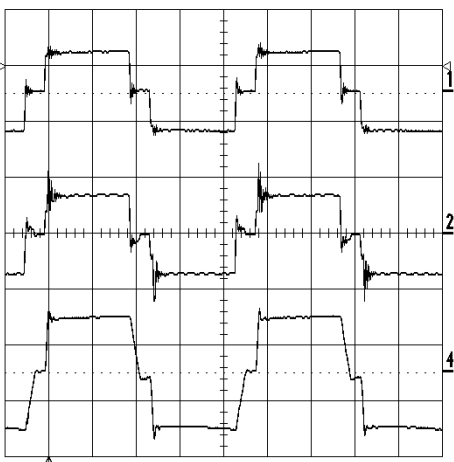


Fig. 13. Experimental waveforms of the main transformer. Bridge output voltage (top trace: 400 V/div), primary voltage of the main transformer (middle trace: 400 V/div) and primary current (bottom trace: 50 A/div), time base: 5  $\mu$ s/div.

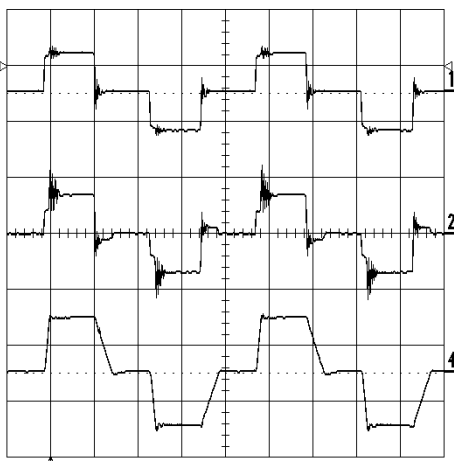


Fig. 14. Experimental waveforms of the main transformer. Bridge output voltage (top trace: 400 V/div), primary voltage of the main transformer (middle trace: 400 V/div) and primary current (bottom trace: 100 A/div), time base: 5  $\mu$ s/div.

imposed on the leakage inductance of the main transformer. This resetting voltage, reflected to the primary side of the auxiliary transformer, is imposed on the leakage inductance; it is divided according to the inductance of the main and auxiliary

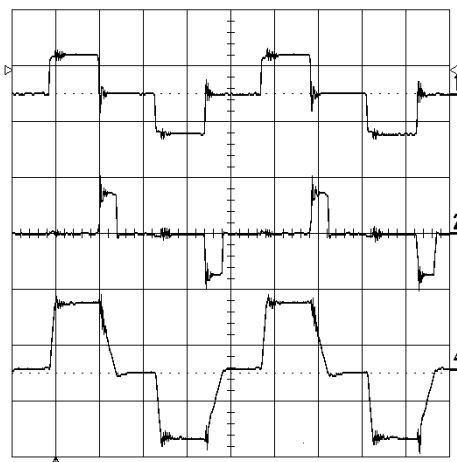


Fig. 15. Experimental waveforms of the auxiliary transformer. Bridge output voltage (top trace: 400 V/div), secondary voltage of the auxiliary transformer (middle trace: 400 V/div) and the secondary current of the auxiliary transformer (bottom trace: 20 A/div), time base: 5  $\mu$ s/div.

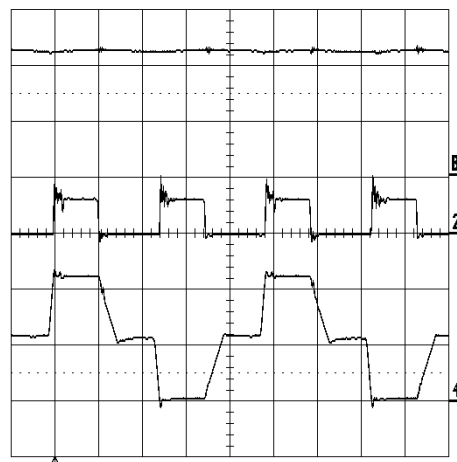


Fig. 16. Experimental waveforms of rectifier. Load current (top trace: 200 A/div), rectifier output voltage (middle trace: 100 V/div) and rectifier diode current (bottom trace: 200 A/div), time base: 5  $\mu$ s/div.

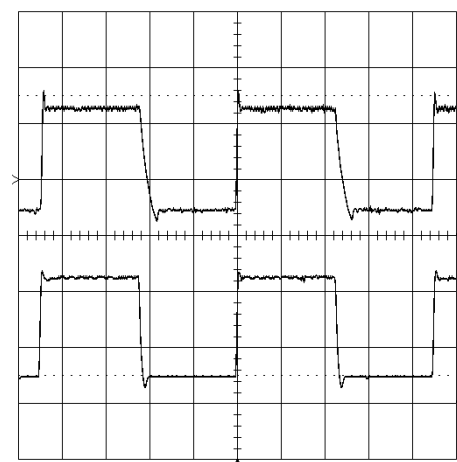


Fig. 17. Pulse operation waveforms. Load current (200 A/div), time base: 1 s/div; Upper trace is for a short-circuited load and lower trace for a rated load.

transformers. In Fig. 15, the top trace is the inverter output voltage; the middle trace is the voltage  $v_{BC}$  of the secondary

winding of the auxiliary transformer; the bottom trace is the secondary current of the auxiliary transformer. Figs. 13–15 show stable ZVZCS operations. In Fig. 16, the top trace is the load current; the middle trace is the rectified voltage; and the bottom trace is current flowing through the rectifying diode  $D_{f1}$ . Fig. 17 shows the load current waveform according to current command. The upper trace is for a short-circuited load, and the lower trace is for a rated load. For both load conditions, desired load currents were obtained.

#### IV. CONCLUSION

A new ZVZCS full bridge dc–dc converter with isolation transformer is proposed. It employs one additional auxiliary transformer to obtain ZCS conditions for the leading leg. The auxiliary circuit including the auxiliary transformer is relatively small. Possibility of magnetic saturation due to asymmetry of circuits or transient phenomena is greatly reduced, which is a very attractive feature. It operates well over a wide range of load conditions, ranging from no load to short-circuited load. The operation of the converter was verified by experiments. It shows high efficiency comparing with previously proposed ZVZCS converters. Due to its simplicity and robustness the proposed topology is thought to be suitable for from low to high power applications.

#### REFERENCES

- [1] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design consideration for high-voltage high-power full-bridge zero-voltage switched PWM converter," in *Proc. IEEE Appl. Power Electron. Conf.*, 1990, pp. 275–284.
- [2] J. G. Cho, G. H. Rim, and F. C. Lee, "Zero-voltage and zero-current switching full bridge PWM converter using secondary active clamp," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 657–663.
- [3] J. G. Cho, J. W. Baek, D. W. Yoo, C. Y. Jeong, H. S. Lee, and G. H. Rim, "Novel zero-voltage and zero-current switching (ZVZCS) full bridge PWM converter using transformer auxiliary winding," in *Proc. IEEE Power Electron. Spec. Conf.*, 1997, pp. 227–232.
- [4] E. S. Kim, K. Y. Joe, M. H. Kye, Y. H. Kim, and B. D. Yoon, "An improved soft switching PWM FB dc/dc converter for reducing conduction losses," in *Proc. IEEE Power Electron. Spec. Conf.*, 1996, pp. 651–656.
- [5] J. W. Baek, C. Y. Jeong, J. G. Cho, D. W. Yoo, H. S. Lee, and G. H. Rim, "Novel zero-voltage and zero-current switching (ZVZCS) full bridge PWM converter with low output current ripple," in *Proc. Telecommunications Energy Conf. (INTELLEC'97)*, 1997, pp. 257–262.
- [6] J. G. Cho, J. W. Baek, C. Y. Jeong, D. W. Yoo, H. S. Lee, and G. H. Rim, "Novel zero-voltage and zero-current switching (ZVZCS) full bridge PWM converter using a simple auxiliary circuit," in *Proc. IEEE Appl. Power Electron. Conf.*, 1998, pp. 834–839.
- [7] E. S. Kim, K. Y. Joe, and S. G. Park, "An improved soft switching PWM FB dc/dc converter using the modified energy recovery snubber," in *Proc. IEEE Appl. Power Electron. Conf.*, 2000, pp. 119–124.
- [8] J. G. Cho, J. A. Sabate, G. Hua, and F. C. Lee, "Zero-voltage and zero-current switching full bridge PWM converter for high power applications," in *Proc. IEEE Power Electron. Spec. Conf.*, 1994, pp. 102–108.
- [9] S. J. Jeon and G. H. Cho, "Zero-voltage and zero-current switching full bridge dc–dc converter for arc welding machines," *Electron. Lett.*, vol. 35, no. 13, pp. 1043–1044, 1999.
- [10] W. McMurray and D. P. Shattuck, "A silicon-controlled-rectifier inverter with improved commutation," *IEEE Trans. Commun. Electron.*, vol. 80, pp. 531–542, 1961.
- [11] I. Barbi and D. C. Martins, "A true PWM zero-voltage switching pole with very low additional RMS current stress," in *Proc. IEEE IAS Annu. Meeting*, 1991, pp. 1228–1235.
- [12] J. A. Lambert, J. B. Vieira, L. C. Freitas, L. R. Barbosa, and V. J. Farias, "A boost PWM soft-single-switched converter with low voltage and current stresses," *IEEE Trans. Power Electron.*, vol. 13, pp. 26–35, Jan. 1998.
- [13] D. C. Martins, F. J. M. Seixas, J. A. Brilhante, and I. Barbi, "A family of dc–dc PWM converter using a new ZVS commutation cell," in *Proc. IEEE Power Electron. Spec. Conf.*, 1993, pp. 524–530.
- [14] L. R. Barbosa, J. B. Vieira, Jr., L. C. Freitas, and V. J. Farias, "An improved boost PWM soft-single-switched converter with low voltage and current stresses," in *Proc. IEEE Appl. Power Electron. Conf.*, 2000, pp. 723–728.



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