A Zero-Voltage-Switching Bidirectional DC–DC Converter With State Analysis and Soft-Switching-Oriented Design Consideration

Gang Ma, Wenlong Qu, Gang Yu, Yuanyuan Liu, Ningchuan Liang, and Wenzhong Li

***Abstract*—This paper proposes a new soft-switching bidirectional dc/dc converter. The proposed converter achieves zero-voltage switching (ZVS) for the entire main switches and zero-current switching for the rectifier diodes in the large-load range. These features reduce switching loss, voltage and current stresses, and diode reverse-recovery effect. The simple electrical isolated topology with the soft-switching characteristic provides an attractive solution for a battery charge/discharge system in an electric vehicle, distributed power system, or uninterruptible power system. This paper describes the operation principle and the ZVS condition in detail. The mathematical model based on the state-space averaging method is also deduced to depict the performance characteristic. Then, design guidelines are presented to ensure the ZVS condition for all the switches. Finally, simulation and experimental results obtained from a 1-kW prototype verify the discussed theoretical analysis.**

***Index Terms*—Bidirectional dc/dc converter, zero-current switching (ZCS), zero-voltage switching (ZVS).**

I. Introduction

RECENTLY, the worldwide energy crisis has been aggravated by the rapidly increasing economy and tremendous demand for energy. The electric vehicle and distributed power system [1]–[7] are thought to be the preferable solutions to this problem. In these applications, the fuel cell is a promising substitute replacing the conventional power source. Thus, the bidirectional dc/dc converter is the prospective choice in these applications and becomes an important topic of power electronics [7], [16], [17]. The demands of a bidirectional dc/dc converter are high frequency, high power density, high efficiency, and high reliability [2]–[8]. Nevertheless, the conventional bidirection dc/dc converters still have some drawbacks: Electric insulation and soft switching is difficult to realize, and the reverse-recovery effect of the rectifier diode restricts the switching speed. These defects limit the high-frequency power conversion applied in a bidirectional dc/dc converter [5]–[8], [11]–[13].

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G. Ma was with the National Laboratory of Power Electronics, Tsinghua University, Beijing 100084, China. He is now with the Power Grid Department, China Power Engineering Consulting Group Corporation, Beijing 100000, China (e-mail: gma@cpecc.net).

W. Qu is with the Department of Electrical Engineering, Tsinghua University, Beijing 100084, China (e-mail: qwl@mail.tsinghua.edu.cn).

G. Yu is with the China Power Engineering Consulting Group Corporation, Beijing 100000, China, and also with the Electric Power Planning and Engineering Institute, Beijing 100011, China (e-mail: gyu@cpecc.net).

Y. Liu is with the China Airport Construction Corporation of the Civil Aviation Administration, Beijing 100000, China (e-mail: liu.yuanyuan82@gmail.com).

N. Liang is with Huazhong University of Science and Technology, Wuhan 430000, China (e-mail: 1988_liang@sina.com).

W. Li is with the University of Rostock, 18057 Rostock, Germany (e-mail: wenzhong.li@med.uni-rostock.de).

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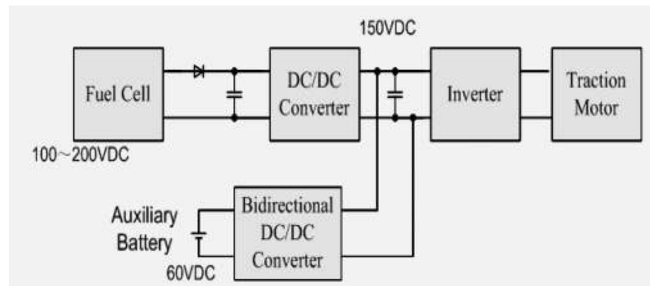

Fig. 1. Block diagram of fuel-cell electric-bus's energy-management system.

Therefore, an isolated bidirectional dc/dc converter with soft switching is the best way to meet the previously mentioned demands. Fig. 1 shows the block diagram of the fuel cell and its application system. In this system, a bidirectional dc/dc converter serves as the approach of two different electrical systems and modulates the direction and quantity of energy flow [8]–[28].

With the comparison of the unidirectional dc/dc converter, it is more difficult to achieve zero-voltage switching (ZVS) in the bidirectional dc/dc converter: more switches, more complicated switching period, and more complex energy flow [6]–[13]. Some traditional soft-switching bidirectional dc/dc converters have the following drawbacks.

The buck/boost converter's topology is simple, but its input and output sides are not electrically insulated, and soft switching is difficult to realize. In addition, the effect of diode reverse recovery cannot be neglected in the boost mode, and it restricts the switching speed of the active switch during the turn-on transient period.

As regards another important bidirectional dc/dc converter topology, the dual full-bridge converter cannot realize the soft switching in the wide load range without accessional components.

Peng *et al.* [1], [6], [15] proposed a new topology with the less-active switches than the full-bridge topology. Several new topologies have been found in the literature [1]–[4] to reduce power loss and improve efficiency. Besides, control strategy such as phase-shift control is also introduced to get the ZVS

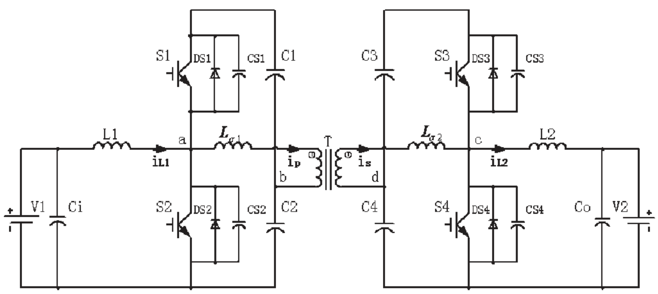

Fig. 2. Bidirectional dc/dc converter.

characteristic as in [12] and [13]. These converters can achieve ZVS for the active switches in both directions.

This paper proposes a novel bidirectional soft-switching dc/dc converter. The isolated converter achieves soft switching for both the active switch and the rectifier diode in either direction of power flow. Compared to other topologies, it can realize ZVS with the least number of active switches in the same output power. This feature reduces the volume and weight of the converter. Besides, soft switching is achieved in the larger load range without any additional component. Due to the hybrid structure in the topology, control strategy is simpler and more flexible. Therefore, these characteristics make the converter a suitable choice for the high-power conversion.

This paper presents the converter's operational principle and state analysis in detail. The mathematical model based on state-space averaging method is also depicted in Section III. Then, the parameter design guidance is introduced to ensure the soft-switching condition. Finally, a 1-kW prototype, which can be applied as the auxiliary power unit for electric vehicle and aerospace application, has been built, and experimental results are given to validate the previous analysis.

II. Operation Principle

A. Circuit Description

Fig. 2 shows the proposed converter topology.

The circuits of the primary and secondary sides are symmetrical. Upper and lower switches conduct complementally.

Upper and lower capacitors are identical. These capacitors are big enough, and the voltages across them can be regarded as constant.

Inductors L_1 and L_2 act as the important components in the energy transfer.

When power flow is transferred from V_1 to V_2, the converter works in the forward mode. The gate drive signal of S_1 is leading to that of S_3. In the reverse mode, energy transferred from V_2 to V_1; the gate drive signal of S_3 is leading to that of S_1.

In the forward mode, the primary side could be regarded as the hybrid of boost converter and half-bridge converter as shown in Fig. 3(a): S_2's duty determines the charging energy of inductor L_1 and influences the voltage across C_1 and C_2. S_1's and S_2's complementary conducting brings the capacitor's voltages of C_1 and C_2 to the primary windings and forms the ac voltage on it. As shown in Fig. 3(b), the principle of the secondary side is similar to the combination of half-bridge converter and buck converter. The secondary winding's voltage is rectified to dc voltage by D_{S3} and D_{S4}, which are the antiparallel diodes integrated in S_3 and S_4.

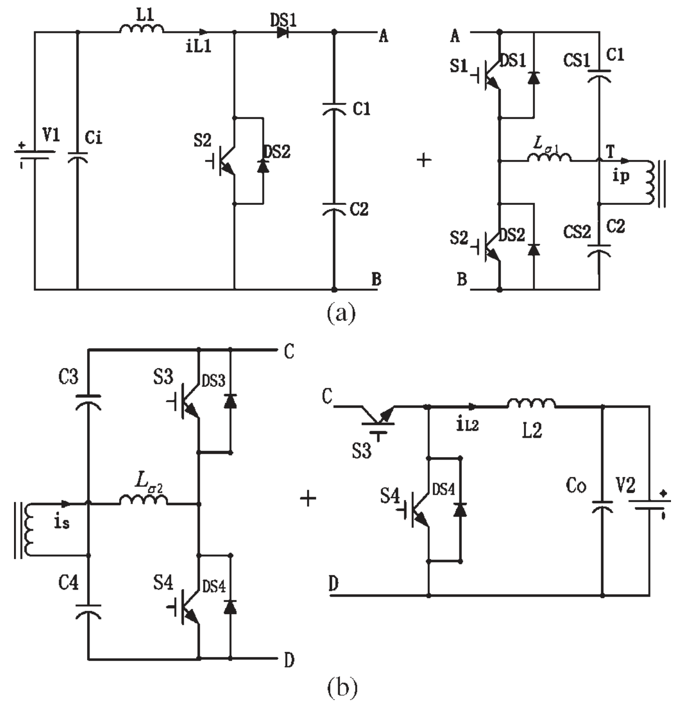

Fig. 3. Illustration of proposed bidirectional dc/dc converter. (a) Illustration of primary side. (b) Illustration of secondary side.

B. Working-Mode Analysis

According to the different control methods, the proposed converter can operate in the following two modes.

Mode 1) *Duty cycle control.* In this mode, the output voltage is modulated mainly by the duties of S_2 and S_4. The primary-side operation theory is similar to that of boost converter, and the secondary side's theory is similar to the theory of buck converter. When the duties of S_1 and S_2 are unequal, the voltages across the capacitors C_1 and C_2 will be unbalanced. This unbalance voltage will also result in the unsymmetrical voltage of the primary winding.

Mode 2) *Phase shift control.* In this mode, all the switches operate in the identical duty-approximate 50%. The output current and voltage can be regulated by the phase-shift angle between the primary and secondary voltages. The entire active switches can achieve ZVS, and all the rectifier diodes turn off with zero-current switching (ZCS). Therefore, this working mode is chosen for the proposed converter.

C. Soft-Switching Principle

The soft-switching principle of the proposed converter is described briefly as follows.

Due to the parallel capacitors, the voltage across the conducting switch cannot change suddenly, and the switch turns off with ZVS.

The resonance of the leakage inductance and the parallel capacitors, occurring in the short interval between the upper

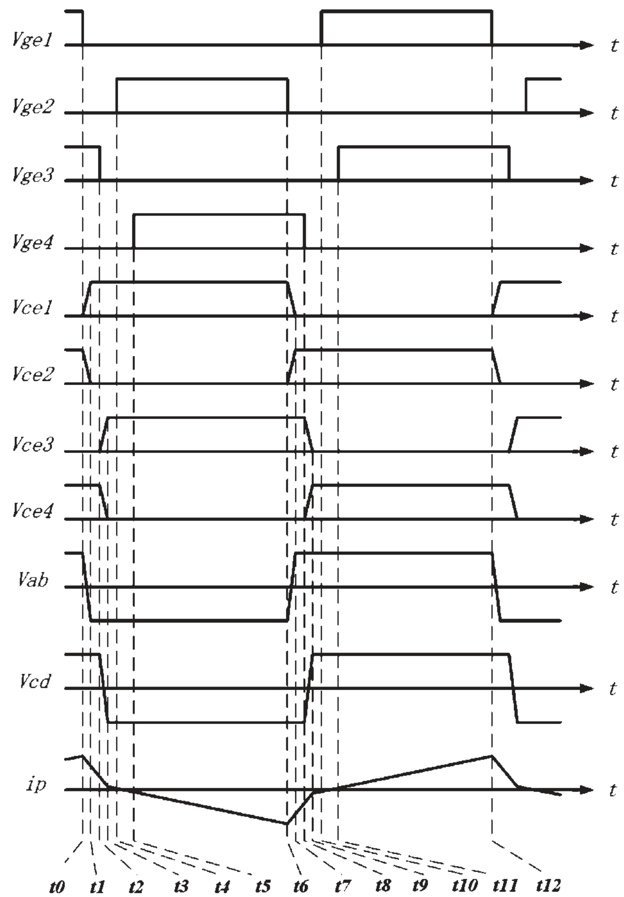

Fig. 4. Theoretical voltage and current waveforms.

and lower switches' conducting, provides the ZVS condition for turning on: when the voltage across the switch decreases to zero, the antiparallel diode begins to conduct. Then, the switch turns on with ZVS.

Similar to the earlier analysis, the switches S_3 and S_4 in the secondary windings also get their ZVS conditions by the integrated antiparallel diode's conducting. Besides, S_3 and S_4's conducting can also diminish the diode reverse-recovery effect of D_{S3} and D_{S4} by soft commutation. For example, after S_3 turns on, the current flowing through D_{S3} decreases gradually and transfers into S_3. When it decreases to zero, D_{S3} will turn off with ZCS, and the diode reverse-recovery effect will be lessened.

Due to the symmetric topology, the converter could also get soft switching in the reverse mode.

Fig. 4 shows the key waveforms of the proposed converter. V_{ce} is the voltage across C, E of switches. V_{ge} is the effective gate drive signal. V_{ab} and V_{cd} are the transformer's primary and secondary windings' voltages. i_p is the primary winding's current.

D. Operational Principles

In the forward mode, the switching cycle can be divided into 12 stages, as shown in Fig. 4. The stages are described as follows.

The converter works in steady state. Before t_0, S_1 and S_3 are conducting. The voltage across S_1 and S_3 are zero. The voltages across C_{S2} and C_{S4} are $V_1/(1-D_{S2})$ and V_2/D_{S3}. D_{S2} and D_{S3} are the duties of S_2 and S_3, respectively. For the proposed converter, the duties of every switch are identical and equal to 50%. V_1 is the input voltage. V_2 is the output voltage.

Stage 1 ($t_0 \sim t_1$): At time t_0, S_1 turns off with ZVS due to C_{S1}. Owing to the leakage inductance $L_{\alpha 1}$, the transformer primary current i_p keeps on flowing in the previous direction. During this stage, C_{S1} is charged, and C_{S2} is discharged while the voltage across C_{S2} begins to decrease

$$V_{CS1} = (i_P - i_{L1}) \cdot Z_1 \cdot \sin\left[\omega_1(t-t_0)\right]$$
$$V_{CS2} = V_1/D - (i_P - i_{L1}) \cdot Z_1 \cdot \sin\left[\omega_1(t-t_0)\right]$$

where $Z_1 = \sqrt{L_\sigma/(2 \cdot C_{CS1})}$, $\omega_1 = \sqrt{1/(2 \cdot L_\sigma \cdot C_{CS1})}$, and i_{L1} is the inductor current of L_1.

Stage 2 ($t_1 \sim t_2$): At time t_1, the voltage across C_{S2} decreases to zero; therefore, D_{S2} is forward-biased and begins to conduct. From this time, S_2 can turn on with ZVS. In this interval, inductor current i_{L1} begins to increase, and i_p begins to decrease. The transformer secondary winding's current i_s, following i_p, also decreases. The voltage's polarity of the secondary windings does not change, while the voltage across $L_{\alpha 1}$ is equal to the sum of primary winding's voltage and the voltage across C_2. T_{10} is C_{S2}'s discharging interval between t_1 and t_0. To ensure ZVS, the following conditions should be fulfilled as:

$$V_{CS2} = V_1/D - (i_P - i_{L1}) \cdot Z_1 \cdot \sin\left[\omega_1(t-t_0)\right] \leq 0.$$

Then,

$$T_{10} \geq \frac{1}{\omega_1} \arcsin\left[\frac{V_1}{D \cdot (i_P - i_{L1}) \cdot Z_1}\right].$$

Stage 3 ($t_2 \sim t_3$): At time t_2, S_3 turns off in ZVS due to C_{S3}. During this stage, C_{S3} is charged, and C_{S4} is discharged, while the voltage across C_{S4} begins to decrease

$$V_{CS3} = (i_{L2} - i_P/n) \cdot Z_2 \cdot \sin\left[\omega_2(t-t_2)\right]$$
$$V_{CS4} = V_2/D - (i_{L2} - i_P/n) \cdot Z_2 \cdot \sin\left[\omega_2(t-t_2)\right]$$

where $Z_2 = \sqrt{L_\sigma/(2 \cdot C_{CS3})}$, $\omega_2 = \sqrt{1/(2 \cdot L_\sigma \cdot C_{CS3})}$, V_2 is battery voltage in the output side, and $i_P/n(i_s)$ is the secondary winding current.

Stage 4 ($t_3 \sim t_4$): At time t_3, the voltage across C_{S4} decreases to zero; therefore, D_{S4} is forward-biased and begins to conduct. From t_3, S_4 can turn on with ZVS. The secondary winding's voltage changes its polarity, and inductor current i_{L2} begins to decrease. C_{S4}'s discharging interval between t_3 and t_2, represented by T_{32}, can be calculated as

$$V_{CS4} = V_2/D - (i_{L2} - i_P/n) \cdot Z_2 \cdot \sin\left[\omega_2(t-t_2)\right] \leq 0.$$

Then,

$$T_{32} \geq \frac{1}{\omega_2} \arcsin\left[\frac{V_2}{D \cdot (i_{L2} - i_P/n) \cdot Z_2}\right].$$

Stage 5 ($t_4 \sim t_5$): At time t_4, S_2 is triggered but does not turn on until i_{L1} is larger than i_p. Then, S_2 turns on with ZVS,

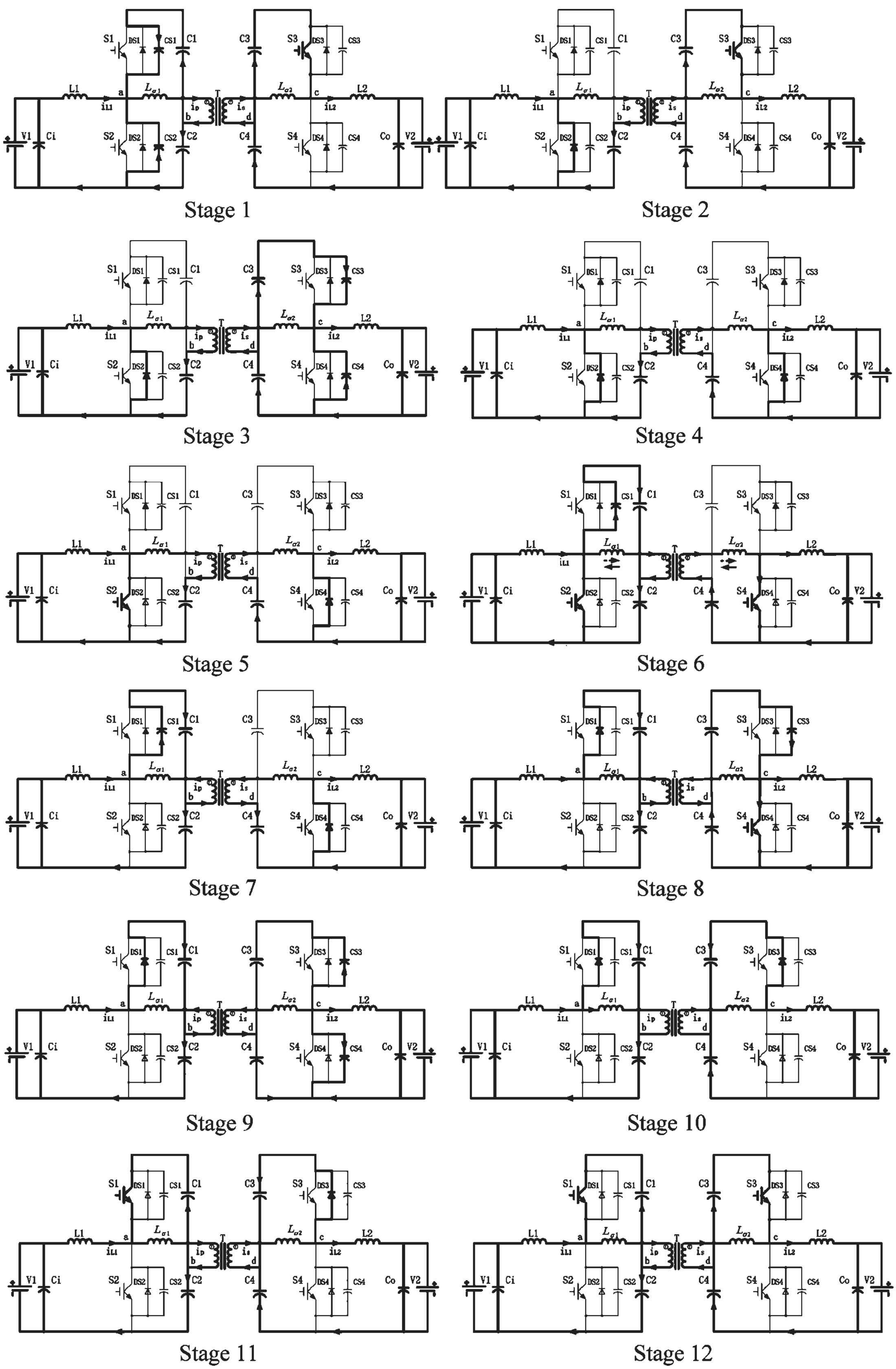

Fig. 5. Stages of operation.

and D_{S2} turns off with ZCS. When i_p decreases to zero, it changes the direction. i_{L2} changes direction at the end of this stage.

Stage 6 $(t_5 \sim t_6)$*:* At time t_5, S_4 is triggered but S_4 does not turn on. When i_{L2} is smaller than i_s, S_4 turns on with ZVS, and D_{S4} turns off with ZCS.

Stage 7 ($t_6 \sim t_7$)*:* At time t_6, S_2 turns off with ZVS due to C_{S2}. Then, C_{S2} is charged, and C_{S1} is discharged, while the voltage across C_{S1} begins to decrease

$$V_{CS2} = (i_P + i_{L1}) \cdot Z_1 \cdot \sin\left[\omega_1(t - t_6)\right].$$

Stage 8 ($t_7 \sim t_8$)*:* At time t_7, the voltage across C_{S1} decreases to zero; therefore, D_{S1} is forward-biased and begins to conduct. From t_7, S_1 can turn on with ZVS. In this interval, i_{L1} begins to decrease, and i_p begins to increase, while i_s follows i_p. The interval between t_7 and t_6 should fulfill the following condition:

$$T_{76} \geq \frac{1}{\omega_1} \arcsin\left[\frac{V_1}{D \cdot (i_P + i_{L1}) \cdot Z_1}\right].$$

Stage 9 ($t_8 \sim t_9$)*:* At time t_8, S_4 turns off with ZVS due to C_{S4}. During this stage, C_{S4} is charged, and C_{S3} is discharged, while the voltage across C_{S3} begins to decrease from V_2/D

$$\begin{aligned} V_{CS4} &= (i_{L2} - i_P/n) \cdot Z_2 \cdot \sin\left[\omega_2(t - t_8)\right] \\ V_{CS3} &= V_2/D - (i_{L2} - i_P/n) \cdot Z_2 \cdot \sin\left[\omega_2(t - t_8)\right]. \end{aligned}$$

Stage 10 ($t_9 \sim t_{10}$)*:* At time t_9, voltage across C_{S3} decreases to zero, and D_{S3} begins to conduct. From that time, S_3 can turn on with ZVS, and the secondary winding's voltage changes its polarity again. In this interval, i_{L2} begins to increase. The interval between t_9 and t_7 should fulfill the following condition:

$$T_{97} \geq \frac{1}{\omega_2} \arcsin\left[\frac{V_2}{D \cdot (i_{L2} - i_P/n) \cdot Z_2}\right].$$

Stage 11 ($t_{10} \sim t_{11}$)*:* At time t_{10}, i_p is larger than i_{L1}; then, S_1 turns on with ZVS, and D_{S1} turns off with ZCS.

Stage 12 ($t_{11} \sim t_{12}$)*:* At time t_{11}, secondary winding's current (i_s) is lower than i_{L2}, so S_3 turns on with ZVS, and D_{S3} turns off with ZCS. A complete period is over.

Fig. 5 shows the stages of the operation.

The operation principle of the reverse mode is similar to that of the forward mode.

E. Comparison With Other Topology

The left part of the proposed converter is similar to that of the converter in [1]. However, the topology in the right part and the operation principle are quite different. These features bring some additional merits as follows.

1) The proposed converter can achieve ZVS in the wide load range.
2) Provide ZVS for all the switches both in the resistance load and in the battery load.
3) Provide ZCS for all the rectifier diode and lessen the diode reverse-recovery effect.

Due to the earlier characteristics, the proposed converter becomes a more feasible choice for all kinds of load in the wider load range.

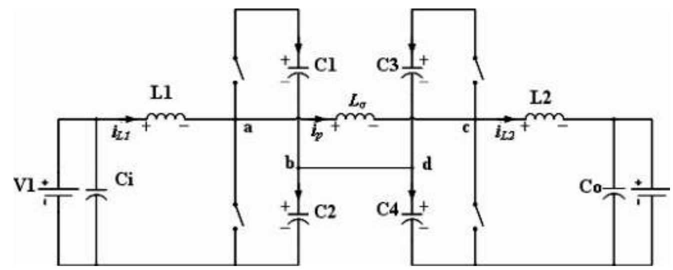

Fig. 6. Primary-referred equivalent circuit.

III. Theoretical Analysis and Mathematical Model

To simplify analysis, the primary-referred equivalent circuit is shown as Fig. 6, where the transformer is replaced by the leakage inductance and the parameters of the secondary side are converted to the primary side.

According to circuit theory, the voltage–second of inductor and ampere–second of capacitor in one period are all zero in the steady state. It means that, in one period, we have the following conditions.

1) The average voltages across the leakage inductance, transformer primary, and secondary windings are all zero.
2) The average voltages across L_1 and L_2 are both zero.

Then, one period can be divided into four modes according to the different switch states, as shown in Figs. 7 and 8.

A. Steady-State Analysis

The steady-state analysis consists of output characteristic and ZVS condition. To simplify the control strategy, the proposed converter operates in the phase-shifted mode with the fixed duty (50%) of every switch. Based on earlier analysis, the output characteristic can be simplified as

$$I_2 = \frac{\Delta\phi(\pi - \Delta\phi)V_1}{\pi\omega L_\sigma}. \tag{1}$$

As shown in Fig. 8, Φ is equal to π, and $\Delta\Phi$ denotes the angle between the arising sides of two voltage waveforms. L_α is the sum of $L_{\alpha 1}$ and $L_{\alpha 2}$. P_2 is the output power. I_2 is the output current of the converter. The transformer primary current i_p can also be expressed as

$$\begin{cases} i_p(0) = -\frac{\pi}{2\omega L_\sigma}V_1 - \frac{2\Delta\phi-\pi}{2\omega L_\sigma}V_2 \\ i_p(\Delta\phi) = \frac{(2\Delta\phi-\pi)}{2\omega L_\sigma}V_1 + \frac{\pi}{2\omega L_\sigma}V_2 \\ i_p(\pi) = \frac{\pi}{2\omega L_\sigma}V_1 + \frac{2\Delta\phi-\pi}{2\omega L_\sigma}V_2 \\ i_p(\pi+\Delta\phi) = -\frac{(2\Delta\phi-\pi)}{2\omega L_\sigma}V_1 - \frac{\pi}{2\omega L_\sigma}V_2. \end{cases} \tag{2}$$

B. ZVS Condition of Different Switches

The ZVS condition can be deduced on the precondition that the antiparallel diode of switch should conduct before the switch is triggered.

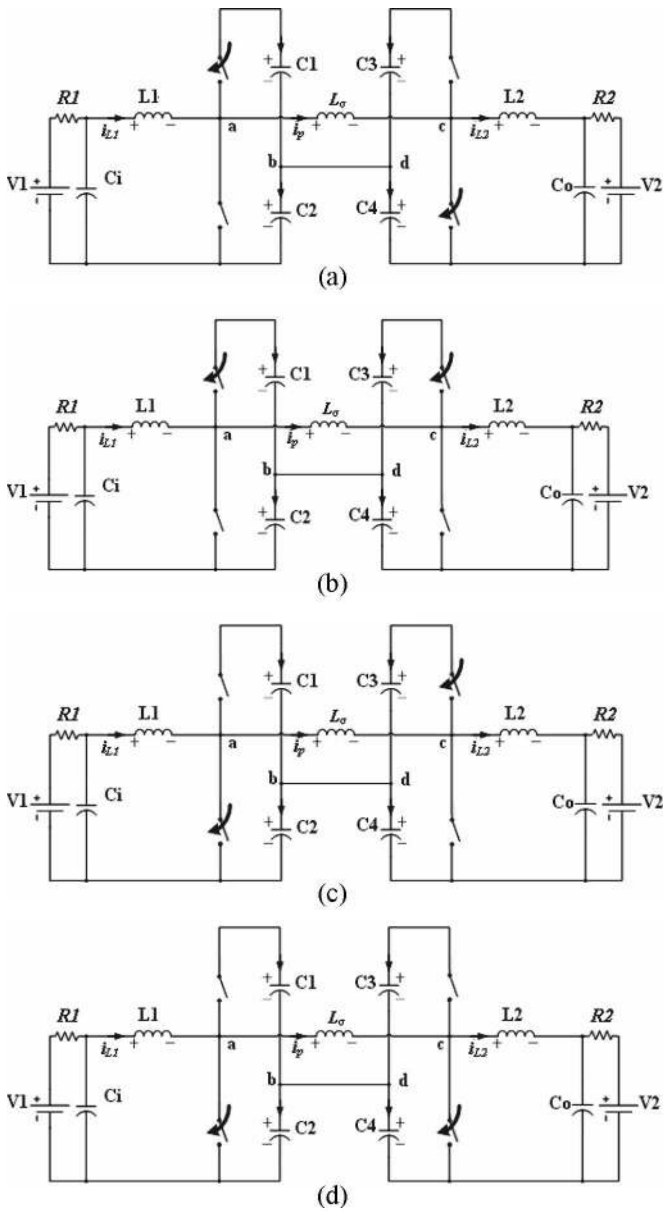

Fig. 7. Four modes in one period. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4.

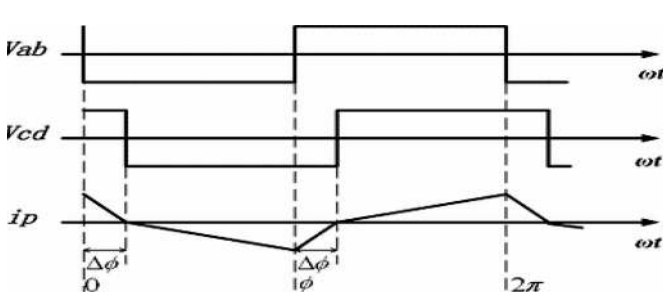

Fig. 8. Idealized transformer voltage and primary current waveform.

Then, the ZVS conditions of the four switches can be drawn as follows:

1) for S_1: $i_p(0) < i_{L1}(0)$;
2) for S_2: $i_p(\Phi) > i_{L1}(\Phi)$;
3) for S_3: $i_p(\Delta\Phi) > i_{L2}(\Delta\Phi)$;
4) for S_4: $i_p(\Phi + \Delta\Phi) < i_{L2}(\Phi + \Delta\Phi)$.

With the high-order terms of $\Delta\Phi$ in the equation neglected, the simplified ZVS condition can be expressed as

$$\frac{L_2}{L_2 + L_\sigma} < \frac{V_2}{V_1} < \frac{L_1 + L_\sigma}{L_1}. \tag{3}$$

All the parameters' values are primary referred. The specialization of the converter given in Section V satisfies (3) and meets the ZVS condition. Therefore, it is concluded that the ZVS conditions can be ensured with the suitable value of L_1 and L_2.

IV. Design Consideration

According to the earlier analysis, the output current is modulated by the phase-shift angle. Then, the output voltage can also be regulated by the phase-shift angle. Consequently, output characteristic can also be expressed as

$$V_2 = \frac{2\omega L_\sigma}{\pi \cdot (\pi - \Delta\phi)} \cdot \frac{P_2}{V_1}. \tag{4}$$

The control unit is based on the TMS320F240. The DSP chip not only generates pulsewidth modulation to regulate the output voltage but also provides other functions including soft start, fault alarm, and various fault protections. Furthermore, the advanced control strategy can be easily introduced into the control algorithm in virtue of the powerful digital-processing capability.

A. Design of Inductor

The inductors play an important part in energy transfer as well as in the implementation of soft switching. Their values should be determined synthetically: very small inductance will result in discontinuous current. However, very large inductance will influence the ZVS condition. Take L_2 for example.

In the previous analysis, L_2 is thought to be large enough to ensure the power supply as a current source. The inductance cannot be too large because of the limitation of volume, weight, and power loss. Hence, the ripple of the output current cannot be neglected. Furthermore, very large value of L_2 will influence the period of D_{S1}'s conducting and result in S_1 losing the ZVS condition. The reason is as follows.

Due to the transformer leakage inductance, when S_2 turns off, the primary winding current will keep its former direction. The sum of i_{L1} and i_p flows through D_{S1} and charges C_1. During this period, the secondary winding current flows through D_{S4} in the former direction, and i_{L2} also freewheels through D_{S4}.

The voltage across the leakage inductance is the sum of V_{C1} and V_{C4}/n. V_{C4}/n is V_{C4} converted to transformer primary side, and n is the turn ratio of transformer. Because the voltage across L_α is large, the primary winding current changes its direction rapidly and increases in the opposite direction. As soon as i_p is equal to i_{L1}, the current flowing through D_{S1} will decrease to zero, and D_{S1} will cease conducting. If the gate drive signal is still not sent at this moment, the voltage across S_1 will increase, and S_1 will lose the ZVS condition.

To ensure the ZVS condition of S_1, the interval between the gate drive signals of S_2 and S_1 should be lessened. Hence, the gate drive signal of S_1 is required to be given before the primary winding current increases to the value of i_{L1}. However, the very short interval between the drive signals of S_1 and S_2 will endanger the safe operation of insulated-gate bipolar transistors (IGBTs). Furthermore, as D_{S4} turns off by a certain reverse voltage, the reverse-recovery effect of D_{S4} cannot be ignored.

On the other hand, the suitable value of L_2 could guarantee i_{L2} decreasing to zero after S_2 turns off. When i_{L2} drops to zero, D_{S4} will cease conducting. Both the primary and secondary windings' voltage will change the polarity gradually, and the voltage across the leakage inductance will decrease, changing from $V_{C1} + V_{C4}/n$ to $V_{C1} - V_{C3}/n$. Therefore, the changing rate of primary winding current will be reduced, and the interval of D_{S1}'s conducting will be prolonged. Thus, the wider ZVS condition for S_1 is created.

The value of L_2 can be calculated as follows:

$$\begin{aligned} i_{L2\min} &= I_{\text{av}} - \frac{1}{2}\Delta i_{L2} \\ &= \frac{P_2}{V_2} - \frac{P_2}{V_2} \cdot \frac{(1-D)T_s R}{2L_2} \\ &= \frac{P_2}{V_2}\left(1 - \frac{1-D}{2\tau_{L2}}\right) \end{aligned} \tag{5}$$

$$\tau_{L2} = \frac{L_2}{R \cdot T_S} \tag{6}$$

$$i_{L2\min} \leq 0. \tag{7}$$

Substituting (5) and (6) into (7), the requirement of L_2 is deduced as

$$L_2 \leq \frac{R \cdot T_S \cdot (1-D)}{2}. \tag{8}$$

In the above formulas, P_2 is the output power, and I_{av} is the average output current. Δi_{L2} is the output-current ripple. D is the duty cycle of the switch, while T_s is the switching period. $i_{L2\min}$ is the minimum of inductor current i_{L2}. The analysis is based on the condition of resistance load, and R is the load resistance. As for other kinds of load, the requirement of the inductor can be expressed as

$$L_2 \leq \frac{V_2^2 \cdot T_S \cdot (1-D)}{2 \cdot P_2}. \tag{9}$$

Substituting the specification (given in Section V) into (9), the requirement of inductor L_2 can be calculated as

$$L_2 \leq \frac{V_2^2 \cdot T_S \cdot (1-D)}{2 \cdot P_{2\text{MAX}}} = \frac{144^2 \cdot 50 \cdot 0.5}{2 \cdot 1500} = 172.8\ \mu\text{H}.$$

In terms of the above design procedure, the converter can achieve the ZVS condition in the large-load range. Besides, D_{S4} softly turns off due to the current decreasing to zero and avoids diode reverse recovery.

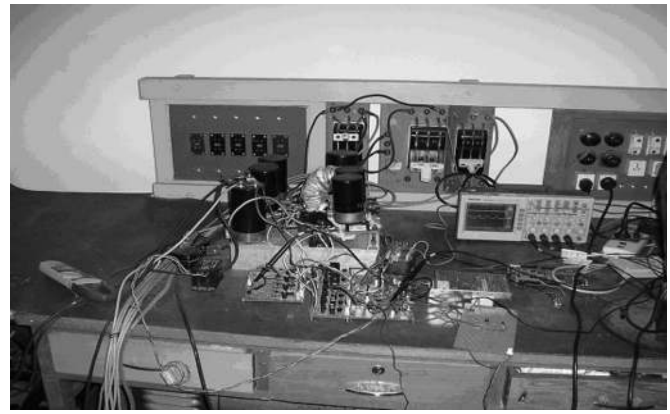

Fig. 9. Photograph of the prototype.

TABLE I
PARAMETERS OF THE PROTOTYPE

Parameters	Symbol	Value
Input voltage	V_1	60 Vdc
Output voltage	V_2	144 Vdc
Rated power	P_2	1000 W
Maxim Power	P_{2Max}	1500 W
Transformer turn ratio	n	2:5
Input inductor	L_1	138μH
Output inductor	L_2	98μH
Leakage inductance	$L_{\sigma 1}$	4μH
Switching frequency	f	20 kHz
Primary switches	S_1, S_2	CM150DY-12H
Secondary switches	S_3, S_4	CM150DY-12H
Parallel capacitance	$C_{S1}, C_{S2}, C_{S3}, C_{S4}$	1μF

B. Design of Dead Time

As explained in the theoretical principle, the duties of the main switches are identical and equal to 0.5. In the practical applications, there should be a blank interval between the drive signals of the switches to prevent the accidental short circuit of power source. This interval is also called dead time.

The dead time of the proposed converter is decided by the following two factors.

1) The interval should be long enough to ensure the safe operation: when the upper (lower) switch begins to turn on, the current in the lower (upper) switch of the same leg must have decreased to zero and turned off for certain.
2) The interval should not affect the soft-switching condition. The detail analysis could be referred in [8]. Therefore, the value of dead time should be decided by both the safe operation and the ZVS condition. Synthetically, the dead time of the proposed converter is deduced as 4 μs.

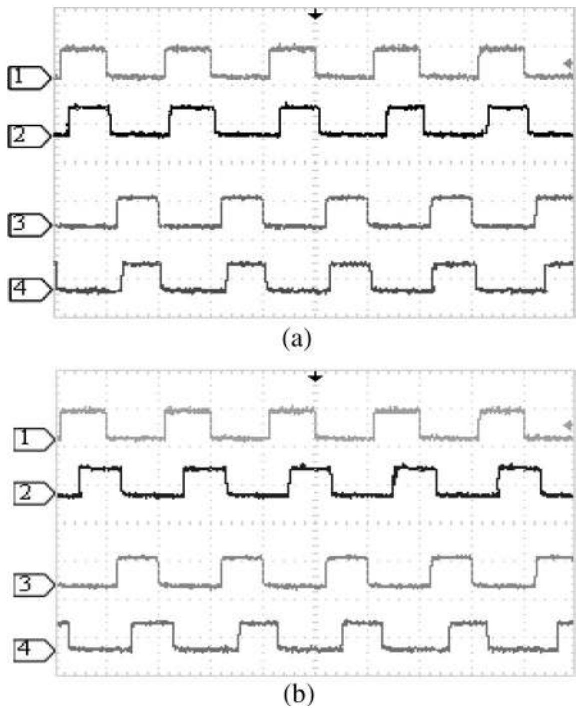

Fig. 10. Waveform of gate drive signal. (a) Gate drive signal in light load. (b) Gate drive signal in heavy load. V_{ge1}: [Ch1: 20 V/div], V_{ge2}: [Ch3: 20 V/div], V_{ge3}: [Ch2: 20 V/div], V_{ge4}: [Ch4: 20 V/div], Time base: 25 μS/div.

C. Design of Parallel Capacitance

Parallel capacitance could help the switch get the zero-voltage turning off. It also influences the zero-voltage turning on. Take the turning-on period of S_2 as an example.

The soft-switching condition of S_2 is that, during the parallel capacitance's discharging interval, the voltage across S_2 decreases to zero, and the antiparallel diode D_{S2} conducts before the gate drive signal V_{ge2} is given. If the capacitance C_{S2} is very large, the discharging period will end after the gate drive signal is given and the zero-voltage turning-on condition is lost.

From the detail operational principle of Stages 2 and 3, the restriction can be deduced as

$$T_d \geq T_{10} \geq \frac{V_1 \cdot 2C_{S2}}{D \cdot (i_p - i_{L1})} \tag{10}$$

where T_d is dead time and equal to 4 μs. The difference between T_{10} and T_d can be neglected. With T_d substituted into (10), the range of parallel capacitance C_{S2} is confined as

$$C_{S2} \leq \frac{(i_p(t_1) - i_{L1}) \cdot D \cdot T_d}{2V_1} \leq \frac{(i_p(t_2) - i_{L1}) \cdot D \cdot T_d}{2V_1}. \tag{11}$$

In terms of the above simplification, the primary current at t_2 can be calculated as

$$i_p(t_2) = i_p(\phi_1) = \frac{2\Delta\phi - \pi}{2\omega L_\sigma} V_1 + \frac{\pi}{2\omega L_\sigma} V_2. \tag{12}$$

For the stability of the proposed converter, the maximum of phase-shift angle is restricted as $\pi/4$. Then, substituting the

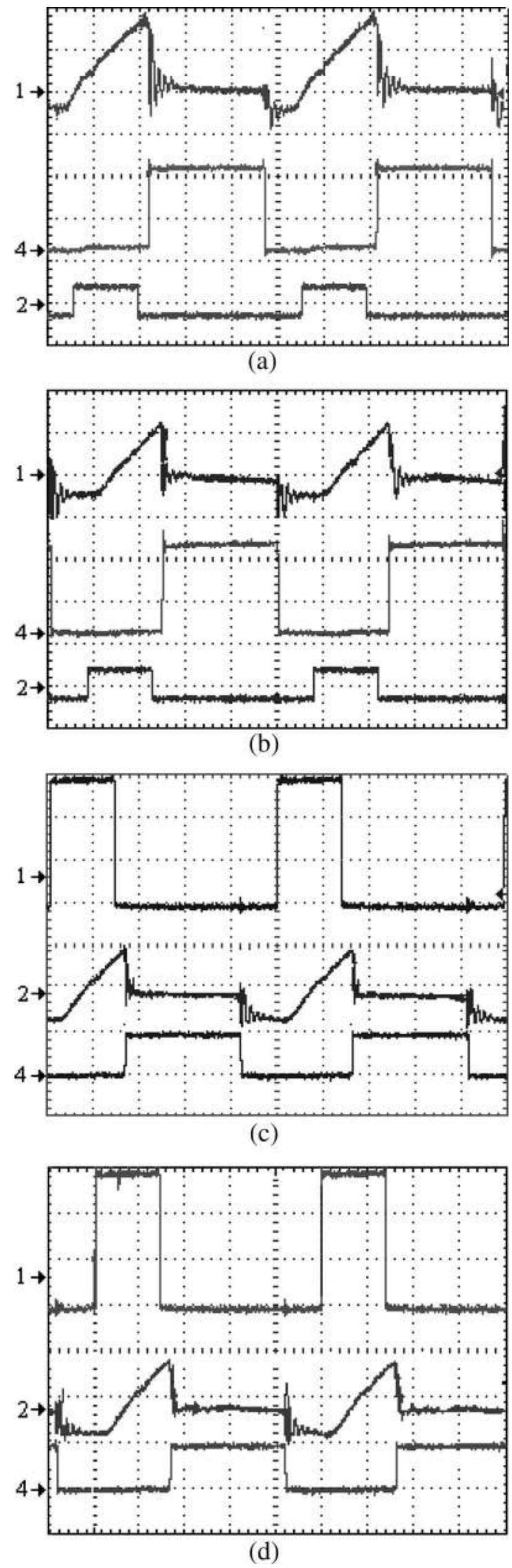

Fig. 11. Collector–emitter voltage V_{ce}, collector current I_{DS}, and gate drive signal V_{ge} of switches in heavy load (P_2: 900 W). (a) S_1: I_{DS1}: [Ch1: 20 A/div], V_{ce1}: [Ch4: 20 V/div], V_{ge1}: [Ch2: 20 V/div]. (b) S_2: I_{DS2}: [Ch1: 20 A/div], V_{ce2}: [Ch4: 20 V/div], V_{ge2}: [Ch2: 20 V/div]. (c) S_3: V_{ge3}: [Ch1: 5 V/div], I_{DS3}: [Ch2: 20 A/div], V_{ce3}: [Ch4: 100 V/div]. (d) S_4: V_{ge4}: [Ch1: 5 V/div], I_{DS4}: [Ch2: 20 A/div], V_{ce4}: [Ch4: 100 V/div]. Time base: 10 μS/div.

specification into (12), $i_p(t_2)$ can be drawn as

$$i_p(t_2) \leq i_p\left(\frac{\pi}{4}\right) = \frac{2\Delta\phi - \pi}{2 \cdot 2\pi \cdot f \cdot L_\sigma} 60 + \frac{\pi}{2 \cdot 2\pi \cdot f \cdot L_\sigma} \frac{144}{2.5} = 86.25 \text{ A}.$$

The minimum of i_{L1} can be calculated by

$$i_{L1} = I_{\text{av}} = \frac{P_2}{V_1 \cdot \eta} \tag{13}$$

where P_2 is output power and η is the efficiency.

With the parameters substituted into the earlier equation, the maximum of C_{S2} is equal to 1.4 μF.

In the specifications of IGBT, parallel capacitance is much less than the maximum of C_{S2} and ensures the ZVS condition.

V. Experimental Verification

A prototype of soft-switching bidirectional dc/dc converter has been built to verify the earlier analysis.

Due to laboratory constraints, IGBTs are chosen as the main switches. In the future, MOSFETs, which are more suitable for the proposed type of soft switching, will be chosen as the main switches in the next-generation prototype.

The prototype is shown in Fig. 9, and its specification is given in Table I.

Fig. 10(a) and (b) shows the waveforms of gate drive signal in different loads. It shows that the phase-shift angle between V_{ge1} and V_{ge3} depends on the load: In light load, the phase-shift angle is small; in heavy load, the phase-shift angle becomes bigger. These results coincide with the output characteristic depicted by (1).

Fig. 11 shows experimental waveforms in 900-W output power, including collector current, gate drive signal, and V_{ce} of each switch, respectively. I_{DS} is the current flowing through the switch, including the IGBT and its antiparallel diode. It shows that the current transfers from the antiparallel diode to the IGBT in the commutation period. The voltage waveforms demonstrate that the voltage across those switches decreases to zero before the gate drive signal is given. These experimental results testify that the switch gets its ZVS condition at heavy load.

In Fig. 12, the experimental results of zero-voltage turn on in 15-W output power are shown. Similar to Fig. 11, Fig. 12 shows gate drive signal and V_{ce} of each switch, respectively. The collector-emitter voltage decreases to zero before the switch gets the gate drive signal. It demonstrates that the switch realizes ZVS in the light load. Both Figs. 11 and 12 prove that switches can achieve ZVS in different output power.

Fig. 13(a) and (b) shows the waveforms when L_2 is 98 μH and 238 μH, respectively, and shows that the different value of inductor L_2 will affect the interval of D_{S1}'s conducting. In Fig. 13(a), S_1 turns on with ZVS. Fig. 13(b) shows that D_{S1} would turn off ahead because of the bigger inductor L_2. Thus, it endangers the ZVS condition of S_1. The waveform verifies the validity of the design consideration.

Fig. 14 shows the efficiency of the proposed converter and that of a hard-switching half-bridge converter with the same parameters. Curve "*" is the efficiency of the proposed one, and the lower curve is that of half-bridge converter. Compared

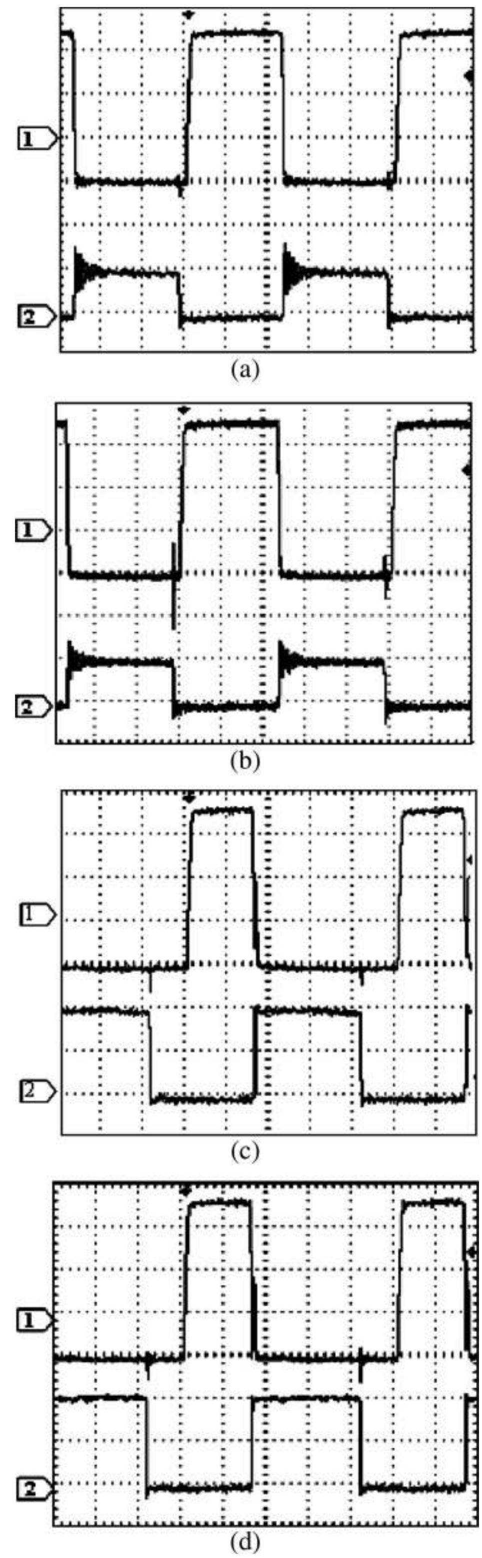

Fig. 12. Collector–emitter voltage V_{ce} and gate drive signal V_{ge} of switches in light load (P_2: 15 W). (a) S_1: V_{ge1}: [Ch1: 5 V/div], V_{ce1}: [Ch2: 50 V/div]. (b) S_2: V_{ge2}: [Ch1: 5 V/div], V_{ce2} [Ch2: 50 V/div]. (c) S_3: V_{ge3}: [Ch1: 5 V/div], V_{ce3}: [Ch2: 50 V/div]. (d) S_4: V_{ge4}: [Ch1: 5 V/div], V_{ce4}: [Ch2: 50 V/div]. Time base: 10 μS/div.

with loss of the switches, the power loss of the inductors cannot be neglected at light load. Therefore, the proposed converter's efficiency is a bit lower than that of the hard-switching converter at light load. With load increasing, the ratio

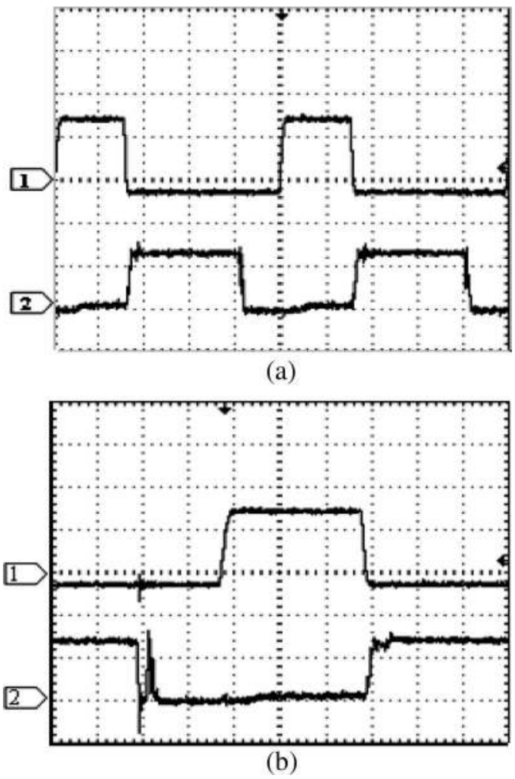

Fig. 13. Collector–emitter voltage V_{ce} and gate drive signal V_{ge} of S_1 with different L_2. (a) $L_2 = 98\ \mu$H, V_{ge1}: [Ch1: 10 V/div], V_{ce1}: [Ch2: 50 V/div], Time base: 10 μS/div. (b) $L_2 = 238\ \mu$H, V_{ge1}: [Ch1: 10 V/div], V_{ce1}: [Ch2: 50 V/div], Time base: 5 μS/div.

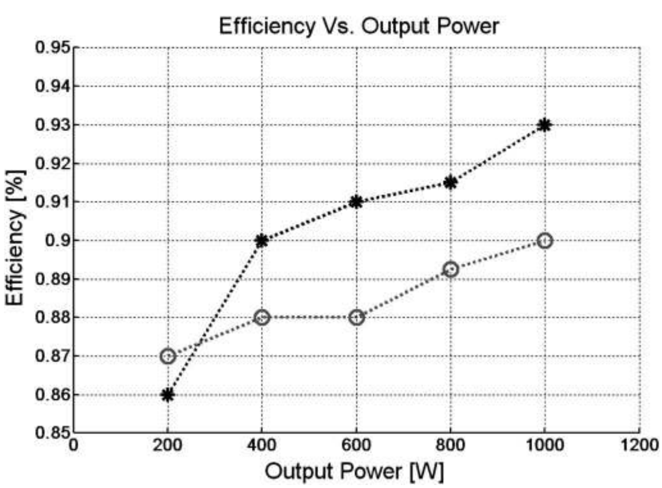

Fig. 14. Efficiency chart.

of the inductors' loss to the switches' loss decreases dramatically, and the inductors' loss is negligible. Then, the efficiency of the proposed converter is higher than that of the hard-switching converter. The comparison illustrates that the efficiency of the proposed topology is about 2% higher from half-load to full-load condition.

VI. Conclusion

This paper has proposed a novel bidirectional dc/dc converter. It has attractive features including simple topology, small number of switches, and flexible control strategy. Moreover, it achieves ZVS for the entire active switches and soft commutation for the rectifier diode over a wide load range in terms of the proposed design consideration. Consequently, the power loss is reduced, and the diode reverse-recovery problem is solved. In addition, it seems more attractive in the high-power applications, and the efficiency can be higher with the suitable main switches. The experimental results demonstrate the validity of the theoretical analysis.

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Gang Ma received the B.S. and M.S. degrees in electrical engineering from North China Electric Power University, Hebei, China, in 1997 and 2000, respectively, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, in 2007.

From 2000 to 2003, he was with the Electric Vehicle Research Center, Institute of Electrical Engineering, Chinese Academy of Sciences, Beijing, where he worked on developing soft-switching power converter for fuel-cell electric vehicles and motor-drive applications. In 2003, he was with the National Laboratory of Power Electronics, Tsinghua University, where he worked on high-efficiency dc–dc converter. He is currently an Engineer with the Power Grid Department, China Power Engineering Consulting Group Corporation, Beijing. His research interests include soft-switching converters, HVdc, modeling and simulation of power-electronic systems, and applications of power electronics.

Wenlong Qu was born in Shanghai, China, on February 6, 1946. He received the B.S. degree in electrical engineering from Tsinghua University, Beijing, China, in 1970.

Since 1970, he has been teaching in the Department of Electrical Engineering, Tsinghua University, where he is currently a Professor. He teaches courses on power electronics. He is the author of more than 70 technical papers on power electronics and motor control. He is the holder of several patents. His research interests include ac and dc motor control, dc–dc converters, soft-switching techniques, electric-vehicle drives, and power-steering-system control.

Gang Yu was born in Shandong Province, China, on January 24, 1961. He received the B.S. degree in electrical engineering from Shandong University, Shandong, China, in 1982, the M.S. degree in electrical engineering from China Electric Power Research Institute, Beijing, China, and the Ph.D. degree in electrical engineering from Tsinghua University, Beijing, in 2007.

From 1982 to 1998, he was with the WeiFang Electric Power Bureau, as Senior Engineer, Deputy Director, and, finally, as Director-in-Chief. From 1998 to 2002, he was the General Manager of the China Power Engineering Consulting Group Corporation, Beijing, where since 2003, he has been a Vice-President. He is currently also the Vice-Director-in-Chief of the Electric Power Planning and Engineering Institute, Beijing. Since 1982, he has been conducting research on power engineering. He has published more than 30 papers. His research interests include testing and detecting technology of power equipment, ultrahigh-voltage ac-transmission projects, substation grounding, HVdc, and applications of power electronics.

Dr. Yu is a Senior Member of the Chinese Society for Electrical Engineering. He serves as the Director of the Power Transmission Study Committee and as Vice-Director of the Engineering Economic Study Committee.

Yuanyuan Liu received the B.S. and M.S. degrees in electrical engineering from Tsinghua University, Beijing, China, in 2005 and 2007, respectively.

In 2005, she was with the National Laboratory of Power Electronics, Tsinghua University, where she worked on high-efficiency dc–dc converters. She is currently an Engineer with the China Airport Construction Corporation of the Civil Aviation Administration, Beijing. Her research interests include soft-switching converters, modeling and simulation of power-electronic systems, and applications of new power semiconductor devices.

Ningchuan Liang was born in Wuhan, China, on January 28, 1988. He is currently working toward the B.S. degree in electrical engineering at Huazhong University of Science and Technology, Wuhan.

His research interests include power systems and automation, soft-switching converters, motor drive control, and modeling and simulation of power systems.

Wenzhong Li received the B.S. and M.S. degrees from Nanjing University of Aeronautics and Astronautics, Nanjing, China, in 1991 and 1994, respectively, and the Ph.D. degree from the National University of Singapore, Singapore, in 2005.

He is currently a Research Fellow with the University of Rostock, Rostock, Germany. He is the author of dozens of technical papers and is the holder of several patents. His research interests include magnetic-nanoparticle-based applications for regenerative medicine, the design and fabrication of the microelectromechanical systems for biomedical applications, and mechanical and electrical integration.