ABILBO: Analog BuILt-in Block Observer[*]

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Abstract

This paper presents a novel multifunctional test structure called Analog BuILt-in Block Observer (ABILBO). This structure is based on analog integrators and achieves analog scan, test frequency generation and test response compaction. A high fault coverage was obtained by using a discrete switched-capacitor ABILBO for testing a biquad filter. The ABILBO area overhead and performance penalty can be very low if functional and testing circuitry are shared. This is typically the case of high order filters based on a cascade of biquads.

1. Introduction

With the advances on analog-digital integrated circuits (ICs), faster and more complex test equipments are needed to meet ever more demanding test specifications. Mixed-signal testers with demanding requirements of speed, precision, memory and noise are very expensive. These testers include circuitry such as precision programmable analog signal generators, waveform digitisers, and specialised digital signal processing hardware.

An attractive alternative to cope with testing issues is to move some or all of the tester functions onto the chip itself or onto the board on which the chips are mounted. The use of built-in self-test (BIST) for high volume production of mixed-signal ICs can reduce the cost per chip during production-time testing and can help to perform diagnosis in the field.

Research on digital BIST has led in the past to the proposal of multifunctional structures capable of scanning test data, generating test patterns and compacting test responses. These structures were called built-in logic block obserservers (BILBOs) [1]. In the realm of analog circuits, some few works have recently presented isolated structures for either scanning analog signals [2,3], or generating test signals [4,5,6,7], or analysing circuit responses [4,8,9,10], but not all. In order to recreate the digital BILBO versatility in the analog domain, a novel multifunctional BIST structure is proposed in this work for use in analog systems. It is called analog built-in block observer (ABILBO).

This paper is organised as follows. The ABILBO structure is described in section 2. Section 3 presents experimental results. In section 4 the integration of the

ABILBO structure at the system level is discussed by means of an example. Finally, section 5 concludes the paper.

2. Analog BILBO
2.1. Test paradigm and general structure

Some of the analog BIST works mentionned above are based on functional, other on fault-based tests. Everyone incurs different costs in terms of hardware overhead, test application time and performance penalty. They have all their own scope of suitable applications.

This specific work is based on a fault-based strategy for AC-testing of filters. An automatic tool is run in order to determine a minimum set of testing measures and frequencies that guarantee the maximum coverage of a predefined set of catastrophic and/or parametric faults of the circuit under test [11]. Although only single-tone signals are used, the test application time is expected to be rather short, since very few frequencies are usually required for fully testing analog filters [11]. Besides this, as shown in [6], the use of multitone signals may lead to a loss on fault coverage when compared to the original set of single-tones.

All the features above, associated to the ability of scanning signals and generating and compacting analog AC-tests using the same hardware resources, have led to the proposal of a novel multifunctional BIST structure - called analog built-in block observer (ABILBO). Because the switched-capacitor (SC) technique is suitable for the integration of analog circuits and can provide easy programmability of time constants, it is used for illustrating the general idea of a flexible BILBO structure for use in analog systems.

Basically, the ABILBO structure is made up of two analog integrators and some additional circuitry (figure 1). Since integrators have duplicated input stages [3], the operational amplifiers can work as voltage followers and then perform analog scan operations (mode1). With the operational amplifiers in the normal mode, switches can be programmed such that either a sinewave oscillator (mode2), or a double-integration signature analyser (mode3) results. Both integrators can be reset by shorting their integration capacitors (mode4). Table 1 draws an analogy between the digital and the analog BILBO structures. Modes 2 and 3 are further discussed in the following sections.

2.2. Programmable sinewave oscillator

A quadrature oscillator is obtained if mode2 is selected in the ABILBO structure below. This oscillator is based on two integrators connected in a ring configuration. A 360° phase shift is ensured because the first integrator is inverting and the second one is non-inverting.
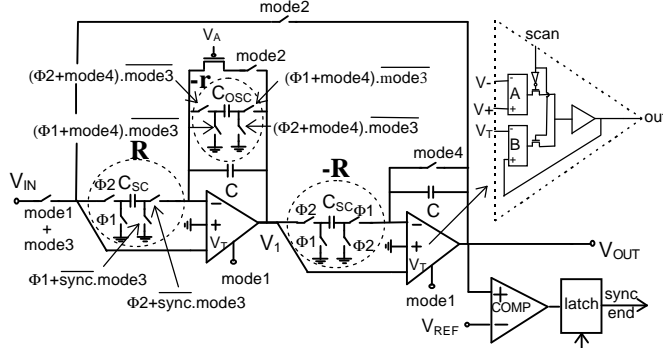

Figure 1. A switched-capacitor ABILBO.

features	digital BILBO	analog BILBO
test paradigm	pseudorandom	fault-based, single-tone
building blocks	registers	integrators
test mode 1	scan	voltage follower
test mode 2	test pattern generation	sinewave oscillator
test mode 3	signature analysis	double-integrator
test mode 4	reset	capacitor discharge

Table 1. Analogy between digital and analog BILBO.

Since the value of the SC resistors in the oscillator is given by $R = \dfrac{1}{f_{CK}.C_{SC}}$, where ϕ_1 and ϕ_2 correspond to the two phases of f_{CK}, an oscillation frequency of $f_{osc} = \dfrac{f_{CK}.C_{SC}}{2\pi C}$ is obtained. The generation of a new test stimulus in the ABILBO structure is thus achieved by changing the clock frequency, while in the digital BILBO just a new clock cycle is needed.

The negative SC resistor **r** in figure 1 results in a positive feedback which ensures circuit instability and a faster growth in the amplitude of the oscillations. Voltage limitation preserving signal symmetry is achieved by using a MOS transistor in parallel with the local feedback branch of the first integrator. The reference voltage at the comparator input in figure 1 (V_{REF}) is made equal to analog ground in the ABILBO oscillator mode. The latch at the output of the comparator allows for easy synchronisation of the test signal generator with the response measurement circuit (signal sync).

2.3. Double-integration signature analyser

A test response compactor is obtained if mode3 is selected in the ABILBO structure. This signature analyser is based on two pure integrators connected in a chain configuration. A signature can be obtained by computing the time for the output of the second integrator to reach a predefined V_{REF}. Since a counter is used for computing digital signatures, counting must be enabled from the integration start up to the time when the comparator output and the signal end (latch output) go high.

Assuming $V_{IN}= -V_0\sin(\omega t+\varphi)$ and $V_{C|t=0}=0$ for the SC double-integration signature analyser, it can be shown that:

$$V_1 = \frac{V_0}{\omega\tau}\left[\cos\varphi - \cos(\omega t + \varphi)\right] \qquad [1]$$

$$V_{OUT} = \frac{V_0}{(\omega\tau)^2}\left[-\sin(\omega t + \varphi) + \omega t.\cos\varphi + \sin\varphi\right] \qquad [2]$$

where $\tau = RC = \dfrac{C}{f_{CK}.C_{SC}}$.

Figure 2(a) shows the effect of the integration of a signal with V_0=1V, f=500Hz, and τ=0.8ms, considering φ=0. Having fixed V_{REF} at +4V and τ at 0.1ms, figure 2(b) gives the time required to reach V_{REF} for the frequency band of operation and different values of V_0. Figure 2(c) gives the time required to reach V_{REF} for the input voltages of operation at different frequencies. In general, it can be seen that signals having different frequencies and voltage amplitudes will require a different time to reach V_{REF}.

Let us now consider phase shift effects. In the case that φ=0, V_{OUT} given by equation [2] is a monotonically increasing function. In the case that φ>0, V_{OUT} is no longer monotonically increasing and the testing times are longer than for φ=0. This is shown in figure 2(d), which also shows that phase deviations can be detected.

It is clear that a maximum integration time T_{max} must exist since some signals may require excessively long times and lead to time counting overflows. T_{max} and V_{REF} limit the input space of signals, together with τ. Figure 2(e) shows the valid input space for the frequency band and input voltages of operation for V_{REF}=4V, T_{max}=5ms and with different values of τ. For example, for τ=0.1ms, all signals underneath the curve will not leave a valid signature; all signals above the curve leave a valid signature.

Contrarily to the digital BILBO, in the ABILBO structure test compaction is performed on each individual circuit response. Nevertheless, signal amplitude, frequency and phase are compacted into a single digital signature that can be accumulated to other responses resulting from different test stimuli.

2.4. Fault coverage

Figures 2(b), 2(c) and 2(d) show that significant signal deviations result in general in different time signatures. On the other hand, figures 2(b) and 2(d) show that the staircase shape of the curves limits the detection of parametric (soft) deviations in signal frequency. In each step level, the time signature is approximately the same for a significant frequency window. The size of these steps can be reduced by considering larger time constants as shown in figure 2(f) for the case of V_0=1V. However, increasing τ, although it increases soft fault detection, increases also the testing time (time required to reach V_{REF}). Secondly, it also increases the probability of false rejection. For example, for the largest τ in figure 2(f), a small change in frequency can result in very different time signatures.

(a)

(b)

(c)

(d)

(e)

(f)
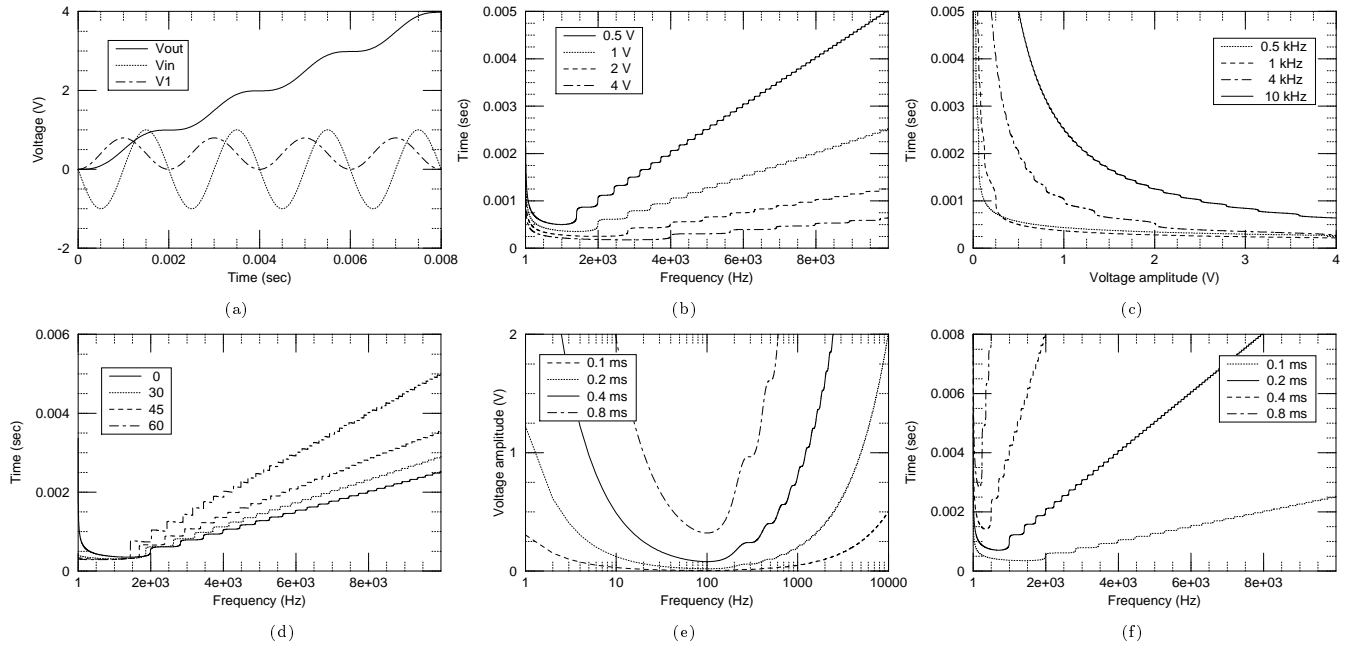
Figure 2. Signature analysis.

Considering two signals $f_1(t)$ and $f_2(t)$ of the valid input space, signature aliasing occurs when $f_1(t)$ and $f_2(t)$ result in approximately the same time signature. This happens when:

$$\frac{V_{01}}{f_1} \cong \frac{V_{02}}{f_2} \qquad [3]$$

This can be seen, for example, in figure 2(b) where a signal $V_{01}=0.5V$ and $f_1=4kHz$ gives a time signature of approximately 2ms as for the signal $V_{02}=1V$ and $f_2=8kHz$.

Considering a linear aliasing behaviour as in equation [3] and that a faulty signal has the same probability of being anywhere in the input space, it can be shown that the worst case aliasing probability is given by:

$$P_{alia\sin g} = max(\partial f, \partial V) \qquad [4]$$

Then, assuming that deviations of ±5% are accepted for the nominal frequency and nominal voltage, the probability of aliasing in the worst case will be 0.05.

Finally, let us consider faults in the ABILBO structure regardless the programmed BIST function. The effects of deviations in passive components is illustrated in figure 2(f), where deviations in the oscillation frequency and in the integrators τ give different time signatures. It can be shown that the mutual influence of t, ω and τ is such that the time signature t is more sensitive to τ variations for large values of ω and large values of τ. Then, in order to ensure a good coverage of ABILBO faults, very low frequencies should be avoided.

3. Experimental results

A discrete version of the SC ABILBO was used for testing the biquad filter of figure 3. Two identical ABILBOs (one for test generation and another for signature analysis) were implemented in protoboard with

$C_{SC}=2.2nF$, $C=22nF$ and $C_{OSC}=0.22nF$. The power supplies were set at +5V and -5V.

Two frequencies were automatically derived by the test generator, $f_1=721Hz$ and $f_2=1442Hz$. The fault set considered includes large deviations (-50% and +100%) of passive components. The theoretical cut frequency of the filter (721Hz) was obtained by using an $f_{CK}\cong45.3kHz$. The other testing frequency (1442Hz) was obtained by simply doubling f_{CK}. To obtain an amplitude $V_0\cong1V$ for the two frequencies, V_A (figure 1) was set at 1V. For the signature analysis, an 8-bit counter clocked at the lowest switching frequency f_{CK} (45.3kHz as above) computes the time needed to reach the threshold voltage $V_{REF}=$ +4V.
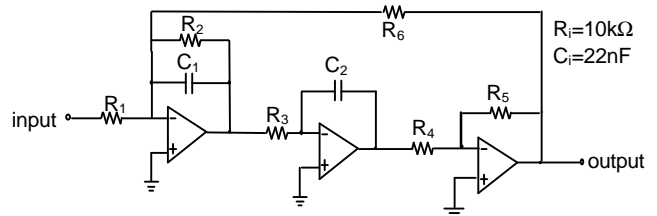
Figure 3. The circuit under test.

The experiments with the faulty filter consisted firstly in injecting component deviations of +100% and -50% ($2.C_i$, $\frac{C_i}{2}$, $2.R_i$, and $\frac{R_i}{2}$) into the circuit and in computing time signatures. A 100% coverage was achieved for these passive component faults.

Secondly, although the precomputed frequencies originally did not consider the detection of small component deviations, deviations of ±20% from the nominal values of resistors and capacitors were

considered in our experiments. The fault coverage decreased slightly, especially due to components to which the filter output voltage is less sensitive for the frequencies applied. This is the case of capacitor C1.

Finally, all faults injected into the oscillator and into the signature analyser were also detected.

In terms of time, a total of 40ms is required to apply the whole test (including the two frequencies) to the biquad filter. The computation of this time considered the oscillator transient response (the dominant term) and the worst case frequency application time (when the signature counter overflows).

4. System level integration: an example

Since integrators are often found in analog circuits, the possibility of sharing the available functional hardware with the ABILBO circuitry could be explored. A typical situation where hardware sharing can be considered is the case of filters based on a cascade of biquads [8]. Let us consider, for example, the 6th order filter of figure 4(a). The programmable biquad cell (PBq) given in figure 4(b) is used as the basic component to implement this analog filter [8]. The analysis of figure 4(b) leads to the conclusion that the PBq can easily accomodate the ABILBO structure given in figure 1, resulting in a very low area overhead and performance degradation while in functional mode. Then, the filter testing could be performed in three major phases according to table 2. The three digital signatures obtained could be accumulated in the same counter.
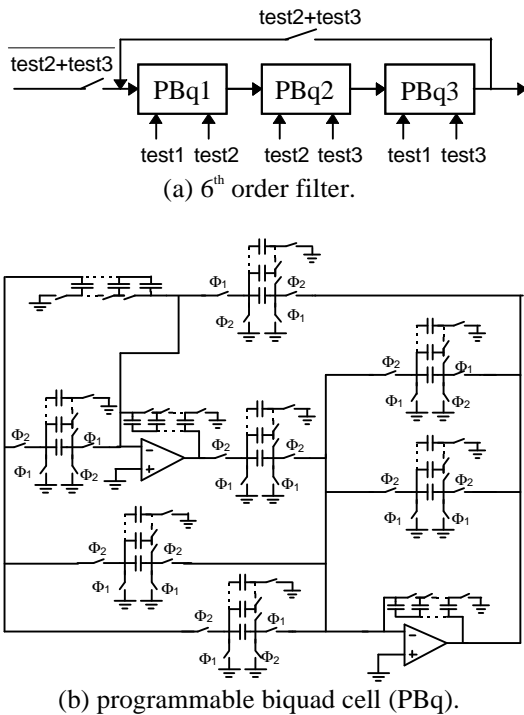

(a) 6th order filter.

(b) programmable biquad cell (PBq).

Figure 4. BIST for a filter based on a cascade of biquads.

5. Conclusions

In this work, we have presented ABILBO, a novel multifunctional BIST structure for use in analog systems. The ABILBO structure, based on two analog integrators and some additional circuitry, recreates in the analog world the scan, test generation, signature analysis and reset capabilities of the digital BILBO.

test phase	test pattern generator	circuit under test	signature analyser
test1	PBq1	PBq2	PBq3
test2	PBq2	PBq3	PBq1
test3	PBq3	PBq1	PBq2

Table 2. Test planning.

We have implemented a switched-capacitor ABILBO in protoboard and have used it for testing a low-pass filter. Experimental results confirm the theory and show that the coverage of deviations of filter and ABILBO passive components can be very high.

We have also shown that, in cases where functional and testing circuitry can be shared, the hardware overhead and performance degradation can become very low. This is typically the case of high order filters based on a cascade of biquads.

In future, continuous-time implementations for the ABILBO structure should be searched and their use for high frequency testing investigated.

6. References

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