Accurate Determination of Ultrathin Gate Oxide Thickness and Effective Polysilicon Doping of CMOS Devices

Ashawant Gupta, Peng Fang, Miryeong Song, Ming-Ren Lin, Don Wollesen, Kai Chen, and Chenming Hu

Abstract— **We present an efficient and accurate method to characterize the physical thickness of ultrathin gate oxides (down to 25 Å) and the effective polysilicon doping of advanced CMOS devices. The method is based on the model for Fowler–Nordheim (F–N) tunneling current across the gate oxide with correction in gate voltage to account for the polysilicon-gate depletion. By fitting the model to measured data, both the gate oxide thickness and the effective poly doping are unambiguously determined. Unlike the traditional capacitance–voltage ($C-V$) technique that overestimates thin-oxide thickness and requires large area capacitor, this approach results in true physical thickness and the measurement can be performed on a standard sub-half micron transistor. The method is suitable for oxide thickness monitoring in manufacturing environments.**

THE gate oxide thickness ($T_{\rm OX}$) of CMOS transistors has been scaled down constantly with the reduction in gate length. With oxides approaching atomic dimensions, it is imperative we formulate methodologies to monitor and precisely control $T_{\rm OX}$. Additionally, for modeling purposes, it is important to accurately determine the electrically active doping concentration of the polysilicon gate (N_P). However, the standard methods for extracting $T_{\rm OX}$ from capacitance–voltage ($C-V$) measurements of large area MOS capacitors are no longer accurate for thin oxides ($T_{\rm OX} < 60$ Å) and consistently result in values larger than real physical thickness. This discrepancy between the electrical and physical/optical characterization techniques is due to the effects of finite thickness of inversion/accumulation layer (including quantum effects) and polysilicon depletion [1]–[4]. Until device simulators can incorporate these effects, there exists an urgent need to identify and characterize the difference between the electrical and physical values of $T_{\rm OX}$. Even though the electrical $T_{\rm OX}$ can suffice for device modeling and design, for process design, physical $T_{\rm OX}$ is required. Here, we report an accurate and efficient approach for determining physical $T_{\rm OX}$ and effective N_P from measured tunneling current across the oxide.

Manuscript received January 29, 1997; revised August 15, 1997.

A. Gupta was with Advanced Micro Devices, Sunnyvale, CA 94088-3453 USA. He is now with Micro Instruments Co., Ambala Cantt 133 001, India.

P. Fang, M.-R. Lin, and D. Wollesen are with Advanced Micro Devices, Sunnyvale, CA 94088-3453 USA.

M. Song was with Advanced Micro Devices, Sunnyvale, CA 94088-3453 USA. She is now with Hannam University, Taejeon 300-791, Korea.

K. Chen and C. Hu are with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720-1772 USA.

Publisher Item Identifier S 0741-3106(97)09065-4.

The Fowler–Nordheim (F–N) tunneling current density $J_{\rm FN}$ is given by [5]

$$J_{\rm FN} = CE_{\rm OX}^2 \exp[-\beta/E_{\rm OX}] \tag{1}$$

where $E_{\rm OX}$ is the electric field across the oxide and C and β are constants; $C = 9.92 \times 10^{-7}$ AV^{-2} and $\beta = 2.635 \times 10^8$ V cm^{-1} [6]. $J_{\rm FN}$ is a unique function of $E_{\rm OX}$, which is related to oxide voltage $V_{\rm OX}$. $V_{\rm OX}$ is a function of the applied gate voltage V_G (substrate grounded) and is given by

$$V_{\rm OX} = E_{\rm OX}T_{\rm OX} = V_G - V_{\rm FB} - \psi_S - V_P \tag{2}$$

where ψ_S is the Si surface potential, $V_{\rm FB}$ is the flat-band voltage, and V_P is the voltage drop in the poly. $V_{\rm FB}$ and V_P are given by

$$V_{\rm FB} = \Phi_{\rm MS} - Q_o/C_{\rm OX} \cong \Phi_{\rm MS} \tag{3}$$

$$V_P = \frac{\varepsilon_{\rm ox}^2 E_{\rm OX}^2}{2q\varepsilon_s N_P} \tag{4}$$

where $q\Phi_{\rm MS}$, in eV (q being electron charge), is workfunction difference between poly and Si, Q_o is effective charge at Si/SiO$_2$ interface, $C_{\rm OX}$ is oxide capacitance, and $\varepsilon_{\rm ox}$ and ε_s are permittivities of SiO$_2$ and Si, respectively. For thin, good-quality gate oxides, $Q_o/C_{\rm OX} < 0.01$ V ($Q_o/q < 10^{10}$/cm^2), and is negligible compared to $\Phi_{\rm MS}$. $\Phi_{\rm MS}$ itself depends on the conduction type of both Si and poly. In this study, n$^+$-poly nMOSFET's and p$^+$-poly pMOSFET's are used. Substrate doping ($N_{\rm SUB}$) for both n and pMOSFET is 2×10^{17}/cm^3. Assuming that poly has same band structure as Si and is degenerately doped, $\Phi_{\rm MS} = -1.0$ V and $+1.0$ V for n and pMOSFET, respectively, at this $N_{\rm SUB}$ doping level. For V_P expression in (4), depletion approximation is used with uniform N_P [3]. Maximum possible V_P is 1.12 V (Si bandgap at 300 K) due to pinning of the Fermi level E_F at the band edges E_C and E_V. Substituting (4) in (2), we get

$$E_{\rm OX} = \frac{1}{A}\left[-T_{\rm OX} + \sqrt{T_{\rm OX}^2 + 2A(V_G - V_{\rm FB} - \psi_S)}\right]$$

where

$$A = \frac{\varepsilon_{\rm ox}^2}{q\varepsilon_s N_P} \tag{5}$$

which is valid for the range where V_P varies with V_G. After saturation of V_P, $E_{\rm OX}$ is obtained from the general expression

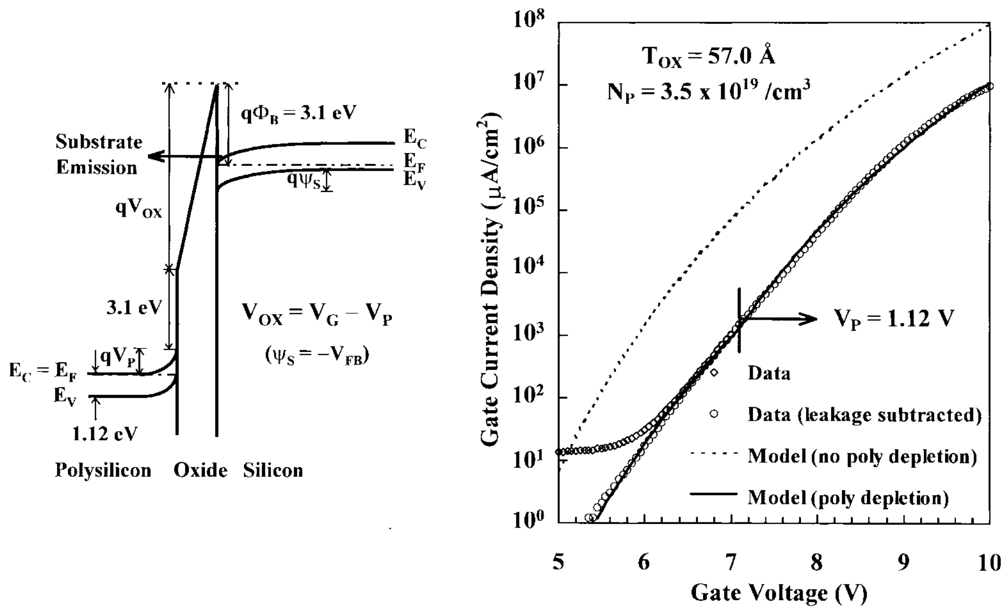

Fig. 1. Schematics of band diagram and fitting results for a 0.35-μm n$^+$-poly nMOSFET biased under a positive V_G, resulting in F–N tunneling of electrons from the substrate. The model with poly depletion matches with the data.

in (2). Using $T_{\rm OX}$ and N_P as fitting parameters $E_{\rm OX}$ can be calculated for the complete F–N bias range and used to predict or match the tunneling current.

Fig. 1 shows the schematics of band diagram and fitting results for a nMOSFET biased with positive V_G (source, drain, and substrate grounded) such that the substrate is inverted and emits electrons. The positive V_G results in depletion of poly and its extent depends on V_G. The maximum possible $V_P = 1.12$ V is shown. For F–N tunneling bias range, ψ_S is a constant since E_F at the Si surface is pinned at E_C, as shown. For $N_{\rm SUB} = 2 \times 10^{17}/{\rm cm}^3$, $\psi_S = +1$ V which is equal to $-V_{\rm FB}$. In fact, for n$^+$-poly nMOSFET, if E_F at the Si surface is pinned at E_C and $Q_o/C_{\rm OX}$ is negligible, then $\psi_S = -V_{\rm FB}$, regardless of $N_{\rm SUB}$. Thus, from (2), $V_{\rm OX} = V_G - V_P$. As seen, $J_{\rm FN}$ predicted by the model with poly depletion matches well with data. Fitting was first performed for the range of V_G where V_P is saturated and $T_{\rm OX}$ is the only variable. A difference of 0.5 Å was distinguishable and for the device shown, the best fit is obtained for $T_{\rm OX} = 57.0$ Å. Then, fixing $T_{\rm OX}$ and varying N_P, fitting was performed for lower V_G as shown in Fig. 2. A difference of $0.5 \times 10^{19}/{\rm cm}^3$ in N_P is easily discernible. The best fit is realized for $N_P = 3.5 \times 10^{19}/{\rm cm}^3$.

Fig. 3 shows that with the same $J_{\rm FN}$ model and constant $N_P = 3.5 \times 10^{19}/{\rm cm}^3$, good match is obtained with data for devices fabricated with same process and target $T_{\rm OX}$ ranging from 60 Å to 25 Å. The oscillations in data for $T_{\rm OX} = 36.5$ Å are due to electron wave interference which is $T_{\rm OX}$ dependent [7], [8]. Recently, these oscillations have been used to extract $T_{\rm OX}$ [8]. However, the technique proposed in this letter is simpler and can be used to monitor $T_{\rm OX}$ variation in manufacturing. $T_{\rm OX}$ characterization results by three different methods are compared in Fig. 4. For optical measurements, Therma-Wave's Opti-Probe 6131 measurement system, which uses a Beam Profile Ellipsometer to measure ultrathin film thickness, was used. For the C–V data, inversion value is used at $E_{\rm OX} \cong 2.5$ MV/cm. To reduce the direct-tunneling leakage current, the substrate was floating during the measurement and the source and drain were grounded. It should be noted that the optical measurements were performed on test wafers and hence, there is an inherent process variation. Still, physical values obtained from $J_{\rm FN}$ match well with optical measurement results, whereas the electrical values obtained from C–V consistently overestimate the thickness.

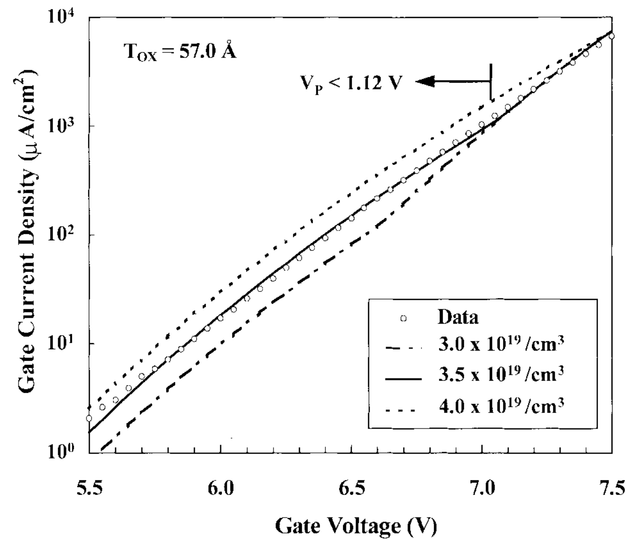

Fig. 2. Sensitivity of the F–N tunneling current model to variation in polysilicon doping in the low current ($V_P < 1.12$ V) range. The oxide thickness is kept constant at the value (57 Å) obtained from fitting the model to the high current ($V_P = 1.12$ V) range.

The case of a pMOSFET biased with positive V_G (substrate emission) is different from the nMOSFET. The Positive V_G results in accumulation of the p$^+$-poly, and $V_P = 0$ since E_F is pinned at E_V. Consequently, N_P is not a fitting parameter. Si substrate is also in accumulation with $E_V = E_F$ at the

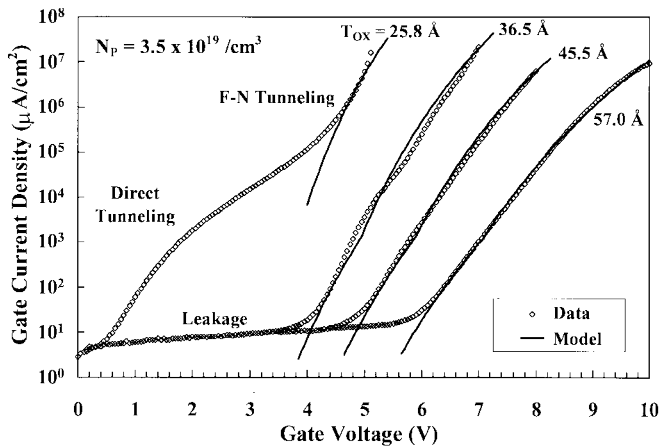

Fig. 3. Substrate emission F–N tunneling current density characteristics for 0.35 μm n$^+$-poly nMOSFET's fabricated with same process but different oxide thickness. With constant poly doping concentration (3.5×10^{19}/cm^3), model matches with data for all the thickness.

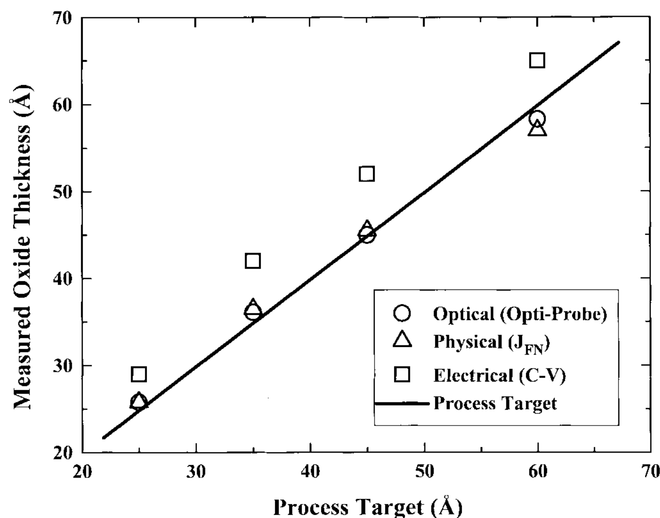

Fig. 4. Oxide thickness characterized by three different measurement techniques. Physical values, obtained from F–N tunneling current data, are consistent with the optical results, whereas the electrical values, obtained from $C-V$ data, are an overestimate.

surface. Hence, $\psi_S = 0.12$ V and from (2), $V_{OX} = V_G - 1.12$. Like the nMOSFET, for F–N tunneling bias range in a p$^+$-poly pMOSFET, this result is independent of N_{SUB}. Consistent with optical measurements, $T_{OX} = 58.3$ Å was obtained by fitting the model to data. This result is also consistent with the nMOSFET substrate emission case discussed earlier. Both the n$^+$-poly nMOSFET and the p$^+$-poly pMOSFET devices are on the same wafer and the difference of 1.3 Å in the results is within the limits of processing variation and the measurement error of this technique. Similar results were obtained for nMOSFET gate emission.

The results so far indicate that J_{FN} model for a nMOSFET substrate emission can be used to accurately characterize T_{OX} and N_P. We further developed this method into a wafer level electrical test technique to monitor T_{OX} during manufacturing. This technique can work even with both T_{OX} and N_P varying, as is expected in a manufacturing environment, if a sufficiently high fixed current is chosen (for example 1 A/cm^2) such that E_F on the n$^+$-poly side is pinned at E_V. The V_G corresponding to this fixed high current is measured. T_{OX} is then calculated from the measured V_G using (2) as band bending in poly is saturated with fixed $V_P = 1.12$ V and poly doping is no longer required for the calculation. This technique was used to monitor T_{OX} variation at different die locations on a wafer. The sensitivity was found to be 0.1 Å and maximum error due to the oscillations in data was ± 1.5 Å [9]..

In summary, the J_{FN} model has been shown to accurately characterize true physical thickness of ultrathin gate oxides (60 Å to 25 Å) after correction is made in V_G to account for poly depletion. Also, the electrically active poly doping concentration is obtained by fitting the model to n$^+$-poly nMOSFET substrate emission data. A single point measurement of $J_{FN} =$ 1 A/cm^2 results in V_G being linearly proportional to T_{OX} and has been used to monitor T_{OX} variation on a wafer. The sensitivity is 0.1 Å, with a maximum error of ± 1.5 Å.

ACKNOWLEDGMENT

The authors would like to acknowledge C. Y. Yang of Microelectronics Laboratory, Santa Clara University, Santa Clara, CA, for his valuable suggestions and contributions.

REFERENCES

[1] R. Rios, N. D. Arora, C.-L. Huang, N. Khalil, J. Faricelli, and L. Gruber, "A physical compact MOSFET model, including quantum mechanical effects, for statistical circuit design applications," in *IEDM Tech. Dig.*, 1995, pp. 937–940.

[2] C.-Y. Lu, J. M. Sung, H. C. Kirsch, S. J. Hillenius, T. E. Smith, and L. Manchanda, "Anomalous $C-V$ characteristics of implanted poly MOS structure in n$^+$/p$^+$ dual-gate CMOS technology," *IEEE Electron Device Lett.*, vol. 10, pp. 192–194, May 1989.

[3] K. F. Schuegraf, C. C. King, and C. Hu, "Impact of polysilicon depletion in thin oxide MOS technology," in *Proc. Int. Symp. VLSI Tech., Syst., and Applicat.*, 1993, pp. 86–90.

[4] N. D. Arora, R. Rios, and C.-L. Huang, "Modeling the polysilicon depletion effect and its impact on submicrometer CMOS circuit performance," *IEEE Trans. Electron Devices*, vol. 42, pp. 935–943, May 1995.

[5] R. H. Fowler and L. W. Nordheim, "Electron emission in intense electric fields," in *Proc. R. Soc. Lond. A*, 1928, vol. 119, pp. 173–181.

[6] Z. A. Weinberg, "On tunneling in metal-oxide-silicon structures," *J. Appl. Phys.*, vol. 53, pp. 5052–5056, 1982.

[7] G. P. Petersson, C. M. Svensson, and J. Maserjian, "Resonance effects observed at the onset of Fowler–Nordheim tunneling in thin MOS structures," *Solid-State Electron.*, vol. 18, pp. 449–451, 1975.

[8] S. Zafar, K. A. Conrad, Q. Liu, E. A. Irene, G. Hames, R. Kuehn, and J. J. Wortman, "Thickness and effective electron mass measurements for thin silicon dioxide films using tunneling current oscillations," *Appl. Phys. Lett.*, vol. 67, no. 7, pp. 1031–1033, 1995.

[9] A. Gupta, "Performance and reliability of advanced silicon-based devices," Ph.D. dissertation, Santa Clara Univ., Santa Clara, CA, 1997.