Accurate Evaluation of CMOS Short-Circuit Power Dissipation for Short-Channel Devices

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ABSTRACT

This paper presents an accurate model for the evaluation of the CMOS short-circuit power dissipation for short-channel devices, on the basis of a CMOS inverter. The improvement of the proposed approach against previous works is due to the new derived, accurate, analytical expressions for the inverter output waveform which include for the first time the influences of both transistor currents, and the gate-to-drain coupling capacitance. The results produced by the suggested model show good agreement with SPICE simulations.

I. INTRODUCTION

Power dissipation in CMOS circuits consists mainly of two parts, the capacitive and the short-circuit power dissipation. Capacitive dissipation caused by charging and discharging the load capacitance is well understood and easy to be estimated. During the input transition in a static CMOS structure, a direct path from power supply to ground is caused, resulting to short-circuit dissipation.

The emphasis of this work is on evaluating analytically, the short-circuit dissipation of a CMOS inverter. The first closed-form expression for the evaluation of the short-circuit power dissipation in a CMOS inverter was presented in [1] where zero load capacitance, and current waveform which is mirror symmetric about a central vertical axis (at the half of the input transition time), were considered. This expression gives the maximum value of the short-circuit power dissipation, and is based on the long-channel square-law MOS model. More recently, in [2],[3] an expression for the short-circuit energy dissipation of the CMOS inverter, without the simplifications of [1], was derived. However, the square-law MOS model was used, and the expression of the output waveform was derived with negligible short-circuit current. An expression for the evaluation of the short-circuit power dissipation, based on an expression for the output waveform which considers the current through both transistors was presented in [4], but also based on the square-law MOS model. Sakurai and Newton [5] presented a formula for the short-circuit energy dissipation, which is a direct extension of the formula presented in [1], for the α-power MOS model. Vemuru and Scheinberg [6] proposed a formula for the evaluation of the short-circuit power dissipation, based on the α-power MOS model, where the analytical expression of the output waveform used, doesn't include the influences of the short-circuit current, and the gate-drain coupling capacitance. A formulation of the short-circuit power dissipation by using an equivalent short-circuit capacitance with no physical mean is presented in [7], where mean charge conservation through the CMOS structure, and a linear rough approximation of the output waveform, are used.

In this work, an analytical expression for the evaluation of the short-circuit power dissipation in a CMOS inverter, without making simplifyied assumptions, is derived. A simple model [8] which includes the velocity saturation effects of short-channel devices, has been chosen. For the derivation, analytical expressions of the output waveform which considers the current through both transistors, are used. In order to avoid an overestimation of the short-circuit power dissipation, the influence of the gate-drain coupling capacitance, is considered.

II. INVERTER OUTPUT WAVEFORM ANALYSIS

The derivation presented in the following are for a rising input ramp,

$$V_{in} = \begin{cases} 0, & t \le 0 \\ V_{DD} \cdot (t/\tau), & 0 \le t \le \tau \\ V_{DD}, & t \ge \tau \end{cases} \quad (1)$$

where τ is the input rise time. The analysis for a falling input ramp is symmetrical. The differential equation which describes the discharge of the load capacitance C_L for the CMOS inverter of Fig. 1, taking into account the gate-drain capacitive coupling (C_M) [8], is derived from the Kirchoff's current law of the output node,

$$I_{C_L} + I_{C_M} + I_p - I_n = 0,$$

$$C_L \frac{dV_{out}}{dt} = C_M \left(\frac{dV_{in}}{dt} - \frac{dV_{out}}{dt} \right) + I_p - I_n. \quad (2)$$

Depending on the region of operation the drain current of the MOSFETs is given by the following equations [8],

$$I_D = 0, \qquad V_{GS} < V_{TN}, \qquad \text{Cutoff}$$

$$I_D = \beta V_O (V_{GS} - V_T), \qquad V_{DS} \ge V_{D-SAT}, \qquad \text{Saturation}$$

$$I_D = \frac{\beta}{1 + V_O^{-1} V_{DS}} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right], \qquad V_{DS} < V_{D-SAT}, \qquad \text{Linear}$$

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where β is the device gain factor, V_T is the device threshold voltage, V_O is the voltage which specifies the effects of carriers velocity saturation, and $V_{D-SAT} = V_O\left[\sqrt{1+2V_O^{-1}(V_{GS}-V_T)}-1\right]$ is the saturation voltage of the device.

In the following, normalized voltages with respect to V_{DD} i.e. $u_{in} = V_{in}/V_{DD} = t/\tau$, $u_{out} = V_{out}/V_{DD}$, $n = V_{TN}/V_{DD}$, $p = |V_{TP}|/V_{DD}$, $v_{on} = V_{ON}/V_{DD}$, $v_{op} = V_{OP}/V_{DD}$, and the variable $x = t/\tau$, are used. Short - circuit power is dissipated when a direct current path from power supply to ground occurs. Due to the input-to-output coupling capacitance (C_M), an overshoot occurs at the early part of the output voltage waveform (Fig. 2). During the overshoot there is no current from power supply to ground because V_{out} is higher than V_{DD}. Thus, short-circuit power is dissipated from the end of the output voltage overshoot ($x=x_1$), until the PMOS device is turned off ($x=1-p$). Considering input ramps such that the NMOS device is still saturated when the input voltage ramp reaches the value $V_{DD} - |V_{TP}|$, which is true for the most practical cases in VLSI circuits, we analyse the three first operation regions (Fig. 2) of the inverter in order to evaluate the short-circuit power dissipation.

Region 1, $0 \le x \le n$: The PMOS transistor is in the linear region. Since, the NMOS transistor is off the discharge of the output node does not start in this region, which means that the end of the output voltage overshoot occurs in the next region. Thus, in this region there is no short-circuit dissipation, but the expression of the output voltage waveform is required, in order to find the initial conditions of the next region. The differential equation (2), using the MOS current equations becomes,

$$\frac{du_{out}}{dx} = c_m + \frac{A_p}{1+v_{op}^{-1}(1-u_{out})}\left[(1-x-p)(1-u_{out}) - \frac{(1-u_{out})^2}{2}\right], \quad (3)$$

where $c_m = \frac{C_M}{C_L+C_M}$, $A_p = \frac{\beta_p V_{DD}\tau}{C_L+C_M}$. The above differential equation is a non-linear Riccati equation [9] which cannot be solved analytically, if a particular solution is not known. Thus, a power-series expansion method [8],[9] has been used, resulting to the following recursive expression,

$$u_{out} = 1 - \sum_{k=1}^{\infty} f_k x^k \quad (4)$$

where, $f_1 = -c_m$, $f_2 = \frac{A_p}{2}(p-1)f_1$, and

$$f_k = \frac{A_p}{k}\left[f_{k-2} + (p-1)f_{k-1} + \frac{1}{2}\sum_{i=1}^{k-2}(f_i f_{k-i-1})\right] - \frac{1}{v_{op}k}\sum_{i=1}^{k-2}\left[(k-i)f_i f_{k-i}\right], \quad \text{for } k>2.$$

Region 2, $n \le x \le x_{satp}$: The NMOS device is saturated and the PMOS device is in the linear region. Note, that the right limit of this region is the normalized time value x_{satp} (Fig. 2) where the PMOS device enters saturation, i.e. $V_{DD} - V_{out} = V_{D\text{-}SATP}$, and is determined by the PMOS saturation condition,

$$u_{satp} = 1 - v_{op}\left[\sqrt{1+2v_{op}^{-1}(1-x_{satp}-p)}-1\right],$$

where u_{satp} is the normalized output voltage value when PMOS device saturates. As we can see in Fig. 2, in the special case of very fast input ramps, the PMOS device is turned off after its linear region, without enters saturation. In region 2, the differential equation (2), becomes,

$$\frac{du_{out}}{dx} = c_m - A_n v_{on}(x-n) + \frac{A_p}{1+v_{op}^{-1}(1-u_{out})} \cdot\left[(1-x-p)(1-u_{out}) - \frac{(1-u_{out})^2}{2}\right], \quad (5)$$

where $A_n = \frac{\beta_n V_{DD}\tau}{C_L+C_M}$. In order to give a solution of (5), we neglect the quadratic current term of the PMOS device, because the charge contributed by this term is negligible [10]. Also, instead of u_{out} at the denominator of the PMOS current, we use the value of the normalized output voltage u'_{satp} at the end of region 2, with the assumption of negligible PMOS current. u'_{satp} is evaluated below by equation (9). After the above approximations, the solution of the differential equation (5) is,

$$u_{out} = 1 + \frac{A_n v_{on}}{G_p} + \left(u_{[n]} - \frac{A_n v_{on}}{G_p} - 1\right)\frac{e^{y^2}}{e^{y_n^2}} + \sqrt{\pi}\, e^{y^2}\left(\frac{A_n y_n v_{on}}{G_p} + \sqrt{\frac{1}{2G_p}}c_m\right)(\text{erf}[y] - \text{erf}[y_n]), \quad (6)$$

where, $u_{[n]} = 1 - \sum_{k=1}^{\infty} f_k n^k$, $G_p = \frac{A_p}{1+v_{op}^{-1}(1-u'_{satp})}$,

$y = \sqrt{\frac{G_p}{2}}(x-1+p)$, $y_n = \sqrt{\frac{G_p}{2}}(n-1+p)$, and erf [y], erf [$y_n$] are the error functions of y, y_n respectively. The above equation gives waveforms very close to those derived from SPICE simulations, which indicates the validation of the above approximations.

In order to continue the analysis for the next region the evaluation of the values x_{satp}, u_{satp}, is required. These values satisfy the PMOS saturation condition, expressed by,

$$u_{out} = 1 - v_{op}\left[\sqrt{1+2v_{op}^{-1}(1-x-p)}-1\right], \quad (7)$$

and they can be found by solving the system of (6) and (7). Due to the error functions of (6), the system cannot be solved analytically. Hence, in the following an efficient method for the calculation of x_{satp}, u_{satp}, is used (Fig. 3). The analytical solution of the differential equation (5), if negligible PMOS current is assumed, is,

$$u'_{out} = u_{12} + c_m x - \frac{A_n v_{on}}{2}(x-n)^2, \quad (8)$$

where $u_{12} = u_{[n]} - c_m n$ is the integration constant, which

is inserted to ensure continuity with respect to region 1. By equating (7) and (8) the normalized time value x'_{satp} in which the inverter leaves region 2, with the assumption of negligible PMOS current, is calculated. After the substitution of x'_{satp} in (8), the normalized voltage u'_{satp} is,

$$u'_{satp} = u_{12} + c_m x'_{satp} - \frac{A_n v_{on}}{2}\left(x'_{satp} - n\right)^2 . \quad (9)$$

The next step of our method is to determine the tangent of the output waveform expressed by (6), at the point which corresponds to x'_{satp} (Fig. 3). This tangent is expressed by,

$$u''_{out} = a x + b \quad (10)$$

where, $a = \left.\frac{du_{out}}{dx}\right|_{x=x'_{satp}}$, and $b = \left(u_{out}\right|_{x=x'_{satp}}) - a\, x'_{satp}$.

From (7) and (10) an accurate approximation for x_{satp} is derived. By substituting this value in (6) the normalized output voltage u_{satp} is evaluated. The error which is inserted to the calculation of x_{satp}, due to the above method is up to 0.5%. Note, that in [6] a rough approximation for x_{satp} is used (x_{satp}=1-n-p), which results to a considerable error in the evaluation of the short-circuit power dissipation.

Region 3, $x_{satp} \le x \le$ 1-p: Both transistors are saturated. The differential equation (2) becomes,

$$\frac{du_{out}}{dx} = c_m - A_n v_{on}\left(x - n\right) + A_p v_{op}\left(1 - x - p\right). \quad (11)$$

The analytical solution of (11) is,

$$u_{out} = u_{23} + c_m x - \frac{A_n v_{on}}{2}\left(x-n\right)^2 - \frac{A_p v_{op}}{2}\left(1-x-p\right)^2 , \quad (12)$$

where the integration constant which is inserted to ensure continuity with respect to region 2, is given by,

$$u_{23} = u_{satp} - c_m x_{satp} + \frac{A_n v_{on}}{2}\left(x_{satp} - n\right)^2 + \frac{A_p v_{op}}{2}\left(1 - x_{satp} - p\right)^2 .$$

III. CMOS SHORT-CIRCUIT POWER DISSIPATION

Short-circuit energy is dissipated from the end of the output voltage overshoot ($x=x_1$), until the PMOS device is turned off (x=1-p). The short-circuit energy dissipation during the falling transition of the output, is given by,

$$E_{SCF} = V_{DD} \int I_{SC}\, dt = V_{DD} \int_{x_1}^{1-p} I_p\, \tau\, dx \quad (13)$$

The condition that, the NMOS transistor is still saturated when the input voltage ramp reaches the value $V_{DD} - |V_{TP}|$ i.e. x=1-p , holds for A_n<28, which is true for the most practical cases in VLSI circuits. Note, that for $A_n \le 1.5$ (very fast input ramps) the end of the output voltage overshoot occurs when the PMOS device is already off, and there is no short-circuit energy dissipation. The application of the Kirchoff's current law to the output node of the inverter (2) yields,

$$I_p = \beta_n V_{DD}^2 v_{on}\left(x-n\right) - \frac{C_M V_{DD}}{\tau} + \frac{\left(C_M + C_L\right)V_{DD}}{\tau}\frac{du_{out}}{dx}$$

Then, the integration of (13) yields,

$$E_{SCF} = \frac{\beta_n V_{DD}^3 v_{on}\,\tau}{2}\left[\left(1-p-x_1\right)\left(1-p+x_1-2n\right)\right] - V_{DD}^2 C_M\left(1-p-x_1\right) + V_{DD}^2\left(C_M + C_L\right)\left(u_{[1-p]} - 1\right), \quad (14)$$

where x_1 is the normalized time value in which the end of the output voltage overshoot occurs and $u_{[1-p]}$ is the value of the normalized output voltage when the PMOS device is turned off, and is calculated from equation (12) for x=1-p. The end of the output voltage overshoot occurs in region 2, due to the fact that the discharge of the output node, which is initially charged at V_{DD}, doesn't start in region 1 since the NMOS device is off. Thus, x_1 must be calculated by equation (6) for u_{out}=1. Since, this equation cannot be solved analytically, a method similar with that used for the calculation of x_{satp} (section II - region 2), is used. Equation (8) for u'_{out}=1 gives the normalized time value (x'_1) in which the end of the overshoot occurs, if negligible PMOS current is assumed. The tangent of the output waveform expressed by (6), at the point which corresponds to x'_1, is given by,

$$u^*_{out} = d\, x + q \quad (15)$$

where, $d = \left.\frac{du_{out}}{dx}\right|_{x=x'_1}$, and $q = \left(u_{out}\right|_{x=x'_1}) - d\, x'_1$.

By setting u^*_{out}=1 in the above equation, an accurate approximation for x_1 is derived, $x_1 = (1 - q) / d$.

The analysis in order to evaluate the short-circuit energy dissipation during the rising output transition is symmetrical, and results to the following formula,

$$E_{SCR} = \frac{\beta_p V_{DD}^3 v_{op}\,\tau}{2}\left[\left(1-n-x_1\right)\left(1-n+x_1-2p\right)\right] - V_{DD}^2 C_M\left(1-n-x_1\right) - V_{DD}^2\left(C_M + C_L\right)u_{[1-n]}, \quad (16)$$

where τ is now the input fall time, x_1 is the normalized time value in which the end of the output voltage undershoot occurs, and $u_{[1-n]}$ is the value of the normalized output voltage when the NMOS device is turned off.

Finally, the short-circuit power dissipation is given by,

$$P_{SC} = \left(E_{SCF} + E_{SCR}\right) f , \quad (17)$$

where f is the switching frequency.

In Fig. 4, the short-circuit energy dissipation percentage of the capacitive energy dissipation ($E_{CF} = C_L V_{DD}^2 / 2$) for a falling output transition, is plotted as a function of $A'_n = \beta_n V_{DD}\,\tau / C_L$. The results have been derived for an inverter with equal NMOS and PMOS gate lengths $L_n = L_p$=0.8 μm, and W_n=4 μm, W_p=6.5 μm in order to achieve equal drain currents at $V_{GS} = V_{DS} = V_{DD}$. The values of the parameters were β_n = 0.5 mA / V^2, β_p = 0.3 mA / V^2, n = 0.17, p =0.15, V_{ON} =0.7 V, V_{OP} =1 V, V_{DD}=5 V, and c_m =0.05. The SPICE measurements have been obtained by using the powermeter subcircuit proposed in [11], for the parameters of a 0.8 μm process. Also, results using the approaches for the evaluation of the short-circuit energy dissipation presented in [2], [3], [4], [6] are given. It can be observed, that the presented approach gives results closer to those derived from SPICE simulations than the other

methods. This occurs because our model includes the influence of the short-circuit current, and the gate-drain coupling capacitance on the expression of the inverter output waveform. Also, a quite accurate method is used for the determination of the time where the short-circuiting transistor changes from the linear to the saturation region. The models for the evaluation of the short-circuit dissipation presented in [1],[5] give inaccurate results, because zero load capacitance is assumed. For example, in an inverter with identical input and output waveform slopes ($A'_n \approx 12$), the short-circuit energy dissipation per transition which is calculated using (14) is about 23% of the value as calculated in [5], and 21% of the value as calculated in [1].

IV. CONCLUSION

In this paper an accurate, analytical model for the evaluation of the CMOS short-circuit power dissipation for short-channel devices, is presented. The comparison of the results produced by the proposed approach with previous works, shows better agreement with SPICE simulations.

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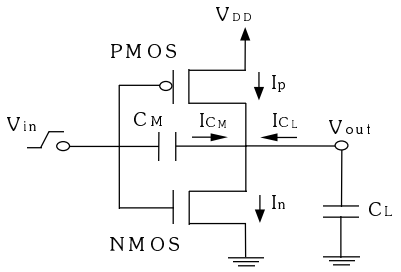

Fig. 1: The CMOS inverter

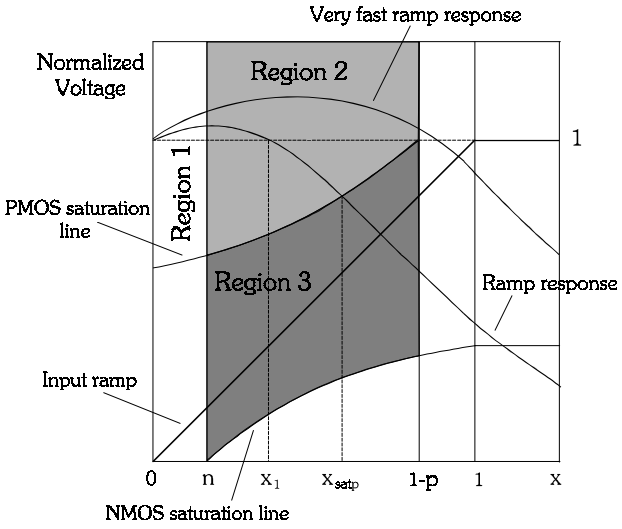

Fig. 2: Operation regions of the inverter.

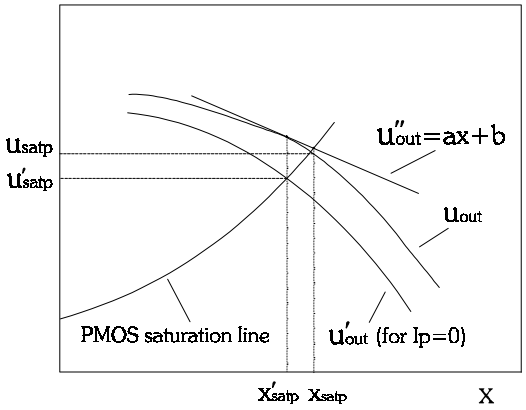

Fig.3: Approximation of the normalized time x_{satp}, in which the inverter is entered region 3.

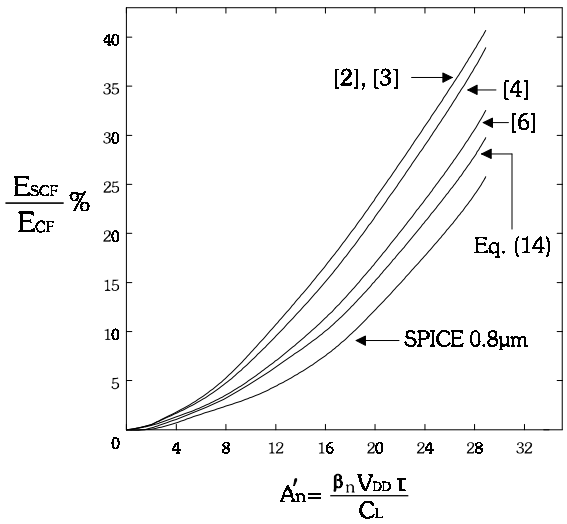

Fig. 4: Comparison between the short-circuit energy dissipation percentage of the capacitive energy dissipation, derived from SPICE simulations and those derived from analytical expressions.