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Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance

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We propose a method to accurately determine the surface potential (ψ_S) based on depletion capacitance, and the interface state density (D_{IT}) was evaluated based on the difference between quasi-static and theoretical capacitances in SiC metal-oxide-semiconductor capacitors ($C-\psi_S$ method). We determined that this method gives accurate values for ψ_S and D_{IT}. From the frequency dependence of the capacitance measured at up to 100 MHz, a significant fast-interface-state response exists at 1 MHz, which results in the overestimation of ψ_S if it is determined based on the flatband capacitance at 1 MHz. The overestimation of ψ_S directly affects the accuracy of the energy level. D_{IT} at a specific energy level is underestimated by the overestimation of ψ_S. Furthermore, the fast interface states that respond at 1 MHz cannot be detected by the conventional high(1 MHz)-low method. The $C-\psi_S$ method can accurately determine the interface state density including the fast states without high-frequency measurements. © *2012 American Institute of Physics*. [doi:10.1063/1.3673572]

I. INTRODUCTION

Silicon carbide (SiC) has been recognized as a promising material for high-power devices because of its high breakdown electric field. SiC power metal-oxide-semiconductor field effect transistors (MOSFETs) are SiC devices that have been commercialized.[1] SiC MOSFETs still suffer from low channel mobility probably because of the high density of interface states. The interface state density is characterized by high-low or conductance methods with the maximum frequency of $0.1 \sim 1$ MHz.[2–14] The existence of fast interface states has been suggested[15,16] but the fast interface states that respond to the maximum probe frequency are undetectable by these methods. Although increasing the frequency is a method to detect fast states, very high-frequency measurements are not easily obtained because of series resistance and inductance. A method based on the difference between quasi-static (low-frequency) and theoretical capacitance is valuable for the detection of fast interface states,[17,18] because measurements are not required at very high frequencies. To accurately determine the interface states by this method, a very accurate surface potential and theoretical capacitance are needed. This may be the main reason why it has not been used for SiC MOS structures to date. The surface potential (ψ_S) can be calculated from quasi-static and oxide capacitances (C_{QS} and C_{OX}) using[17,18]

$$\psi_S(V_G) = \int (1 - C_{QS}/C_{OX}) dV_G + A. \quad (1)$$

A certain ambiguity exists in the determination of the integration constant (A). For example, this constant is often determined based on the flatband capacitance in high-frequency measurements, assuming that the high-frequency capacitance does not include a contribution from the interface states. If the probe frequency is not high enough, the flatband capacitance contains a component of the fast interface states leading to a large error in the surface potential.

The high-low and conductance methods also need an accurate surface potential for an evaluation of the interface state density at a specific energy level. Interface state densities in SiC MOS structures, which were evaluated by high-low[4–9] or conductance[2,3] methods by different groups, are widely distributed even though MOS capacitors undergoing similar processes can be compared. The variations are likely partly due to the use of an erroneous surface potential and it is important to establish an accurate and standard method to determine the surface potential and interface state density.

In this study, we propose a method to accurately determine the integration constant of the surface potential based on the depletion capacitance and to evaluate the interface state density in SiC MOS structures from the quasi-static and theoretical capacitance. We refer to the proposed method as the "$C-\psi_S$ method" in this paper. Moreover, we increased the maximum frequency in the high-low and conductance methods to 100 MHz using a system suitable for high frequency measurements. The interface state densities evaluated by these methods are thus compared.

II. SAMPLE PREPARATION AND MEASUREMENT DETAILS

The MOS capacitor that was characterized in this work consisted of a 32-nm-thick oxide formed by dry oxidation at 1300 °C on an n-type 4 H-SiC (0001) epilayer. The SiC epilayer was 8.4 μm thick and was doped with nitrogen to 1.33×10^{16} cm^{-3}. The thickness and resistivity of the n-type

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SiC substrate were 335 μm and 0.022 Ωcm, respectively. A circular Ni electrode (gate) with a diameter of 604 μm was used.

Measurements were carried out at room temperature ($T = 304$ K) in a dark box. The impedance was measured at probe frequencies from 1 kHz to 100 MHz with an oscillation voltage of 25 mV using Precision Impedance Analyzer (4294 A, Agilent Technologies), which was connected to the sample through a probe kit (42941 A, Agilent Technologies). Using the probe kit, the probe and wire impedance can be effectively eliminated, which greatly improves the accuracy of the high frequency measurements. The quasi-static capacitance was measured with a delay time of 0.1 s using Quasi-static CV Meter (595, Keithley). The gate voltage was swept from depletion (−5 V) to accumulation (15 V) at a rate of about 0.1 V/s for the voltage-sweep measurements.

III. EXPERIMENTAL RESULTS AND ANALYTICAL PROCEDURE

A. *C*–*V* measurements

Figure 1(a) shows the quasi-static capacitance (C_{QS}) and the parallel-mode capacitance (C_P) measured at different frequencies for the fabricated SiC MOS capacitor. Figure 1(b) shows the parallel-mode conductance (G_P) measured at different frequencies. The existence of interface states can be detected at about $1 \sim 2$ V as the peak of conductance. Figure 2 shows equivalent circuits for (a) depletion to weak accumulation and (b) strong accumulation where C_{OX}, C_D, C_{IT}, G_{PIT}, and Z are the oxide capacitance, the semiconductor capacitance, the interface-state capacitance, the interface-state conductance, and the series parasitic impedance, respectively. For strong accumulation, C_D, C_{IT}, and G_{PIT} can be ignored because of the infinitely large C_D, and the measured C_P and G_P should be independent of gate voltage. At about 15 V, both C_P and G_P show very little change against the gate voltage indicating that the MOS capacitor is in the strong-accumulation condition. However, C_P and G_P changed significantly depending on the frequency, which is due to a change in the series parasitic impedance. Therefore, the quasi-static capacitance at 15 V is assumed to be C_{OX}, and the values of $Z(\omega)$ are determined for each frequency from the impedance measured at 15 V and C_{OX}, assuming strong accumulation (Fig. 2(b)).

B. Determination of the surface potential by the *C*–ψ_s method

Taking into account the C_{OX} and Z values, $C_D + C_{IT}$ at less than 15 V can be determined by assuming the equivalent circuit shown in Fig. 2(a). On the other hand, the surface potential $\psi_S(V_G)$ can be obtained using Eq. (1), except for the integration constant A. The integration constant A can be uniquely determined, as shown in Fig. 3, where $1/(C_D + C_{IT})^2$ is plotted against ψ_S. In Fig. 3, a linear correlation is evident for the sufficiently negative ψ_S (depletion region). At a sufficiently high frequency and upon depletion, the interface states do not respond and no inversion carriers are generated at the SiC MOS interface. Therefore, $C_D + C_{IT}$ can be approximated as the depletion capacitance (C_{dep})

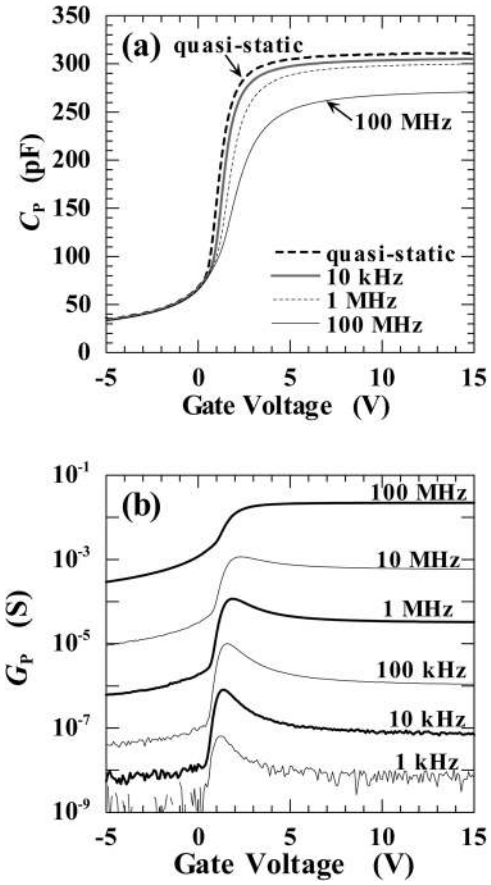

FIG. 1. (a) Capacitance-voltage and (b) conductance-voltage characteristics of a n-type SiC MOS capacitor measured at different frequencies (parallel mode). The quasi-static capacitance is also plotted in (a).

and a linear relationship can be established between $1/(C_D + C_{IT})^2$ and ψ_S,[17,18]

$$\frac{1}{(C_D + C_{IT})^2} \approx \frac{1}{C_{dep}^2} = -\frac{2\psi_S}{S^2 \varepsilon_{SiC} e N_D} \text{(depletion)} \quad (2)$$

where S (0.286 mm^2) is the area of the gate electrode, ε_{SiC} ($9.7\varepsilon_0$) is the dielectric constant of SiC, and N_D is the donor concentration of the SiC epilayer. Based on Eq. (2), the constant A was determined so that the extrapolation of the straight line should intersect the origin of the plot, as shown in Fig. 3. The donor concentration was also determined from the slope of the straight line ($N_D = 1.33 \times 10^{16}$ cm^{-3}).

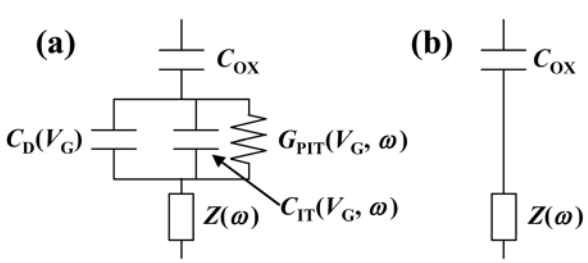

FIG. 2. Equivalent circuits for a MOS capacitor in (a) depletion to weak accumulation and (b) strong accumulation where C_{OX}, C_D, C_{IT}, G_{PIT}, and Z are the oxide capacitance, the semiconductor capacitance, the interface-state capacitance, the interface-state conductance, and the series parasitic impedance, respectively.

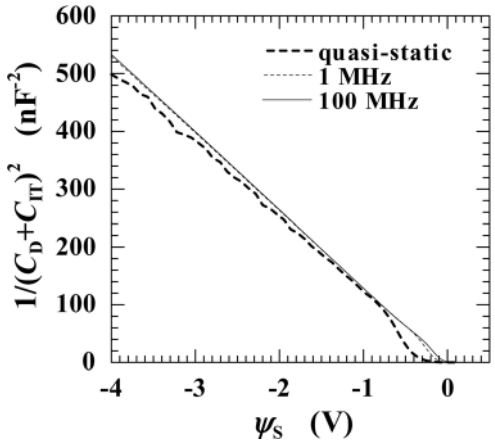

FIG. 3. $1/(C_D+C_{IT})^2$ versus surface potential ψ_S for depletion at various frequencies of a n-type SiC MOS capacitor, which was determined from the results given in Fig. 1.

C. Evaluation of interface state density in the $C-\psi_s$ method

Using the obtained surface potential, the theoretical semiconductor capacitance ($C_{D,theory}$) can be calculated by[17,18]

$$C_{D,theory}(\psi_S) = \frac{SeN_D\left|\exp\left(\frac{e\psi_S}{kT}\right)-1\right|}{\sqrt{\frac{2kTN_D}{\varepsilon_{SiC}}\left\{\exp\left(\frac{e\psi_S}{kT}\right)-\frac{e\psi_S}{kT}-1\right\}}}, \quad (3)$$

assuming that there are no holes in the n-type SiC. Figure 4 shows the C_D+C_{IT} values plotted against ψ_S at different frequencies, where the $C_{D,theory}$ calculated from Eq. (3) is also plotted. The measured C_D+C_{IT} approached $C_{D,theory}$ with an increase in the frequency because the carriers trapped at the interface states hardly respond to a sufficiently high frequency ($C_{IT}\approx 0$). A significant difference exists between C_D+C_{IT} at 1 MHz and $C_{D,theory}$ indicating that a significant portion of the fast interface states respond at 1 MHz. In contrast, 100 MHz seems to be almost sufficient for the interface carriers not to respond. The interface state density is given by[17,18]

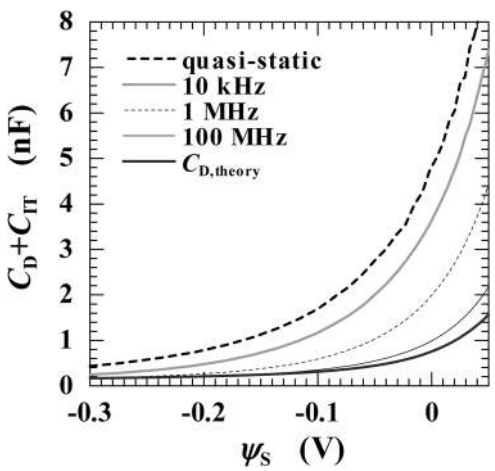

FIG. 4. C_D+C_{IT} versus surface potential ψ_S at various frequencies for a n-type SiC MOS capacitor, which was determined from the results given in Fig. 1. The theoretical semiconductor capacitance $C_{D,theory}$ is also plotted.

$$D_{IT} = \frac{(C_D+C_{IT})_{QS} - C_{D,theory}}{Se^2}, \quad (4)$$

where $(C_D+C_{IT})_{QS}$ is the C_D+C_{IT} measured under quasi-static conditions.

D. Evaluation of the interface state density by the high-low method

For the high-low method, the interface state density is given by[17,18]

$$D_{IT} = \frac{(C_D+C_{IT})_{QS} - (C_D+C_{IT})_{HF}}{Se^2}, \quad (5)$$

where $(C_D+C_{IT})_{HF}$ is the C_D+C_{IT} measured at high frequency and is assumed to be C_D. Because C_D+C_{IT} approaches $C_{D,theory}$ with an increase in the frequency, as shown in Fig. 4, using $(C_D+C_{IT})_{HF}$ at higher frequency gives a more accurate interface state density. Therefore, we used $(C_D+C_{IT})_{HF}$ at 100 MHz while a $(C_D+C_{IT})_{HF}$ of $0.1\sim 1$ MHz is usually used in the conventional high-low method.

E. Evaluation of the interface state density by the conductance method

Figure 5(a) shows the frequency dependence of G_{PIT}/ω at various surface potentials. Bell-shaped peaks originate from the interface states, and the interface state density is related to G_{PIT}/ω by[10,17]

$$G_{PIT}/\omega = e^2SD_{IT}\int_{-\infty}^{+\infty}\frac{\ln\left(1+(\omega\tau\exp(\eta))^2\right)}{2\omega\tau\exp(\eta)} \times\frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{\eta^2}{2\sigma^2}\right)d\eta, \quad (6)$$

where the interface state density (D_{IT}), the time constant of the interface states (τ), and the standard deviation (σ) are fitting parameters. The bold lines in Fig. 5(a) are G_{PIT}/ω calculated from Eq. (6) to fit the experimental results. It is noted that the measurement at up to about 10 MHz is necessary to fit correctly because the peaks exist up to about 1 MHz. The values of τ and σ obtained by fitting are shown in Fig. 5(b) where E_C-E_T was calculated by

$$E_C - E_T = e(0.19\text{V} - \psi_S), \quad (7)$$

taking into account the Fermi level of the SiC epilayer ($E_C-0.19$ eV). The values of τ and σ are reasonable compared to earlier reports.[10,19,20]

IV. DISCUSSION

Figure 6 shows the interface state densities obtained by the $C-\psi_S$ method ($C-\psi_S$), the high-low method using a high frequency of 100 MHz (high$_{100M}$−low$-\psi_S$), and the conductance method (conductance$-\psi_S$), where the E_C-E_T of the horizontal axis was calculated from Eq. (7) using the surface potential determined by the proposed method. The use of the correct surface potential is denoted by adding the term "$-\psi_S$." The D_{IT} distribution obtained by the $C-\psi_S$

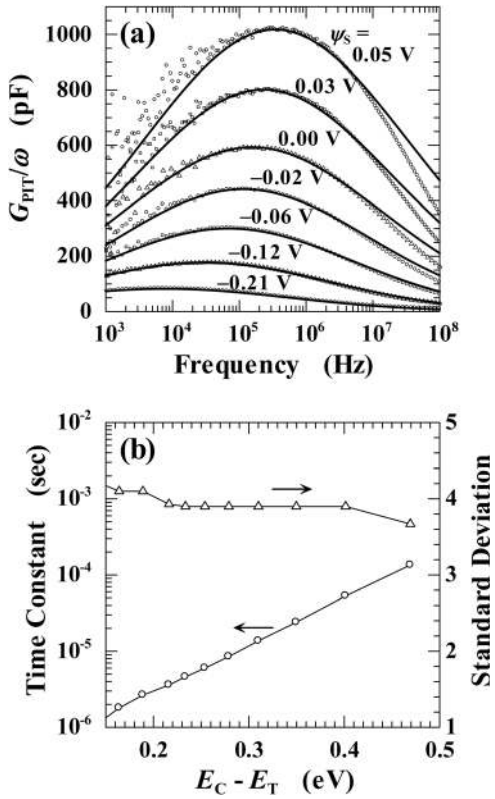

FIG. 5. (a) Interface-state conductance G_{PIT} normalized by angular frequency ω at various surface potentials ψ_S, where the symbols are experimental results and the bold lines are theoretical results fitted to the experimental results. (b) Time constant τ and standard deviation σ obtained by fitting G_{PIT}/ω.

method agrees very well with that by the conductance$-\psi_S$ method indicating the validity of the proposed method. The surface potential and the theoretical semiconductor capacitance ($C_{D,theory}$) were correctly determined. The high$_{100M}$ − low$-\psi_S$ method also gave an accurate interface state density because 100 MHz was almost sufficient for the fast states not to respond.

The D_{IT} distribution obtained by the conventional high-low method using a high frequency of 1 MHz, which was evaluated by the surface potential determined by a conventional method (refer to the next paragraph), is also plotted in Fig. 6 (conventional high-low). The conventional high-low

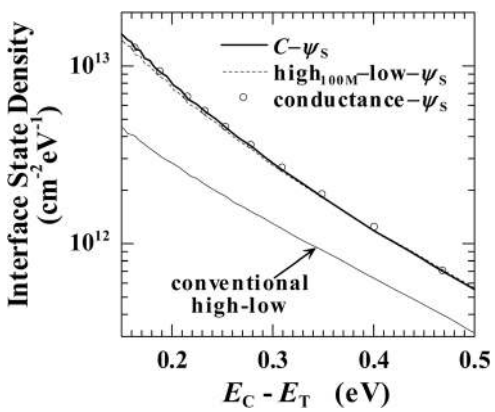

FIG. 6. Distributions of the interface state density evaluated by various methods for the same n-type SiC MOS capacitor.

method underestimated the density $2\sim3$ times because of the following two factors. First, the fast interface states that respond to higher than 1 MHz are not detected. Second, the surface potential error results in an error of E_C-E_T.

For the conventional high-low method, the integration constant of the surface potential was determined so that the surface potential is zero at the gate voltage at which the capacitance of 1 MHz is equal to the theoretical flatband-capacitance. If the conventional method is employed, the integration constant is erroneously determined because the capacitance of 1 MHz includes C_{IT}. The surface potential determined by the conventional method was overestimated by 0.077 V for the MOS capacitor characterized in this study,

$$\psi_S(\text{conventional}) = \psi_S(\text{proposed}) + 0.077\text{V}, \quad (8)$$

which results in the underestimation of E_C-E_T,

$$E_C - E_T(\text{conventional}) = E_C - E_T(\text{proposed}) - 0.077\ \text{eV}. \quad (9)$$

Because the interface state density of the SiC MOS structures increases exponentially toward the conduction band edge, a small shift in E_C-E_T results in a large change in the interface state density at specific energy levels. Therefore, the correct determination of the surface potential and E_C-E_T is very important.

It should be emphasized that the $C-\psi_S$ method is superior to the other methods from two points of view. First, the $C-\psi_S$ method can detect fast interface states without frequency limits. Second, the $C-\psi_S$ method requires simple measurements as only capacitance measurements with one voltage sweep is enough, while the conductance method needs more time-consuming $G-f$ measurements at different voltages. The $C-\psi_S$ method can be applied to not only SiC MOS structures but also other metal-insulator-semiconductor structures. The requirements are that the doping concentration (N_D) is uniform near the MOS interface and no inversion (minority) carriers are collected at the interface.

V. CONCLUSIONS

We propose a method to accurately determine the surface potential based on depletion capacitance and evaluated the interface state density based on the difference between quasi-static and theoretical capacitances in SiC MOS capacitors ($C-\psi_S$ method). We confirmed by an agreement with the conductance methods that the proposed method gives an accurate surface potential and interface state density. Significant fast-interface-states exist that respond to 1 MHz, which results in an overestimation of the surface potential if it is determined by the flatband capacitance of 1 MHz. The overestimation of surface potential results in the interface state density at a specific energy level being underestimated by the underestimation of E_C-E_T. The high-low method using a high frequency of 1 MHz underestimated the interface state density because the fast interface states cannot be detected. The high-low method using a high frequency of 100 MHz gave an accurate interface state density because 100 MHz is almost sufficient for the fast states not to respond.

In this paper, the proposed methods were only applied for the dry-oxide MOS capacitor. We have also investigated the NO-nitride MOS capacitors with low interface state density, and we have found that the proposed methods have additionally given valuable information. By detailed investigations and analyses, we confirmed that the proposed $C-\psi_S$ method gives accurate interface state density for the NO-nitride MOS capacitors. These results will be presented in a subsequent publication.

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