Accurate Testing of ADC's Spectral Performance Using Imprecise Sinusoidal Excitations

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Abstract

Analog to Digital Converter (ADC) is the world's largest volume mixed-signal circuit. It is also a key building block in nearly all system on chip (SoC) solutions involving analog and mixed-signal functionalities. ADC testing is also crucial for built-in-self-test (BIST) solutions of AMS testing in SoC technology which is identified by the ITRS as one of four most daunting SoC challenges. ADC spectral testing is of critical importance to a large class of integrated circuits and is particularly challenging for high speed and/or high resolutions circuits. In this paper we use Spectrally Related Excitations (SRE) to accurately test the spectral performance of ADCs. Unlike standard approaches, the SRE approach uses low-cost imprecise sine signals as input to the ADC and uses the spectral relationship between multiple input signals to separate distortion inherent in the ADC from that in the input. Efficient DSP algorithms are used to determine the true spectral performance of the ADC. This approach works in both production test and BIST environments. Simulation results show two sine waves with < 60 dB purity can be used to accurately test spectral performance of high resolution ADCs with SFDR in excess of 100 dB. The low-cost SRE signals can be readily generated with simple RC filters with lax band edge requirements. Extensive simulation shows that the algorithm is robust to filter errors, to nonstationarity in the test environment, and to measurement noise.

1. Introduction

As the world's leading volume mixed-signal circuit, ADC testing represents one of the most challenging AMS testing tasks. Parametric specifications such as DNL and INL measure the ADC's static performance and are critically important to instrumentation applications, medical applications, image processing, and so on, in which accuracy of each converted code is of major concern. Production test of static linearity of high resolution ADCs is challenging and costly due to long test times per unit and large investments in commercial mixed-signal testers. Furthermore, as the industry integrates increasingly more functionalities into a single chip, analog and mixed-signal components become deeply embedded and testing access becomes increasingly difficult. Built-in-self-test solutions of AMS testing become critical in solving ITRS's one of the four "most daunting SoC challenges." [1] As the most fundamental building block, cost effective testing of ADC plays a key role.

Many attempts have been made to provide built-in-self-test (BIST) solutions to ADC linearity testing to reduce costs associated with using testers and to enable testing of deeply embedded SoCs. Excellent examples include the work of Roberts, Azais, Sanchez, and many others [e.g. 2-7]. Invariably, their approaches have been aimed at replicating a standard tester on a chip. Unfortunately, these approaches have found little industrial adoption. A fundamental problem with these approaches is their need for a highly accurate signal to stimulate the DUT. Requirements for the stimulus input are typically substantially more precise than those of the DUT making the signal generator more challenging to design than the DUT itself and raising the question of whether a test circuit is also needed for the signal generator! Recently, the authors' group developed a new approach for ADC static linearity testing in which two functionally related easy-to-generate signals are used to accurately characterize the ADC. The approach was validated by extensive simulation and experimental results obtained in industry in which 7 bit linear signals were used to test a 16 bit ADC achieving comparable results to those obtained by a state-of-the-art mixed-signal tester with 20 bit linear ramp signals. [8, 9]

In many applications, spectral measures such as SFDR, SINAD, THD, IMD, SNR, etc. that characterize the dynamic performance of the ADC are of critical importance. Both the static errors and dynamic errors degrade spectral performance. Dynamic errors refer to the additional sources of error introduced by the time variation of the analog signal being sampled. Sources include harmonic distortion from the analog input stages, signal-dependent variations in the time of samples, dynamic effects in amplifiers and comparators, and frequency-dependent variations in threshold levels. The discrete Fourier transform (DFT) is used extensively for frequency domain analysis and is the prevalent technique used for spectral performance testing. [10-12] According to the IEEE standard on ADC testing, input sine wave signals must have spectral purity far exceeding the targeted performance of the ADC under test. This is because practical sine waves contain harmonic distortion components that corrupt the ADC output. To ensure testing accuracy, standard approaches require input sine signals to be at least 10 times or 3 bits more accurate than the ADC under test. For example, if ADCs with targeted 16-bit SFDR performance are to be tested, the input sine wave signal should have its largest harmonic distortion component at the –118 dB level or lower. Such high purity sine waves are very challenging to obtain and are virtually impossible in a built-in-self-test environment.

In this paper, we introduce a new spectral testing technology that uses two low-cost Spectrally Related Excitations (SRE) to accurately determine the spectral performance of ADCs. Section 2 describes the SRE approach and shows how two imprecise sine inputs with spectral relationship can be used to separate the distortion inherent in the ADC from that in the input and determine the true spectral performance of the ADC. Section 3 provides simulation results showing that two < 60-dB-pure sine waves can be used to accurately test spectral performance of high resolution ADCs with SFDR in excess of 100 dB. Extensive simulation also shows that the SRE approach is robust to filter errors, to nonstationarity in the test environment, and to measurement noise.

2. Accurate spectral testing with imprecise sine inputs

An ADC is a device that converts a continuous time signal x(t) into a discrete-time quantized-amplitude signal y(t). In the ideal case, y(t) will only differ from x(t) by a quantization error Q(t) which is bounded by $FS/2^n$ where FS is the full scale range of the ADC input and 2^n is the total number of quantization levels of an n-bit ADC. However, due to unavoidable errors in the manufacturing of the device, an actual ADC will have y(t) deviate from its desired values, causing the ADC's behavior to be nonlinear.

In the frequency domain, the ADC linearity is measured with

several spectral specifications. Let the ADC input x(t) be a pure sine wave. The ADC output y(t) ideally should be a pure sine wave. However, static and dynamic non-idealities of the ADC will cause y(t) to differ from a pure sine wave. The spectral contents of $y(t)$, denoted as Y(f), should be ideally a spectral line at the input signal frequency, but nonlinearities of the ADC will cause spectral lines to appear at harmonics frequencies in the output spectrum. The spectral values at these harmonic frequencies measure the amount of nonlinearity in the ADC and are called harmonic distortion. Total harmonic distortion (THD) measures the total power of all the harmonic distortion components divided by the intended signal (or the first harmonic) power. Spectral lines persistent at frequencies other than the harmonic frequencies are spurious distortion components. The spurious-free dynamic range (SFDR) of an ADC measures the ratio of the output signal amplitude to the amplitude of the largest harmonic or spurious spectral component observed over the full Nyquist band. Both THD and SFDR are typically expressed in decibels (dB).

As defined above, $x(t) = \sin(\omega t)$ is periodic, the steady state output $y(t)$ is also periodic and admits a Fourier series representation. Suppose the input sine wave and the ADC's clock have been synchronized and the ADC's gain error has been corrected, then the output y(t) can be expressed as:

$$y(t) = \sin\omega t + a_2 \sin 2\omega t + b_2 \cos 2\omega t + a_3 \sin 3\omega t + b_3 \cos 3\omega t + \cdots \quad (1)$$

where the a_i and b_i are the Fourier coefficients of $y(t)$ and they are assumed to be much less than 1 in magnitude. The THD and SFDR of an ADC can be calculated by a_i, b_i as:

$$THD = 10\log_{10}\left(\sum_{i\geq 2} a_i^2 + b_i^2\right)$$
$$SFDR = -20\log_{10}\left(\max_{i\geq 2}\sqrt{a_i^2 + b_i^2}\right) \quad (2)$$

Straightforward trigonometric manipulation will lead us to:

$$\begin{aligned} y(t) &= \sin\omega t + a_2 \sin 2\omega t + b_2 \cos 2\omega t + a_3 \sin 3\omega t + b_3 \cos 3\omega t + \cdots \\ &= \sin\omega t + 2a_2 \sin\omega t \cos\omega t + b_2(2\cos^2\omega t - 1) \\ &\quad + a_3 \sin\omega t(3 - 4\sin^2\omega t) + b_3(1 - 4\sin^2\omega t)\cos\omega t + \cdots \\ &= \sin\omega t + 2a_2 \sin\omega t \cos\omega t + b_2(1 - 2\sin^2\omega t) \\ &\quad + a_3 \sin\omega t(3 - 4\sin^2\omega t) + b_3(1 - 4\sin^2\omega t)\sqrt{1 - \sin^2\omega t} + \cdots \end{aligned} \quad (3)$$

To avoid unnecessary algebraic complication, higher order terms are not carried in the equations. Since $\sin(\omega t) = x(t)$ in Equation (3), $y(t)$ can be expressed as a function of $x(t)$ as follows:

$$y(t) = x + 2a_2 x\sqrt{1-x^2} + b_2(1-2x^2) + 3a_3 x - 4a_3 x^3 + b_3\sqrt{1-x^2} - 4x^2 b_3\sqrt{1-x^2} + \cdots \quad (4)$$

This equation forms the bases for us to develop the mentioned key relationships among the distortion components of the ADC and its input/output signals in the SRE approach. First let us feed an imprecise sinusoidal signal $x_1(t)$ to the ADC input and denote the corresponding ADC output steady state response by $y_1(t)$. Since x_1(t) is imprecise, it is no longer a pure sine wave. Instead it is a periodic signal with higher order harmonic distortions. Suppose we can scale the magnitude and synchronize the phase of the input signal, we can assume, without loss of generality, that $x_1(t)$ has the following Fourier Series form:

$$x_1(t) = \sin\omega t + \alpha_2 \sin 2\omega t + \beta_2 \cos 2\omega t + \alpha_3 \sin 3\omega t + \beta_3 \cos 3\omega t + \cdots \quad (5)$$

where $|\alpha_i|$, $|\beta_i|$ <<1 describe the harmonic distortion components of the imprecise input sine wave. They are assumed to be much less than 1 since sine waves with about 0.1% distortion are relatively easy to generate in practice.

The ADC's output response will have distortions that are the combined effect of the input distortion and the ADC's harmonic distortion. Nevertheless, $y_1(t)$ is also going to be a periodic signal. Substituting x by $x_1(t)$ in Equation (4) and neglecting all terms with higher order products of a_i, b_i , α_i, and β_i, it can be shown after lengthy trigonometric algebra that $y_1(t)$ has the following Fourier Series representation:

$$\begin{aligned} y_1(t) &= \sin\omega t + (a_2 + \alpha_2)\sin 2\omega t + (b_2 + \beta_2)\cos 2\omega t \\ &\quad + (a_3 + \alpha_3)\sin 3\omega t + (b_3 + \beta_3)\cos 3\omega t \\ &\quad + \cdots + (a_i + \alpha_i)\sin i\omega t + (b_i + \beta_i)\cos i\omega t + \cdots \end{aligned} \quad (6)$$

which is surprisingly simple but very intuitive. Here again, we have, without loss of generality, assumed that the ADC's gain error and offset error have been corrected. Otherwise, a simple scaling and DC shift will be needed. The DC component will not affect the computation of the spectral lines at nonzero frequencies. The scaling factor due to gain error will not affect the computation of the spectral specifications since these specifications are computed with a normalized first harmonic.

If a coherent data record of the output y_1(t) is obtained, it can be transformed into the spectral domain via FFT to get $Y_1(f)$. Let

$$h_{y1\,i} = Y_1(f)\,|_{i-th\,harmonic} \quad (7)$$

where h_{y1i} is the spectral line at the i-th harmonic of $y_1(t)$. From Equations (6) and (7) and relationship between Fourier Series and Fourier Transform, we can be obtain:

$$b_i + \beta_i - j(a_i + \alpha_i) = 2h_{y1i} \quad \textit{for all } i \quad (8)$$

From Equation (8), we can get the relationships between harmonic distortion components of the input imprecise sine wave x_1(t), those of the ADC's steady state output response y_1(t), and the ADC's harmonic distortion as defined with a pure sine wave stimulus, namely:

$$h_{y1\,i} = h_{x1\,i} + h_{ADC\,i} \quad \textit{for all } i \quad (9)$$

Therefore, if the input harmonics can be identified, the following equation can be used to identify the ADC's harmonic distortion.

$$h_{ADB\,i} = h_{y1\,i} - h_{x1\,i} \quad \textit{for all } i \quad (10)$$

To facilitate the isolation and identification of the input harmonic distortion and the ADC harmonic distortion, we generate a second signal x_2(t) by passing x_1(t) through a simple low pass filter as depicted in Figure 1 where SF is a scaling factor.

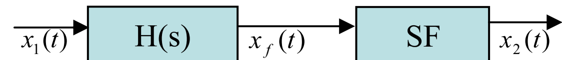

Figure 1. Diagram of how x_1(t) is generated

For simplicity, the transfer function for the low pass filter is selected to be:

$$H(j\omega) = \left(j\frac{\omega}{\omega_0} + 1\right)^{-1} \quad (11)$$

where ω_0 is the corner frequency of the low pass filter. Let $X_f(j\omega)$, $X_1(j\omega)$ be the Fourier transform of x_f(t), x_1(t) respectively. From the above diagram, we have:

$$X_f(j\omega) = H(j\omega)X_1(j\omega) \quad \{12)$$

The coefficient of the fundamental component of x_f(t)

$$h_{f1} = \frac{1}{2}(\beta_1 - j\alpha_1)\left(j\frac{\omega}{\omega_0} + 1\right)^{-1} = j0.5\left(j\frac{\omega}{\omega_0} + 1\right)^{-1} \quad (13)$$

Notice that here we are using a slight abuse of notation and are denoting both the independent variable frequency of the filter and the fundamental frequency of the first input signal by the same notation ω. The coefficient of the i-th (for all i) harmonic of x_f(t)

will be given in Equation (14).

$$h_{fi} = (\beta_i - j\alpha_i)0.5\left(j\frac{i\omega}{\omega_0}+1\right)^{-1} \qquad (14)$$

In order for x_2(t)'s fundamental component to be sinωt or the base harmonic spectral line to be j/2, the scaling factor SF should be $j\omega/\omega_0 + 1$. Therefore the coefficient of the *i*-th harmonic of x_2(t) is given as the following:

$$h_{x2\,i} = \frac{1}{2}(\beta_i - j\alpha_i)\left(j\frac{\omega}{\omega_0}+1\right)\left(j\frac{i\omega}{\omega_0}+1\right)^{-1} \qquad (15)$$

Since x_2(t) is also periodic, using it as an input to the ADC, we can similarly get another periodic signal y_2(t) as the steady state output response of the ADC. In the time domain, y_2(t) is given as:

$$\begin{aligned} y_2(t) = {} & \sin\omega t + (a_2 - 2\,\mathrm{Im}(h_{x_2 2}))\sin 2\omega t + (b_2 + 2\,\mathrm{Re}(h_{x_2 2}))\cos 2\omega t \\ & + (a_3 - 2\,\mathrm{Im}(h_{x_2 3}))\sin 3\omega t + (b_3 + 2\,\mathrm{Re}(h_{x_2 3}))\cos 3\omega t \\ & + \cdots + (a_i - 2\,\mathrm{Im}(h_{x_2 i}))\sin i\omega t + (b_i + 2\,\mathrm{Re}(h_{x_2 i}))\cos i\omega t + \cdots \end{aligned} \qquad (16)$$

If the Fourier transform of this output is taken and the spectral lines at various harmonic frequencies are denoted by

$$h_{y2\,i} = Y_2(f)\,|_{i-th\ harmonic}$$

we can get another set of harmonic balance equations for all *i*:

$$\left[2\,\mathrm{Re}(h_{x2\,i}) + b_i\right] - j\left[-2\,\mathrm{Im}(h_{x2\,i}) + a_i\right] = 2h_{y2\,i} \qquad (17)$$

After combining Equations (9) and (17), the following matrix equations can be obtained for each i,

$$\begin{bmatrix} 0 & 1 & 0 & 1 \\ -1 & 0 & -1 & 0 \\ 0 & 1 & -\dfrac{\omega\omega_0(i-1)}{i^2\omega^2+\omega_0^2} & \dfrac{i\omega^2+\omega_0^2}{i^2\omega^2+\omega_0^2} \\ -1 & 0 & -\dfrac{i\omega^2+\omega_0^2}{i^2\omega^2+\omega_0^2} & \dfrac{\omega\omega_0(1-i)}{i^2\omega^2+\omega_0^2} \end{bmatrix} \cdot \begin{bmatrix} a_i \\ b_i \\ \alpha_i \\ \beta_i \end{bmatrix} = \begin{bmatrix} 2\,\mathrm{Re}(h_{y1\,i}) \\ 2\,\mathrm{Im}(h_{y1\,i}) \\ 2\,\mathrm{Re}(h_{y2\,i}) \\ 2\,\mathrm{Im}(h_{y2\,i}) \end{bmatrix} \qquad (18)$$

From Equation (18), a_i, b_i can be calculated using the two sets of data records from $y_1(t)$ and $y_2(t)$. Once a_i, b_i are known, we can substitute a_i, b_i into Equation (2) to calculate SFDR or THD.

3. Simulation Results

The SRE approach is applied to spectral performance testing of high-resolution flash ADCs. A flash ADC is chosen because it has more independent error sources and is more challenging to fully characterize than most other structures. Specifically, an imperfect n-bit ADC is generated with random resistor mismatch in the R-string. Using an ideal sinusoid and FFT, the true spectral performance of the ADC is determined through simulation.

In the SRE approach, simulated low-purity sine waves are used as the input signals to test the ADC's spectral performance. To do this, harmonic distortions are randomly added to a pure sine wave to form the first input signal x_1(t). The spectrum of the first input signal x_1(t) in one particular run is shown in Figure 2.

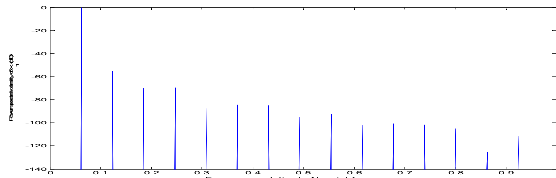

Figure 2. Spectrum of imprecise sinusoidal input signal

As can be seen, x_1(t) has many harmonic distortion components. The second harmonic has power at the –55.1 dB level relative to the full-scale signal power. Hence the purity of x_1(t) is only 55.1dB, or about 9-bit. The corresponding steady state ADC output signal y_1(t) is recorded and coherent samples are taken for use in FFT. The output spectrum of y_1(t) is displayed in Figure 3. If standard procedures for ADC spectral testing were to be followed with this data record, an incorrect conclusion would be drawn that the ADC had 55 dB SFDR, whereas the true SFDR of the ADC should be 104 dB as verified by ideal sinusoidal testing. The computed SFDR is basically the SFDR of the input signal itself. Hence we have verified that in the standard testing method, a low purity sine wave signal cannot be used as an excitation signal to test the spectral performance of the ADC, since the output spectrum will be corrupted by the input distortion.

The SRE approach uses a second imprecise sine wave input. The second input is obtained by filtering the first imprecise sine wave through a simple low pass filter. By doing so, the spectra of the two imprecise sine waves are related to each other through the filter transfer function. This known relationship is used to correctly estimate the ADC's true spectral performance.

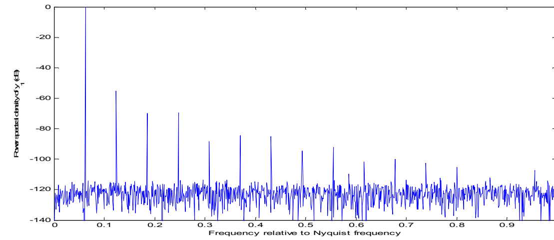

Figure 3. ADC output spectrum with x_1(t) as input

After we obtained the spectra of both Y_1(f) and Y_2(f) we can calculate a_i, b_i, α_i, β_i according to Equation (18). Then equation (2) can be used to calculate SFDR and THD. Figure 4 plots both the true ADC spectrum and the estimated ADC spectrum as computed by the SRE method. The true SFDR is 104.0 dB, measured with infinitely accurate sine input; the estimated SFDR calculated by the SRE method is 104.8 dB. It must be emphasized that the accurate SFDR result from SRE was obtained with input signals with only 55.1 dB purity. This compares with the industry standard which will require an input signal whose purity is 124 dB or 21-bit pure.

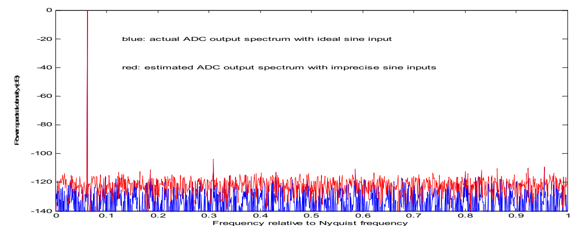

Figure 4. True and SRE estimated ADC spectrum

Robustness to filter bandwidth

In the above simulations, we assume that the low pass filter's corner frequency ω_0 can be adjusted by choosing appropriate R and/or C values so that ω_0 is equal to ω, the base harmonic frequency of the imprecise input sinusoidal signal. However, due to finite tuning ability in R and C, there will be residual mismatches between ω_0 and ω. In this case we can rewrite $\omega_0=\omega(1+\Delta)$. However, this knowledge of the filter mismatch was not known to the algorithms. Even though in real life ADC testing, it is very easy to tune the corner frequency of the filter to be as accurate as .1% mismatch of the frequency of the input signal, we performed extensive simulations for mismatches ranging from 0.1% to 10% in this paper. The simulation results are summarized in table 1. The SFDR and THD columns are testing results with infinite pure sine input and SFDR1 and THD1 are testing results from the SRE

approach using 9-10 bit pure sine wave inputs. Diff is the SFDR difference.

Table 1. Testing results with various filter errors

Δ	Nbit	INL	SFDR	THD	SFDR1	THD1	Diff
0.1%	16	1.7	96.4	-91.6	96.7	-91.7	-0.3
	16	1.4	100.2	-94.5	100.4	-94.6	-0.1
0.3%	15	1.9	88.8	-86.4	88.8	-86.3	0
	16	2.6	93.9	-91.4	94.6	-91.9	-0.7
1%	16	1.2	101.7	-95.5	101	-95.1	0.8
	15	1.3	90.9	-87.4	91	-87.5	-0.1
3%	16	1.5	96.2	-92	96.6	-92	-0.3
	15	1.6	91	-85.7	91.1	-85.9	-0.2
10%	16	1.3	98.9	-94	99.1	-93.9	-0.2
	16	1.6	92.1	-91.1	92.1	-91.1	0

From table 1, it is clear that the accuracy of our algorithm does not deteriorate when the mismatch becomes bigger. Our algorithm is very robust to filter corner frequency errors.

Effects of test environment nonstationarity

In real life testing, the testing environment will not be exactly the same during the time for measuring $y_1(t)$ and $y_2(t)$. In this simulation, we investigate the robustness of the proposed algorithms with respect to the nonstationarity of the testing environment. The most common nonstationarity could be the drifts of the V_{ref} of the signal generator relative to the V_{ref} of ADC under test. In the following simulation results, we model this relative drift between the two reference voltages by a linear gradient error in V_{ref} of the input signal with respect to time. Other types of gradient errors could be easily handled but were omitted here. Table 2 summarized the SFDRs for different ppm per minute linear gradients in V_{ref}. From table 2, we can see that the nonstationarity linear gradient does not affect the accuracy of our algorithm.

Table 2. Testing results for various V_{ref} gradients

Grad	Nbit	INL	SFDR	THD	SFDR1	THD1	Diff
50ppm	16	2.3	91.9	-90.7	91.9	-90.6	0.1
	17	2.2	102.4	-96.6	102.5	-96.7	-0.1
500	17	1.9	100.7	-97	100.6	-97.2	0
	15	0.9	95.2	-90.6	95.3	-90.4	-0.1
5000	14	1.5	84.8	-81	85.2	-81.6	-0.4
	15	1.2	89.5	-88.3	89.8	-88.6	-0.3
50000	15	1.2	96.3	-90.5	95.9	-90.8	0.4
	15	1.1	91.5	-89.4	91.2	-89.1	0.3

Effects of measurement noise

There will be some additive noise to the input signal in real life ADCs. This noise would cause the ADC's noise floor in the spectrum to be higher. If the noise floor is as high as the largest harmonic distortion component, it will be very difficult to get the accurate SFDR for the ADC. In this simulation, we investigate the performance of our new algorithm in the presence of additive noise at the ADC input node. In the following simulations, σ is the standard deviation of the random noise added to the imprecise input signal. From table 3, we can see that our algorithm can give very accurate SFDR reading when σ <= 1 LSB. Notice that the SFDR and THD columns represent ideal sine wave testing without additive measurement noise.

Table 3. Testing results with various levels of input additive noise

σ	Nbit	INL	SFDR	THD	SFDR1	THD1	Diff
0.1	16	1.3	104.8	-98	106.1	-98.4	-1.2
	16	2.3	92.1	-90.7	92.1	-90.6	-0.1
0.3	16	2.6	94.5	-89.9	94.5	-90.2	0
	15	1.6	94.9	-89.8	94.6	-89.6	0.3
1	18	3.8	103.4	-98.4	103	-98.3	0.4
	17	3.4	95.9	-91.9	95.6	-91.7	0.3
3	14	0.5	92	-89.8	85.9	-78	6.1
	16	1.2	100.3	-96.1	98.7	-90	1.6
6	14	0.7	92.9	-88.9	80.6	-71.9	12.2
	14	1.8	81.4	-79.8	75.0	-70.4	6.4

4. Conclusion

We have presented the SRE approach to accurate spectral performance testing for high resolution ADCs. Unlike standard approaches to ADC spectral testing which require excitation signals that are a decade or 3 bits better than the target performance of the ADC, the new approach uses two spectrally related, low-cost, easy-to-generate, 9-10 bit pure sine wave signals to excite the ADC. The spectral relationship between the two excitations is used to separate the distortion inherent in the ADC from that in the input. DSP algorithms can then be used to compute the ADC spectral performance without being affected by the errors in the input signal. Simulation results show that 9-10 bit pure sine waves can be used to accurately test ADCs with over 100 dB SFDR performance. The approach is also shown to be robust to filter errors, to test environment nonstationarity, and to additive input noise.

The SRE approach offers immediate significant cost saving in ADC testing that is currently done with very expensive testing equipment. It also offers a solution to certain high end parts for which there exist no viable spectral testing solutions currently. Since the proposed approach uses easy-to-generate signals that can be readily implemented on chip, it can be fully integrated to provide a low-cost BIST solution to ADC testing in SoC.

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