

# Active Counter Electrode in a-SiC Electrochemical Metallization Memory

K. A. Morgan<sup>a</sup>, J. Fan<sup>b</sup>, R. Huang<sup>a</sup>, L. Zhong<sup>b</sup>, R. Gowers<sup>b</sup>, J. Y. Ou<sup>a</sup>, L. Jiang<sup>b</sup>, and C. H. De Groot<sup>a</sup>

<sup>a</sup>Faculty of Physical Sciences and Engineering, University of Southampton, UK

<sup>b</sup>Faculty of Engineering and the Environment, University of Southampton, UK

E-mail: [kam2g11@soton.ac.uk](mailto:kam2g11@soton.ac.uk)

**Abstract:** Cu/amorphous-SiC (a-SiC) electrochemical metallization memory cells have been fabricated with two different counter electrode (CE) materials, W and Au, in order to investigate the role of CEs in a non-oxide semiconductor switching matrix. In positive bipolar regime with Cu filaments forming and rupturing, the CE influences the OFF state resistance and minimum current compliance. Nevertheless, a similarity in SET kinetics is seen for both CEs, which differs from previously published SiO<sub>2</sub> memories, confirming that CE effects are dependent on the switching layer material or type. Both a-SiC memories are able to switch in the negative bipolar regime, indicating Au and W filaments. This confirms that CEs can play an active role in a non-oxide semiconducting switching matrix, such as a-SiC. By comparing both Au and W CEs, this work shows that W is superior in terms of a higher R<sub>OFF</sub>/R<sub>ON</sub> ratio, along with the ability to switch at lower current compliances making it a favourable material for future low energy applications. With its CMOS compatibility, a-SiC/W is an excellent choice for future resistive memory applications.

## 1. Introduction

Resistive memory is a potential new type of non-volatile memory, with simple structures, high density and low power. Very promising resistive memories have been demonstrated using an array of materials, including metal-oxides such as TiO<sub>2</sub>, HfO<sub>2</sub> and ZrO<sub>2</sub>, and solid electrolytes such as Ag<sub>2</sub>S and GeSe [1-3]. The majority of these materials however require atomic layer deposition (ALD). Compared to sputtering, ALD is slower, more expensive with low-throughput and is not available in all CMOS labs. Adding these non-native new materials to the technology line increases the cost and complexity of fabrication.

SiC is a promising material for embedded resistive memory because it can be integrated in the back-end-of-the-line as SiC is already commonly used for CMOS interlayer dielectrics [4-6]. SiC resistive memory can therefore be incorporated easily into the CMOS fabrication line, resulting in a low cost and simple approach to integrating RRAM into mature CMOS architecture. It has been shown recently that amorphous SiC (a-SiC) based resistive memories present high state stability and high R<sub>OFF</sub>/R<sub>ON</sub> ratio. With this and its extremely high ionizing radiation tolerance, it is very suited for use in harsh and space environments [7].

SiC resistive memory is a type of electrochemical metallization memory (ECM); traditionally this is described as a metal-insulator-metal structure with an active electrode, an ion conductor and an inert CE [8]. When sufficient bias is applied, the metal ions in the active electrode oxidise and dissolve into the ion conductor. These metal cations then travel through the ion conductor layer and reduce on the inert electrode, building up a metallic filament. The active electrode is often Ag or Cu, resulting in Ag and Cu filaments [3].

The ion conductor layer has been shown to play a crucial role on the transport and kinetics of ECM cells [8]. Large areas of work have also been conducted showing the importance of the active electrode material, due to its direct role in filament formation and rupturing. The role of the CE however has been largely overlooked, where in many cases it was assumed to be physically and chemically inert, disregarding its effects on the resistive memory characteristics [9-14]. In

2014 however, Yang et. al. was the first to demonstrate the diffusion of inert metals, using Ni and Pt in SiO<sub>2</sub>, both of which had previously been treated as inactive [15]. More recently, Wang et. al. reported similar effects, showing repeatable resistive switching with Pd in a SiO<sub>x</sub> matrix [16].

The CE reaction is thought to be rate limiting for the total cell reaction, where possible CE reactions include reduction of the switching matrix, reaction of residual oxygen or oxygen ions and redox reaction of moisture [17-18]. Studies into the theory of CE effects in SiO<sub>2</sub> memories, linked to moisture, were firstly discussed by Tappertzhofen et. al. in 2014. More recently, CEs were shown to influence SiO<sub>2</sub> cells in terms of ion concentration, affecting device behaviour before switching [19]. The electrochemical activity following a switching event also exhibited the same trend, whereby metal ion concentration influenced the SET kinetics [20].

Currently the literature demonstrating the electrochemical activity of inert electrodes is mostly based upon oxide switching layers such as SiO<sub>2</sub> and Ta<sub>2</sub>O<sub>5</sub> [17]. The process however has been shown to be material dependent in terms of the switching layer, where Pd and Pt CE filamentary formation was seen in SiO<sub>2</sub>, but was not possible in Al<sub>2</sub>O<sub>3</sub> and HfO<sub>2</sub> [18]. As Valov et al. states in [17], a generalisation for CE effects cannot be made for all resistive memories; rather, each switching material should be looked at individually. This work aims to investigate the role of CEs in a semiconducting non-oxide switching layer, to further understand the role of CEs in ECM memories.

Previously nonpolar switching was observed in non-oxide switching cell, Cu/a-SiC/Au [21], indicating the active role of the CE, although no CE comparison was conducted. In order to further understand the role of the CE on a-SiC switching matrix, Cu/a-SiC resistive memory is fabricated and electrically measured, with two different CEs. This stable switching material, a-SiC, is ideal for studying effects of CEs, with large R<sub>OFF</sub>/R<sub>ON</sub> ratios enabling any small change caused by the electrodes to be detected.

In this work, the “inert” CEs are Au and W, commonly used in resistive memories [22-26]. In order to investigate the effects of the CEs in a-SiC, firstly the positive bipolar regime, theoretically based upon active (Cu) filaments, is measured for both Au and W cells. DC and pulsed measurements are measured whereby conduction mechanisms, area dependency, multi-level switching and pulsed time dependencies are investigated and compared for Au and W memories. The role of CE filaments is particularly evident in the negative bipolar regime, indicating Au and W filaments.

## 2. Methods

Amorphous SiC Cu/a-SiC/Au and Cu/a-SiC/W memory cells were fabricated at the Southampton Nanofabrication Centre cleanroom facility. 1 μm thick SiO<sub>2</sub> was thermally grown on Si wafers, electrically isolating the resistive memory stack above from the Si wafer. 300nm layer of Au and/or W was deposited via non-reactive magnetron sputtering forming the bottom electrodes. A 250nm layer of SiO<sub>2</sub> was deposited next, followed by photolithography and reactive ion etching, thus creating the active device areas. A 40nm layer of a-SiC was deposited, directly followed by a 300nm layer of Cu using RF and DC sputtering, respectively. The final devices were created using lift off.

Both types of CE memory cells were measured using both DC and pulsed setups. The DC setup allow detailed IV sweeps to be obtained whilst providing vital information about the conduction mechanism. Pulsed measurements replicate the switching regime that resistive memory would undergo when used for information storage and processing.

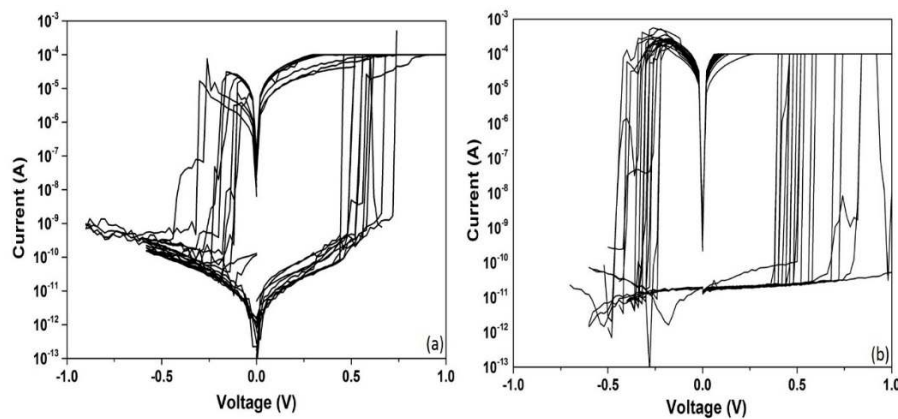
DC measurements were conducted using an Agilent B1500A device parameter analyser by applying voltage to the top Cu electrode and grounding the Au/W electrodes. All memory cells were first formed, followed by cycles of SET and RESET with a current compliance of 0.1mA during SET. Pulsed IV sweeps were conducted using a Keithley 4200-SCS semiconductor characterisation system with pulse widths ranging from 500 $\mu$ s to 0.5s.

### 3. Results and Discussion

The positive bipolar regime for memory cells with Au and W CEs will be demonstrated first, followed by the negative bipolar regime.

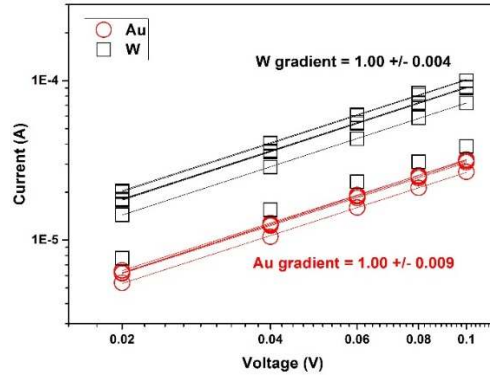
DC sweeps for typical Cu/a-SiC with Au and W CEs are shown in Fig. 1. Both show repeatable positive bipolar switching with distinctive  $R_{OFF}$  and  $R_{ON}$  maintained for many cycles, indicating the high stability of these a-SiC resistive memories, with very high  $R_{OFF}/R_{ON}$  ratios as seen previously for a-SiC [7,21,27]. The W electrode cell however exhibits an even higher  $R_{OFF}/R_{ON}$   $\geq 2 \times 10^7$ , compared to the Au electrode cell, due to a lower OFF state current.

Previous work demonstrated an increase in OFF state resistance can be caused by a presence of an oxide barrier at the counter electrode, for materials with high oxygen affinity, such as W [19]. A change in resistance and presence of an oxide barrier has been related to the ion concentration. In [19], fifteen CE materials in a Cu/SiO<sub>2</sub> memory were compared; W was found to have one of the highest ion concentrations during anodic oxidation of the active electrode, whereas Au had one of the lowest, related to a redox reaction. Thus the increased OFF state resistance seen in this work for W, compared with Au, could be attributed to an oxygen layer formed by a redox process, due to the presence of moisture. The moisture for this process is likely to originate from the fabrication processes that are performed after the W and Au layers are deposited. As W has a higher affinity to oxygen than Au, moisture would more likely affect the W memories, leading to a lower OFF resistance.



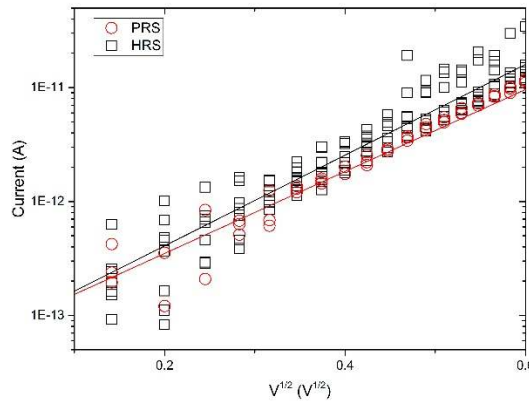
**Fig. 1.** Typical DC sweep of ultra-high  $R_{OFF}/R_{ON}$  Cu/SiC resistive memory with CEs of (a) Au and (b) W.

Previously, Cu/a-SiC/Au resistive memories ON state conduction has been identified as metallic Ohmic conduction [28]. To see if changing the CE effects the ON state current, Cu/a-SiC/W is compared to Cu/a-SiC/Au in Fig. 2, for typical memory cells. The same linear relationship between current and voltage confirms the ON state conduction is Ohmic for both memories in positive bipolar regime.



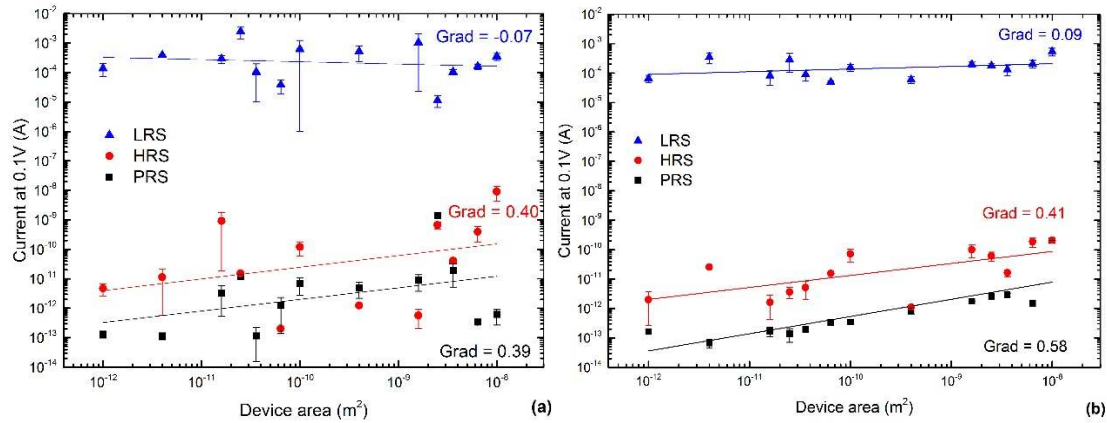
**Fig. 2.** I-V plots of Cu/SiC memories with Au and W electrodes showing the ON state with gradient of 1.00 for both materials indicating ohmic conduction.

The OFF and pristine state conduction for positive bipolar Cu/a-SiC/Au resistive memories has been previously identified as Schottky emission [28]. Fig. 3 shows a linear fit for a  $I-V^{1/2}$  plot for Cu/a-SiC/W, indicating the OFF and pristine state conduction is Schottky emission for W memories as well. The Schottky emission behaviour seen in both memory types originates from Schottky barriers between the metal electrodes and the a-SiC, contributing to their high  $R_{OFF}$ . Differences in  $R_{OFF}$ , whereby W exhibits a higher  $R_{OFF}$  despite Au having a higher work function than W, likely originates due to fermi level pinning, occurring from oxidising/reducing reactions and inter-diffusion at the interface [29].



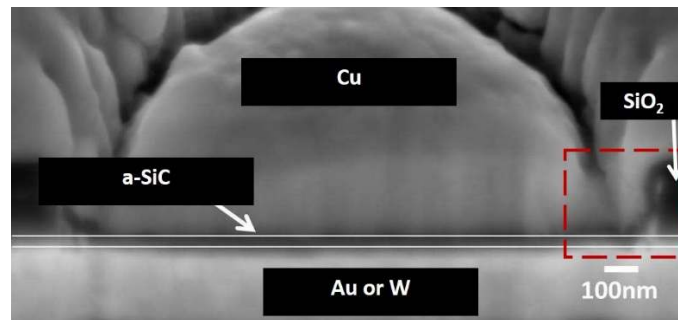
**Fig. 3.** Plot of  $I$  vs  $V^{1/2}$  for pristine (PRS) and high resistance, OFF, state (HRS) of a typical Cu/a-SiC/W device, indicating Schottky emission.

Whilst Ohmic conduction indicates that current is flowing through a metallic filament in the ON state, Schottky emission indicates homogenous conduction rather than filamentary for the OFF state. Area dependency of the current can be measured in order to verify this by identifying homogenous and filamentary conduction. Current vs. area is plotted for both Au and W CE memories, in the ON, OFF and pristine states, as shown in Fig. 4. The ON state for both memories exhibit no area dependency, as seen by a gradient of  $\sim 0$ , indicating that the conduction mechanism is filamentary, in agreement with Ohmic conduction measured in Fig. 2 and in [28]. The similarity between the Au and W memories for ON state conduction in terms of Ohmic behaviour and metallic filamentary conduction is as expected as the active electrode is of the same material, Cu, indicating Cu filaments are responsible.



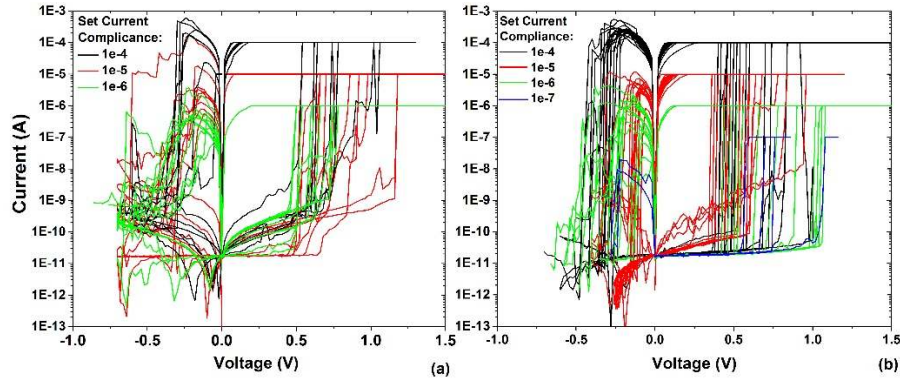
**Fig. 4.** Current vs area for multiple devices of (a) Cu/a-SiC/Au and (b) Cu/a-SiC/W, showing no area dependence in low resistance, ON, state (LRS) for both i.e. filamentary conduction, and perimeter dependence i.e.  $A^{1/2}$ , for pristine (PRS) and high resistance, OFF, state (HRS) for both.

The OFF and pristine states for both memories show a gradient of  $\sim 0.5$ . The area dependency indicates that the dominant conduction mechanism is not due to residual filaments, suggesting that the majority of the filaments fully rupture when switching OFF, leading to extremely high  $R_{OFF}$  and therefore high  $R_{OFF}/R_{ON}$  of a-SiC memory. The square root relation indicates that the current flows mainly around the periphery of the memory cells in the OFF state rather than across the whole area. The reason for this could be due to non-conformal coating of a-SiC over the step layer of  $SiO_2$ , resulting in corner effects, leading to electric field crowding. The layout, with the  $SiO_2$  step, is highlighted in the dashed box in Fig 5.



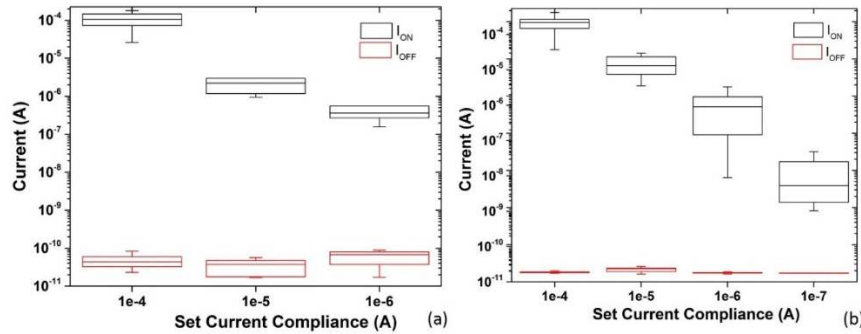
**Fig. 5.** SEM cross section of a-SiC RRAM device [7].

Multilevel positive bipolar switching is obtained by both the Au and W electrode memories, for a high number of repeatable DC cycles as shown in Fig. 6. This was achieved through limiting the SET current compliance, whilst having no current compliance during the RESET. A relationship between the reset current,  $I_{RESET}$ , and the current compliance is seen for both Au and W memories, whereby a smaller current is needed in order for the memories to RESET, when a smaller current compliance is used for the previous SET. A difference arises between the memory types when a low current compliance of  $10^{-7}A$  is used: The W electrode memories successfully SET and RESET with this compliance, whereas the Au electrode memories were unable to SET. This indicates that a higher compliance is needed for Cu filaments to connect successfully with a Au CE, compared to a W electrode, thus showing appropriate selection of a CE choice is imperative for low power applications.



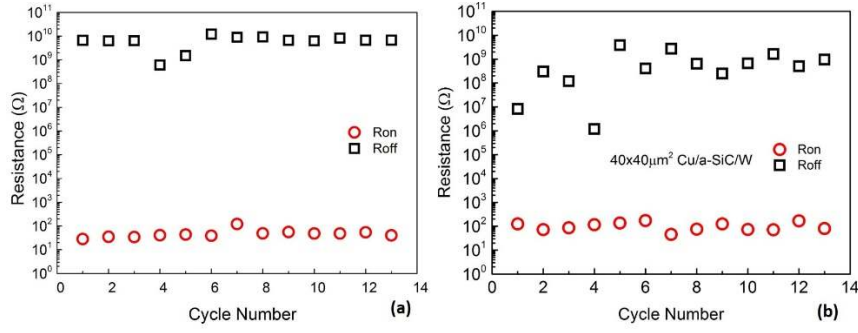
**Fig. 6.** Multi-level switching of (a) Cu/a-SiC/Au and (b) Cu/a-SiC/W using up to four different current compliance levels.

For low power and FPGA applications, the ability to control  $I_{ON}$  is vital. Fig. 7 shows that by varying the current compliance, the ON state current at 0.1V can be varied for both the Au and W electrode memories, for multiple measurements for each level. The box plots show statistical variation between device-to-device and cycle-to-cycle. Due to the initial large  $R_{OFF}/R_{ON}$  window at 0.1mA, both memory types show clear multilevel switching with distinct regions for each level, indicating the great potential for a-SiC memory to be used for multilevel switching.

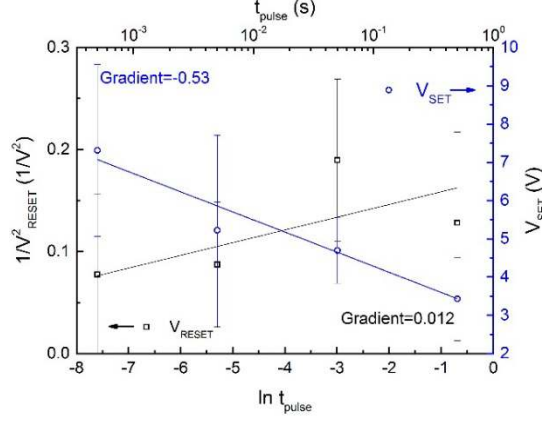


**Fig. 7.** Boxplots of  $I_{OFF}$  and  $I_{ON}$  read during DC cycles, using 0.1V DC read. Different current compliance levels used during SET, reducing  $I_{ON}$ , whilst  $I_{OFF}$  remains unchanged. 3 levels seen for Cu/SiC resistive memories with (a) Au CEs, whilst 4 levels seen for resistive memories with (b) W CEs.

Previously, Cu/a-SiC/Au cells have shown repeatable pulsed switching with the highest  $R_{OFF}/R_{ON}$  ratio for any electrochemical metallization memory of  $R_{OFF}/R_{ON} \geq 10^8$  as shown in Fig. 8a [7]. Typical pulsed switching for W electrode cells is shown in Fig. 8b, with  $R_{ON} \sim 100 \Omega$  and  $R_{OFF} \sim 10^9 \Omega$ . Although this is a very high  $R_{OFF}/R_{ON} \geq 10^7$  compared to literature, the slightly reduced OFF resistance compared to Au memories is attributed to a low  $R_{OFF}$  reading on the fourth cycle. This has been seen previously in other work, where a lack of current compliance in the pulsed regime results in the collapse of  $R_{OFF}/R_{ON}$  [30]. This is not attributed to the role of the W electrode, as evidenced by no degradation seen in OFF resistance for repeated DC cycles, as shown in Fig. 1 and 6.



**Fig. 8.** Pulsed measurements for (a) Cu/SiC/Au with  $R_{ON} \sim 30\Omega$  and  $R_{OFF} \sim 1G\Omega$  and (b) Cu/SiC/W with  $R_{ON} \sim 100\Omega$  and  $R_{OFF} \sim 1G\Omega$ .



**Fig. 9.** Time dependencies of pulsed switching for Cu/SiC/W memories, using pulse widths of  $500\mu s$ - $0.5s$ .

Using pulsed measurements, investigations into the switching kinetics by comparison to an analytical model is performed. By plotting pulse time against SET and RESET voltages, the switching mechanism can be identified as either ion hopping or thermally assisted ion hopping, whilst the ion hopping distance and the filament diameter can be extracted. In comparison to the previously published results for Au [7], Fig. 9 shows the same relation between pulse time and voltages for W memories. The numerical model by Ielmini et al. defines the filament growth rate as:

$$\frac{d\phi}{dt} = Ae^{-\frac{E_{A0} - \alpha qV}{kT_0(1 + \frac{V^2}{8T_0\rho k_{th}})}}$$

where  $\Phi$  is the filament diameter,  $A$  is a constant,  $E_{A0}$  is the energy barrier for ion hopping,  $\alpha$  is the barrier lowering coefficient,  $q$  is elementary charge,  $V$  is the applied voltage,  $k$  is the Boltzmann constant,  $T_0$  is room temperature,  $\rho$  is the electrical resistivity and  $k_{th}$  is the thermal conductivity. The RESET process follows the same equation, with a negative sign inserted on the right.

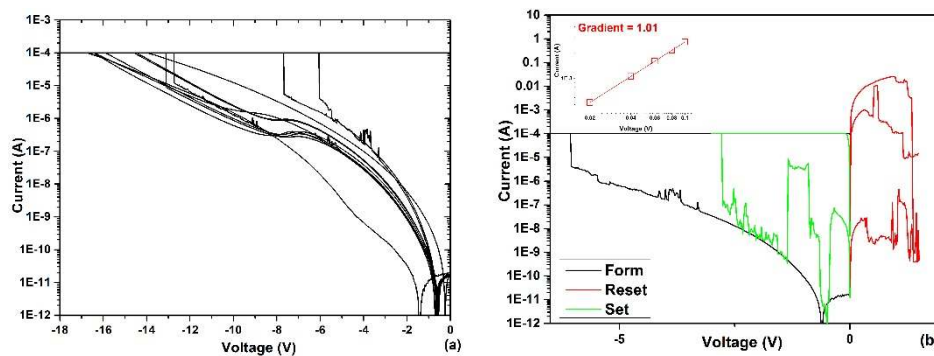
By taking a condition of the numerical model whereby  $\rho k_{th} \gg V^2/8T_0$  or  $\rho k_{th} \ll V^2/8T_0$ , the equations can be reduced, resulting in two pulse time dependencies:

$$\tau_{pulse} \propto e^{\frac{E_{A0} - \alpha qV}{kT_0}} \quad \text{and} \quad \tau_{pulse} \propto e^{\frac{E_{A0} + 8\rho k_{th}}{kV^2}}$$

For both Au in [7] and W presented here, the SET is attributed to ionic motion without joule heating, as shown by the exponential relation between  $V_{SET}$  and  $t_{SET}$  in Fig. 9, whilst the RESET is attributed to ionic motion with joule heating, as shown by the exponential relation between pulse width and  $1/V^2$  in Fig. 9. The CE material has shown to have little effect on the time

dependencies, and thus mechanisms, as both W and Au memories have extremely high OFF resistances, although W is slightly larger, similar ON resistances and both share the same Cu filament thermal conductivity. This is verified by similar ion hopping distances that are extracted for both Au and W memories, whereby Au distance is 1.52 nm and W distance is 1.12 nm. The trend of faster switching speeds seen previously for CEs with higher affinities to oxygen, is not seen here [17]. The difference observations between [17] and this work is most likely to originate from the different switching matrixes, where this work used non-oxide switching matrix, a-SiC, and Valov et. al. used SiO<sub>2</sub>. A difference in CEs does occur however in the filament diameter extraction where Au was estimated to have 4 nm in diameter for filaments in the ON state, whereas W only exhibits approximately 1 nm diameter. This difference in diameter indicates a difference in filament reduction at the CE for a-SiC system.

Using negative bipolar regime i.e. using a negative voltage to form and SET the memory cells, the role of the CE and possible Au and W filaments can be studied. Cu/a-SiC/Au memory cells have already shown to exhibit switching using negative voltage to SET and positive voltage to RESET, as shown by their nonpolar behaviour in [21]. Cu/a-SiC/W memory cells show similar behaviour whereby negative voltages can be used to form these memories as shown by multiple devices in Fig. 10a. Some memory cells are also capable of being RESET and SET, resulting in the same high R<sub>OFF</sub>/R<sub>ON</sub> ratio seen for the positive bipolar regime, as shown in Fig. 10b, albeit at a much lower yield compared to positive bipolar regime. As Cu is more mobile than W and Au, it is expected that these memories are easier to switch in the positive regime, with Cu filaments, than in the negative regime, with possible Au and W filaments. The ON conduction mechanism for W memories was confirmed as Ohmic as shown by the linear relation in the insert in Fig. 10 (b), which indicates that metallic filaments are being formed. The ability to form and switch in the negative regime with memories that have “inert” Au and W electrodes indicates the possibility of Au and W filaments.



**Fig. 10.** Negative bipolar switching of Cu/a-SiC/W showing (a) forming and (b) subsequent SET and RESET, with insert showing Ohmic conduction as ON mechanism.

Observing possible Au and W filaments in this work indicates that the electrochemical activity of inert electrodes is not only apparent in memories with oxide switching layers i.e. SiO<sub>2</sub>, but in non-oxide semiconducting layers as well. Whilst these inert metals may require a higher electric field for migration and have lower electrochemical activity compared to traditionally active electrodes such as Cu, the generalisation that inert electrodes are inactive is not valid. Careful consideration must be taken when selecting the switching layer/CE structure for resistive memories.

#### 4. Conclusion



By studying resistive memories with two different types of CE materials, Au and W, the role of the CE was studied for a non-oxide semiconducting switching matrix. This was performed in both positive bipolar, allowing the effects of the CE on the active filament e.g. Cu, to be studied, and the negative regime, looking into potential CE filaments e.g. Au and W.

In the positive bipolar regime, both Au and W memories exhibited high  $R_{OFF}/R_{ON}$  ratios, indicating the high stability and potential of a-SiC resistive memory, and have the same conduction mechanism of Ohmic in the ON state and Schottky emission in OFF state. The  $R_{OFF}$  of the W memory was found to be slightly higher, potentially originating from an oxide barrier at the W/a-SiC interface, due to W's higher affinity to oxygen than Au. The lack of area dependency in the ON state for both memory types indicates filamentary conduction, whilst a square root area dependency for the OFF state and pristine, PRS, suggests the OFF current may in part originate from the perimeter of the devices rather than solely from residual filaments. Both memories show great potential for multi-level switching due to the extremely high  $R_{OFF}/R_{ON}$ , indicating a-SiC memory is promising for FPGA applications. In particular, Cu/a-SiC/W memories, with abilities to switch at low current compliances due to lower  $R_{OFF}$ , makes W a preferred electrode material as in comparison with Au for potential low energy applications. Pulsed measurements allowed the Cu filament growth mechanisms to be investigated further whereby the W memories were estimated to have 1 nm Cu filament diameter compared to a larger 4 nm Cu filament diameter estimated for Au. This difference, along with the reduced  $R_{OFF}$  and ability to switch at lower current compliances, indicate that CE materials effects the active electrode filament, and memory as a whole, when using a semiconducting switching matrix. The SET kinetics for the Au and W memories were seen to be similar, unlike previous  $\text{SiO}_2$  memories which showed faster SET switching speeds for CE's with higher oxygen affinities [20], which in this case would be W. This indicates that CE effects on SET switching kinetics are absent in a-SiC and perhaps for non-oxide semiconducting memories.

Using negative voltages, both Au and W have been formed and SET with evidence of Au and W filaments, illustrating the CE is not inert in an a-SiC system. Superior resistive memory properties exhibited by the W electrode, along with its CMOS compatibility, indicates W is a strong choice for future CEs for a-SiC resistive memory.

In this work, the CE in an a-SiC system has been shown to play an active role. Differing CE effects seen here for a-SiC, in comparison to CE effects seen for  $\text{SiO}_2$  and  $\text{Ta}_2\text{O}_5$  [17], confirms that CE effects differ depending on the switching layer material [18]. Resistive memory is made up of a huge array of materials and combinations; being able to predict and control the effects caused by material combinations is vital for the future of this research field. This work, with a-SiC, non-oxide semiconducting switching layer, complements previous work, adding to the understanding of CE effects in resistive memories.

## 5. Acknowledgements

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## 6. References

- [1] Wong H S P et al. 2012 *Proc. of the IEEE* **100** 6 1951-1970
- [2] Akinaga H and Shima H 2010 *Proc. of the IEEE* **98** 12 2237-2251
- [3] Waser R and Aono M 2007 *Nature Materials* **6** 833-840
- [4] King S W, French M, Bielefeld J and Lanford W A 2011 *J. of Non-Crystalline Solids* **357** 15 2970-2983

- [5] King S W et al. 2013 *J. of Non-Crystalline Solids* **379** 1 67-79
- [6] King S W 2015 *J. Solid State Sci. Technol.* **4** 1 3029-3047
- [7] Morgan K et al. 2015 *AIP Advances* **5** 07712
- [8] Valov I, Waser R, Jameson J R and Kozicki M N 2011 *Nanotechnology* **25** 22 254003
- [9] Valov I 2013 *Chem. Electro. Chem.* **1** 26-36
- [10] Yang Y, Gao P, Gaba S, Chang T, Pan X and Lu W 2012 *Nature Communications* **3** 732 1-8
- [11] Menzel S, Tappertzhofen S, Waser R and Valov I 2013 *Phys. Chem. Chem. Phys.* **15** 6945-6952
- [12] Menzel S and Waser R 2014 *Phys. Status Solidi RRL* **8** 1862-6270
- [13] Yu S, Liang J, Wu Y and Wong H-S P 2010 *Nanotechnology* **21** 46 465202
- [14] Waser R and Aono M 2007 *Nature Materials* **6** 833-840
- [15] Yang Y et al. 2014 *Nature Communications* **5** 4232
- [16] Wang Z et al. 2016 *Nanoscale* **8** 14023-14030
- [17] Valov I and Lu W D 2016 *Nanoscale* **8** 13828
- [18] Valov I, Luebben M, Wedig W and Waser R 2016 *ECS Transactions* **5** 75 27-39
- [19] Tappertzhofen S, Waser R and Valov I 2014 *ChemElectroChem* **1** 8 1239-1421
- [20] Luebben M, Menzel S, Park S G, Yang M, Waser, R and Valov I 2017 *Nanotechnology* **28** 135205
- [21] Zhong L, Jiang L, Huang R and de Groot C H 2014 *AIP Applied Physics Letters* **104** 093507
- [22] Jana D et al. 2015 *Nanoscale Res Lett.* **10** 188
- [23] Peng et al. 2012 *Appl. Phys.Lett.* **100** 072101
- [24] Pan et al. 2010 *Prog. In Nat. Science: Materials International* **20** 1-15
- [25] Liu et al. 2012 *Advances Materials* **24** 1844-1849
- [26] Yu S and Wong H –S P 2011 *IEEE Trans. On Electronic Devices* **58** 5 1352-1360
- [27] Zhong L, Reed P A, Huang R, de Groot C H and Jiang L 2014 *Solid-State Electronics* **94** 98-102
- [28] Zhong L, Reed P A, Huang R, de Groot C H and Jiang L 2014 *Microelectronic Engineering* **119** 61-64
- [29] Kim W-G et al. 2010 *Microelectronic Engineering* **87** 2 98-103
- [30] Kreupl F et al. 2008 *IEEE International Electron Devices Meeting* San Francisco, USA 1-4