Active Gate Delay Time Control of Si/SiC Hybrid Switch for Junction Temperature Balance over a Wide Power Range

Zongjian Li, *Student Member*, *IEEE*, Jun Wang, *Senior Member*, *IEEE*, Linfeng Deng, Zhizhi He, Xing Yang, *Senior Member*, *IEEE,* Bing Ji, *Senior Member*, *IEEE*, and Z. John Shen, *Fellow, IEEE*

***Abstract*—The optimal gate delay time control between the two internal devices to achieve the excellent electrical and thermal performance of the Si/SiC hybrid switch is considerably affected by several factors and requires careful adjustment to suit the different operation conditions of power converters. However, the conventional gate control solution for the hybrid switch applies a fixed delay time to achieve the minimum switching loss at a specific load current, resulting in disparities in junction temperature of internal devices over a wide load range. This effectively reduced the safe operating area by risking one internal switch subjected to overrated junction temperature in a wide range operation with regard to power handling condition. To avoid such a serious risk of reliability degradation or thermal breakdown, a novel active gate delay time control strategy based on the electro-thermal coupling loss model is proposed. The gate delay time was dynamically adjusted and optimized according to the operation conditions of power converters so that the operation junction temperature difference of the two internal devices can be minimized. Experimental results demonstrate that the junction temperature of the hybrid switch decreases by 20ºC at 8kW load condition and its maximum power handling capability increases by 18% without compromising the power converter's efficiency in a 20 kHz Si/SiC hybrid switch based DC/DC buck converter compared with the conventional approach.**

***Index Terms*—SiC MOSFET, IGBT, Hybrid switch, Junction temperature, Control.**

I. INTRODUCTION

SiC power MOSFETs are the center of attention in the race to medium-voltage device innovation to displace silicon IGBTs because of low specific on-resistance, fast switching speed and high switching frequency capability in recent years [1-4]. However, their significantly higher cost/ampere ($/A) are the major roadblocks for the SiC MOSFET's widespread employment in the commercial mainstream power electronics systems [5-6]. In recent years, the Si/SiC hybrid switch of paralleling a high current Si IGBT and a low current SiC MOSFET was reported to achieve an improved cost/performance tradeoff [7-9], which is a promising solution to address the high cost issue of SiC devices [10-13].

The Si/SiC hybrid switch needs optimal gate delay time control between its two internal switches to achieve improved electrical and thermal performance because its gate configuration is different from conventional discrete power semiconductor devices [14-21].When the internal IGBT's turn-off is prior to SiC MOSFET's turn-off for an appropriate gate delay time, zero voltage switching (ZVS) off operation of the internal IGBT and the minimum total turn-off switching loss of the hybrid switch can be achieved [14-17]. When the IGBT's turn-on is prior to SiC MOSFET's turn-on for a very short gate delay time, the hybrid switch can achieve a minimum turn-on switching loss because of the high di/dt during the switching on transient [18-19]. To improve the over current capability of the hybrid switch, the main IGBT turn-on shortly prior and turn-off shortly after the auxiliary SiC MOSFET for a carefully chosen gate control delay time under the heavy load condition is proposed in [20-21]. In [22], the gate control delay time strongly influences the junction temperatures of the two internal devices in converter applications. And even a minor variation of the gate control delay time would induce significant fluctuation of their junction temperatures, which may result in a severe junction unbalance between the two internal devices or a serious risk of thermal breakdown of one internal devices of the hybrid switch under heavy load conditions [23-26].

The optimal gate control delay time of the hybrid switch is influenced by several limiting factors, such as the internal switches' junction temperatures [22], sizing selection [13], packaging choice and parasitic inductance [19], etc. Moreover, it also varies with operation conditions of power converters, such as the load condition and ambient temperature of the hybrid switch based converter [20-21]. The main reason is that adjustment of the gate delay time control can change the distribution of power losses and junction temperatures of the IGBT and SiC MOSFET inside the hybrid switch, and achieve the minimum total power loss or junction temperatures under different operation conditions [22]. However, any gate delay time control determined for

Manuscript received December 25, 2018; revised March 22, 2019; accepted September 2, 2019. Date of current version September 14, 2019. This work was supported by the National Natural Science Foundation of China under grant. (Project *No. 51607182*), and the High Level Assets Assembling Project of Hunan Province under Grant. (Project *No. 2018RS3049*). (*Corresponding author: Jun Wang, Zongjian Li*)

Zongjian Li, Jun Wang, Linfeng Deng, Zhizhi He, Xing Yang, and Z. John Shen are with the College of Electrical and Information Engineering, Hunan University, Changsha 410082, China. (e-mail:lzjq1@hnu.edu.cn, junwang@hnu.edu.cn).

Bing Ji is with the School of Engineering, University of Leicester, University Road, Leicester, LE1 7RH, United Kingdom (e-mail: bing.ji@le.ac.uk)

the specified load current only provides a sole and fixed value in these previous works, which cannot adapt to the requirement of different operating conditions in a real power converter operation and therefore put the device at risk of over temperature or temperature dependent catastrophic failures.

In order to solve this problem, an active gate delay time control strategy with real-time optimized gate delay time adjustment based on the electro-thermal coupling power loss model of the hybrid switch is proposed. The control algorithm aims to achieve the minimum operating junction temperature difference of the hybrid switch's two internal devices without compromising the power conversion efficiency within a wide load condition. The thermoelectric coupling power loss model of the hybrid switch for the DC/DC buck converter is developed and analyzed in Section II. In Section III, the active gate delay time control strategy is introduced. Then the experimental results using the conventional fixed gate delay time control and the active gate delay time control are compared and analyzed. Section IV concludes the paper.

II. ELECTRO-THERMAL COUPLING POWER LOSS OF SI/SIC HYBRID SWITCH

The basic schematic of the Si/SiC hybrid switch is shown in Fig.1. The cost-effective Si/SiC hybrid switch combines the advantages of the high current Si IGBT and the low current SiC MOSFET, and offers smaller conduction loss because most of the load current flows through the SiC MOSFET at a low current level and the Si IGBT at a high current level.

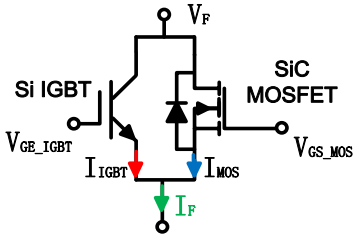


Fig.1.Schematic of a hybrid switch

The specific gate control pattern is preferred for the hybrid switch to reduce the switching loss of the hybrid switch, as shown in Fig.2. T_{on_delay} and T_{off_delay} are the turn-on gate delay time and turn-off gate delay time between the IGBT and SiC MOSFET inside the hybrid switch, respectively. The zero voltage switching (ZVS) off operation of the IGBT is achieved by turning off the IGBT prior to the SiC MOSFET, which can greatly reduce the IGBT's turn-off switching loss induced by tail current. Because the IGBT's turn-on speed is slower than that of the SiC MOSFET, the SiC MOSFET undertakes the hard switching on action and the IGBT is ZVS switching on when the gate turn-on delay time of the hybrid switch is zero.

In order to achieve the real-time optimized gate turn-off delay time adjustment varying with the load conditions of the hybrid switch converter, the Si/SiC hybrid switch's electro-thermal coupling power loss model associated with its gate turn-off delay time for the DC/DC buck converter applications is built and analyzed in this work.

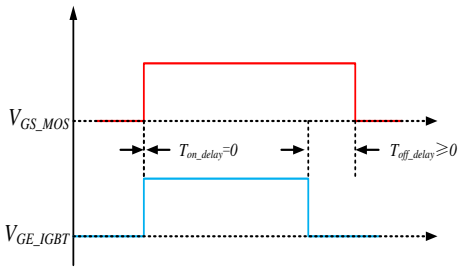


Fig. 2.Gate control pattern of the hybrid switch

A. *Conduction loss of the hybrid switch*

When the forward voltage drop of the hybrid switch is smaller than the knee voltage of the Si IGBT, the forward current fully flows through the SiC MOSFET, and the critical forward current can be derived as

$$I_{MOS} = I_{knee} = \frac{V_{knee}}{R_{ds}} \tag{1}$$

where V_{knee} is the knee voltage of the IGBT, R_{ds} is the specific on resistance of the SiC MOSFET, I_{knee} is the critical forward current of the SiC MOSFET when the forward voltage drop of the hybrid switch is the V_{knee} voltage. When the forward voltage of the hybrid switch larger than the knee voltage of the IGBT, the forward current flows through both the SiC MOSFET and the IGBT. Approximating the on-state characteristic of the IGBT with an equivalent straight line with an intercept of V_{knee} and a slope of R_{ce}, the current distribution between the SiC MOSFET and the IGBT can be derived as

$$I_{MOS} = \frac{R_{ce}}{R_{ce}+R_{ds}} I_F + \frac{V_{knee}}{R_{ce}+R_{ds}} \tag{2}$$

$$I_{IGBT} = \frac{R_{ds}}{R_{ce}+R_{ds}} I_F - \frac{V_{knee}}{R_{ce}+R_{ds}} \tag{3}$$

Where R_{ce} is the equivalent differential on-state resistance of the IGBT, I_F is the total forward current of the hybrid switch. Considering the temperature coefficient of the on state characteristics of the IGBT and SiC MOSFET, V_{knee} and R_{ce} of the IGBT, and R_{ds} of the SiC MOSFET are functions of the junction temperature, respectively, as given by

$$R_{ds}(T_{j\_MOS}) = R_{ds}(25°C) + T_{CR\_MOS}(T_{j\_MOS} - 25°C) \tag{4}$$

$$R_{ce}(T_{j\_IGBT}) = R_{ce}(25°C) + T_{CR\_IGBT}(T_{j\_IGBT} - 25°C) \tag{5}$$

$$V_{knee}(T_{j\_IGBT}) = V_{knee}(25°C) + T_{CV\_IGBT}(T_{j\_IGBT} - 25°C) \tag{6}$$

Where T_{j_MOS} and T_{j_IGBT} are the junction temperatures of the SiC MOSFET and the IGBT, respectively. T_{CR_IGBT} and T_{CV_IGBT} are the temperature coefficients of the IGBT's knee voltage and equivalent on-state resistance, respectively, and T_{CR_MOS} is the temperature coefficient of the SiC MOSFET's specific on resistance. The temperature coefficient of the on-state characteristic can be calculated from the 25℃ and the hot values from the datasheets of the IGBT and SiC MOSFET, e.g. for T_{CR_MOS} applies:

$$T_{CR\_MOS} = \frac{R_{ds}(150°C) - R_{ds}(25°C)}{150°C - 25°C} \tag{7}$$

Therefore, the conduction loss of the SiC MOSFET and the IGBT at a given operating point can be derived as

$$E_{cond\_MOS}(I_F,T_{j\_MOS})=\begin{cases} I_{MOS}^2\bullet R_{ds} & ;\ I_F<I_{knee} \\ (\frac{R_{ce}}{R_{ce}+R_{ds}}I_F+\frac{V_{knee}}{R_{ce}+R_{ds}})^2\bullet R_{ds} & ;\ I_F\ge I_{knee} \end{cases} \quad (8)$$

$$E_{cond\_IGBT}(I_F,T_{j\_IGBT})=\begin{cases} 0; & I_F<I_{knee} \\ (\frac{R_{ds}}{R_{ce}+R_{ds}}I_F-\frac{V_{knee}}{R_{ce}+R_{ds}}) & \\ \times\left[V_{knee}+(\frac{R_{ds}}{R_{ce}+R_{ds}}I_F-\frac{V_{knee}}{R_{ce}+R_{ds}})\bullet R_{ce}\right] & ;\ I_F\ge I_{knee} \end{cases} \quad (9)$$

B. Switching loss of the hybrid switch

The IGBT's turn-off prior to the SiC MOSFET is preferred to achieve the ZVS operation of the IGBT inside the hybrid switch. The typical waveforms of the turn-off process of the hybrid switch consisting of a 1200V/25A IGBT and a 1200V/12.5A SiC MOSFET at T_{off_delay} = 1.6μs are shown in Fig.3. When the IGBT is turned off prior to the SiC MOSFET, the SiC MOSFET is conducted 100% of the load current during the short gate turn-off delay time, and then undertakes hard switching off operation.

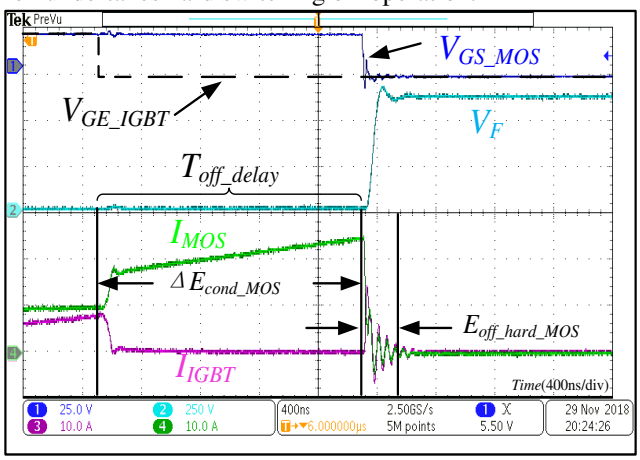


Fig. 3 Turn-off process of Si/SiC hybrid switch

The total turn-off switching loss(E_{off_MOS}) of the SiC MOSFET consists of the hard switching off loss ($E_{off\_hard\_MOS}$) and the additional conduction loss (ΔE_{cond_MOS}) during the short gate turn-off delay time, which can be expressed as

$$E_{off\_MOS}=E_{off\_hard\_MOS}+\Delta E_{cond\_MOS} \quad (10)$$

The hard switching off loss ($E_{off\_hard\_MOS}$) of the SiC MOSFET is related to the forward current, DC-link voltage and junction temperature in power converter applications. An empirical formula of the turn-off switching loss of the SiC MOSFET based on a non-linear approximation is given as[26].

$$E_{off\_hard\_MOS}(I_F,T_j)=E_{off\_MOS\_ref}(\frac{I_F}{I_{ref}})^{a_{I\_MOS}}(\frac{V_{DC}}{V_{ref}})^{b_{V\_MOS}} \times(1+T_{CS\_off\_MOS}(T_{j\_MOS}-T_{j\_ref})) \quad (11)$$

Where V_{DC} is the DC link voltage of the converter. I_{ref}, V_{ref} and T_{j_ref} are the reference forward current, DC link voltage and SiC MOSFET's junction temperature taken from the datasheet. a_{I_MOS} and b_{V_MOS} are the exponents for the current dependency and DC link voltage dependency of the SiC MOSFET's switching off loss, respectively. $T_{cs\_off\_MOS}$ is the temperature coefficients of the SiC MOSFET's switching off loss. $E_{off\_MOS\_ref}$ is the turn-off switching loss of the SiC MOSFET at a specific operating condition in the datasheet.

As show in Fig.3, the SiC MOSFET undertakes 100% of the load current during the gate turn-off delay time. The additional conduction loss ΔE_{cond_MOS} during the gate turn-off delay time could be modeled as a linear function of the gate turn-off delay time T_{off_delay} at the certain forward current condition, which is expressed in Eq. (12).

$$\Delta E_{cond\_MOS}(I_F,T_{j\_MOS})=\left[I_F^2\cdot R_{ds}(T_{j\_MOS})\right]\bullet T_{off\_delay} \quad (12)$$

When the turn-off gate signal is applied, the MOS channel current in IGBT rapidly decreases to zero and all load current is commutated to the SiC MOSFET. The IGBT is turned off without undertaking high voltage since the SiC MOSFET is still conducted, as shown in Fig.3. The large amount of stored charge in N-base region of the IGBT decreases exponentially due to the minority carrier recombination during the gate turn-off delay time [10]. The turn-off switching loss of the IGBT can be modeled as

$$E_{off\_IGBT}=(E_{off\_hard\_IGBT}-E_{res})\bullet e^{-\tau\bullet T_{off\_delay}}+E_{res} \quad (13)$$

Where E_{res} is the residual turn-off switching loss of the IGBT, and τ is the exponential time constant for the dependency of the IGBT's switching off loss on the gate turn-off delay time, respectively. Their values can be obtained from the double pulse test at the same condition with the converter applications. Fig. 4 shows the typical dependency of the IGBT's turn-off switching loss on its gate signal's turn-off delay time.

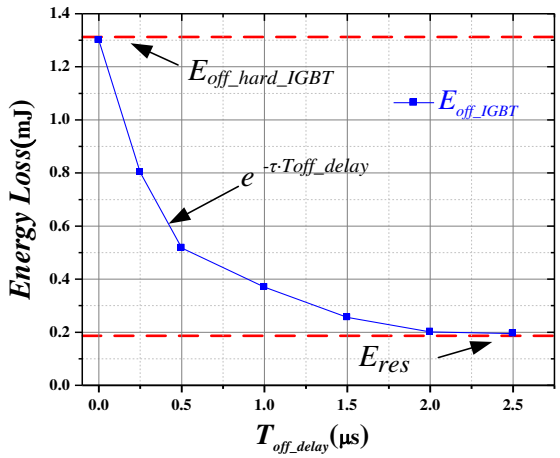


Fig. 4 Dependency of the IGBT's turn-off switching loss on its gate signal's turn-off delay time.

The E_{res} is caused by which the IGBT has to undertake the DC-link voltage and remove the remaining plasma when the SiC MOSFET is hard switching off [27]. The magnitude of E_{res} is mainly influenced by the DC link voltage. When the gate turn-off delay time between the IGBT and the SiC MOSFET is long enough, the magnitude of E_{res} is almost constant at the certain DC link voltage. $E_{off\_hard\_IGBT}$ is the hard switching off loss of the IGBT at a certain forward current. When the gate turn-off delay time is zero or negative, the IGBT undertakes the hard switching off operation, and the SiC MOSFET is ZVS switching off. The hard switching off loss of the IGBT can be extracted from the IGBT manufacture's datasheet with the non-linear approximation as shown in Eq. (14).

$$E_{off\_hard\_IGBT}(I_F,T_j)=E_{off\_hard\_IGBT\_ref}(\frac{I_F}{I_{ref}})^{a_{I\_IGBT}}(\frac{V_{DC}}{V_{ref}})^{b_{V\_IGBT}} \times(1+T_{CS\_off\_IGBT}(T_{j\_IGBT}-T_{j\_ref})) \quad (14)$$

Where a_{I_IGBT} and b_{V_IGBT} are the coefficients for the power dependency of the IGBT's switching off loss on the current dependency and DC link voltage, respectively. $T_{cs\_off\_IGBT}$ is the temperature coefficient of the IGBT's switching off loss. $E_{off\_hard\_IGBT\_ref}$ is the turn-off switching loss of the IGBT extracted from the datasheet at the specific operating condition.

The gate turn-on delay time between the SiC MOSFET and the IGBT inside the hybrid switch is selected to be zero in order to simplify the loss model of the hybrid switch. The measured waveforms of the turn-on process of the hybrid switch at T_{on_delay} = 0μs are shown in Fig.5.

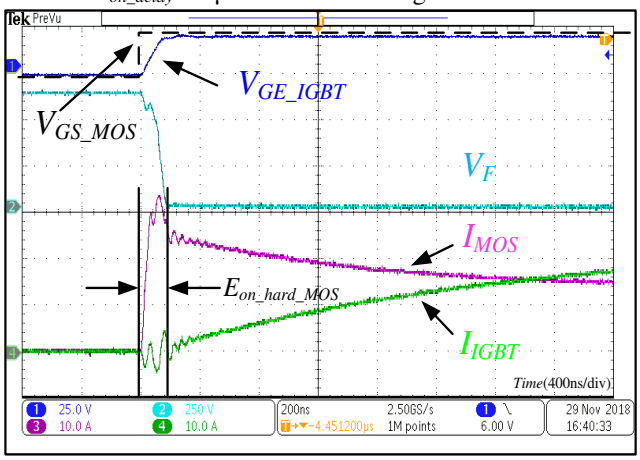


Fig. 5.Turn-on process of Si/SiC hybrid switch

Because the IGBT's turn-on speed is slower than that of SiC MOSFET, the SiC MOSFET undertakes the hard switching on action, and the IGBT is ZCS switching on when the gate turn-on delay time of the hybrid switch is zero. The hard switching on loss of the SiC MOSFET can be extracted from the manufacture's datasheet with the non-linear approximation as shown in Eq.(15).

$$E_{on\_MOS}(I_F,T_j)=E_{on\_MOS\_ref}(\frac{I_F}{I_{ref}})^{c_{I\_MOS}}(\frac{V_{DC}}{V_{ref}})^{d_{V\_MOS}} \times(1+T_{CS\_on\_MOS}(T_{j\_MOS}-T_{j\_ref})) \quad (15)$$

Where c_{I_MOS} and d_{V_MOS} are the coefficients for the power dependency of the SiC MOSFET's turn-on switching loss on the load current and DC link voltage, respectively. $T_{cs\_on\_MOS}$ is the temperature coefficients of the SiC MOSFET's switching on loss. $E_{on\_MOS\_ref}$ is the switching on loss of the SiC MOSFET taken from the datasheet at the reference operating point.

Therefore, neglecting the load current ripple, the total power loss of the SiC MOSFET and the IGBT inside the hybrid switch could be expressed as

$$P_{loss\_MOS}(I_F,T_{j\_MOS}) =(D-f_{sw}\bullet T_{off\_delay})E_{cond\_MOS}+f_{sw}(E_{off\_MOS}+E_{on\_MOS}) \quad (16)$$

$$P_{loss\_IGBT}(I_F,T_{j\_IGBT}) =(D-f_{sw}\bullet T_{off\_delay})E_{cond\_IGBT}+f_{sw}\bullet E_{off\_IGBT} \quad (17)$$

Where D is the duty cycle of the DC/DC buck converter, the f_{sw} is the switching frequency. The Eq.(16) and Eq.(17) show that the power losses of the SiC MOSFET and IGBT inside the hybrid switch are functions of the gate turn-off delay time. Because the junction temperature of the power device is dependent on its power loss, the two internal switches' junction temperatures inside the hybrid switch are strongly affected by its gate turn-off delay time.

C. *Loss model verification*

In this work, a 20 kHz hybrid switch based DC/DC buck converter prototype is built, as shown in Fig.6.

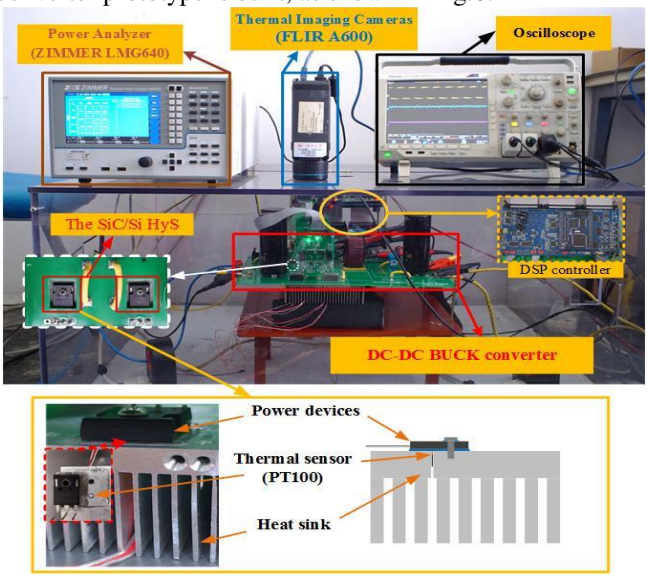


Fig.6 Buck converter prototype based on Si/SiC hybrid switch

The CREE 1200V/12.5A SiC MOSFET (C2M0160120D) and Infineon 1200V/25A Si IGBT (IGW25N120H3) are selected to constitute the hybrid switch. The CREE 1200V/12.5A SiC MOSFET (C2M0160120D) and the CREE 1200V/15A SiC Schottky diode (C4D15120D) are parallel connected as the freewheeling diode to achieve the synchronous rectification operation. They are assembled on a heat sink, and a designed gate driver is used to achieve the specific gate control patterns of the hybrid switch. The case temperature of the hybrid switch are measured by the temperature sensor PT100 from the bottom side as show in Fig.6. The parameters of the buck converter are shown in TABLE I.

TABLE I Parameters of the Hybrid Switch Buck Converter

No.	*Parameters*	*Values*
1	Supply Voltage	600V
2	Output Voltage	300V
3	Power Rating	1~9.5kW
4	Switching Frequency	20kHz
5	Inductor	1mH
6	Output Capacitor	2200μF

In the steady state operation of the buck converter， the average junction temperature of the hybrid switch's two internal devices can be calculated with the aid of their thermal resistances R_{th}. Therefore, the simplified thermal

equivalent circuit diagrams of the hybrid switch can be expressed as shown in Fig.7.

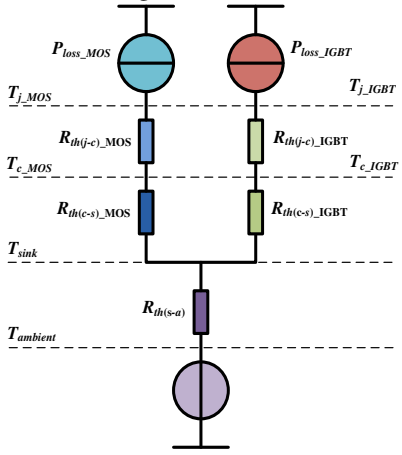


Fig. 7. Simplified thermal equivalent circuit diagram of the hybrid switch

The $R_{th(j-c)\_MOS}$ and $R_{th(j-c)\_IGBT}$ are the junction to case thermal resistance of the SiC MOSFET and IGBT, respectively. As given in the manufacturer's datasheets, they are 0.9K/W and 0.46K/W, respectively. $R_{th(c-s)\_MOS}$ and $R_{th(c-s)\_IGBT}$ are the case to heat sink thermal resistance of the SiC MOSFET and IGBT, respectively, which are determined by the cooling strategy adopted by the hybrid switch based converter. $R_{th\_(s-a)}$ is the heat sink to ambient thermal resistance, which is dependent on the geometry of the heat sink and the heat dissipation way of the hybrid switch based converter. Because the package of both the internal SiC MOSFET and the IGBT are TO-247 in this experiment, and they are assembled on the same heat sink, the $R_{th\_(c-s)}$ of the SiC MOSFET and IGBT are considered the same. The relationship between the average junction temperature and the power loss of the power device in the steady state can be expressed as

$$T_j = T_c + R_{th(j-c)} \cdot P_{loss} \tag{18}$$

The power losses of the hybrid switch are temperature-dependent in the loss model. In order to obtain the precise power loss and junction temperature of the hybrid switch, the losses based on the power loss model can be determined iteratively at the calculated junction temperature. In the first duty cycle, the starting value is the power dissipation at the case temperature measured by the temperature sensor PT100, and then a new and more precise loss value is generated. After several iterations, the final power loss value and junction temperature will be reached. In the following duty cycle, the loss and junction temperature can be obtained recursively. The dependency of the power loss and the junction temperature of the hybrid switch on the gate turn-off delay time at 6kW output power rating is shown in Fig.8 and Fig.9, respectively. $P_{loss\_IGBT\_m}$ and $P_{loss\_MOS\_m}$ are the measured power losses of the internal IGBT and the SiC MOSFET, respectively, which are calculated by the integral of the measured voltage and current waveforms over the period of a duty cycle in the steady state. $T_{j\_MOS\_m}$ and $T_{j\_IGBT\_m}$ are the calculated junction temperature of the internal IGBT and the SiC MOSFET using Eq.(18) based on the $P_{loss\_IGBT\_m}$ and $P_{loss\_MOS\_m}$, respectively. $P_{loss\_IGBT\_c}$ and $P_{loss\_MOS\_c}$ are the calculated power loss of the IGBT and the SiC MOSFET based on the loss model, respectively. $T_{j\_MOS\_c}$ and $T_{j\_IGBT\_c}$ are the estimated junction temperature of the internal IGBT and the SiC MOSFET based on $P_{loss\_IGBT\_c}$ and $P_{loss\_MOS\_c}$, respectively. The calculated power loss and junction temperature of the hybrid switch based on the loss model are consistent with those of the measured power loss and junction temperature.

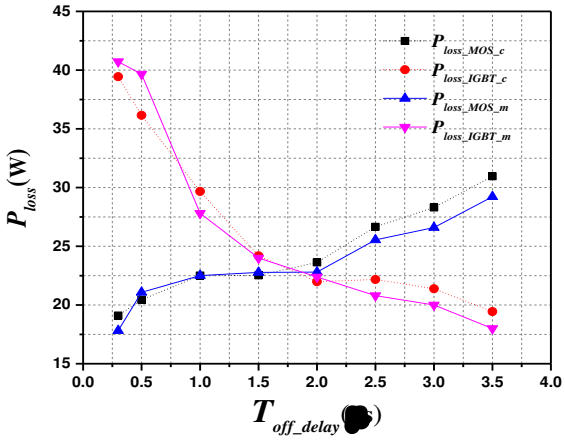


Fig. 8. Comparison of the measured power loss and calculated power loss

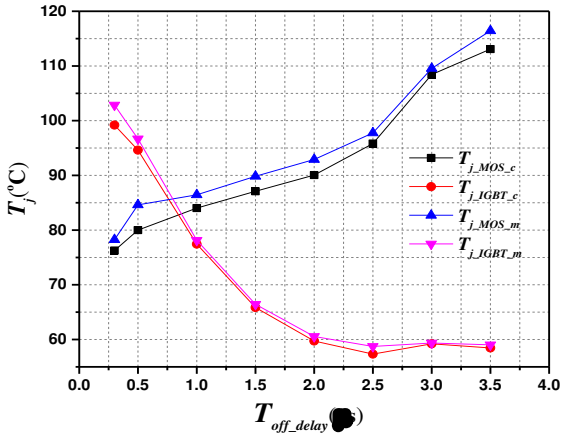


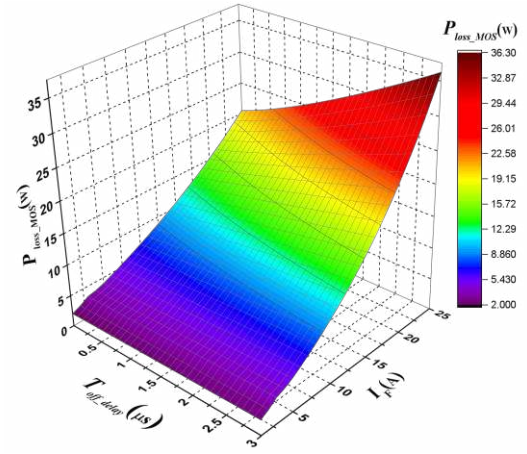
Fig. 9.Comparison of the measured junction temperature and calculated junction temperature

When the gate turn-off delay time of the hybrid switch is very short, the IGBT's large power loss makes its junction temperature much higher than that of the SiC MOSFET. When the gate turn-off delay time of the hybrid switch is too long, the large additional conduction loss of SiC MOSFET makes its junction temperature much higher than that of the IGBT. For example, the junction temperature of the SiC MOSFET is 50°C higher than that of the IGBT at T_{off_delay}=3.5μs. The power losses of the SiC MOSFET and IGBT are evenly distributed when the gate turn-off delay time at T_{off_delay}=1.8μs. Because the thermal resistance of the two internal devices are different, their junction temperature are balanced at T_{off_delay}=0.8μs.

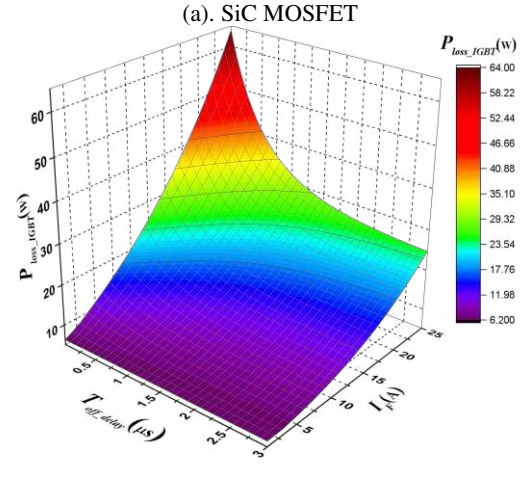
D. Loss distribution and junction temperature unbalance discussion

The losses and junction temperatures of the hybrid switch's two internal devices are strongly dependent on its gate turn-off delay time and the load conditions of the hybrid switch based converter. In order to illustrate the dependency of the loss and junction temperature distribution of the hybrid switch on its gate turn-off delay time and operation current, the case to heat sink thermal resistance $R_{th(c-s)}$ and

the heat sink to ambient thermal resistance $R_{th\_(s-a)}$ are set to be 0.25K/W and 2K/W, respectively. And the ambient temperature is set to be 27℃. The power loss dependency of the SiC MOSFET and IGBT on the gate turn-off delay time and forward current rating are show in Fig.10. The x-axis and y-axis represent the gate turn-off delay time and the operation current rating, respectively. And the z-axis is the total power loss of the SiC MOSFET or the IGBT.



(a). SiC MOSFET



(b). IGBT

Fig.10 Dependency of the hybrid switch's power loss on gate turn-off delay time and operation current

Because the conduction loss and switching loss of the SiC MOSFET and the IGBT inside the hybrid switch at the small operation current is small, the dependency of the loss distribution between the two devices on the gate signal's delay time is weak. When the load current is large, the loss distribution between the two devices is strongly influenced by the gate signal's delay time. When the gate turn-off delay time increases, the power loss of the SiC MOSFET increases, while the power loss of the IGBT decreases. The dependency of the total power loss of the hybrid switch on the gate signal's turn-off delay time and operation current are show in Fig.11. When the operation current of the hybrid switch is 25A, the minimum total power loss of the hybrid switch can be achieved if the gate turn-off delay time is around 1.5μs. And the minimum total power loss of the hybrid switch under a load current of 11A can be achieved if the gate turn-off delay time is around 2μs. In one word, the optimal gate turn-off delay time to achieve the converter's minimum total power loss is varying with the operation current.

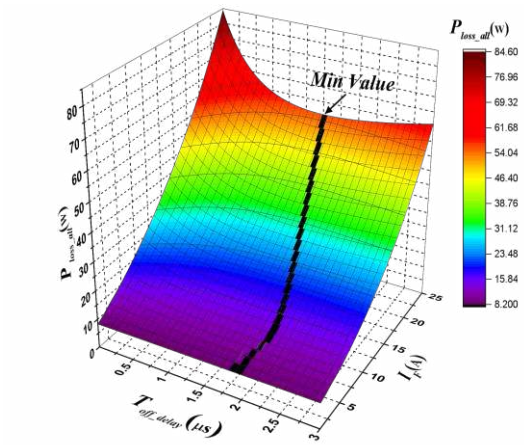
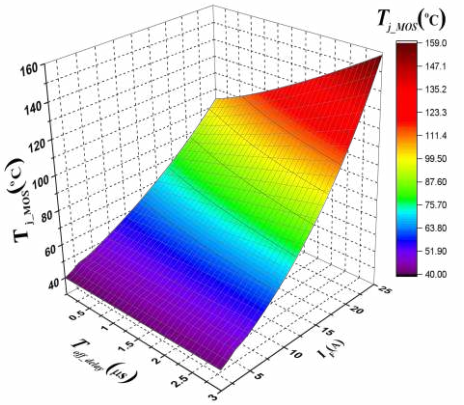
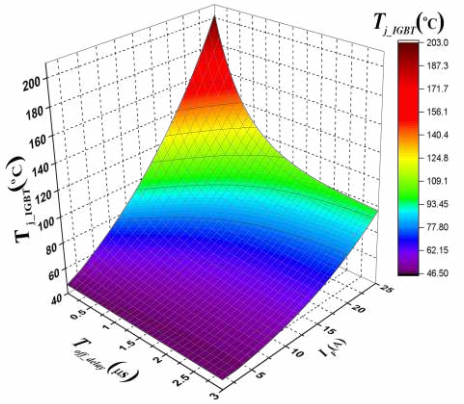


Fig. 11.Dependency of the hybrid switch's total power on gate turn-off delay time and operation current

The junction temperature dependency of the SiC MOSFET and IGBT on the gate signal's turn-off delay time and forward current rating are show in Fig.12. The junction temperature distribution of the hybrid switch is similar to its loss distribution. It is because the junction temperature is strongly dependent on the loss of the power device. When the operation current is large, too small or too large gate turn-off delay time induce the severe junction temperature unbalance between the two internal devices. The severe junction temperature unbalance may make the IGBT or SiC MOSFET's junction temperature reach its junction temperature limit more easily and reduce the hybrid switch's safe junction temperature margin.



(a). SiC MOSFET



(b). IGBT

Fig.12 Dependency of the hybrid switch's junction temperature on gate turn-off delay time and operation current

The junction temperature difference of the two internal switches of the hybrid switch is defined as

$$\Delta T_j = T_{j\_MOS} - T_{j\_IGBT} \tag{19}$$

Where T_{j_MOS} and T_{j_IGBT} is the estimated junction temperature of the SiC MOSFET and the IGBT, respectively. The dependence of ΔT_j on the gate turn-off delay time and operation current is shown in Fig.13. The z-axis is the ΔT_j between the SiC MOSFET and the IGBT. According to the degree of the junction temperature difference between the two internal devices, the ΔT_j is divided into 6 areas.

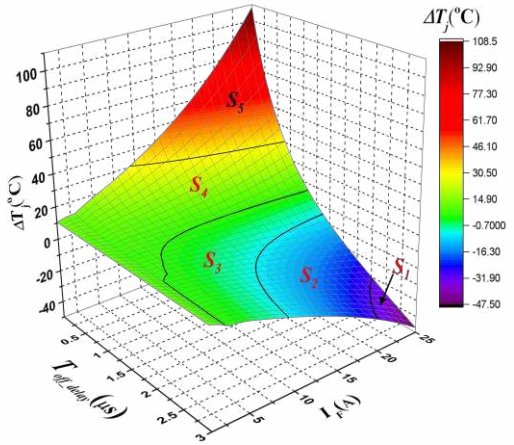


Fig.13 Dependence of the hybrid switch's junction temperature difference on gate turn-off delay time and operation current

The boundary lines of these 6 areas and the minimum T_{j_marjin} within these areas are shown in Table II. The T_{j_marjin} is the junction temperature safety margin of the hybrid switch at a certain forward current rating and gate turn-off delay time, which is defined as

$$T_{j\_margin}(T_{off\_delay}, I_F) = T_{j\_limit} - \max[T_{j\_MOS}(T_{off\_delay}, I_F), T_{j\_IGBT}(T_{off\_delay}, I_F)] \tag{20}$$

where T_{j_limit} is the upper maximum operation junction temperature limit of the hybrid switch. The minimum T_{j_marjin} is the smallest junction temperature safety margin within the operation areas. Therefore, the larger minimum T_{j_marjin}, the more reliable operation condition of the hybrid switch can be achieved within this area.

TABLE II. Junction Temperature Difference and Smallest Junction Temperature Safety Margin

Area	*Boundary Lines of Areas*	Minimum T_{j_marjin}
S_1	$\Delta T_j \leq$-30 ºC	SiC MOSFET overheating
S_2	-30 ºC<$\Delta T_j \leq$-5 ºC	T_{j_marjin}>5 ºC
S_3	-5 ºC<ΔT_j<5 ºC	T_{j_marjin}>25 ºC
S_4	5 ºC$\leq\Delta T_j$<30 ºC	T_{j_marjin}>7ºC
S_5	$\Delta T_j \geq$30 ºC	IGBT overheating

When the hybrid switch is operated within the area S1 and S5, the absolute junction temperature difference between its internal device is more than 30ºC, which may easily make the junction temperature of its one internal device be close to or even over its maximum operation junction temperature limit. Therefore, the S_1 and S_5 are not the preferred operation areas for the hybrid switch.

When the hybrid switch is operated within the area S_2 or S_4, the absolute junction temperature difference between its internal devices is between 5ºC and 30ºC. The high junction temperature unbalance inside the hybrid switch reduces the operation junction temperature safety margin of the hybrid switch. The minimum T_{j_marjin} is higher than 5ºC and 7ºC within the operation area S_2 and S_4, respectively.

The junction temperature difference of the hybrid switch is smaller than 5ºC when the hybrid switch is operated within S_3 operation area. Benefiting from the almost balanced junction temperature of the hybrid switch, the largest junction temperature safety margin is achieved during the S_3 area. The minimum T_{j_marjin} is higher than 25ºC within the area S_3. The large junction temperature safety margin of the hybrid switch improves the maximum output power capability and over load capability of the hybrid switch based converter. The optimal gate turn-off delay time to achieve the hybrid switch's operation within the S_3 area is varying with the operation current.

III. ACTIVE THERMAL CONTROL OF HYBRID SWITCH

In the previous reported studies, the fixed gate control delay time of the hybrid switch is commonly used to reduce the total switching loss of the hybrid switch. However, the optimal gate control delay time of the hybrid switch needs adjustment according to the varied operation conditions of power converters because its total power loss, junction temperatures and junction temperature difference are strongly dependent on the gate turn-off delay time and operation current. The inappropriate fixed gate control delay time risks one internal device's junction temperature subjected to its operation junction temperature upper limit within a wide load condition, which endangers the safe operation of the hybrid-switch based converter under certain extreme operation conditions.

A. Fixed gate turn-off delay time control

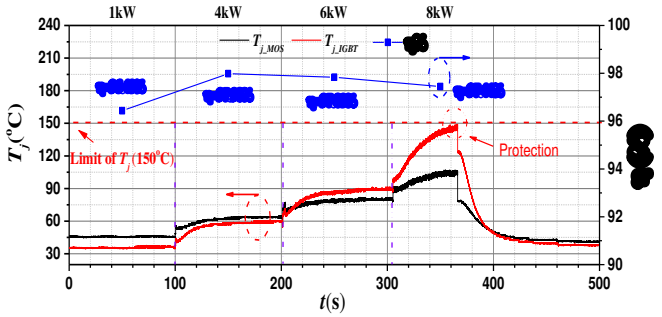
When the output power of the DC/DC buck converter varying with the load condition variation, the junction temperatures of the SiC MOSFET and the IGBT inside the hybrid switch and the measured efficiency of the DC/DC converter at three types fixed gate turn-off delay times are shown in Fig.14. The conversion efficiency of the hybrid switch measured by the power analyzer ZIMMER LMG640.

When the output power is 1kW, the 96.58% conversion efficiency of the converter is achieved at T_{off_delay}=3μs, which is higher than those at T_{off_delay}=0.6μs and T_{off_delay}=1.8μs. This is because the large gate turn-off delay time reduces the total power loss of the hybrid switch under the light load condition. When the output power is 6kW, the highest 97.91% conversion efficiency of the converter is achieved at T_{off_delay}=1.8μs among these three types fixed gate delay time control mode, which is 0.1% higher than that at T_{off_delay}=3μs. The reason is that the large switching off loss of the IGBT at T_{off_delay}=0.6μs and large additional conduction loss of the SiC MOSFET at T_{off_delay}=3μs reduce the conversion efficiency of the hybrid switch based converter.

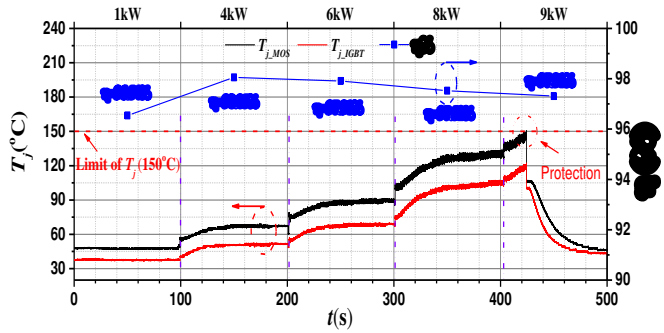
When the output power of the hybrid switch converter is smaller than 6kW, the junction temperature of the SiC MOSFET and the IGBT are below their operation junction

temperature limits at these three types gate delay time control mode. When the output power is increased to 8kW, the junction temperature of the SiC MOSFET and IGBT is 132ºC and 101ºC, respectively, at T_{off_delay}=1.8μs. However, the junction temperature of the IGBT or the SiC MOSFET is higher than its operation junction temperature limit (150 ºC) and triggers the over temperature protection at T_{off_delay}=0.6μs or T_{off_delay}=3μs, while the junction temperature of the corresponding SiC MOSFET or the IGBT is only 100ºC and 91ºC when triggering the protection.

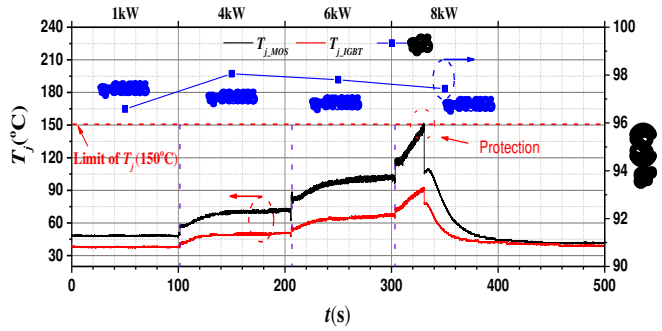
When the output power is increased by 9kW, the junction temperature of the SiC MOSFET is higher than its operation junction temperature limit at T_{off_delay}=1.8μs, which those of the corresponding IGBT is only 120 ºC. The severe junction temperature unbalance caused by the fixed gate turn-off delay time restricts the full utilization of the two internal devices of the hybrid switch in converter applications. And the maximum output power handling capability of the hybrid switch based converter is reduced because one of the internal devices reaches its operation junction temperature limit much earlier than another device under the unbalance junction temperature condition.



(a).T_{off_delay}=0.6μs



(b).T_{off_delay}=1.8μs



(c).T_{off_delay}=3μs

Fig.14 T_j of the hybrid switch at several fixed gate turn-off delay time

B. *Active gate delay time control*

In order to avoid a serious risk of overheating of the hybrid switch's internal device within a wide load condition, the active gate delay time control strategy based on the electro-thermal coupling loss model is proposed as shown in Fig 15. The basic control diagram of the Si/SiC hybrid switch buck converter is consisted of the active gate delay time controller and the output voltage controller. These two controllers are implemented on the TMS320F28335 digital signal processor.

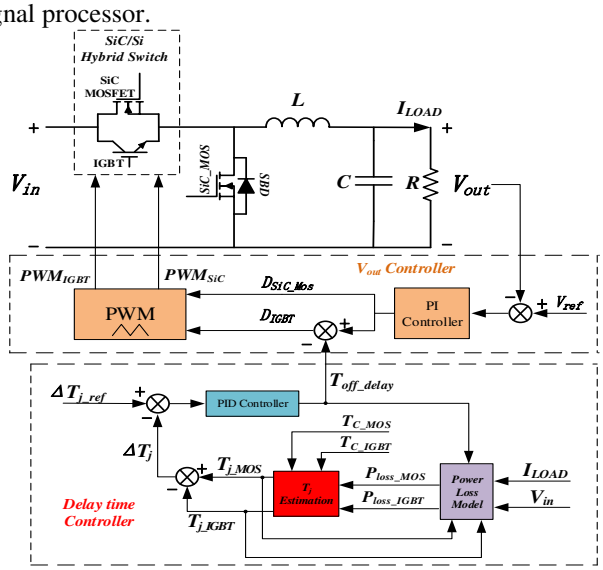


Fig.15 Block diagram of the active gate turn-off delay time controller

The duty cycle of the buck converter is calculated by the output voltage controller at first. The output voltage controller is realized with a single output voltage control loop to keep the output voltage stable of the hybrid switch buck converter. When using the gate control pattern as shown in Fig.2, the equivalent duty cycle of the buck converter is determined by the duty cycle of the auxiliary SiC MOSFET. And appropriate reducing the duty cycle of the IGBT could realize the gate turn-off delay time of the hybrid switch. Therefore, the output voltage controller determines the duty cycle of the auxiliary SiC MOSFET. And the duty cycle of the IGBT is calculated by the active gate delay time controller to achieve the appropriate gate turn-off delay time.

The active gate delay time controller consists of the Si/SiC hybrid switch power loss model, junction temperature estimation unit and the delay time close loop controller.

Firstly, the power loss of the hybrid switch are calculated based on the electro-thermal coupling loss model calibrated with the measured DC voltage and load current.

Secondly, the average junction temperatures of the two internal devices under the steady state are estimated based on Eq.(18) with the calculated power loss, measured case temperature and the extracted thermal resistance from the device datasheet.

Then the junction temperature difference ΔT_j between the two internal devices is compared to the junction temperature difference reference ΔT_{j_ref}. And the junction temperature difference error as the input of the PID controller to adjust the gate turn-off delay time. When the ΔT_j between the SiC MOSFET and the IGBT is higher/lower than the reference junction temperature difference ΔT_{j_ref}, the PID controller will adjust the duty cycle of the IGBT to change the gate turn-off delay time between the two devices to achieve their junction temperature balance. The parameters of the PID

controller can be calculated by the basic Ziegler—Nichols tuning rules, or empirical based method.

Finally, the gate turn-off delay time is used to calibrate the duty cycle of the IGBT to achieve its ZVS turn-off while keep the SiC MOSFET's duty cycle unchanged simultaneously.

Because of the duty cycle of the buck converter without change when the active gate delay time controller adjusts the gate turn-off delay time, the active gate delay time controller is independent from the output voltage controller and has no effect on the dynamic response and stability of the buck converter.

When the ΔT_{j_ref} is set as the 0ºC, the junction temperatures of the hybrid switch with the active gate turn-off delay time control strategy at various load conditions are shown in Fig.16.

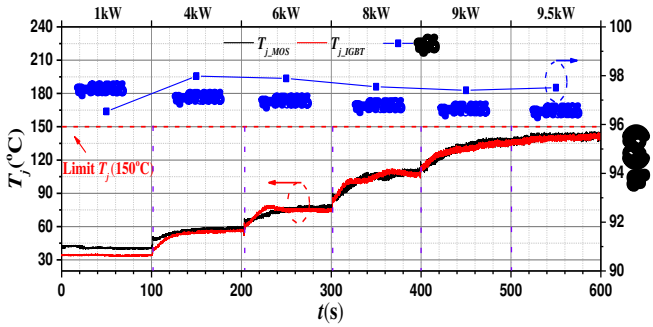


Fig.16. T_j of the hybrid switch with the active junction temperature balance control

When the output power is 1kW, the junction temperature of the IGBT is a little smaller than that of the SiC MOSFET. It is because the SiC MOSFET undertakes the most conduction loss and switching loss under the small operation current condition.

When the output power changes from 2kW to 8kW, the junction temperature between the two devices inside the hybrid switch is balanced during the load varying condition. Using the active gate turn-off delay time control strategy, the maximum junction temperature of the hybrid switch is about 112ºC under 8kW load condition, which is 20ºC smaller than that at the fixed T_{off_delay}=1.8μs under the same load condition.

When the junction temperature of the hybrid switch reaches the operation junction temperature limit, the maximum output power handling capability is 9.5kW using the active gate turn-off delay time control strategy, which is 1.5kW larger than that at the T_{off_delay}=1.8μs fixed gate turn-off delay time control mode.

When using the active gate turn-off delay time control, the conversion efficiency of the buck converter increases by 0.03% compared to the fixed T_{off_delay}=1.8μs control mode under 8kW output power condition. When the output power is 6kW, the conversion efficiency with the active gate delay time control decreases by 0.02% compared to at the fixed T_{off_delay}=1.8μs, and increases by 0.06% and 0.08% compared to the at the T_{off_delay}=0.6μs or at the T_{off_delay}=3μs, respectively. Therefore, achieving the balanced junction temperature between the two internal devices inside the hybrid switch is without obvious compromising on the conversion efficiency of the hybrid switch converter within a wide load range. Furthermore, the hybrid switch with the active gate turn-off delay time control achieves the larger safe operation junction temperature margin, more reliable working condition and larger maximum output power capability within a wide load condition compared to the fixed gate turn-off delay time control mode.

C. *Reduction of the junction temperature swing*

As the power loss's magnitude of the SiC MOSFET and the IGBT inside the hybrid switch depends on the gate turn-off delay time and the load condition, the invoked magnitude of the junction temperature swings also varies. Usually, the transient junction temperature swing of the power device caused by the switching and conduction losses during a PWM period is small magnitude and most of them are filtered out by device thermal capacitances [25]. On the other hand, the average junction temperature swing of the device caused by the converter's load variation is in large magnitude and creates cyclic heating and cooling process of power device, also called thermal cycles [24]. The thermal cycles are the main cause of failures and destruction of the power devices over long-term operation. Therefore, the hybrid switch's average junction temperature swing difference between using the fixed gate turn-off delay time control and the active gate turn-off delay time control are analyzed and compared.

When the load condition of the hybrid switch buck converter cycles between 2kW and 8kW, the junction temperatures of the hybrid switch at fixed T_{off_delay}=1.8μs and using the active gate turn-off delay time control are shown in Fig.17 and Fig.18, respectively.

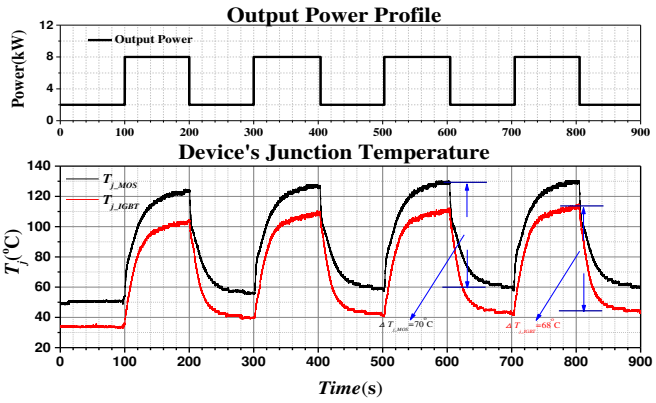


Fig.17. Average junction temperature swing of the hybrid switch with fixed gate turn-off delay time

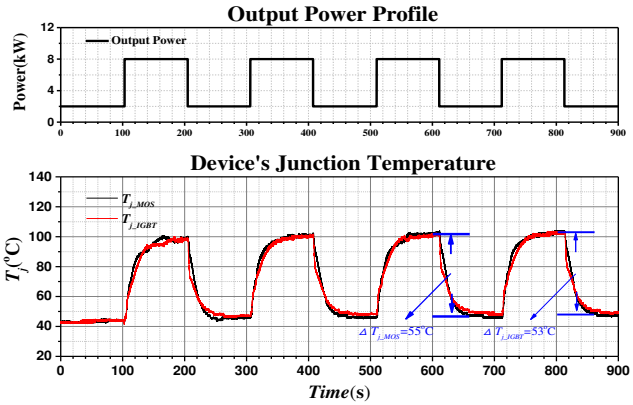


Fig.18. Average junction temperature swing of the hybrid switch using the active gate turn-off delay time control

The severe junction temperature unbalance at the conventional fixed gate control delay strategy induces a large junction temperature swing of the hybrid switch during the

load condition fluctuations. The junction temperature swing of the SiC MOSFET and the IGBT is 70ºC and 66ºC during the load fluctuation, respectively. When using the active gate delay time control**,** the junction temperatures are balanced between the two internal devices during the load fluctuation. Therefore, the same junction temperature swings of the two internal devices are achieved, which avoids the accelerating aging of one internal device caused by its larger junction temperature swing during the load fluctuation condition. Moreover, because of the balance junction temperature leading to a smaller junction temperatures compared to the fixed T_{off_delay}=1.8μs gate control mode under the same load condition, the SiC MOSFET and the IGBT inside the hybrid switch has smaller magnitude of the junction temperature swing under the same cyclic load conditions. As shown in Fig.18, the junction temperature swings of the SiC MOSFET and the IGBT are 55ºC and 54ºC during the load fluctuation, respectively. The maximum junction temperature swing of the hybrid switch with the active gate turn-off delay time control is 15ºC smaller than that at the fixed T_{off_delay}=1.8μs. It means that the active gate delay time control strategy is helpful to improve the long-term reliability of the hybrid switch.

IV. CONCLUSION

In this paper, a novel active gate delay time control method based on the electro-thermal coupling loss model of the Si/SiC hybrid switch is proposed to achieve the minimum operation junction temperature difference of the hybrid switch's two internal devices within a wide load range. Different from the conventional fixed gate delay time control, the proposed method continuously adjusts the optimized gate control delay time of the hybrid switch according to the operation conditions of the converter, which helps improve the maximum operation junction temperature margin, and reduce the junction temperature swing during the cyclic load condition of the hybrid switch. The active gate turn-off delay time controller is independent to the converter's output voltage controller and doesn't affect the dynamic performance and stability of the hybrid switch converter. Using the active gate delay time control method, the hybrid switch achieves the 18% rise in maximum power handling capability, 20 ºC reduction in maximum junction temperature under the 8kW power rating and 15ºC reduction in maximum junction temperature swing during the same load cyclic compared with the conventional approach in the 20kHz DC/DC buck converter applications.

REFERENCES

[1] J. W. Palmour, "Silicon carbide power device development for industrial markets," 2014 IEEE International Electron Devices Meeting, San Francisco, CA, 2014, pp. 1.1.1-1.1.8.

[2] G. Wang, F. Wang, G. Magai, Y. Lei, A. Huang and M. Das, "Performance comparison of 1200V 100A SiC MOSFET and 1200V 100A silicon IGBT," 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, 2013, pp. 3230-3234.

[3] S. Hazra et al., "High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications," in IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4742-4754, July 2016.

[4] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath and C. A. Teixeira, "The Benefits of SiC mosfets in a T-Type Inverter for Grid-Tie Applications," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 2808-2821, April 2017.

[5] T. Wu, J. Chen, S. Mao and M. J. Schutten, "1200V SiC MOSFETS for high voltage power conversion," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 2921-2926.

[6] J. Racsbkowski, D. Peftitsis and H. P. Nee, "Silicon Carbide Power Transistors: A New Era in Power Electronics Is Initiated," in IEEE Industrial Electronics Magazine, vol. 6, no. 2, pp. 17-26, June 2012.

[7] M. Rahimo et al., "Characterization of a Silicon IGBT and Silicon Carbide MOSFET Cross-Switch Hybrid," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 4638-4642, Sept. 2015.

[8] R. A. Minamisawa, U. Vemulapati, A. Mihaila, C. Papadopoulos and M. Rahimo, "Current Sharing Behavior in Si IGBT and SiC MOSFET Cross-Switch Hybrid," in IEEE Electron Device Letters, vol. 37, no. 9, pp. 1178-1180, Sept. 2016.

[9] U. R. Vemulapati, A. Mihaila, R. A. Minamisawa, F. Canales, M. Rahimo and C. Papadopoulos, "Simulation and experimental results of 3.3kV cross switch "Si-IGBT and SiC-MOSFET" hybrid," 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD), Prague, 2016, pp. 163-166.

[10] A. Q. Huang, X. Song and L. Zhang, "6.5 kV Si/SiC hybrid power module: An ideal next step?," 2015 IEEE International Workshop on Integrated Power Packaging (IWIPP), Chicago, IL, 2015, pp. 64-67.

[11] X. Song and A. Q. Huang, "6.5kV FREEDM-Pair: Ideal high power switch capitalizing on Si and SiC," 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, 2015, pp. 1-9.

[12] C. Zeng et al., "Comparison of SiC Synchronous Rectification and Schottky Diode in Voltage Source Inverters," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 1903-1906.

[13] F. Yuan et al., "Sizing Selection Optimization of SiC/Si Hybrid Switch in DC/DC Buck Converters," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018, pp. 6160-6164.

[14] A. Deshpande and F. Luo, "Design of a silicon-WBG hybrid switch," 2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Blacksburg, VA, 2015, pp. 296-299.

[15] Zhang, W., Anwar, S., Costinett, D. J. and Wang, F, "Investigation of Cost-effective SiC Based Hybrid Switch and Improved Inductor Design Procedure for Boost Converter in Electrical Vehicles Application." Sae Technical Papers 2015.2(2015):209-214.

[16] Ye Wang, Nan Zhu, Cheng Yan and Dehong Xu, "Efficiency improvement of 2- and 3-level inverters for distributed photovoltaic application using hybrid devices," 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC), Taipei, 2015, pp. 1-7.

[17] Z. Li et al., "Optimal control strategies for SiC MOSFET and Si IGBT based hybrid switch," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 1717-1721.

[18] Z. Zhang, L. Zhang and J. Qin, "Optimization of Delay Time between Gate Signals for Si/SiC Hybrid Switch," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 2018, pp. 1882-1886.

[19] A. Deshpande and F. Luo, "Practical Design Considerations for a Si IGBT + SiC MOSFET Hybrid Switch: Parasitic Interconnect Influences, Cost and Current Ratio Optimization," in IEEE Transactions on Power Electronics.doi: 10.1109/TPEL.2018.2827989

[20] J. He; R. Katebi; N. Weise, "A Current-Dependent Switching Strategy for Si/SiC Hybrid Switch Based Power Converters," in IEEE Transactions on Industrial Electronics , vol.PP, no.99, pp.1-1

[21] T. Zhao and J. He, "An optimal switching pattern for "SiC+Si" hybrid device based Voltage Source Converters," 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1276-1281.

[22] J. Wang, Z. Li, X. Jiang, C. Zeng and Z. J. Shen, "Gate Control Optimization of Si/SiC Hybrid Switch for Junction Temperature Balance and Power Loss Reduction," in IEEE Transactions on Power Electronics, vol. 34, no. 2, pp. 1744-1754, Feb. 2019.

[23] Schulz, M. "Thermal management details and their influence on the aging of power semiconductors." European Conference on Power Electronics and Applications IEEE, 2014:1-6.

[24] M. Andresen, K. Ma, G. Buticchi, J. Falck, F. Blaabjerg and M. Liserre, "Junction Temperature Control for More Reliable Power

Electronics," in IEEE Transactions on Power Electronics, vol. 33, no. 1, pp. 765-776, Jan. 2018.

[25] M. H. M. Sathik, S. Prasanth, F. Sasongko, S. K. Padmanabhan, J. Pou and R. Simanjorang, "A dynamic thermal controller for power semiconductor devices," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 2792-2797.

[26] Arendt Wintrich, Ulrich Nicolai, Werner Tursky and Tobias Reimann. "Application Manual Power Semiconductors," SEMIKRON International GmbH, Germany, 2015, pp.275-277

[27] J. Fuhrmann, S. Klauke and H. Eckel, "Passive IGBT turn-off during short-circuit type V," PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2016, pp. 1-7.

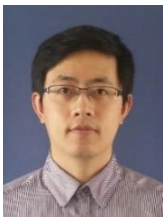
Zongjian Li received the B.S. degree in electronic information engineering from the College of engineering, Hunan Normal University, Changsha, China, in 2012. He is currently pursuing the Ph.D. degree in Electric Engineering in the College of Electrical and Information Engineering, Hunan University, Changsha, China. His research interests include Silicon Carbide power electronic devices and their applications.

Jun Wang （ S'06-M'10-SM'15 ） He received the Ph.D. degree at North Carolina State University, Raleigh, NC, USA in Electrical Engineering in 2010. He then worked as a device design engineer at Texas Instruments, Inc. in Bethlehem, PA, USA between 2010 and 2013. He became a professor in the College of Electrical and Information Engineering at Hunan University in 2014. He has been an associate editor of the IEEE Journal of Emerging and Selected Topics in Power Electronics since 2017. His research interests include power semiconductor devices and their applications in power electronics systems.

Linfeng Deng got his PhD from the Univer sity of Hong Kong. He is currently an assist ant professor of School of Electrical and Inf ormation Engineering, Hunan University, C hina. His research field includes power semi conductor devices, and pulse power technol ogy.

Zhizhi He received the B.S. degree in electrical engineering from North University of China, Taiyuan, China in 2017. He is currently working toward the M.S. degree in electrical engineering in the School of Hunan University. His research interests include power electronic devices, gate drivers and high power density converters.

Xin Yang (M'15) received the B.Eng. degree from the Huazhong University of Science and Technology, China, in 2009, the M.Sc. degree (with distinction) from Imperial College London, U.K., in 2010, and the Ph.D. degree from the University of Cambridge, U.K., in 2014. From 2015 to 2018, he was an Assistant Professor in the National University of Defense Technology, China. He is currently a full professor in Hunan University, China. His research interests mainly include power electronics, high power semiconductor device modeling and simulation, reliability of power electronic circuits. Dr. Yang was the recipient of Cambridge Overseas Scholarship, Henry Lester Scholarship (three times), IEEE IES Studentship and the Cambridge University Lundgren Fund. He is an associate editor of IET power electronics.



Bing Ji (M'13 - SM'18) received the BEng in Electrical Engineering and English as his double major from Dalian University of Technology, China, in 2004. He obtained MSc(Dist) and PhD in Power Electronics both from Newcastle University, U.K., in 2007 and 2012, respectively. He has undertaken different research roles in industry and academia since 2012. He joined the University of Leicester in 2015 as a lecturer of Electrical Power Engineering. His research interests include reliabile power semiconductor devices and modules, batteries and converters, intelligent gate drivers, thermal management, virtual prototyping, and high power-density converters in electric vehicle and aerospace applications. He is also a member of the IET.

Z. John Shen(S'89-M'94-SM'01-F'11) received BS from Tsinghua University, China, in 1987, and M.S. and Ph.D. degrees from Rensselaer Polytechnic Institute, Troy, NY, in 1991 and 1994, respectively, all in electrical engineering. Between 1994 and 1999, he held a variety of positions including Senior Principal Staff Scientist with Motorola. He was on faculty of the University of Michigan-Dearborn between 1999 and 2004, and the University of Central Florida between 2004 and 2012. He joined the Illinois Institute of Technology in 2013 as the Grainger Chair Professor in Electrical and Power Engineering. He has also held a courtesy professorship with Hunan University, China since 2007; and with Zhejiang University, China since 2013. His research interests include power electronics, power semiconductor devices and ICs, automotive electronics, renewable and alternative energy systems, and electronics manufacturing. Dr. Shen is a recipient of the 2012 IEEE Region 3 Outstanding Engineer Award, the 2003 NSF CAREER Award, the 2006 IEEE Transaction Paper Award from IEEE Society of Power Electronics, the 2003 IEEE Best Automotive Electronics Paper Award from IEEE Society of Vehicular Technology, and the 1996 Motorola Science and Technology Award. He has served as VP of Products 2009-2012, Associate Editor and Guest Editor in Chief of the IEEE Transactions on Power Electronics, technical program chair and general chair of several major IEEE conferences.