Active Harmonic Elimination for Multilevel Converters

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***Abstract*—This paper presents an active harmonic elimination method to eliminate any number of specific higher order harmonics of multilevel converters with equal or unequal dc voltages. First, resultant theory is applied to transcendental equations characterizing the harmonic content to eliminate low order harmonics and to determine switching angles for the fundamental frequency switching scheme and a unipolar switching scheme. Next, the residual higher order harmonics are computed and subtracted from the original voltage waveform to eliminate them. The simulation results show that the method can effectively eliminate the specific harmonics, and a low total harmonic distortion (THD) near sine wave is produced. An experimental 11-level H-bridge multilevel converter with a field programmable gate array controller is employed to implement the method. The experimental results show that the method does effectively eliminate any number of specific harmonics, and the output voltage waveform has low THD.**

***Index Terms*—Active harmonic elimination, field programmable gate array (FPGA) controller, multilevel converter.**

I. Introduction

MULTILEVEL converters have received more and more attention because of their capability of high voltage operation, high efficiency, and low electromagnetic interference (EMI) [1], [2]. The desired output of a multilevel converter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the converter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. This results in low switching losses, and because of several dc sources, the switches experience a lower dv/dt. As a result, multilevel converter technology is promising for high power electric devices such as utility applications [3]. For these applications, the output voltage of the converters must meet maximum total harmonic distortion (THD) limitations such as those specified in IEEE 519 [4]; therefore, some kind of method must be used to control the harmonics.

The traditional PWM method, space vector pulse-width modulation (PWM) method, sub-harmonic PWM method (SH-PWM) [5], and switching frequency optimal PWM (SFO-PWM) [6] for multilevel converters require equal dc voltage sources. For fundamental switching scheme, the transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination theory [7]–[9] has been employed to determine the switching angles to eliminate specific harmonics, such as the fifth, seventh, 11th, and the 13th. However, as the number of dc sources increases, the degrees of the polynomials in these equations are large and one reaches the limitations of contemporary computer algebra software tools (e.g., Mathematica or Maple) to solve the system of polynomial equations using resultants [11]. Another method to eliminate harmonics in multilevel inverters is highlighted in [15].

The benefit of the fundamental frequency switching method is its low switching frequency compared to other control methods. Generally, the computational complexity of the resultant method limits its use to multilevel converters with equal dc sources. If one wanted to apply the method to multilevel converters with unequal dc sources, the set of transcendental equations to be solved are no longer symmetric and require the solution of a set of high-degree equations, which is beyond the capability of contemporary computer algebra [12]. In order to use the method, the constant dc source voltages must be maintained which increases the cost of the system [13].

Because of the computational difficulty of the resultant method for high degree polynomials, a new active harmonic elimination algorithm is proposed in this paper to eliminate higher order harmonics. First, the low order harmonics (e.g., the fifth, seventh, 11th, and 13th) can be eliminated using a fundamental frequency switching scheme for the equal dc voltage situation or by using a unipolar switching scheme for the unequal dc voltage situation in which the switching angles are determined using elimination theory. Next, specifically chosen higher harmonics (the odd, nontriplen harmonics, such as the 19th, 23rd, 25th, and 29th in the experiments) are eliminated by using an additional switching angle (one for each higher harmonic) with corresponding higher frequency to generate the opposite of the harmonic to cancel it. Therefore, the output voltage waveform will have low THD.

Here, an experimental 11-level H-bridge multilevel converter with a field programmable gate array (FPGA) controller is employed to implement the method. The experimental results show that the method can effectively eliminate any number of specific harmonics for multilevel converters with equal dc voltages or unequal dc voltages, and the output voltage waveform has much less THD than that from the fundamental switching scheme and the unipolar switching scheme.

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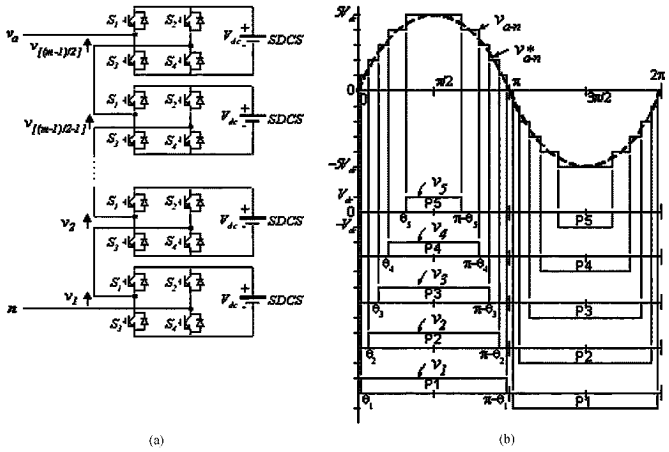

Fig. 1. (a) Topology of single phase cascaded H-bridge multilevel converter and (b) output waveform of multilevel converter using fundamental frequency switching scheme.

The active harmonic elimination method also offers flexibility with the option of increasing the switching frequency for higher order harmonic elimination. In order to eliminate more harmonics than the number of levels in a multilevel converter, the switching frequency must be higher because generating the opposite higher order harmonics needs more switchings in a cycle, however.

II. Harmonic Elimination for Multilevel Converter With Equal dc Voltages

A. Low Order Harmonic Elimination

A cascaded H-bridge multilevel converter uses several dc sources to synthesize a sinusoidal wave. Fig. 1(a) shows the topology of a single-phase cascaded H-bridge multilevel converter. The control of the multilevel converter is to choose a series of switching angles to synthesize a desired sinusoidal voltage waveform. The 11-level multilevel converter output voltage waveform generated by the fundamental frequency switching scheme is shown in Fig. 1(b).

If the dc voltages for all the H-bridges are equal, which is defined as V_{dc} here, the Fourier series expansion of the output voltage waveform using fundamental frequency switching scheme as shown in Fig. 1 is

$$V(\omega t)=\sum_{n=1,3,5\ldots}^{\infty}\frac{4V_{dc}}{n\pi}(\cos(n\theta_1)+\cos(n\theta_2)+\cos(n\theta_3)+\cdots+\cos(n\theta_s))\sin(n\omega t) \quad (1)$$

where s is the number of dc sources in a cascaded H-bridge multilevel converter. Ideally, given a desired fundamental voltage V_1, one wants to determine the switching angles $\theta_1,\ldots,\theta_s$ so that $V(\omega t)=V_1\sin(\omega t)$, and specific higher harmonics of $V(\omega t)=Vn(n\omega t)$ are equal to zero. For a three-phase application, the triplen harmonics in each phase need not be cancelled as they automatically cancel in the line-to-line voltages. For example, in the case of $s=5$ dc sources, the fifth, seventh, 11th, and 13th order harmonics can be canceled.

The switching angles can be found by solving (2), shown at the bottom of the page, where the modulation index m is defined as $m=\pi V_1/(4V_{dc})$.

These transcendental equations characterizing the harmonic content can be converted into polynomial equations, and the resultant method is employed to find all their solutions when they exist [7], [8]. The 11-level solutions are shown in Fig. 2(a). The higher order harmonic voltages V_n are computed by (1), and the THD for the corresponding solution is computed according to $\mathrm{THD}=\sqrt{\sum_{n=5,7,11,\ldots}^{49}V_n^2/V_1}$ is shown in Fig. 2(b).

From the solution set shown in Fig. 2(a), the solutions exist only for m in a range from 1.88 to 4.23. Futhermore, even in this range there are intervals of m for which no solution exists. Also, some modulation indices have more than one set of solutions with different values for their residual harmonics and thus THD. For practical applications, the set of switching angles with the lowest THD will be used for implementation.

B. High Order Harmonic Elimination

From (1), the voltage content can be divided into four parts

$$V(\omega t)=V_{p1}(t)+V_{p2}(t)+V_{p3}(t)+V_{p4}(t) \quad (3)$$

1) Fundamental frequency voltage:

$$V_{p1}(t)=\frac{4V_{dc}}{\pi}[\cos(\theta_1)+\cos(\theta_2)+\cdots+\cos(\theta_s)]\sin(\omega t). \quad (4)$$

2) Triplen harmonic voltages:

$$V_{p2}(t)=\sum_{n=3,9,15,\ldots}\frac{4V_{dc}}{n\pi}[\cos(n\theta_1)+\cos(n\theta_2)+\cdots+\cos(n\theta_s)]\sin(n\omega t). \quad (5)$$

3) Low order harmonic voltages that can be eliminated by applying the resultant method:

$$V_{p3}(t)=\sum_{n=5,7,11,13}\frac{4V_{dc}}{n\pi}[\cos(n\theta_1)+\cos(n\theta_2)+\cdots+\cos(n\theta_s)]\sin(n\omega t). \quad (6)$$

$$\begin{aligned}
\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)&=m\\
\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)&=0\\
\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)&=0\\
\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)&=0\\
\cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)&=0
\end{aligned} \quad (2)$$

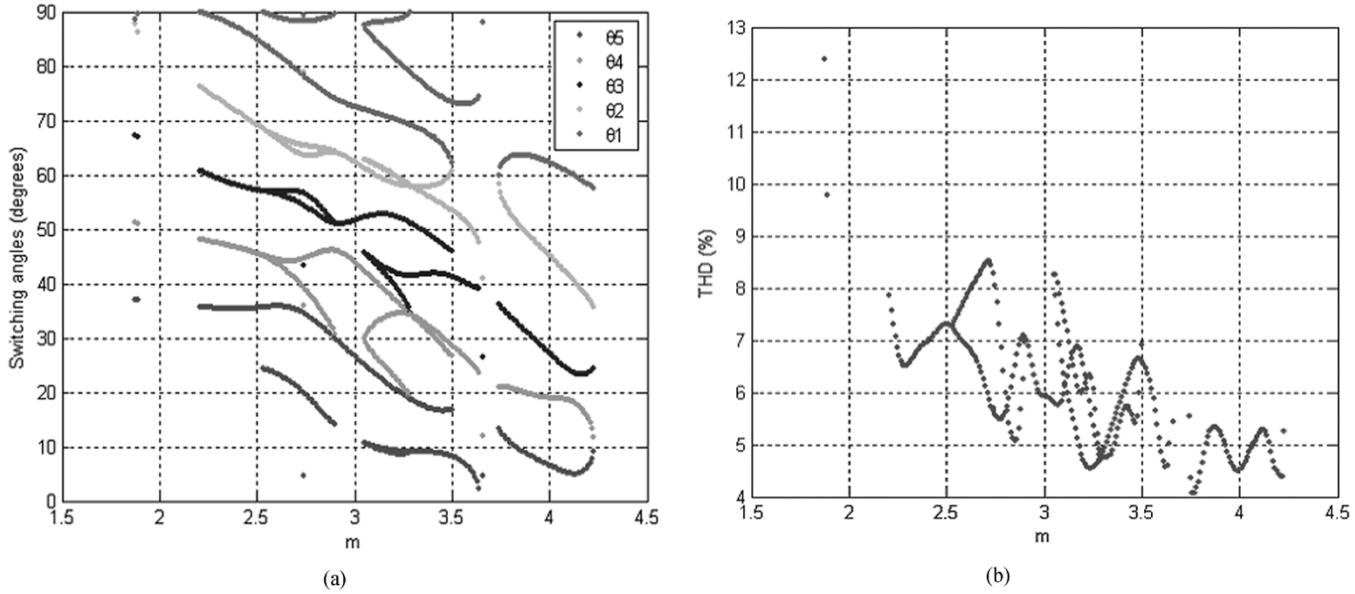

Fig. 2. (a) Solutions for switching angles versus m and (b) corresponding THD versus m.

4) High order harmonic voltages that are not eliminated by applying the resultant method:

$$V_{p4}(t) = \sum_{n=17,19,23,\ldots} \frac{4V_{dc}}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\sin(n\omega t). \quad (7)$$

Using the resultant method of [10], [11], V_{p1} is set, and V_{p3} given in (6) is identically zero by choosing the switching angles appropriately. Assuming the application is a balanced three-phase system, V_{p2} in (5) need not be eliminated because these harmonics cancel in the line-line voltage. This then leaves V_{p4} in (7). To eliminate these harmonics, a square wave is generated (one for each of these harmonics) whose fundamental is the opposite of the harmonic that is to be eliminated. For example, to eliminate the 17th harmonic (let $h = 17$), a square wave whose Fourier series expansion is

$$V_{k_1}(t) = -\sum_{q=1,3,5,7,\ldots} \frac{4V_{dc}}{q\pi}[\cos(qh\theta_1) + \cos(qh\theta_2) + \cdots + \cos(qh\theta_s)]\sin(qh\omega t) \quad (8)$$

is generated. The $q = 1$, $h = 17$ term of (8) cancels the $n = 17$ term of (7) and the next harmonic of concern that is produced by (8) is at $5 \times 17 = 85$. This harmonic and higher ones (7×17, etc.,) are easy to filter using a low-pass filter. Repeating the above procedure, the 19th, 23rd,..., 49th harmonics can all be eliminated. The net effect of this method is to remove the low order harmonics at the expense of generating new higher order harmonics and increasing the switching frequency. This method is referred to as active harmonic elimination method because the harmonic elimination is realized in the converter, not by a passive filter. The THD of the output voltage that eliminates all of the low order harmonics up to 31st versus $m = \pi V_1/(4V_{dc})$ is shown in Fig. 3. Compared to the fundamental frequency switching method, the THD is much lower.

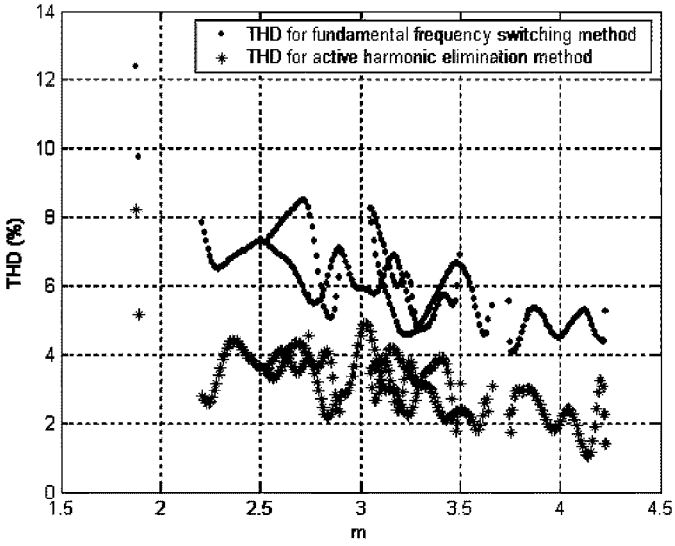

Fig. 3. THDs for active harmonic elimination method to eliminate harmonics up to 31st and for fundamental frequency switching method.

Fundamental frequency switchings to eliminate harmonics incurs only five switching per cycle to control the fundamental and eliminate the fifth, seventh, 11th, and 13th harmonics. To eliminate the nth harmonic (when more harmonics are desired to be eliminated than there are levels in the converter), the multilevel converter active devices are required to switch an extra n times in a cycle. The additional number of switchings in a cycle for the active harmonic elimination method is $N_{sw} \leq \sum_{n=17,19,23,25,29,31} n$, where n is the harmonic number.

If a harmonic is near zero and the time step resolution is lower than that required to eliminate the harmonic, then switching will not occur. In this work, no attempt was made to eliminate residual harmonics with amplitudes less than 0.5% of the fundamental.

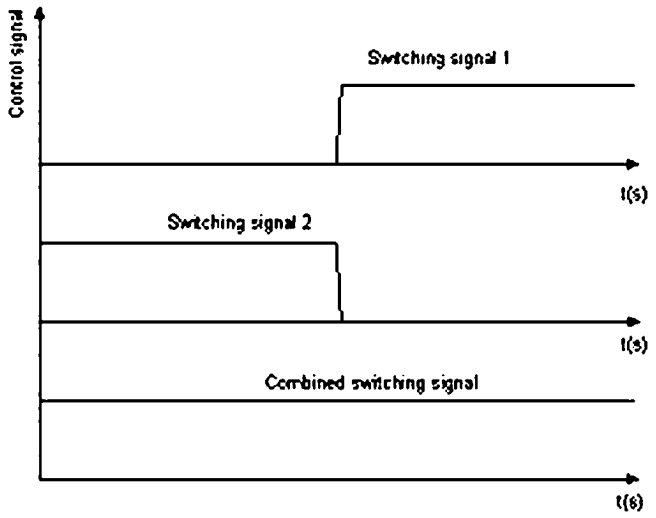

Fig. 4. Minimum pulse width case of switching signal 2 OFF followed by switching signal 1 ON.

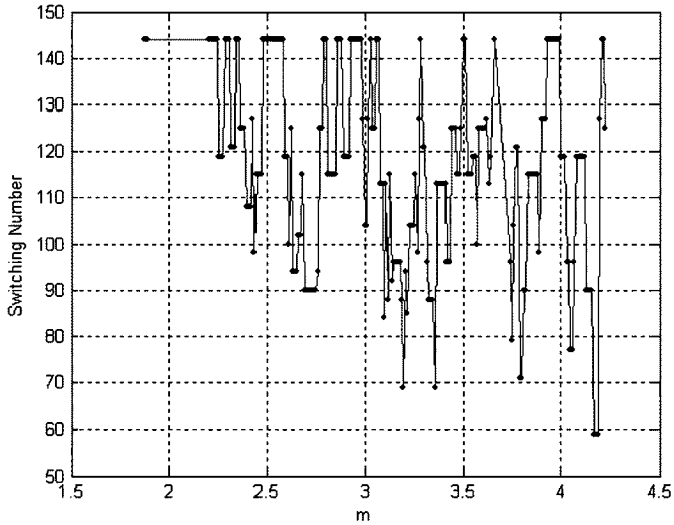

Fig. 5. Switching number for a cycle to eliminate harmonics up to 31st.

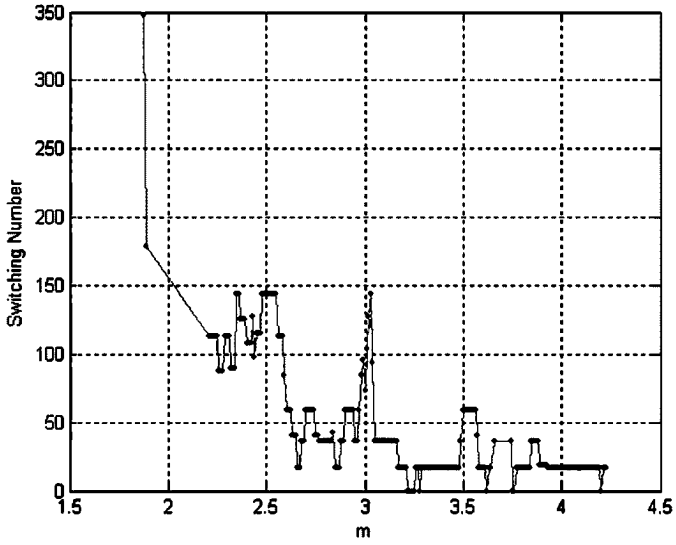

Fig. 6. Switching number for a cycle for 5% THD.

The number of switchings can be computed according to

$$N_{sw} = \sum_{h_i \in \{17,19,23,\ldots,h_{\max}\}} h_i \tag{9}$$

where h_i is the harmonic number of those harmonics chosen for elimination, i.e., harmonics whose amplitudes are greater than 0.5% of the fundamental, and $h_{\max}$ is the maximum harmonic eliminated.

Another case involves minimum pulse width (which is 8.136 μs in the experiments); specifically if a switching OFF time is immediately followed by a switching ON time smaller than the minimum pulse width, then the switch will be left ON until the next switching OFF occurs. This is illustrated in Fig. 4. The switching signal 2 OFF is followed by switching signal 1 ON, and the combined switching signal is left ON. The minimum pulse width will decrease the number of switchings during each period. Although, it is not easy to analytically compute the reduced switching frequency because of the minimum pulse width requirement, the number of switchings can be counted in the simulations.

Using the harmonic elimination method outlined in this paper, there are three possible harmonic elimination strategies.

1) Eliminate all lower harmonics up to a certain number.
2) Eliminate enough harmonics such that THD is below a set limit.
3) Eliminate as many harmonics as possible for a given limit on switching frequency.

As an example of the first strategy, the harmonics are eliminated up to 31st, and the THD is shown in Fig. 3. The switching number for one cycle is shown in Fig. 5. It can been seen that if we eliminate the harmonics up to 31st, the THD will be below 5% except for a few low modulation indices.

For the second strategy, if the THD limit is set to 5% and harmonics with amplitudes less than 0.5% are ignored, the switching number computed for one cycle by (9) is shown in Fig. 6. From Fig. 6, it can be seen that to eliminate harmonics such that the THD of the output voltage is below 5%, the switching number is below 50 for half of the modulation range; it is below 150 for most of the modulation range.

Here, the switching number in a cycle determines the effective switching frequency. For example, if the number of switchings is 50 for a multilevel converter, and the desired output frequency is 60 Hz which is synthesized by five dc sources, then the effective switching frequency is $50 \times 60 = 3\,000$ Hz; however, the switching frequency for each switch is only $50 \times 60/5 = 600$ Hz.

As it is seen from (1), the harmonic spectrum of the active harmonic elimination method is linearly attenuated by the order of the harmonics. For a traditional PWM method, the harmonics in the converter output voltage waveform appear as sidebands, centered around the switching frequency and its multiples [14]. The traditional PWM method cannot completely eliminate the specified low order harmonics. The active harmonic elimination method here can completely eliminate all the specified harmonics. The harmonic elimination method can also be referred to as a computed PWM method because its pulses are computed.

To verify the proposed harmonic elimination method, a simulation case to eliminate harmonics up to 31st with $m = 2.28$ was

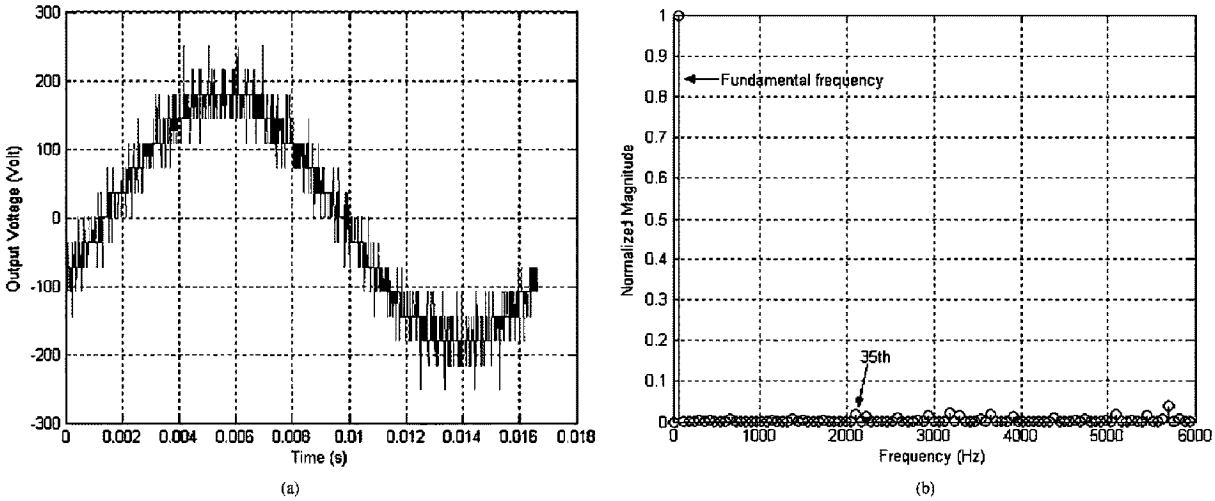

Fig. 7. (a) Simulation line-line voltage with $m = 2.28$ and (b) its corresponding normalized FFT analysis for harmonic elimination up to 31st.

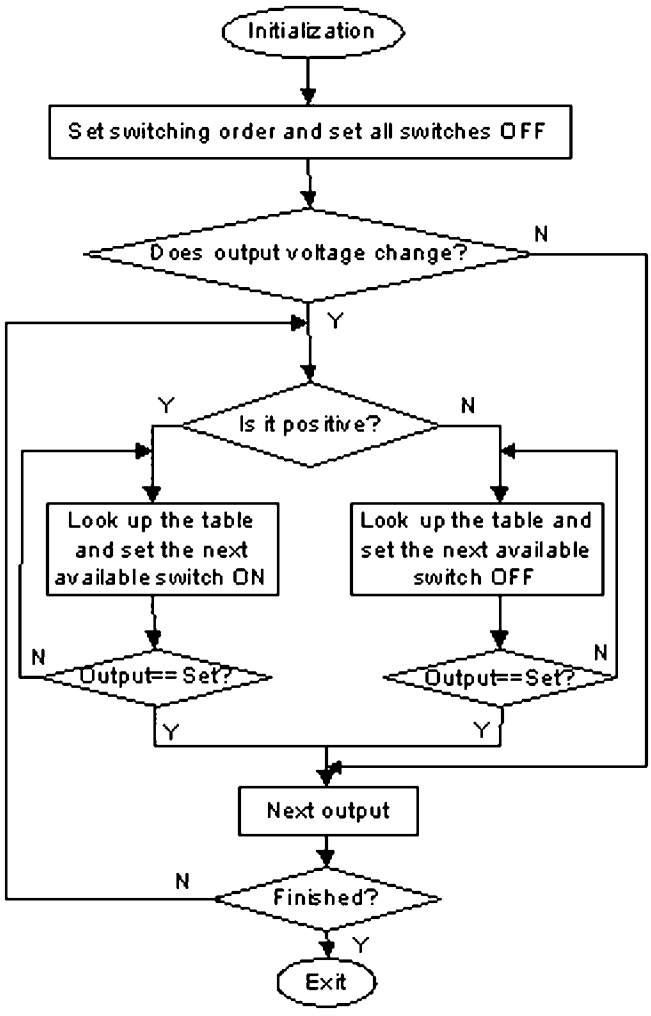

Fig. 8. Control flow chart for first on, first off strategy.

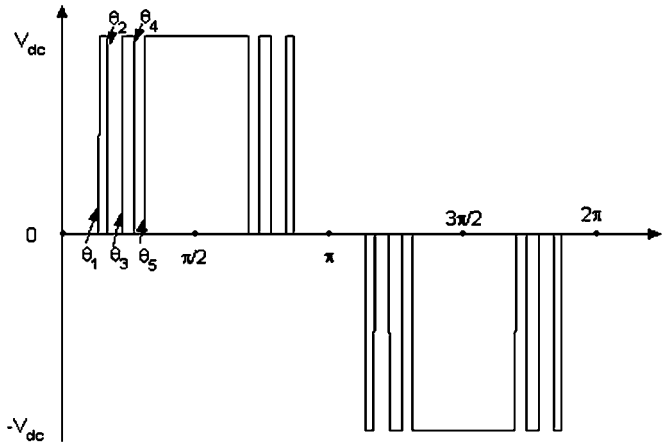

Fig. 9. Five-angle unipolar switching output.

performed. Here, the simulation scheme uses the computed control signals to output ideal phase voltages, from which line-line voltages are found. The line-line voltage and its normalized FFT analysis are shown in Fig. 7. As expected, the line-line voltage has no triplen harmonics and the first nonzero harmonic is the 35th harmonic. There are some spikes in the line-line voltage due in part to the subtraction of one phase voltage from another and in part due to the switching by the multilevel converter to eliminate higher order harmonics.

C. Switching Controls

To balance the switching loss during a whole cycle, the first-on, first-off strategy is employed to control the switching for equal dc voltage situation. The idea for first-on, first-off strategy is to switch the active devices in a rotational pattern such that this strategy distributes the switching times between several levels, and each level has about the same average switching times in a cycle. This strategy can also balance the load between several levels. The control flowchart is shown in Fig. 8. The strategy works as follows: If the next output voltage is higher than the previous voltage, the strategy picks the next available switch in the switch table and turns it on. This process is repeated until the output voltage reaches the desired voltage. A similar procedure is used when the next output voltage is lower than the previous voltage. This process continues until the voltage for a whole cycle has been synthesized.

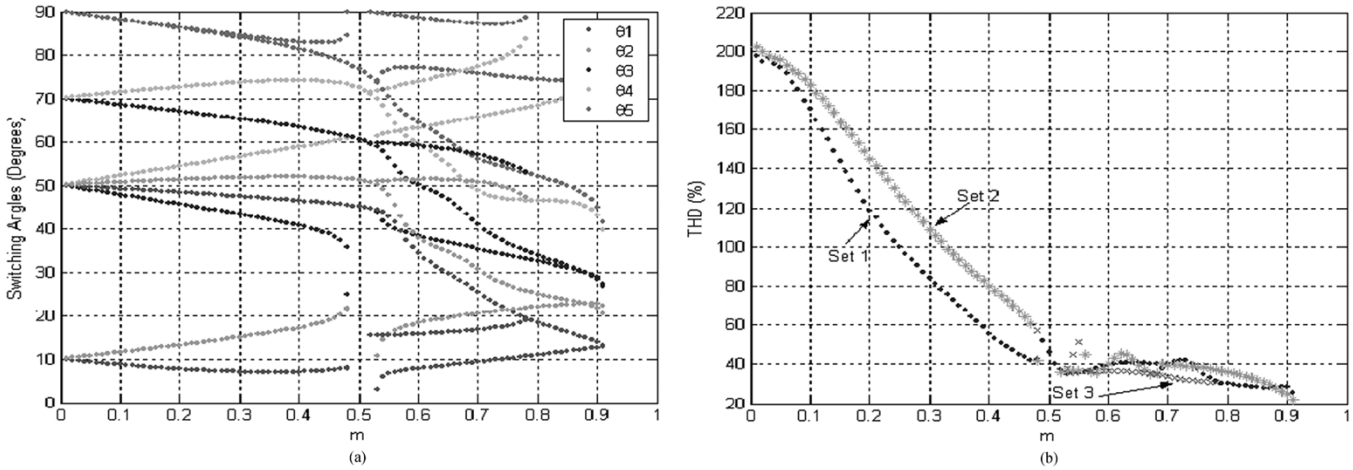

Fig. 10. (a) Five-angle solutions versus m and (b) corresponding THD versus m.

III. Harmonic Elimination for Multilevel Converter with Unequal dc Voltages

A. Decoupled Control and Harmonic Elimination for Multilevel Converter with Unequal dc Voltages

To extend the active harmonic elimination method to cascaded H-bridge multilevel converters with unequal dc voltages, the multilevel converter must be controlled as a set of decoupled, independent H-bridges. Here, a five-angle unipolar switching scheme is used to control each H-bridge, whose output is shown in Fig. 9. Another approach for harmonic elimination with bipolar waveforms has been described in [16].

The Fourier series expansion of the output voltage waveform as shown in Fig. 9 is

$$V(t)=\sum_{n=1,3,5...}^{\infty}\frac{4V_{dc}}{n\pi}[\cos(n\theta_1)-\cos(n\theta_2)+\cos(n\theta_3)-\cos(n\theta_4)+\cos(n\theta_5)]\sin(n\omega t) \quad (10)$$

similar to the equal dc voltage situation, the switching angles can be used to determine the fundamental frequency magnitude and harmonic contents. Here, the fifth, seventh, 11th, and 13th order harmonics are chosen to be eliminated. That is, the switching angles must satisfy (11), shown at the bottom of the page.

The resultant method described in [11] is again used to find the solutions (when they exist) again. The switching angles (θ_1, θ_2, θ_3, θ_4, and θ_5) solutions versus the modulation index m are shown in Fig. 10(a) and (b) which shows the THD corresponding to these solutions.

As seen from the switching angle solutions shown in Fig. 10(a), the solutions exist in a range of the modulation indices from 0 to 0.91. Some modulation indices have no solutions, while there are multiple solution sets for other modulation indices.

Fig. 10(b) shows that different solution sets have different THD values, and that the THD is high for the low modulation index range.

A cascaded H-bridge multilevel converter can be viewed as several unipolar converters connected in series, and these unipolar converters can each be controlled independently. The control method inherently cannot generate low order harmonics because each individual unipolar converter does not generate low order harmonics even with unequal dc voltage sources. Each unipolar converter for $i=1,\ldots,s$ (here s is the number of dc voltage sources) is required to satisfy the equations described in (11), i.e., (12), shown at the bottom of the next page. The whole output voltage of the multilevel converter can be expressed as

$$V(t)=\sum_{i=1}^{s}\sum_{n=1,3,5...}^{\infty}\frac{4c_iV_{dci}}{n\pi}[\cos(n\theta_{i1})-\cos(n\theta_{i2})+\cos(n\theta_{i3})-\cos(n\theta_{i4})+\cos(n\theta_{i5})]\sin(n\omega t). \quad (13)$$

The total modulation index $m=\Sigma_{i=1}^{s}c_i(V_{dci}/V_{dc})m_i$, where V_{dc} is the nominal dc voltage, V_{dci} is the ith dc voltage and c_i (with $c_i\in\{-1,0,1\}$) is a "combination coefficient." If c_i is -1, the unipolar converter outputs negative voltage; if c_i is 0, the unipolar converter output is zero; and if c_i is 1, the unipolar converter outputs positive voltage. For convenience, let $k_i=(V_{dci}/V_{dc})$ so that $m=\Sigma_{i=1}^{s}c_ik_im_i$. The goal is to

$$\begin{aligned}
\cos(\theta_1)-\cos(\theta_2)+\cos(\theta_3)-\cos(\theta_4)+\cos(\theta_5)&=m\\
\cos(5\theta_1)-\cos(5\theta_2)+\cos(5\theta_3)-\cos(5\theta_4)+\cos(5\theta_5)&=0\\
\cos(7\theta_1)-\cos(7\theta_2)+\cos(7\theta_3)-\cos(7\theta_4)+\cos(7\theta_5)&=0\\
\cos(11\theta_1)-\cos(11\theta_2)+\cos(11\theta_3)-\cos(11\theta_4)+\cos(11\theta_5)&=0\\
\cos(13\theta_1)-\cos(13\theta_2)+\cos(13\theta_3)-\cos(13\theta_4)+\cos(13\theta_5)&=0
\end{aligned} \quad (11)$$

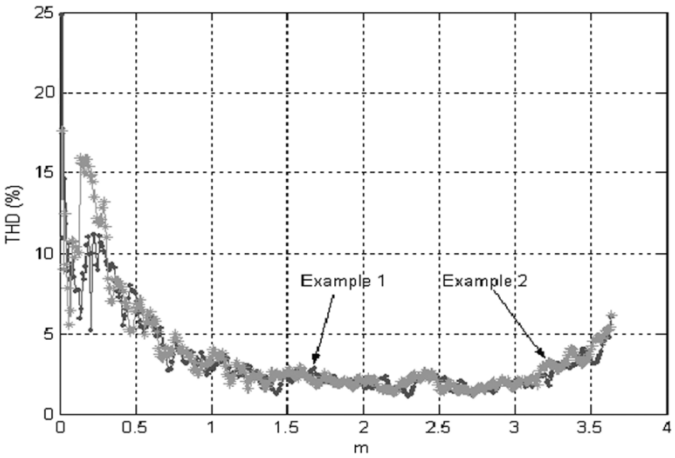

Fig. 11. Minimum THD with fifth to 25th harmonics eliminated.

find then for each modulation index m the combination (c_i, m_i) for $i = 1, \ldots, s$ of the dc sources that gives the lowest THD.

For example, for $s = 4$, the goal is the lowest THD and the elimination of the fifth, seventh, 11th, 13th, 17th, 19th, 23rd, and 25th harmonics. The goal is to find a combination with s separate dc sources with lowest higher order harmonic distortion

$$\text{THD} = \frac{\left(\sqrt{\Sigma_{i=29,31,35,37,\ldots}^{49} V_i^2}\right)}{V_1}. \tag{14}$$

Here, the THD is computed using only the higher order harmonics because the fifth, seventh, 11th, and 13th harmonics are eliminated by the unipolar switching scheme, and the 17th, 19th, 23rd, and 25th are eliminated by the active harmonic elimination method which generates corresponding opposite harmonics to cancel them. A combination of the unipolar switching strategy with the lowest THD is given by (14). Therefore, there are no fifth, seventh, 11th, 13th, 17th, 19th, 23rd, and 25th harmonics, and the 29th, 31st, 35th, 37th, 41st, 43rd, 47th, and 49th are very low.

Consider a numerical example in which $k_1 = 1.1617$, $k_2 = 1.0278$, $k_3 = 0.9722$, $k_4 = 0.9444$. In this case, for each m one must solve $m = \Sigma_{i=1}^{s} c_i k_i m_i$ for the (c_i, m_i) that minimize the THD. The minimum THD achieved by this method is shown in Fig. 11 and labeled Example 1. As another example, let $k_1 = 1.0556$, $k_2 = 1.0278$, $k_3 = 1.0$, $k_4 = 0.9444$ and again the minimum achievable THD is also plotted in Fig. 11 and labeled as Example 2. Although the THD for an individual unipolar converter is high, these examples show that it can be low for a combination of several unipolar converters.

Here, a square wave whose Fourier series expansion is

$$V(t) = -\sum_{i}^{s} \sum_{q=1,3,5\ldots} \frac{4c_i k_i V_{dc}}{q\pi} [\cos(qh\theta_{i1}) - \cos(qh\theta_{i2}) + \cos(qh\theta_{i3}) - \cos(qh\theta_{i4}) + \cos(qh\theta_{i5})] \sin(qh\omega t) \tag{15}$$

is needed to eliminate higher harmonics ($h = 17$, 19, 23, or 25). Similar to the equal dc voltage situation, here, with $h = 17$, the $q = 1$ term of (15) cancels the $n = 17$ term of (13) and the next harmonic of concern that is produced by (15) is at $5 \times 17 = 85$. This harmonic and higher ones (7×17, etc.,) are easy to filter using a low-pass filter. Repeating the above procedure, the 19th, 23rd, etc., harmonics can all be eliminated. The additional number of switching in a cycle for the active harmonic elimination method is $N_{sw} \leq \sum_{\text{n}=17,19,23,25} n$, which is the same as the equal dc voltages case. For example, if the harmonics are eliminated through the 25th, the upper limit switching number is 84 for all the H-bridges.

To verify the theoretical computation, a simulation with $m = 2.86$ and $k_1 = 1.1617$, $k_2 = 1.0278$, $k_3 = 0.9722$, $k_4 = 0.9444$ is implemented using the same simulation scheme as used in the case of equal dc voltages. Fig. 12(a) shows the simulation result with the harmonic elimination up to 25th, and it also contains spikes as previously explained.

The FFT analysis of the line-line voltage of the simulation is shown in Fig. 12(b). The fifth, seventh, 11th, 13th, 17th, 19th, 23rd, and 25th harmonics are zero, and the 29th, 31st, 35th, 37th, 41st, 43rd, 47th, and 49th are very low, near zero.

B. Switching Control Strategy

For the equal dc voltage case, the first-on, first-off strategy is used to distribute switchings and balance the switching loss between several levels during a whole cycle. For the unequal dc voltage case, the switchings for one dc voltage level cannot be switched by the other dc voltage sources. Therefore, first-on, first-off strategy cannot be used to control a multilevel converter with unequal dc sources. To address this problem, a pulse-based switching control strategy is used. A harmonic voltage is split into a series of pulses. If a voltage level cannot generate the necessary pulse, another voltage level is used to generate this pulse based on the following equation:

$$V_{dc1} \cos(\theta_1) = V_{dc2} \cos(\theta_2) \tag{16}$$

where θ_1 and θ_2 are the harmonic switching angles for voltage V_{dc1} and V_{dc2}. Under this condition, two pulses are guaranteed to have the same fundamental frequency content. This process is repeated until all the necessary harmonic pulses have been

$$\begin{aligned}
\cos(\theta_{i1}) - \cos(\theta_{i2}) + \cos(\theta_{i3}) - \cos(\theta_{i4}) + \cos(\theta_{i5}) &= m_i \\
\cos(5\theta_{i1}) - \cos(5\theta_{i2}) + \cos(5\theta_{i3}) - \cos(5\theta_{i4}) + \cos(5\theta_{i5}) &= 0 \\
\cos(7\theta_{i1}) - \cos(7\theta_{i2}) + \cos(7\theta_{i3}) - \cos(7\theta_{i4}) + \cos(7\theta_{i5}) &= 0 \\
\cos(11\theta_{i1}) - \cos(11\theta_{i2}) + \cos(11\theta_{i3}) - \cos(11\theta_{i4}) + \cos(11\theta_{i5}) &= 0 \\
\cos(13\theta_{i1}) - \cos(13\theta_{i2}) + \cos(13\theta_{i3}) - \cos(13\theta_{i4}) + \cos(13\theta_{i5}) &= 0
\end{aligned} \tag{12}$$

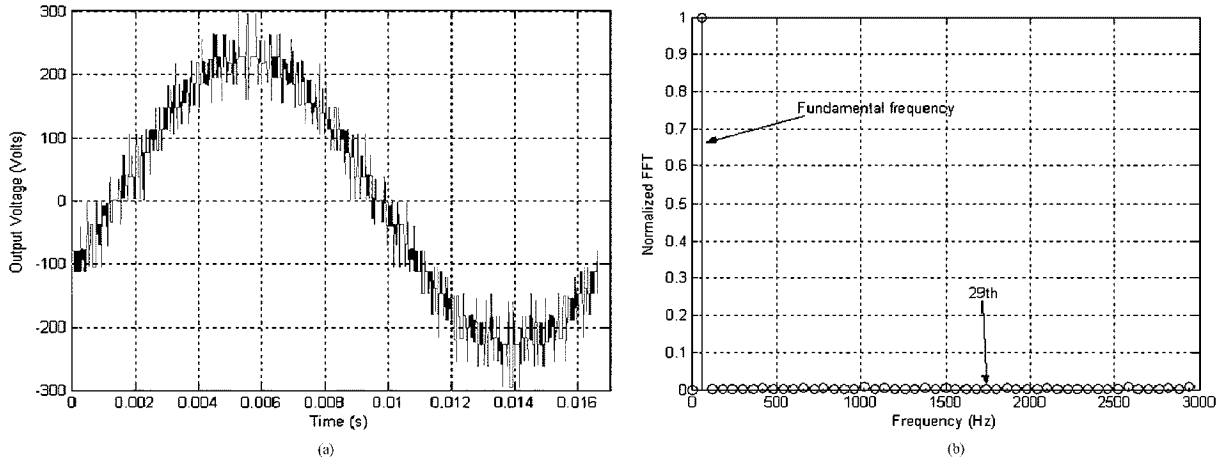

Fig. 12. (a) Simulation voltage waveform with fifth to 25th harmonics eliminated ($f = 60$ Hz) (THD $= 1.79\%$) and (b) normalized FFT analysis of line-line voltage.

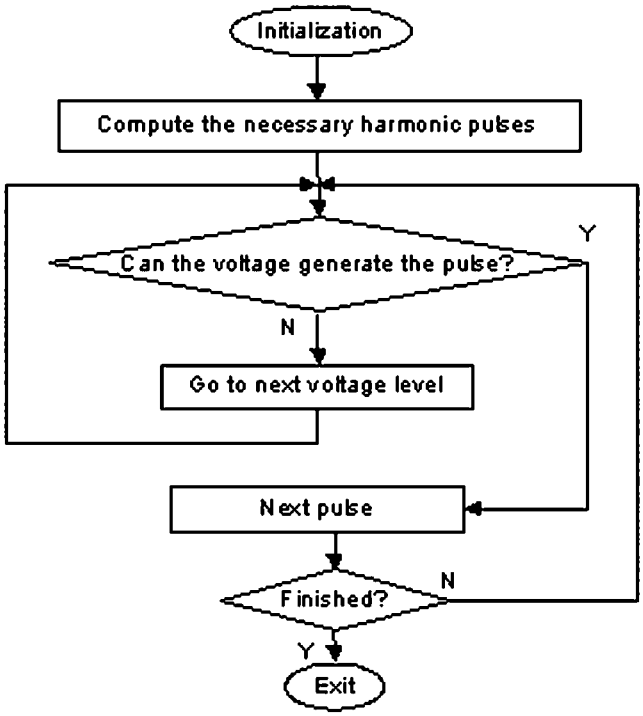

Fig. 13. Pulse based switching strategy.

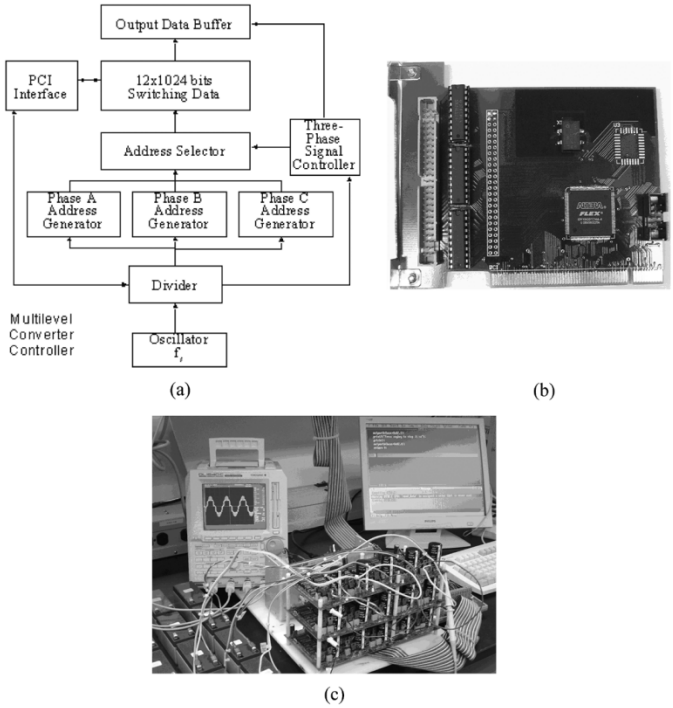

Fig. 14. (a) Block diagram for the FPGA controller, (b) picture of the FPGA controller board, and (c) experimental setup.

generated such that the output voltage will not contain the specified harmonics. This switching control strategy is outlined in the flowchart shown in Fig. 13.

IV. Hardware Implementation

A real-time controller based on an Altera FLEX 10 K FPGA is used to implement the active harmonic elimination algorithm proposed here. The block diagram of the controller is shown in Fig. 14(a) and a picture of the experimental controller board is shown in Fig. 14(b). The whole experimental setup is shown in Fig. 14(c).

The switching signal data are stored in a 12×1024 b in-chip RAM, which is capable of storing one half cycle of data for a multilevel converter with up to 13 dc sources. An oscillator generates a fixed frequency clock signal, and a divider is used to generate the specified control clock signal corresponding to the multilevel converter output frequency. Three phase address generators share a public switching data RAM because they have the same switching data with only a different phase angle. (The switching data is only for one half cycle because the switching data is symmetric.) For each step, the three-phase signal controller controls the address selector to fetch the corresponding switching data from the RAM to the output buffer. The oscillator's frequency is denoted as f_s, the multilevel converter output frequency is denoted as f_0, and there are 2048 steps for each multilevel converter output cycle. The divider number N is then given by

$$N = \frac{f_s}{\left(\frac{f_0}{2048}\right)}. \tag{17}$$

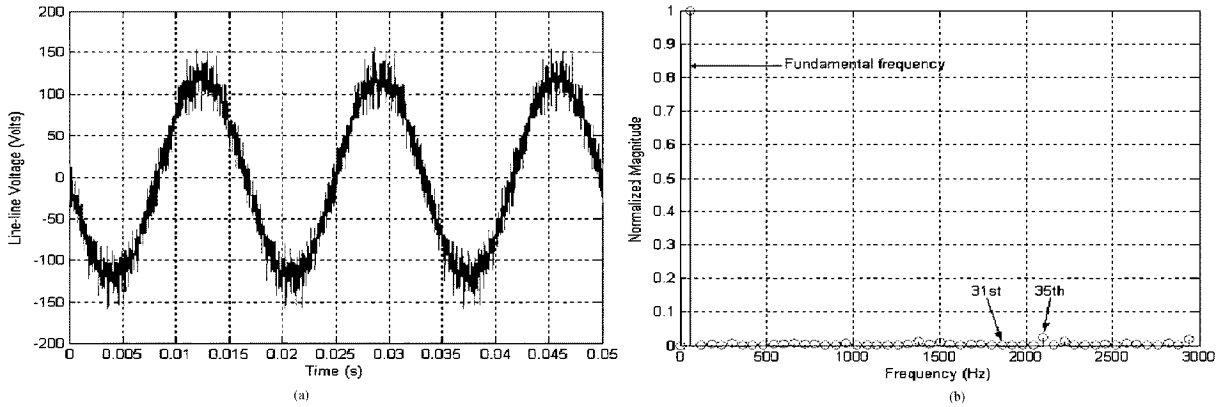

Fig. 15. (a) Experimental line-line voltage with harmonic elimination up to 31st and (b) normalized FFT analysis of line-line voltage. ($m = 2.28$, $f = 60$ Hz).

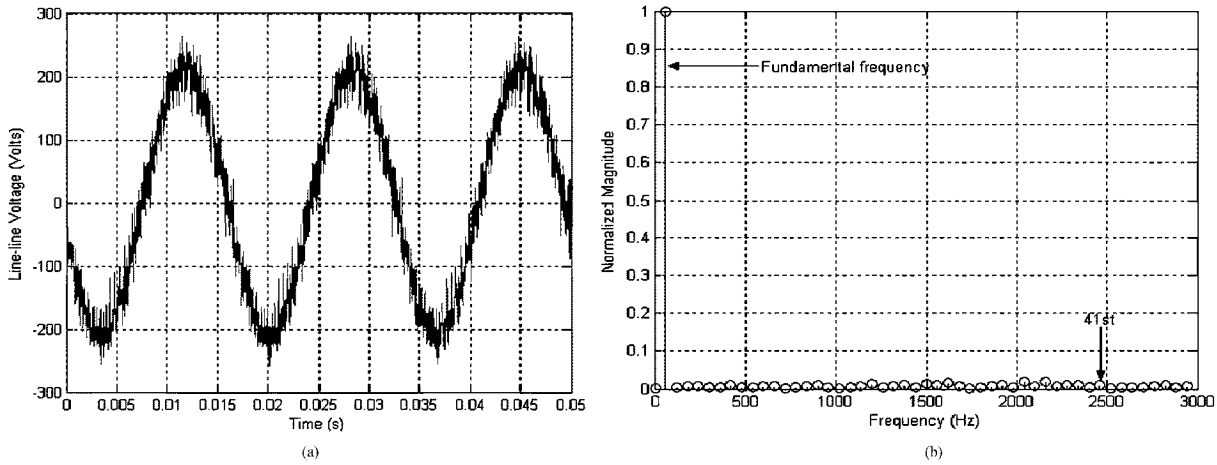

Fig. 16. (a) Experimental line-line voltage with harmonic elimination up to 37th and (b) normalized FFT analysis of line-line voltage. ($m = 2.68$, $f = 60$ Hz).

The control resolution or the step size is

$$T_s = \frac{1}{\left(\frac{f_0}{2048}\right)}. \tag{18}$$

If the output frequency f_0 is 60 Hz, (18) gives the control resolution as 8.138 μs.

For convenience of operation, the FPGA controller was designed as a card to be plugged into a personal computer, which used a peripheral component interconnect (PCI) bus to communicate with the microcomputer. By designing the control system like this, the microcomputer and the FPGA controller can work together to guarantee real-time implementation of the active harmonic elimination algorithm. The microcomputer is used to interface with the user, determine the lowest THD switching angle set, compute the switching signal data, and store the switching signal data into the RAM of the controller. The control signals are generated by FPGA hardware instead of software to guarantee real-time control performance of the system. The system structure also guarantees low computational load of the microcomputer because it just computes the switching data once for each modulation index m and its computational time does not disturb the system's control performance.

V. Experimental Results

The proposed active harmonic elimination method for a multilevel converter with equal dc voltages and with unequal dc voltages has been implemented in an 11-level (5-dc sources) H-bridge multilevel converter. This prototype converter has been built using 60-V, 100-A metal oxide semiconductor field effect transistors (MOSFETs) as the switching devices.

The first experimental study is for the equal dc voltage case. The prototype system was configured to have a nominal dc link of 24 V for each dc source. Fig. 15(a) shows the results of eliminating up to the 31st harmonic with $m = 2.28$ for a 60-Hz phase line-line voltage waveform. Fig. 15(b) shows the FFT analysis of the line-line voltage.

From the FFT plot in Fig. 15(b), it is seen that all harmonics below the 31st have been eliminated. The first nonzero harmonic voltage is the 35th. The THD based on theoretical computation, simulation, and experiment are 3.18%, 3.30%, and 4.0%, respectively.

The second experiment was to eliminate up to the 37th harmonic, again with equal dc voltage sources. The multilevel converter was configured to have a nominal dc link of 36 V for each source. Fig. 16(a) shows the line-line voltage waveform with $m = 2.68$, and Fig. 16(b) shows the FFT analysis of the line-line voltage.

From the FFT plot in Fig. 16(b), it is seen that all harmonics below the 37th have been eliminated. It also can be seen that the 35th harmonic is not exactly zero, this is because the control time step resolution is limited to that of the FPGA resolution which is approximately 8 μs. The first nonzero harmonic voltage is the 41st, which is consistent with both the theoretical computation and simulation. The THD based on theoretical

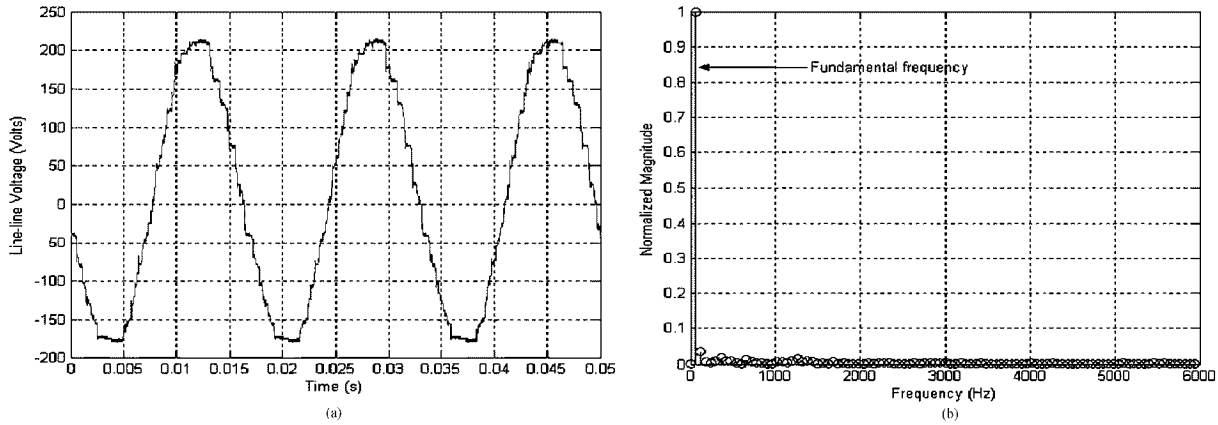

Fig. 17. (a) Experimental line-line voltage with harmonic elimination up to 37th and a 1.1 μF capacitor filter and (b) normalized FFT analysis of line-line voltage. ($m = 2.68$, $f = 60$ Hz).

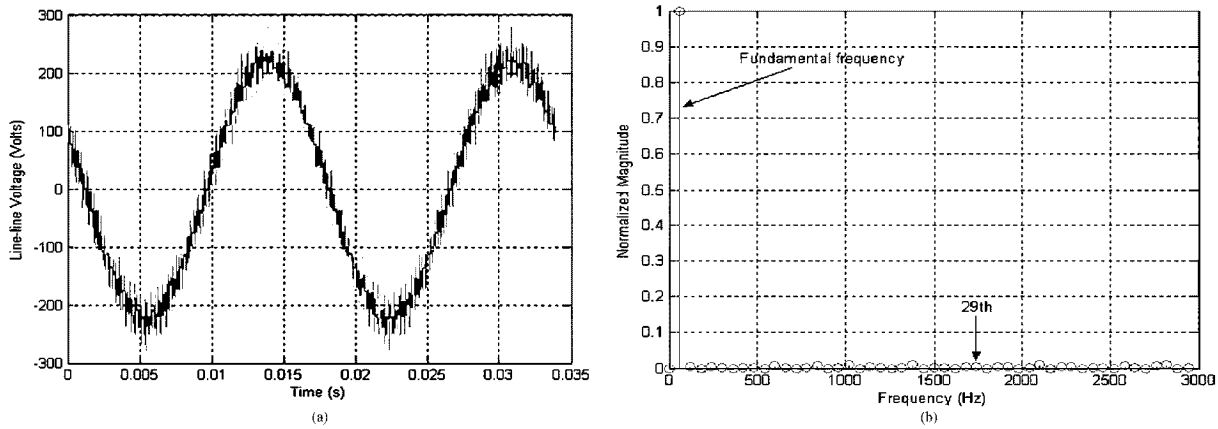

Fig. 18. (a) Experimental line-line voltage with harmonic elimination up to 25th and (b) normalized FFT analysis of line-line voltage. ($m = 2.86$, $f = 60$ Hz).

computation, simulation, and experiment are 3.37%, 3.47%, and 3.23%, respectively.

As a modification to the second experiment, a 1.1 μF capacitor was added to the output of the converter as a filter, and the output line-line voltage is shown in Fig. 17(a). Its normalized FFT analysis is given in Fig. 17(b). It can be seen from Fig. 17 that the output voltage is very near a sinusoidal waveform.

From the FFT analysis in Fig. 17(b), it is obvious that all the higher order harmonics are zero. The THD is 2.58%, which results from low order harmonics. This shows that a small filter can eliminate residual higher order harmonics, and a low THD voltage is then achieved. However, an unexpected 2nd harmonic appears in the spectrum because the charging and discharging current of the capacitor and battery cause the positive half cycle and the negative half cycle to be asymmetrical. This can be seen in the voltage waveform of Fig. 17(a). The reasons for the asymmetry of the voltage are the internal resistances of batteries, switching losses, and capacitor losses. Carefully designed experiments can eliminate the unexpected even harmonics. For practical applications, the converter will be connected with a load and filter, and higher order harmonics will not appear in the output voltages.

In the experiments, the THD is a little higher than that of theoretical computation and simulation because the control resolution is limited to 8 μs, and the switches are not ideal.

The third experiment was done for a case with unequal dc voltages. The proposed switching control method was implemented to eliminate the nontriplen harmonics up to the 25th where $Vdc = 36.0$ V, $m = 2.86$ and $k_1 = 1.1617$ ($V_{dc1} = 41.8$ V), $k_2 = 1.0278$ ($V_{dc2} = 37.0$ V), $k_3 = 0.9722$ ($V_{dc3} = 35.0$ V), $k_4 = 0.9444$ ($V_{dc4} = 34.0$ V).

Fig. 18(a) shows the 60-Hz output line-line voltage waveform. Fig. 18(b) shows the FFT analysis of the line-line voltage. From the FFT plot in Fig. 18, it is seen that all harmonics up to the 25th have been eliminated. The THD based on theoretical computation, simulation, and experiment are 1.31%, 1.79%, and 2.28%, respectively.

From the above experimental results, it can be derived that the proposed active harmonic elimination method can decrease the THD of an output voltage generated by the fundamental frequency switching scheme or unipolar switching scheme. The experiments correspond very well with the theoretical computation and simulation.

From the previous discussion, it can be seen that if lower THD is desired, more switchings are required. However, more switchings will result in higher switching loss. Therefore, for a specific application, there is a tradeoff between THD and efficiency. Because this is a multilevel converter, its effective switching frequency can be higher than the actual switching frequency of individual devices.

VI. Conclusion

An active harmonic elimination method has been proposed and developed to eliminate any number of specific harmonics for multilevel converters with equal dc voltages or unequal dc voltages. The simulation results and experimental results show that the algorithm can be used to eliminate any number of specific higher order harmonics effectively and result in a dramatic decrease in the output voltage THD.

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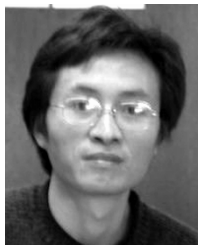

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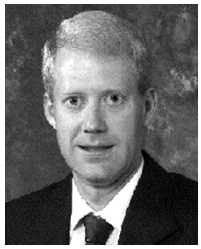

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