Active Pixel CMOS Image Sensor with Single Transistor Architecture

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ABSTRACT

CMOS active pixel image sensor with single transistor architecture (1T CMOS APS) is proposed in this paper and verified by experiment data. By switching the photo sensing pinned diode, reset and select can be achieved by diode pull-up and capacitive coupling pull-down of the source follower. Thus, the reset and select transistors can be removed. In addition, the reset and select signal lines can be shared to reduce the metal signal line, leading to a very high fill factor. The pixel design and operation principles are discussed in detail in this work. The functionality of the proposed 1T CMOS APS architecture has been experimentally verified by a fabricated chip in a standard 0.35 μm CMOS AMIS technology.

Keywords: CMOS image sensors, single-transistor active pixel sensor (1T-APS), fill factor, pinned diode

1 INTRODUCTION

In recent years, there have been continuous research efforts to reduce pixel pitch and/or increase fill factor for high density or high resolution CMOS image sensors (CIS) systems. The most common way to achieve this is to reduce the number of in-pixel transistors based on the conventional 3T or 4T pixel architecture [1]. Sharing the transistors with neighboring pixels has proven to be an effective approach that lead to 2.5T [2], 1.75T [3] and 1.5T [4] pixel structures. In our former work, we have developed an active diode reset pixel that uses the in-pixel photosensing diode itself to perform the reset operation. It avoids the need of an extra reset transistor and results in a compact and simple 2T-APS structure [5].

In this letter, we have developed a new pixel architecture that eliminates both the reset and select transistors by using negative voltage coupling to perform the select operation. This would lead to the ultimate single in-pixel transistor with reduced interconnect lines. The proposed operation and characteristics of the 1T CMOS APS will be presented in this paper.

2 PIXEL ARCHITECTURE AND OPERATION

The cross-section of a 1T-APS pixel is shown in Figure 1. The layout and schematic of a 2-by-2 pixel array are shown in Figure 2. The source follower (M1) is the only transistor in the pixel. As the sensing element of the pixel, the pinned diode structure contains two back-to-back diodes formed by P+/N-well and N-well/P-substrate covering the same area as shown in Figure 2(a). The P+ terminal is connected to the control signal line.

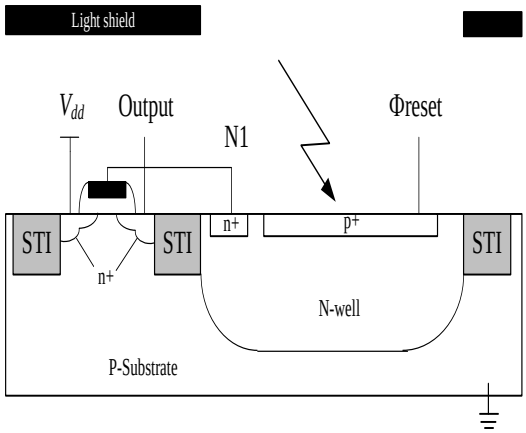
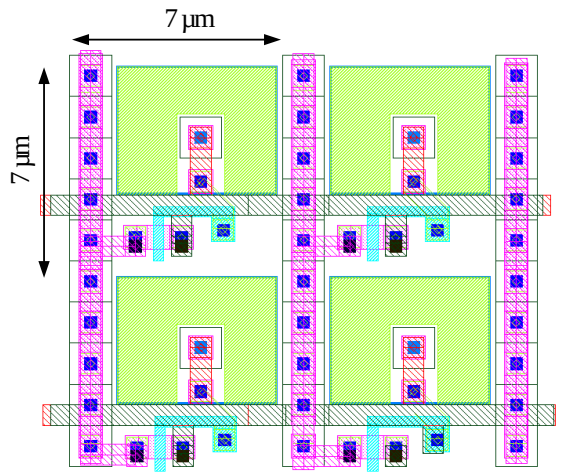
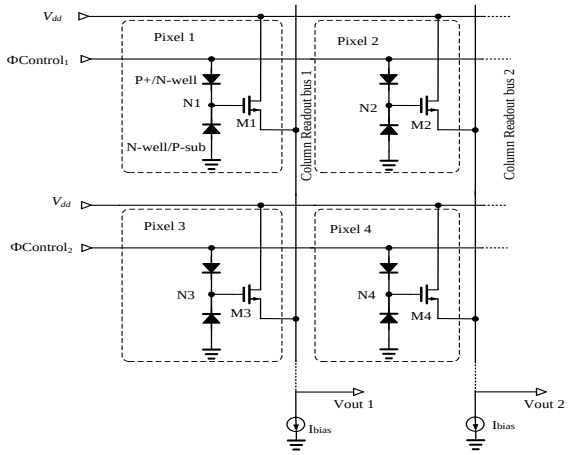


Figure 1: The cross–section of the proposed 1T-APS pixel (N1 stands for the charge sensing node)

The timing diagram to operate a 2-by-2 array shown in Figure 2(b) is given in Figure 3. To reset the active pixel (pixel 1 and 2 in Figure 2(b)), a positive voltage pulse is applied to P+ terminal of the pixels in the assigned row to turn-on the P+/N-well diodes and pull-up the integration nodes through the diode charging current. A charging current will be injected through the diode to the integrating node. Following the reset, the control signal returns to zero to start the current integration mode. The P+/N-well diode becomes part of the photodiode to generate photocurrent for integration. It should be noted that when switching the control signal from reset to the integration mode, the P+/N-well reverse junction diode capacitor is abruptly added to the integration node. The charge stored in the integration node will be redistributed to the newly added capacitor, leading to a sudden voltage drop on the output waveform and deteriorating the dynamic range of the pixel [5]. The magnitude of the voltage drop is proportional to the capacitance of the reset diode and can be adjusted by the area of the P+/N-well diode. To restore the dynamic range of the circuit, a bootstrapping technique can be used to raise the reset voltage at the P+ node beyond the supply voltage [6].



(a)



(b)

Figure 2: (a) The layout of a 2-by-2 pixel array; (b) The schematic a 2-by-2 pixel array

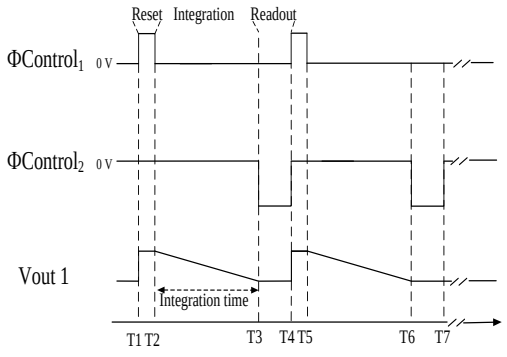


Figure 3:Timing diagram of a 2×2 1T-APS test structure

After the integration phase, the signal will be read. In order to deactivate all the inactive pixels (pixel 3 and 4 in Figure 2(b)), a negative inhibiting voltage is pulsed to the P+ terminals of the P+/N-well diodes so that the integrating nodes are pulled down to zero by capacitive coupling, regardless of the amount of residual charges at the integration nodes as a result of previous operations. The magnitude of the inhibiting voltage is in proportion to the reset voltage level of the integration node, which has to be generated by an on-chip negative charge pump [7] circuit.

Since there is no select transistor to control the pixel output, the 1T CMOS APS can only be operated row by row. Therefore the readout speed for 1T CMOS APS will be slower than that of the conventional APS. For a large-scale image sensor array, the image sensing area should be divided into blocks to increase the parallelism in signal readout.

3 EXPERIMENT RESULTS

The proposed 1T CMOS APS array has been demonstrated in a 0.35µm commercially available AMIS CMOS technology. The resulting pixel size is 7µm×7µm including the guard ring with a fill factor of 46%. The responsivity of the individual diode is first evaluated and the result is shown in Figure 4. It is observed that the photo current density of the N-well/P-substrate diode is about ten times larger than that of the P+/N-well diode. Therefore, the dimension of the P+/N-well diode is not critical for the sensitivity of the photo diode, and can be designed to optimize the capacitive coupling effect during reset and inhibiting operations.

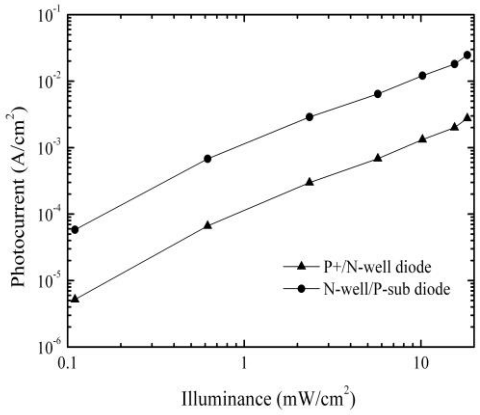


Figure 4: Optical response curves of photodiodes

The fabricated sensor uses the minimum area of the P+/N-well diode to reduce the sudden voltage drop after reset and maintain the dynamic range. The supply voltage used is 3.3V and the inhibiting voltage is -6V. The input waveform and pixel responses under different illumination intensities are shown in Figure 5. The voltage after reset is

about 1.7V due to voltage drop at the diode and the threshold voltage of the source follower. This voltage drop is similar to the conventional 3T CMOS APS architecture, which can be recovered by using a bootstrapping circuit. The voltage drop due to switching of the P+/N-well diode is about 300mV, which is reasonable and does not cause significant deterioration in the dynamic range. The experimental result also shows that at -6V, the inhibiting voltage can successfully deactivate the pixel when it is inactive.

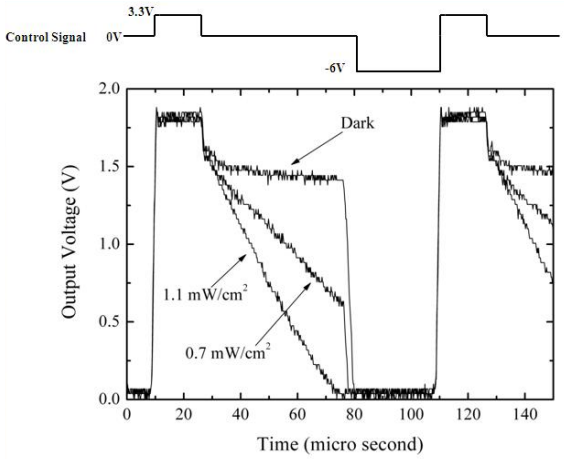


Figure 5: Measurement pixel output characteristics under different light intensity together with the darkness conditio

4 CONCLUSION

We have developed a single-transistor CMOS active pixel sensor architecture and experimentally demonstrated it. The new architecture significantly increases the fill factor and pixel density by reducing the number of in-pixel transistors and interconnect lines. There are some drawbacks in the new pixel architectures, including slower speed, lower dynamic range due to extra voltage drop after reset and the need of a negative voltage to inhibit the inactive pixels. The drawbacks, however, can be overcome by design techniques such as dividing large sensor array into blocks, bootstrapping, and the inclusion of on-chip charge pump circuits.

ACKNOWLEDGMENT

This work was partially supported by the Key Project of National Natural Science Funds of China (61036004). This work is also supported by the supported by the National Natural Science Foundation of China (Grant No. 61204063), the Shenzhen Science & Technology Foundation (CXB201005250031A), and the Fundamental Research Project of Shenzhen Science & Technology Foundation (JC201005280670A, JC201105180781A, JCYC20120618163025041).

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