Active pixel sensors: the sensor of choice for future space applications

Johan Leijtens(1), Albert Theuwissen(2), Padmakumar R. Rao(2), Xinyang Wang(2), Ning Xie(2)

[(1)]TNO Science and Industry, Postbus 155, 2600 AD Delft, The Netherlands, email: johan.leijtens@.tno.nl
[(2)]Delft University of Technology, Mekelweg 4, 2628CD Delft, The Netherlands

ABSTRACT

It is generally known that active pixel sensors (APS) have a number of advantages over CCD detectors if it comes to cost for mass production, power consumption and ease of integration. Nevertheless, most space applications still use CCD detectors because they tend to give better performance and have a successful heritage. To this respect a change may be at hand with the advent of deep sub-micron processed APS imagers (< 0.25-micron feature size). Measurements performed on test structures at the University of Delft have shown that the imagers are very radiation tolerant even if made in a standard process without the use of special design rules. Furthermore it was shown that the 1/f noise associated with deep sub-micron imagers is reduced as compared to previous generations APS imagers due to the improved quality of the gate oxides. Considering that end of life performance will have to be guaranteed, limited budget for adding shielding metal will be available for most applications and lower power operations is always seen as a positive characteristic in space applications, deep sub-micron APS imagers seem to have a number of advantages over CCD's that will probably cause them to replace CCD's in those applications where radiation tolerance and low power operation are important

Keywords: 0,18 micron, CMOS, APS, Sunsensor, Microned, TNO, TU-Delft, Radiation tolerant, Low noise.

1. IMAGERS FOR SPACE APPLICATIONS.

For any space application there will be a trade-off concerning several key performance parameters when selecting an imager. The main criteria used for this are:

- Quantum efficiency* fill factor
- Reliability
- Power consumption
- Radiation tolerance

Although CCD's still perform significantly better on the first criterion (mainly due to the higher fill factor), APS imagers in the meantime seem to outperform CCD's on all the other ones. Reliability of the sensors system and power consumption are interrelated in the sense that CCD's generally require several highly accurate voltages to operate properly and timing circuits need to be integrated on a different chip because of process incompatibilities. All in all, this inevitably leads to a more complex and therefore less reliable sensor system. In addition to this, the large capacitances that need to be driven for a CCD will automatically lead to higher power consumption.

At the University of Delft significant effort is spent in designing an APS imager in a 0.18-micron CMOS process which is intended to be used for TNO's micro digital sunsensor. The design of the sensor has made significant process [1].

Due to the use of standard CMOS technology a lot of functionality can be included in the chip without significantly increasing power consumption.

Additional tests performed on test structures have shown that the use of a standard deep sub-micron CMOS process comes with a number of advantages without additional effort.

Sensors, Systems, and Next-Generation Satellites XI
edited by Roland Meynart, Steven P. Neeck, Haruhisa Shimoda, Shahid Habib
Proc. of SPIE Vol. 6744, 67440V, (2007) · 0277-786X/07/$18 · doi: 10.1117/12.735512

2. THE MICRO DIGITAL SUN-SENSOR.

The micro digital sun-sensor is one of these products under development at TNO in co-operation with the Delft University of Technology. It is developed in frame of the Dutch "Microned" program. This program is intended to increase the knowledge and stimulate the application of micro system technology in the Netherlands.

A sunsensor is an attitude control sensor that senses the position of the sun with respect to its mounting plane. This type of sensor typically operates as a photo-diode of which the current produced is proportional to the angel of incidence (coarse sun-sensors) or a photo diode array with a suspended membrane (fine sun-sensors). In case the photodiode array is a real 2D array, the sensors are called digital sun-sensors. TNO's digital sunsensors currently use a standard active pixel sensor array and a standard FPGA for signal processing. The APS sensors are selected because the amount of light available is much more than the signal required for proper operation and their ability to do windowing (create a window of interest on the sensor which is read out at a higher speed while discarding the information from the other part of the sensor). This has lead to fairly compact (11cm*12cm footprint) sensors that have a high degree of flexibility and allows one to readout the sun position at a very high rate while achieving a low power consumption (1.3W without and 1.7W with DC/DC converter). During the design of the qualification model (which includes a DC/DC converter), it was however noted that the power supply sub-circuits actually account for a large part of the mass and power budgets.

The idea behind the digital sunsensor is quite simple. A sunsensor can only do a sensible job in case the sun is present. This observation has lead to the concept of a sun-sensor powered with a self-standing solar cell power supply. During the phase A of the sensor design, it was concluded that three main items would eventually limit the size of the package:

- Size of the connector used.
- Power consumption.
- Size of the patch antenna.

The micro digital sunsensor consists of a dedicated Active Pixel Sensor (APS) that includes both an Analog to Digital converter and the required digital signal processing for centroïd calculation of the sunspot incident on the APS sensor. The sunspot is generated by means of a membrane pinhole in front of the detector device that is directly bonded to the APS chip. This APS+ (= APS imager including ADC and processing electronics) leads to a very small and low power device (estimated APS+ size 6*7*2mm^3).

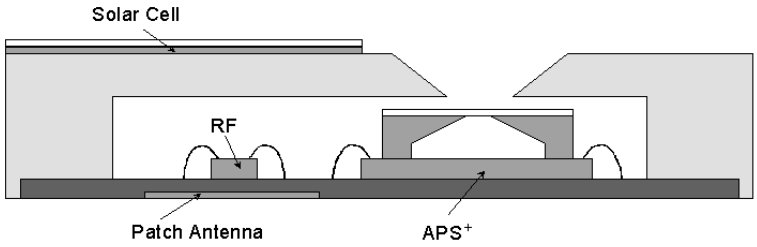

Fig. 1. µDSS cross section.(not to scale)

This highly integrated sensing core can be used to device small but capable sensor systems that can provide sun attitude information with an accuracy that is currently only available for much larger sensors. The level of integration foreseen for this sensor can never be achieved with CCD's, which makes it a logical choice to use a CMOS APS. The total functionality as projected for the APS+ is quite high as can be seen in fig 2. This complexity in combination with the low power consumption of the 0,18-micron process are key to the high performance of the APS+ and the micro digital sunsensor.

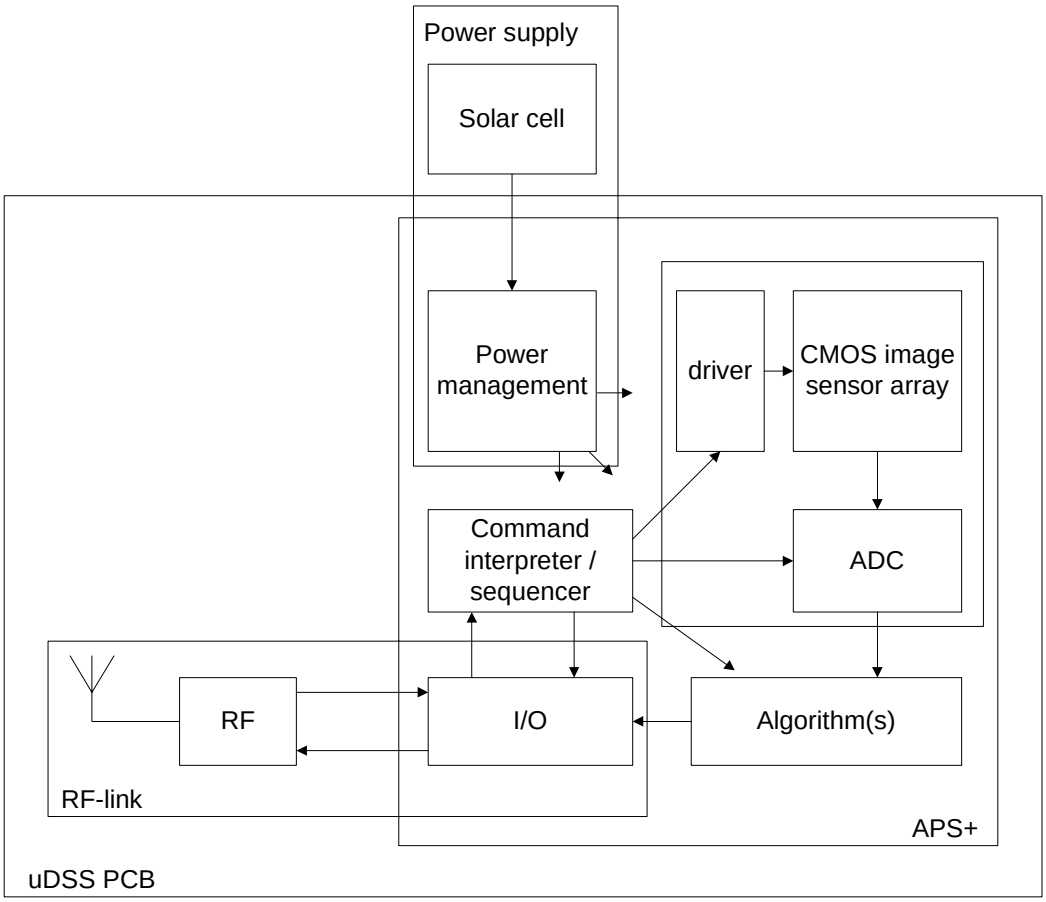

Fig.2. Block Diagram

3. APS+ FUNCTIONALITY

The APS+ is a 512*512 pixel sensor array which has basically two main modes of operation:

- Sun acquisition mode
- Sun tracking mode

During sun acquisition, the entire array is scanned and checked for sun presence. During sun tracking, only the sun illuminated portion of the sensor and some small parts around it are scanned in order to reduce the number of readout cycles as much as possible (thus reducing power consumption). By using a dedicated readout mode during the sun acquisition mode, the power consumption can be kept more or less constant for both modes of operation (thus easing the power sub-system design). The windowing function is essential for the tracking mode of operation: which is one of the main reasons to use a CMOS APS. The dedicated sun acquisition mode could also only be implemented in a CMOS process.

The tracking mode uses the so called winner takes all principle. During the acquisition process, a row and a column profile are created automatically. This means that in one read of the row and one read of the column bus, a full profile of the detector surface can be generated indicating where the highest intensities are present on the imager.(see fig(3)).

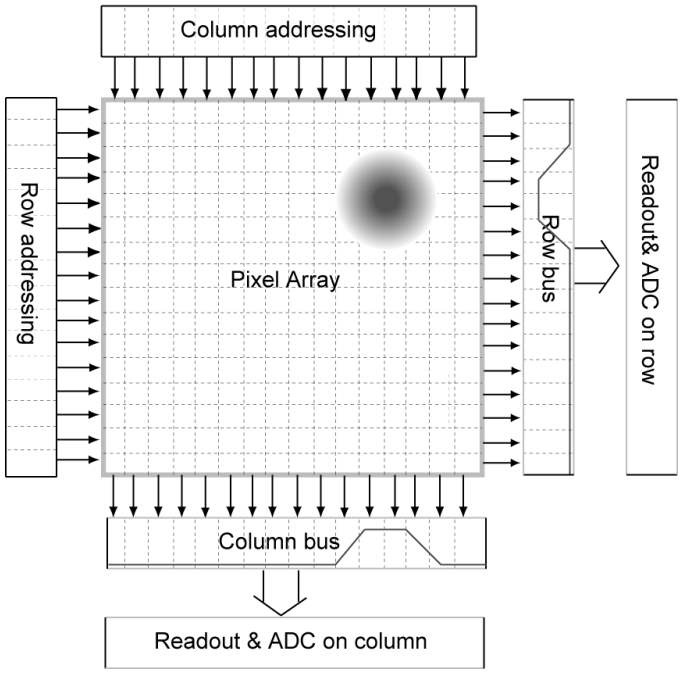

Fig. 3. Sun acquisition column readout

In order to prevent duplication of the readout electronics and in order to be able to use the ADC for reading out both the row and column profiles, at strategic positions in the array, switches are located that will allow to make a connection between the row and column busses (fig 4).

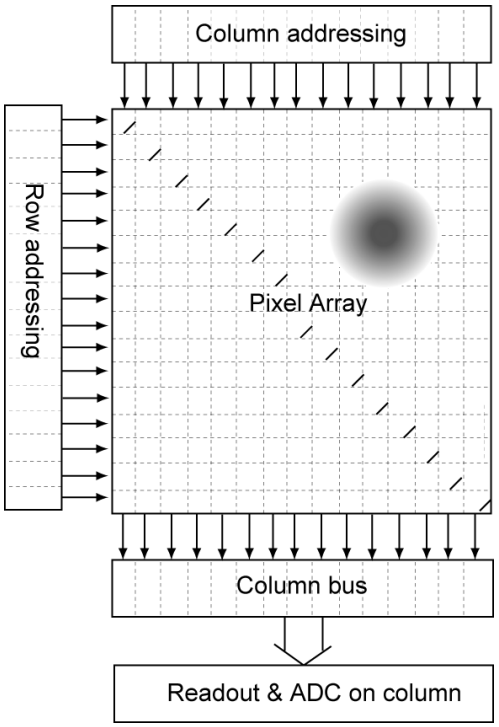

Fig.4. Architecture with readout and ADC sharing

These switches allow to realize the same functionality but with significantly less circuitry (thus saving valuable real estate). During the acquisition process, first a column profile is created and read out (512 clock cycles) and then the switches are closed and a row profile is readout (another 512 clock cycles). This way, 510x512 clock cycles are saved with respect to reading out the entire array and the required number of cycles is comparable to the number of clock cycles needed to readout the 21x21 pixels tracking window that will be positioned around the approximately 10 pixel wide sun image.

4. 0.18 MICRON CMOS IMAGER PROPERTIES.

Most of the properties (like power dissipation etc) are fairly predictable in case the manufacturers design data is used. In order to investigate the intrinsic properties of the used 0.18-micron CMOS process with respect to a number of less well known properties, a number of dedicated test structures have been generated. These test structures called finger gated-diodes (FGD's in short) are used to characterize certain properties of the process. This not only comprised fixed pattern noise [Ref2] but also gamma irradiation testing [Ref3] and [Ref 4].

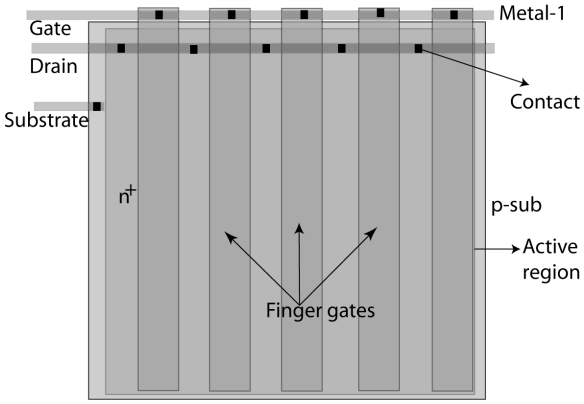

Fig. 5. Finger gated-diode structure

The used test structures are fairly simple (fig5) but allow the investigators to directly control the gate, thus allowing an as strict as possible discrimination between edge, bulk and gate effects.

These fairly simple test structures were used to do some fundamental verifications on the behavior of image sensors created in the standard process. Standard process in this case means that no special layout provisions where take to for instance enhance radiation resistance.

A number of properties have been evaluated, with the most striking ones being 1/f noise and radiation tolerance.

4.1. 1/f noise

During the investigations performed .[Ref2] it was found that the random telegraph noise exhibited by the pixels under investigation yielded noise voltages with discrete levels (fig6). This is especially true for pixels exhibiting much 1/f noise. The bulk of the pixels show standard thermal noise behavior (pixels A,B,C) with sometimes a reading that is significantly higher (C) the more noisy pixels (E,F,G) however show distinct discrete levels of output signal.

More in depth analysis showed that the most likely of this noise behavior are due to interface traps at the silicon/ silicon dioxide interface of the source follower. The fact that the discrete levels exist, is a good indication that only a very limited number of these traps are present, which has lead to the conclusion that the deposited oxides are of very high quality.

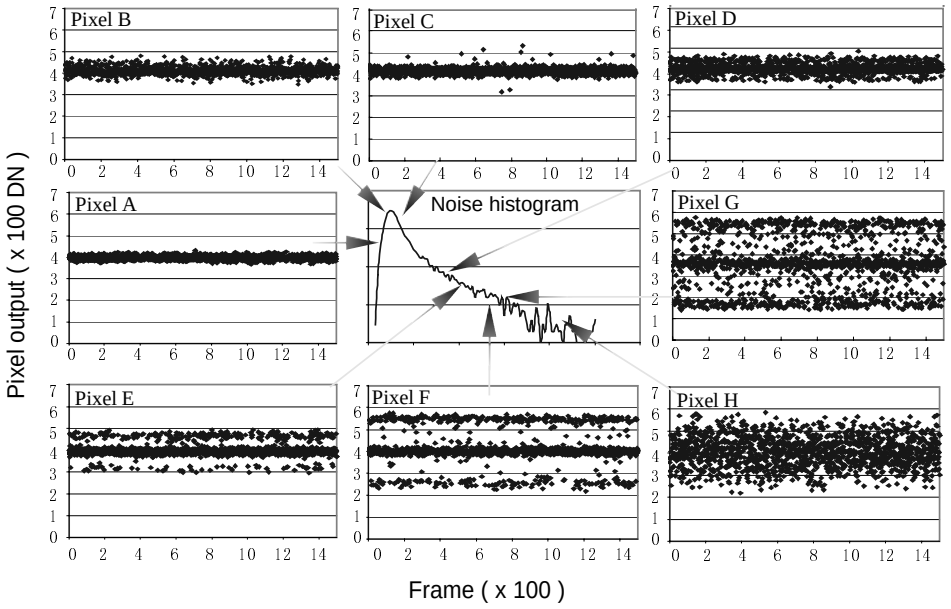

Fig. 6. Noise measurements on APS pixel

During further investigations [Ref3] it was found that the same traps located in the transmission gate are also responsible for the generation of fixed pattern noise, leading to the conclusion that although the used oxides are of very high quality, further improvement of the oxide quality would lead to further improvement for the APS imagers in both 1/f noise behavior and fixed pattern noise.

4.2. Radiation tolerance

In order to establish the suitability of the APS imagers for space or medical X-ray applications, a number of irradiation tests have been performed using gamma radiation. The results of these tests [Ref4,Ref5] have shown that even though no special design precautions have been taken, the pixels as produced show significant radiation tolerance.

Fig 7 shows that a general decrease in quantum efficiency can be observed which is limited to some 10% for 400 Grays (40 krad) and 20% for 800 gray (80 krad). This linear decrease of sensitivity is in good agreement with the predictions. Fig 8 shows an increase in dark current which is acceptable too, leading to the conclusion that 0.18-micron APS imagers are much more radiation tolerant then common CCD imagers or APS imagers generated in processes with larger feature sizes.

As most space programs require no larger radiation tolerance than 20 krad(Si) and as it has been proven that special design rules can increase radiation tolerance of 0.5 micron processes to the 100krad level, 0,18 micron technology seems very well suited for use in space application.

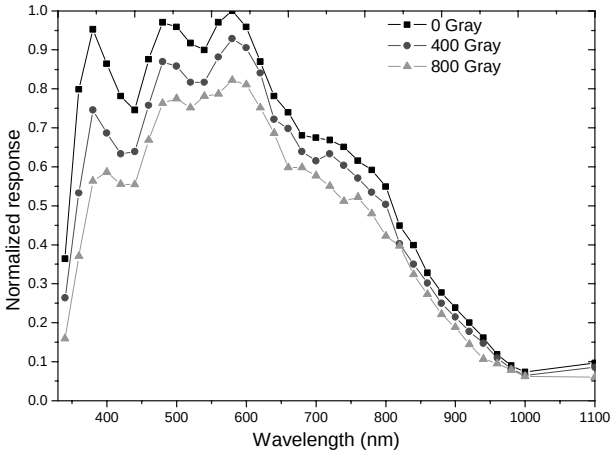

Fig. 7. Spectral response as a function of wavelength and gamma radiation dose

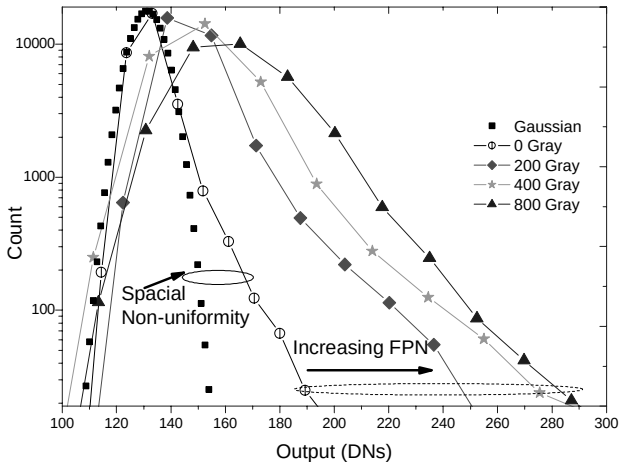

Fig. 8. Dark signal histogram (at room temperature) as a function of gamma radiation dose

5. CONCLUSIONS

0.18-micron CMOS processes are more and more used to create imagers that are both small and power efficient. Investigations have shown that even standard imagers that use these processes are capable of performing as required even after having received a serious dose of gamma radiation.

The possibility to add signal processing capabilities opens up new application possibilities at minimum additional power demand, thus allowing making highly integrated imaging systems.

Although some issues (which are also worked on) are still acting in favour of CCD's (like quantum efficiency linearity and blue response) the increased radiation tolerance, possibility to add signal processing functionality, lower power consumption and mainstream silicon processes used, drive people more and more into the conclusions that Active pixel sensors are the sensors of choice for future space applications.

6. REFERENCES

1. Ning Xie, CMOS image sensor in 0.18 μm Technology for a Micro-Digital Sun Sensor , Graduation thesis Delft University of technology, July 2007.
2. Xinyang Wang, Padmakumar R. Rao, Adri Mierop, Albert J.P. Theuwissen "Random Telegraph Signal in CMOS Image Sensor Pixels", IEEE International Electron Device Meeting (IEDM), US, Dec 2006.
3. Xinyang Wang, Padmakumar R. Rao and Albert J.P. Theuwissen "Fixed-Pattern Noise Induced by Transmission Gate in Pinned 4T CMOS Image Sensor Pixels", European Solid-State Device Research Conference (ESSDERC), Switzerland, Sep 2006.
4. Padmakumar R. Rao, Xinyang Wang, Adri J. Mierop and Albert J.P. Theuwissen, "Gamma-Ray Irradiation Effects on CMOS Image Sensors in Deep Sub-Micron Technology", International Image Sensor Workshop, Ogunquit, June-2007.
5. Padmakumar R. Rao, Xinyang Wang, Albert J.P. Theuwissen, "Radiation Hardness of Deep-Submicron CMOS Technology Evaluated by Gated-Diode Measurements", Sense of contact-2007.