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Adaptive DC-Link Voltage Control for Shunt Active Power Filters Based on Model Predictive Control

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ABSTRACT DC-link voltage directly affects the compensation range and performance of shunt active power filters (SAPFs). DC-link voltage in SAPF is generally high, fixed, and dependent on rated power. DC-link voltage could become excessive in low-load conditions, which increases switching loss and switching noise. Optimized DC-link voltage was obtained in this study to enhance compensation adaptability for variable nonlinear loads and fluctuation in grid voltage. We proposed a novel adaptive DC-link voltage control for SAPFs, which reduced switching noise and switching loss during operation. The proposed DC-link voltage control method employed model predictive current control, proportional voltage control and calculation of optimal DC-link voltage. A real-time observer, which was insensitive to distorted grid condition, was used to capture peak grid voltage. Finally, simulations and the results of experiments were used to verify the effectiveness and feasibility of the proposed DC-link voltage control method.

INDEX TERMS Shunt active power filters, DC-link voltage, model predictive control, switching loss, switching noise.

I. INTRODUCTION

An increasing number of nonlinear loads are interfaced into power grids, which introduces harmonics and reactive power [1], [2]. Harmonics induces several issues in electrical devices, such as transformer overheating, communication disturbances, LC resonance, increased neutral current, and low power factor [3], [4]. A low power factor induces reactive power, which increases system losses and reduces grid stability. Shunt Active Power Filters (SAPFs) are used to compensate for the challenges posed by increasing amounts of nonlinear loads in power grids [5].

Maintaining the stability of DC-link voltage directly affects the system output and it is important in ensuring the normal operation of converters. DC-link voltage adjusters are crucial in SAPFs because capacitors are required on the DC side of SAPFs to mitigate instantaneous active power, which maintains the stability of DC-link voltage [6], [7].

In [8], it is denoted that the switching loss increases with DC-link voltage: SAPFs with high DC voltage produce high switching loss, and vice versa. DC-link voltage in SAPFs is usually high, fixed and dependent on rated compensation power. Output range increases with increasing DC-link voltage; hence, DC-link voltage could become excessive for low-load conditions. This increase switching loss and switching noise. Many optimization schemes, based on hardware [9], [10] and software [11-13], have been proposed to mitigate these challenges. Software optimization schemes are preferred, because unlike hardware optimization schemes, they don't alter SAPF topology or incur additional costs.

In [14], a drop regulator, which considered coupling point voltage and load power level, was proposed to optimize the reference DC-link voltage. This drop regulator partially realized comprehensive optimization among the power loss, switching noise, and SAPF compensation. The reduction of reference DC-link voltage as point of common coupling (PCC) voltage decreases is unsuitable for some operation conditions. In systems with low short-circuit capacities, PCC voltage decreases with increasing load power, which is contradictory to the increasing demand for higher compensating capacities. The load in power grids changes in real time; therefore, harmonics also change in real time. Switching noise and switching loss are significantly reduced if DC-side voltage is adjusted according to load condition in real time. In [12], an adaptive DC-link voltage control

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strategy was proposed, which relied on a selective harmonic detection function to extract amplitude information from each sub-harmonic current and grid voltage. The peak value of AC-side voltage can be obtained using Kirchhoff's law; however, the process is complicated when tracking hybrid-frequency current. In [13], method from [12] were applied to traditional two-level SAPF. The reference DC-link voltage was obtained through accumulating the required DC-link voltage related to each harmonic. This method ignored the effect of phases; therefore, it couldn't precisely calculate the lowest voltage, and it caused additional power loss [15]. The implementation of the method was also complex to implement the aforementioned methods [16].

Model predictive control (MPC) is able to control multiple-targets through simple constraints and cost function. MPC is applied in a single-frequency two-level inverter to realize the current control and modulation. Switching frequency under MPC is just 1/5-1/4 of sampling frequency [17]; thus, the output inductance of L-type filter should be larger in order to improve filtering. This means the DC-link voltage has additional space for compression when load changes [18]. There is a need to conducting research into adaptive DC-link control for SAPFs with MPC current loop.

The main contributions of this paper are as follows:

1) We propose an adaptive DC-link voltage method to optimize the compensating performance and power loss. The proposed method is independent of selective harmonic detection. It is unnecessary to consider amplitude information and phase effects between harmonic current and coupling point voltage.

2) This study applied the proposed adaptive DC-link voltage control for SAPF with MPC current tracking in order to comprehensively reduce switching loss and switching noise.

This paper used a mathematical model to explain why DC-link voltage affects compensation in SAPFs. The impact of harmonic current phase on the calculation of reference DC-link voltage is analyzed in traditional methods based on FFT. Then a novel passive observation method was used to achieve the lowest theoretical voltage level and avoid selective harmonic detection. Finally, we used simulations and the results of experiments to verify the effectiveness and superiority of the proposed method for adaptive DC-link voltage control.

II. SYSTEM ANALYSIS

A. SAPF MODELING

The object of research in this paper is a typical three-phase three-wire SAPF with *L*-type filter, as shown in Fig. 1. Referring to Fig. 1, subscripts distinguish phases A, B and C. e represents PCC voltage, i_S represents source current, i_{Lx} is load current, i_C represents output current from SAPF, v_N represents AC-side voltage relative to DC-link neutral point, and u_{dc} represents DC-link voltage.

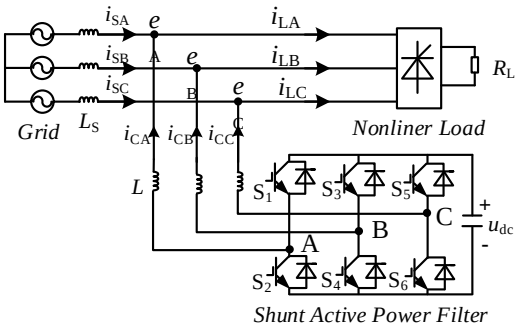

FIGURE 1. SAPF topology.

The space vector transformation is

$$\boldsymbol{x} = \frac{2}{3}(x_A + \alpha \cdot x_B + \alpha^2 \cdot x_C) \tag{1}$$

where $\alpha = e^{j2\pi/3}$ is the rotation operator and $\boldsymbol{x}$ is the space vector form of variables x_A, x_B and x_C. Space vector were adopted to simplify analysis.

According to Kirchhoff's voltage law, the continuous-time vector model of SAPF is

$$\boldsymbol{v} = R\boldsymbol{i}_C + L\frac{\mathrm{d}\boldsymbol{i}_C}{\mathrm{d}t} + \boldsymbol{e} \tag{2}$$

where L and R are output inductance and equivalent thermal resistance respectively. Heat loss is usually neglected to simplify analysis. Then, Equation (2) can be rewritten:

$$\frac{\mathrm{d}\boldsymbol{i}_C}{\mathrm{d}t} \approx \frac{1}{L}(\boldsymbol{v} - \boldsymbol{e}) \tag{3}$$

Referring to (3), the gradient of compensation current $\mathrm{d}\boldsymbol{i}_C/\mathrm{d}t$ is determined by grid voltage $\boldsymbol{e}$ and the AC side voltage of SAPF $\boldsymbol{v}$. Considering that $\boldsymbol{e}$ is dominated by the power grid, $\boldsymbol{v}$ is the unique degree of freedom to adjust $\boldsymbol{i}_C$. So harmonic suppression improves with larger adjustment range for $\boldsymbol{v}$.

The switching function of each leg is defined as

$$S_A = \begin{cases} 1, (S_1: \mathrm{ON},\ S_2: \mathrm{OFF}) \\ 0, (S_1: \mathrm{OFF}, S_2: \mathrm{ON}) \end{cases} \tag{4}$$

$$S_B = \begin{cases} 1, (S_3: \mathrm{ON},\ S_4: \mathrm{OFF}) \\ 0, (S_3: \mathrm{OFF}, S_4: \mathrm{ON}) \end{cases} \tag{5}$$

$$S_C = \begin{cases} 1, (S_5: \mathrm{ON},\ S_6: \mathrm{OFF}) \\ 0, (S_5: \mathrm{OFF}, S_6: \mathrm{ON}) \end{cases} \tag{6}$$

Referring to (4)-(6), the AC side voltage of SAPF $\boldsymbol{v}$ can be expressed with the vector of switching function $\boldsymbol{S}$

$$\boldsymbol{v} = \boldsymbol{S}u_{dc} \tag{7}$$

It means that $\boldsymbol{v}$ is indirectly restricted by DC-link voltage u_{dc} and switching function vector $\boldsymbol{S}$.

B. IMPACT OF DC-LINK VOLTAGE ON SWITCHING NOISE

This section illustrates the relationship between DC-link voltage and switching noise. To ease analysis, only one SAPF phase is considered. Fig.2 shows an equivalent circuit of one SAPF phase and illustrates its different switching states. Referring to Fig. 2, regions of the circuit that experience current flow are highlighted in green.

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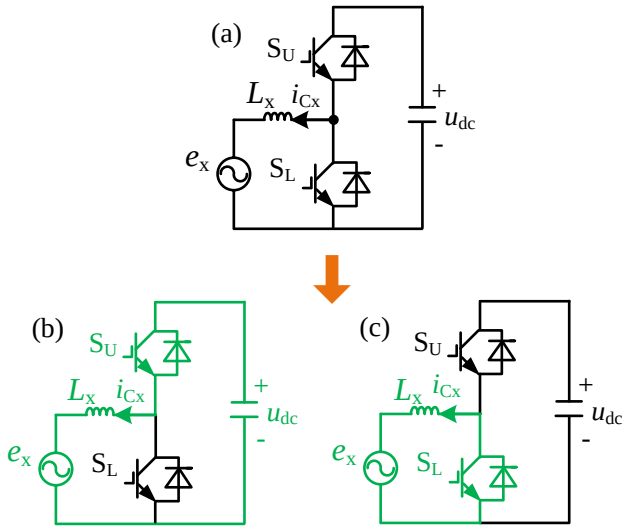

FIGURE 2. **Circuit of SAPF phase during different switching states. (a) equivalent circuit, (b) upper IGBT: switched ON, (c) Lower IGBT: switched ON.**

In convert models, output current is generally approximated as a constant in each switching window. Output current takes the form of a triangular wave in practice. Fig.2(b) and Fig.2(c) illustrates the current flowing through the circuit when the upper IGBT or lower IGBT is ON respectively. Meanwhile, the rising slope of output current is $(u_{dc}\text{-}e_x)/L_x$, and the falling slope is $-e_x/L_x$. So if L_x and e_x are given, the falling slop is constant, while the rising slope increases with u_{dc}. There are a series of potential current waves in each switching window as the u_{dc} changes. Referring to Fig.3, i^* is reference current. It is in Fig.3 that i_{ot} and i_{pt} reach the reference current, while i_{ut} is unsuccessful due to insufficient DC-link voltage.

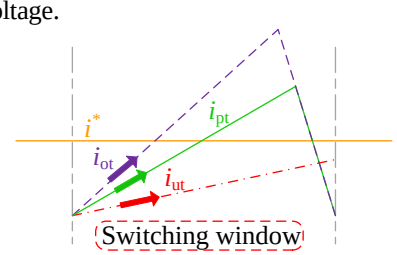

FIGURE 3. **Potential current in each switching window.**

Although the rising slope of output current means a larger output range, the ripple in current increases. Referring to Fig.3, i_{pt} is the optimal current because its amplitude of fluctuation is smaller than that of i_{ot}. That is why the fixed DC-link voltage, which depends on the rated output power, is excessive and causes higher switching noise during low load conditions. Adaptively changing DC-side voltage with load can effectively reduce the switching noise.

The optimization of performance can be achieved through adjusting DC-link voltage. The minimum DC-link voltage required is equal to the maximum modulus of AC-side voltage vector to be synthesized. Thus, the reference DC-link voltage is derived from (7) as

$$u_{dcref} = \lambda \cdot V_{max} \tag{8}$$

where V_{max} is the peak modulus of the AC-side voltage vector, and λ is the impact factor of the DC-link voltage utilization, also known as the reciprocal of voltage utilization.

III. The PROPOSED ADAPTIVE DC-LINK VOLTAGE CONTROL

The proposed adaptive DC-link voltage control employs the calculation of optimal DC-link voltage, proportion voltage regulation, model predictive current control and $i_p i_q$ harmonic detection. Proportion voltage regulation and $i_p i_q$ harmonic detection were both implemented using traditional method. Hence, this section mainly introduces the calculation of optimal DC-link voltage and model predictive current control.

A. MODEL PREDICTIVE CURRENT CONTROL

Model predictive control is chosen to keep DC-link voltage at relatively low levels because of it is a good auxiliary for the high efficiency of DC-link voltage utilization.

The MPC depends on an accurate model of the controlled object. The vector of compensation current in the continuous-time model (3) can be approximately transferred into a discrete-time expression using the forward Euler approximation with sampling period T_s,as seen in (9)

$$\boldsymbol{i}_C(k) = \frac{1}{L}\left[L\boldsymbol{i}_C(k-1) + T_s\boldsymbol{v}(k) - T_s\boldsymbol{e}(k)\right] \tag{9}$$

where $\boldsymbol{x}(k)$ is the instantaneous value of vector $\boldsymbol{x}$ at kT_s.

The one–step predictive current vector in $\alpha\beta$ frame is expressed as

$$\boldsymbol{i}_C^p(k+1) = \frac{1}{L}\left[L\boldsymbol{i}_C(k) + T_s\boldsymbol{v}(k+1) - T_s\boldsymbol{e}(k+1)\right] \tag{10}$$

Seven voltage vectors of SAPF can generate 7 potential compensation currents, which can be predicted using the compensating current dynamics in (10). Through evaluating each predictive compensating current using a predefined cost function, the optimal voltage vector was used to minimize error between one-step predictive reference and real current in each sampling interval. The cost function measuring error between the reference and the predictive compensating current in orthogonal coordinate was defined in terms of quadratic error as

$$J(k) = \mathrm{Re}^2\left[\boldsymbol{i}_C^*(k+1) - \boldsymbol{i}_C^p(k+1)\right) + \mathrm{Im}^2\left[\boldsymbol{i}_C^*(k+1) - \boldsymbol{i}_C^p(k+1)\right] \tag{11}$$

where $\boldsymbol{i}_C^*(k+1)$ is the predictive reference vector obtained from the Lagrange extrapolation equation [19].

Predictive control requires complex calculations; therefore, a second order Lagrange extrapolation equation was used to predict references,

$$\boldsymbol{i}_C^*(k+1) = 3\boldsymbol{i}_C(k) - 3\boldsymbol{i}_C(k-1) + \boldsymbol{i}_C(k-2) \tag{12}$$

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B. CALCULATION OF OPTIMAL DC-LINK VOLTAGE

1) THEORETICAL MINIMUM DC-LINK VOLTAGE REQUIRED (FIRST METHOD)

Only the modulus of each harmonic amplitude was calculated in [12], [13] using an imprecise method. Based on [12], [13], a detailed analytic method for calculation optimal DC-link voltage is proposed as follows.

In order to simplify analysis, it is assumed that the harmonics of nonlinear load requiring compensation only contain the 5th negative and 7th positive sequences

$$\boldsymbol{i}_{\mathrm{C}} = \boldsymbol{i}_{5^-} + \boldsymbol{i}_{7^+} \tag{13}$$

Assuming voltage vector $\boldsymbol{e}$ is $|\boldsymbol{e}|e^{j\omega t}$, then 5th negative and 7th positive sequences are expressed as $|\boldsymbol{i}_{5^-}|e^{-j(5\omega t+\rho_5)}$ and $|\boldsymbol{i}_{7^+}|e^{j(7\omega t+\rho_7)}$ respectively, where ω is the angular frequency at which the grid voltage vector rotates, while ρ_5 and ρ_7 are the initial phases of 5th and 7th harmonic vectors with respect to the α-axis of the stationary coordinates.

So the voltage vector of the SAPF seen in Fig.1 can be synthesized in the $\alpha\beta$ frame as (14), using (3) and (13).

$$\boldsymbol{v} = |\boldsymbol{e}|e^{j\omega t} - 5j\omega L|\boldsymbol{i}_{5^-}|e^{-j(5\omega t+\rho_5)} + 7j\omega L|\boldsymbol{i}_{7^+}|e^{j(7\omega t+\rho_7)} \tag{14}$$

Multiplying (14) with synchronous rotation factor $\boldsymbol{e}^{-j\omega t}$ in dq frame, (15) was obtained.

$$\boldsymbol{v}e^{-j\omega t} = |\boldsymbol{e}| + 5\omega L|\boldsymbol{i}_{5^-}|e^{-j(6\omega t+\pi/2+\rho_5)} + 7\omega L|\boldsymbol{i}_{7^+}|e^{j(6\omega t+\pi/2+\rho_7)} \tag{15}$$

where, $\boldsymbol{e}^{-j\omega t}$ has no effect on the modulus of voltage vector $\boldsymbol{v}$.

Ignoring the smoothing effect of line reactors in the circuit of 6-pulse rectifiers, the content of the n^{th} harmonic is only $1/n$ that of the fundamental current. Assuming that fundamental current vector is $\boldsymbol{i}_1$, (15) can be expressed as

$$\boldsymbol{v}e^{-j\omega t} = |\boldsymbol{e}| + \omega L|\boldsymbol{i}_1|(e^{j(6\omega t+\pi/2+\rho_7)} + e^{-j(6\omega t+\pi/2+\rho_5)}) \tag{16}$$

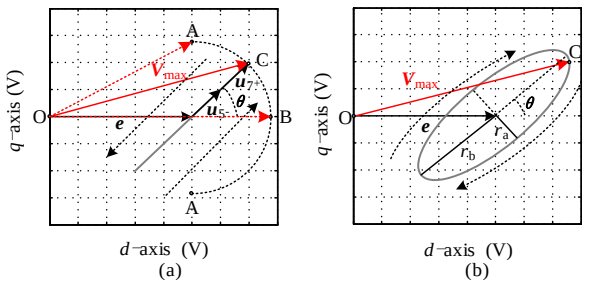

FIGURE 4. Voltage trajectories in selective compensation mode. (a) $|u_5^-|=|u_7^+|$, (b) $|u_5^-|\neq|u_7^+|$.

Fig.4 illustrates the trajectories of the AC side voltage vector in the dq frame. The synthesized trajectory in Fig.4(a) is a straight line, where $\boldsymbol{u}_5^-$ and $\boldsymbol{u}_7^+$ are the voltages on inductor with the same modulus $\omega L|\boldsymbol{i}_1|$ and angular frequency 6ω but with the opposite rotating orientation. θ is the angle between the inductor voltage and d-axis, which is related to the initial phases of the harmonic components. The peak value here can be solved with geometrical method as

$$V_{\max} = |\boldsymbol{v}_{\max}| = \mathrm{CO} = \sqrt{(|\boldsymbol{e}| + 2\omega L|\boldsymbol{i}_1|\cos\theta)^2 + (2\omega L|\boldsymbol{i}_1|\sin\theta)^2} \tag{17}$$

where θ is $(\rho_7-\rho_5)/2$.

For 6-pulse thyristor rectifiers, θ varies with the trigger angle. Correspondingly, $V_{\max}$ varies from minimum OA to maximum OB with θ changing from 0 to $\pi/2$. The margin error between OA and OB shown in Fig.4(a) is proportional to $L|\boldsymbol{i}_1|$. That means that any simplification or approximation which only considers harmonic amplitude in a high-capacity SAPF, cannot obtain accurate $V_{\max}$. In adaptive DC-link voltage control, harmonics requiring compensation have random amplitudes and initial phases. The method for obtain $V_{\max}$ must consider the harmonic phase of each order in order to maintain optimal DC- link voltage.

The 5th and 7th harmonic current are both stochastic. The trajectory of $\boldsymbol{v}$ in the dq frame takes the form of the ellipse shown in Fig.4(b). Referring to Fig.4(b), the length of the major semi-axis is $r_{\mathrm{b}} = |\boldsymbol{u}_5^-|+|\boldsymbol{u}_7^+|$, the length of the minor semi-axis is $r_{\mathrm{a}} = ||\boldsymbol{u}_5^-|-|\boldsymbol{u}_7^+||$, θ here is the angle between the major semi-axis and d-axis, and $V_{\max}$ here is the longest distance between origin O and C. The procedure for solving the coordinate of ellipse C requires a high-order equation and is difficult to solve online using DSP.

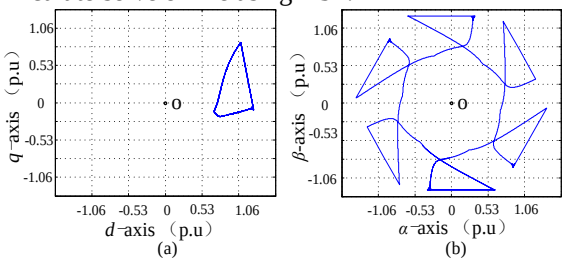

FIGURE 5. Voltage trajectories in full compensation mode. (a) voltage trajectory in the dq frame, (b) voltage trajectory in the αβ frame.

Fig.5 shows the trajectories of voltage vectors used to compensate all harmonics produced by a non-controlled rectifier with a 10 Ω resistive load on DC side and 1 mH line reactors on AC side. As the orders of the harmonics increases, voltage trajectory becomes more complex and the coordinate of C becomes more diffucult to solve.

2) THEORETICAL MINIMUM DC-LINK VOLTAGE REQUIRED (SECOND METHOD)

Using SAPF for harmonic compensation is more complex in multi-machine systems than in conventional single-unit schemes. Considering initial phases, there is a significant difference between AC-side voltage demands, even if the order of harmonics are the same. A simple passive method for observing voltage demand and the optimizing anti-disturbance is detailed as follows.

The model of the voltage demand observer is expressed by replacing current vector $\boldsymbol{i}_{\mathrm{C}}$ in (9) with harmonic reference vector $\boldsymbol{i}_{\mathrm{h}}^*$ as given by (18).

$$\boldsymbol{v}(k+1) = \frac{L}{T_{\mathrm{s}}}\left[\boldsymbol{i}_{\mathrm{h}}^*(k+1) - \boldsymbol{i}_{\mathrm{h}}^*(k)\right] + \boldsymbol{e}(k+1) \tag{18}$$

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TABLE I
RELATIONSHIP BETWEEN DC-LINK VOLTAGE AND THD$_i$

u_{dc}/V	0	700	750	800	850	900	950	1000	1050	1100	1150	1200
R_L/ Ω	THD$_i$/%											
5	22.76	10.58	9.02	7.77	5.88	4.24	2.87	1.72	1.54	1.48	1.69	1.79
10	25.22	10.85	9.4	7.41	5.07	3.39	2.76	2.21	2.48	2.72	2.66	2.63
15	26.22	11.01	9.13	5.99	3.6	3.09	2.86	3.2	3.22	3.34	3.31	3.42
20	26.8	10.81	8.54	5.4	4.14	3.58	4.01	4.01	4.04	4.06	4.42	4.35
25	27.2	11.07	7.84	5.22	4.04	4.31	4.24	4.67	4.85	4.94	4.97	5.3
30	27.49	10.94	7.39	4.83	4.99	4.78	5.24	5.25	5.29	5.75	5.92	6.02

TABLE II
RELATIONSHIP BETWEEN DC-LINK VOLTAGE AND FACTOR λ

		λ=1.4		λ=1.45		λ=1.5		λ=1.55		λ=1.6	
R_L/ Ω	THD$_i$/%	u_{dc}/V	THD$_i$/%	u_{dc}/V	THD$_i$/%	u_{dc}/V	THD$_i$/%	u_{dc}/V	THD$_i$/%	u_{dc}/V	THD$_i$/%
5	22.76	1183	1.86	1225	1.82	1268	1.82	1310	1.92	1352	1.88
10	25.22	982	2.76	1017	2.67	1052	2.73	1087	2.63	1122	2.77
15	26.22	883	3.99	914	3.41	946	3.34	977	3.51	1009	3.4
20	26.8	835	4.7	865	4.42	895	4.01	924	3.96	954	4.16
25	27.2	797	6.13	825	5.26	854	4.87	882	4.99	911	4.82
30	27.2	767	7.46	794	5.72	821	5.48	849	5.86	876	5.51

According to (18), instantaneous modulus $|\boldsymbol{v}(k+1)|$ of voltage vector $\boldsymbol{v}$ is calculated in each sample cycle. By comparing $|\boldsymbol{v}(k+1)|$ with $|\boldsymbol{v}(k)|$ and storing the larger value into register periodically, the peak AC-side voltage V_{max} was confirmed within 1/|*order*-1| of the fundamental period. Here, *order* represents the lowest order of harmonic designed to be compensated, and the sign determined by the rotating direction of the component in the $\alpha\beta$ frame. For instance, *order* is -5 for a load corresponding to Fig.5 and -1 for an imbalance load. In order to ensure applicability of the algorithm, in this paper, *order* was set to -1 when inter-harmonic were not considered. This meant V_{max} was obtained in the half-period of the fundamental component.

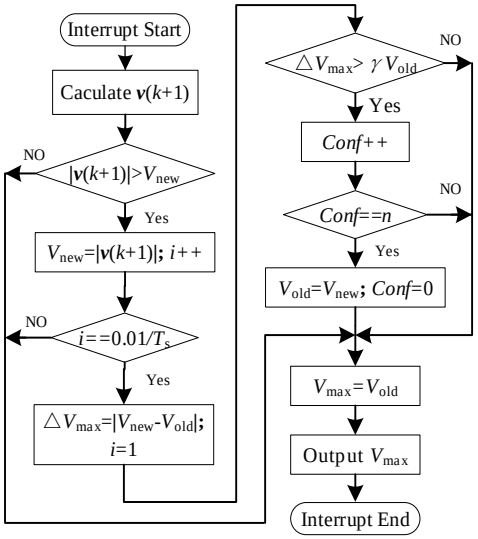

FIGURE 6. Flow diagram of the detection of peak AC-side voltage V_{max} in 50 Hz system.

The observer was extremely sensitive under non-ideal conditions due to high sampling frequency. So, PCC voltage disturbance, impedance L_s of grid transmission lines and other stochastic factors strongly interfered with peak AC-side voltage V_{max}. And active power component was introduced into reference current $\boldsymbol{i}_h^*$ because harmonic detection takes time during the dynamic process. The deviation between the extracted peak and the steady-state peak was significant. Correspondingly, the reference voltage u_{dc}^* fluctuated frequently, which increased the amount of nonessential power surge and led to unnecessary power loss.

In order to optimize anti-disturbance, the process of updating AC-side voltage V_{max} must consider threshold γ and the number of comparison n. Fig.6 shows the flow diagram for obtaining peak AC-side voltage V_{max}. Referring to Fig.6, V_{new} is the peak AC-side voltage in the latest 10 ms observation window, and V_{old} is the peak AC-side voltage output during previous observation windows. Fig.6 illustrates that peak AC-side voltage V_{max} is updated with V_{new} only when the absolute variation between V_{new} and V_{old} exceeds γV_{old} and lasts for n observation. It was concluded that γ and n should be properly increased when L_s is relatively large in order to keep u_{dc}^* steady. The selected n should be such that n/|*order*-1| fundamental period is longer than the response time of harmonic detection and the period of short-term disturbance.

When the number of confirmed comparisons is at a certain value, it becomes obvious that changes in peak voltage results from changes in load or power quality, rather than errors caused by stochastic noises like current rippers or short-term voltage disturbances.

Tables III and IV respectively show the mathematical operators required by the first and second methods of calculation theoretical minimum DC-link voltage. Referring to Table III, the operational complexity is mainly caused by fast Fourier transform (FFT), and it depends on the number of harmonics considered. The complexity of calculations increases with the number of harmonics considered. The operators (> and ==) in Table IV perform simple logical operations which do not contribute to increasing the complexity of calculations, unlike the additions and multiplications in Table III. The proposed second method in Table IV is, therefore, much simpler than the first method in Table III in terms of operation. Consequently, the second method for calculating theoretical minimum DC-link voltage was adopted DC-link voltage control in this paper.

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TABLE III
MATHEMATICAL OPERATORS IN THE FIRST METHOD OF CALCULATING THEORETICAL MINIMUM DC-LINK VOLTAGE

Calculation	Operator						
	+	×	x^2	√x	sin x	cos x	|x|
FFT(5^{th}) [16]	13566	4360					
FFT(7^{th}) [16]	13566	4360					
V_{max} (17)	2	8	2	1	1	1	2
Operations	27134	8728	2	1	1	1	2

Note: '+' addition, '×' multiplication, 'x^2' square,'√x' square root, 'sin x' sine of an angle, 'cos x' cosine of an angle '|x|' absolute.

TABLE IV
MATHEMATICAL OPERATORS IN THE SECOND METHOD OF CALCULATING THEORETICAL MINIMUM DC-LINK VOLTAGE

Calculation	Operator					
	+	-	×	/	>	==
v(k+1) (18)	3	3	5	1		
V_{max} Fig.7	2				2	2
Operations	5	3	5	1	2	2

Note: '+' addition, '-' subtraction, '×' multiplication, '/' division, '>' more,'==' equal.

3) SELECTION IMPACT FACTOR IN (8)

SAPF charging process consists of a stage of uncontrolled rectification and a stage of controlled rectification.

Uncontrolled rectification is the first stage. DC-link voltage can reach an extreme value of 2.45 times of the root mean of PCC phase voltage E_s [20]. A balance between the grid and converter is established.

After uncontrolled rectification, the next stage of SAPF charging is controlled rectification. Reference current is controlled by controllers in the outer loop with the support of an initial DC-link voltage of $2.45E_s$. Active current is pumped until DC-link voltage reaches reference voltage.

The regulation range of DC-link voltage is expressed as

$$2.45E_s \le u_{dc} \le u^*_{dc,limit} \tag{19}$$

where $2.45E_s$ is the minimum DC-link voltage required to ensure the normal operation of the current loop, and $u^*_{dc,limit}$ is the DC-link voltage limit to meet the electric strength of components.

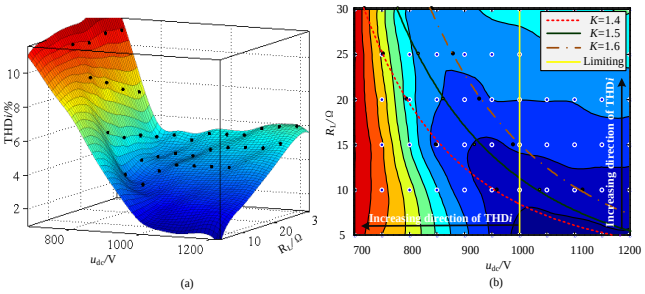

FIGURE 7. Graph of THD_i. (a) surface of THD_i, (b) THD_i contour.

Several simulations were conducted as part of selecting impact factor λ. These simulations highlighted the advantages of the proposed adaptive DC-link voltage control. Eleven different levels of DC-link voltage from 700 V to 1200 V were selected and the load resistance of the uncontrolled rectifier R_L covered 6 different levels from under-loading to overloading, in order to evaluate compensation performance. Table I shows the THD_i results of different load resistances and DC-link voltages. To be more visualized, the distribution surface of THD_i is set up by fitting the data from Table I.

Table I shows the relationship between DC-link voltages and THD_i results in different load resistances. The distribution surface of THD_i in Fig. 7(a) was obtained by fitting data from Table I.

Referring to Fig. 7(b), contour is dense when DC-link voltage is at relatively low levels, and harmonic compensation performance is significantly improved with DC-link voltage. When DC-link voltage is high, the contour gets sparse, and there is no obvious improvement in performance, meaning the system operates in a region where THD_i remains steady. DC-link voltage was limited to 1000 V in consideration of the tolerance of electric devices.

Another conclusion drawn from Table I is that low DC-link voltage causes under-tracking, which worsens compensation globally, while setting DC-link voltage at appropriate levels preserves performance. With increased load resistance, the system functions during under-tracking, which causes the fundamental component to deteriorate, leading to a slight increase in THD_i.

In summary, it is important that the system operates in the steady region of THD_i in order to achieve good compensation. DC-link voltage should be suppressed at certain low levels to reduce power loss.

Table II shows the total harmonic distortion rate of grid currents and DC-link voltages at different impact factors λ. The data in Table II was fitted to obtain the curves in Fig. 7(b). Table II denotes that DC-link voltage is low and THD_i is high, especially with light loads, where impact factor λ is 1.4. Impact factor λ of 1.5 and 1.6 ensures THD_i remains in a steady region in spite of load changes. Comparison revealed that an impact factor λ of 1.5 maintained low DC-link voltage. Therefore, 1.5 was selected as impact factor λ in the proposed adaptive DC-link voltage control.

IV. SIMULATION AND EXPERIMENT

TABLE V
PARAMETERS OF SIMULATION AND EXPERIMENT

Symbol	Quantity	Simulation	Experiment
e_s	PCC voltage (ph-ph)	380V	60V
L_s	impedance of transmission line	0.2mH	0.2mH
f	system frequency	50Hz	50Hz
C	DC-link capacitor	2200uF	3900 uF
L	filter of SAPF	4mH/2mH	4mH
f_s	sample frequency	40kHz	20kHz
γ	threshold	3%	3%
n	times of comparison in Fig.6	2	10

Simulations and experiments were conducted to verify the effectiveness of the proposed adaptive DC-link voltage control. The parameters of the simulation and experiment are

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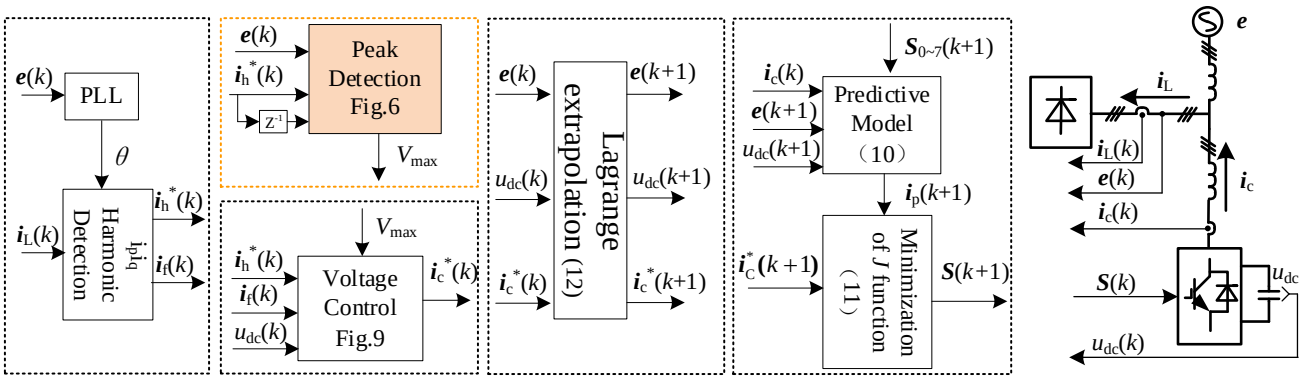

FIGURE 8. **Block diagram of proposed adaptive DC-link voltage control for SAPF.**

shown in Table V. Referring to Fig. 8, the proposed adaptive DC-link voltage control for SAPF comprised of algorithms for harmonic detection, PCC peak voltage detection, and adaptive DC-link voltage control. DC-link voltage control is detailed in Fig. 9. The focus of this paper is adaptive DC-link voltage control; therefore, the i_pi_q detection method [21] employed was not discussed in this paper.

Referring to Fig. 9, voltage deviation is coupled into fundamental current $i_f(k)$ from load current in order to achieve active power deviation. Power deviation is then adjusted with a proportional controller in order to achieve reference active current. Reference output current $i_c^*(k)$ was then obtained by superimposing the reference harmonic current $i_h^*(k)$. DC-link voltage can indirectly be controlled using predictive current loop. Considering the wide adjustable range of DC-link voltage during the adaptive process, we used a proportional controller to obtain a fast response. Some limits were imposed on related variables in order to prevent overcurrent and overvoltage in electric devices.

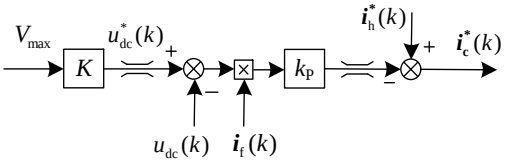

FIGURE 9. **Loop control for DC-side voltage.**

A. VERIFICATION OF ADAPTABILITY

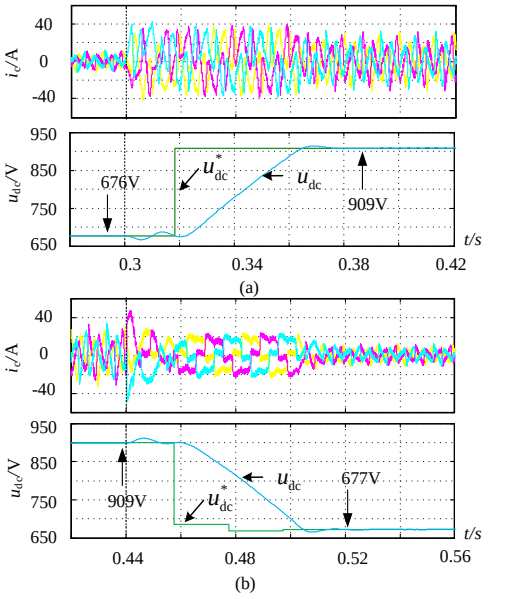

FIGURE 10. **Dynamic waveforms of DC-link voltage with current-source load. (a) dynamic waveforms of load increase, (b) dynamic waveforms of load decrease.**

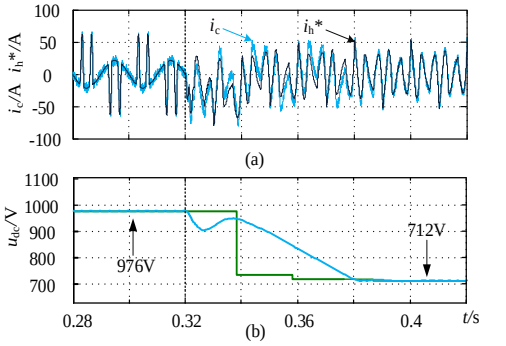

FIGURE 11. **Dynamic waveforms of different harmonic characteristics. (a) harmonic current and compensation current, (b) DC-link voltage.**

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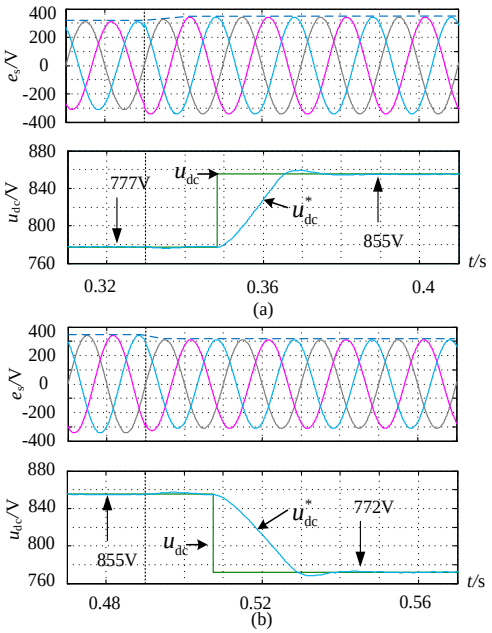

FIGURE 12. **Dynamic waveforms of DC-link voltage with voltage fluctuation in the grid. (a) grid voltage increase, (b) grid voltage decreases.**

Fig.10, Fig.11 and Fig.12 show the corresponding dynamic waveforms of the adaptive process. Fig.10 shows that the DC-link voltage self adjusts when load resistance changes from 60 Ω to 22 Ω. Fig.11 shows adaptation to different harmonic characteristics, and that SAPF line reactors change to 2 mH in order to improve the tracking of voltage harmonic source. Initially, there was a voltage harmonic source, while compensating current and DC-link voltage were 23 A RMS and 976 V, respectively. At 0.32 s, there was a current harmonic source, while compensating current remained 23 A RMS and DC-link voltage fell to 712 V. In Fig. 12, the DC-link voltage adjusts conformably when grid voltage fluctuates between 380 V and 420 V. In summary, the proposed adaptive DC-link voltage control for SAPF has the ability to adjust DC-link voltage according to the load power, harmonic characteristics, and fluctuations in grid voltage.

B. EXPERIMENTAL VERIFICATION

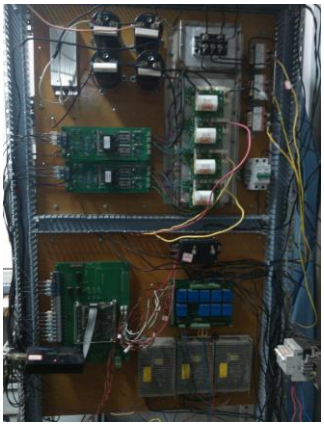

FIGURE 13. **Experimental platform.**

Referring to Fig. 13, experiments were conducted on an SAPF with small capacity in order to verify the proposed adaptive DC-link voltage control. The power devices used in these experiments were IGBT@BSM50GB120DLC from Infineon, the controller was DSP@TMS320F2812 from Texas Instruments, the measuring instrument was a FLUKE435 power quality analyzer, and the digital oscilloscope was TDS1002B-SC from Tektronix. Considering more complex conditions in actual operation, the experiments set n = 10 in Fig. 6 in order to ensure the stability of reference DC-link voltage.

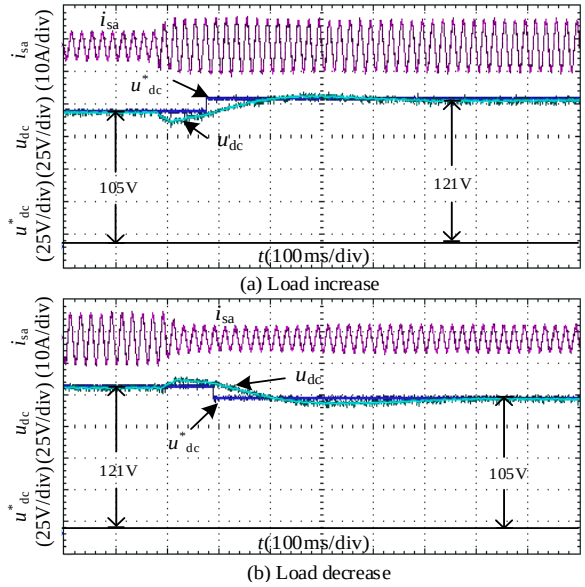

FIGURE 14. **Dynamic waveforms of DC-link voltage when R_L changed suddenly.**

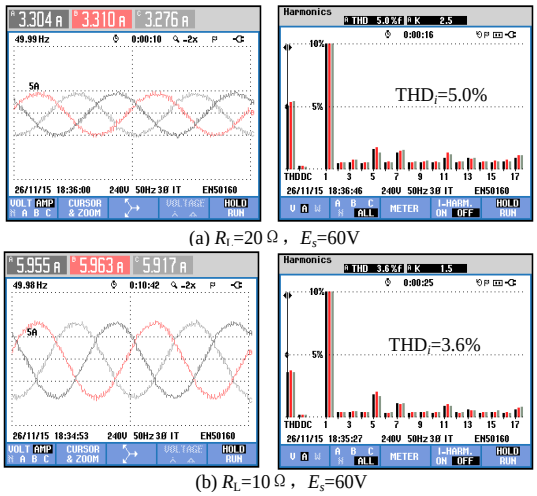

FIGURE 15. **Waveforms and spectrums of i_{sa} when load is steady.**

Figs.14 and Fig.15 show the dynamic and steady waveforms corresponding to load adaptability using the proposed adaptive DC-link voltage control. Grid voltage between phases was 60 V, and load resistance in the experiment changes between 20 Ω and 10 Ω. DC-link voltage automatically adjusted to optimal values. The distortion rate

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of the system side currents was 5.0% and 3.6%, a decrease of 1.1% and 0.4%, respectively, compared with that of the fixed 130 V DC-link voltage. The estimated switching loss reduced by 19.23% and 6.9% with respect to fixed voltage condition, according to the methods in [16] and the IGBT specification in the Infineon datasheet.

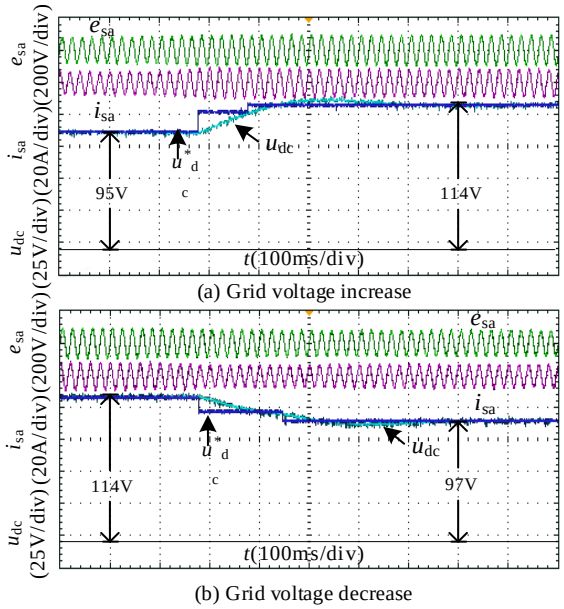


FIGURE 16. **Dynamic waveforms of DC-link voltage with fluctuating E_s.**

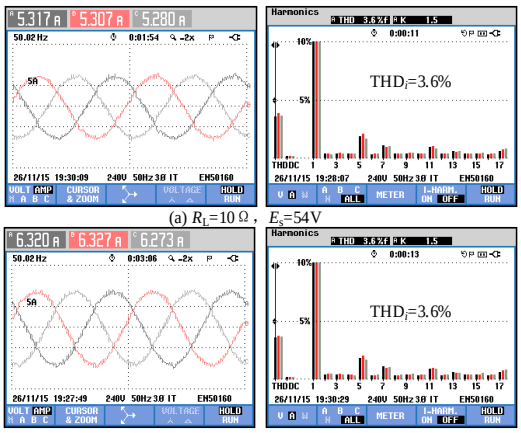


FIGURE 17. **Waveforms and spectrums of i_{sa} when grid voltage was steady.**

Figs. 16 and 17 respectively show the dynamic and steady waveforms corresponding to the grid adaptability using the proposed adaptive DC-link voltage control. Load resistance is 10 Ω and grid voltage changes between 54 V and 64 V. DC-link voltage changes to 95 V and 114 V. The distortion rate of system side current was 3.6%, a decrease of 0.5% and 0.1%, respectively, compared with that of the fixed 130V DC-link voltage. Switching loss reduced by 26.9% and 12.3%.

The results of these experiments demonstrated that DC-link voltage automatically adjusts to achieve optimal compensation, verifying the feasibility and efficiency of the proposed adaptive DC-link voltage control for SAPF.

V. CONSLUSIONS

This paper proposed a novel adaptive DC-link voltage control for SAPF in a three-phase three-wire power system. The feasibility and accuracy of existing peak detection methods were discussed and the effects of different harmonic characteristics on DC-link voltage were analyzed. The derived observation model for passive DC-link voltage considered both grid voltage and harmonics, and it was optimized to enhance anti-disturbance. Finally, simulations and experiments were conducted with the proposed adaptive DC-link voltage control to validate that the following.

1) MPC is efficient in tracking harmonic current in SAPFs.

2) The proposed adaptive DC-link voltage control is able to automatically adjust DC-link voltage according to load and harmonic current. Compensation improves significantly, and DC-link voltage increases with load. When load is low, DC-link voltage is suppressed at an optimal level, which optimizes power loss and THD$_i$.

3) The proposed adaptive DC-link voltage control is also able to tune DC-link voltage according to voltage fluctuations in the power grid.

4) The proposed adaptive DC-link voltage control does not depend on selective harmonic detection.

In summary, the proposed adaptive DC-link voltage control is feasible, simple, and effective. It can be applied to all kinds of active compensators with similar principles.

REFERENCES

[1] W. Feng, K. Sun, Y. Guan, J. M. Guerrero and X. Xiao, "PCC voltage power quality restoring strategy based on the droop controlled grid-connecting microgrid," in *JOE*, vol. 2017, no. 13, pp. 1399-1403, 2017.

[2] J. Zeng et al., "Analysis and hardware implementation of virtual resistance based PV inverters for harmonics suppression," in *IET Gener. Transm. Distrib.*, vol. 13, no. 20, pp. 4592-4603, 22 10 2019

[3] J. S. Subjak and J. S. McQuilkin, "Harmonics-causes, effects, measurements, and analysis: an update," in *IEEE Trans. Ind. Appl.*, vol. 26, no. 6, pp. 1034-1042, Nov.-Dec. 1990.

[4] X. Sun *et al.*, "Study of a Novel Equivalent Model and a Long-Feeder Simulator-Based Active Power Filter in a Closed-Loop Distribution Feeder," in *IEEE Trans. on Ind. Electron.*, vol. 63, no. 5, pp. 2702-2712, May 2016

[5] N. Xie, Q. Xu, J. Zeng, X. Liu, W. Zhang and C. Zhang, "Noval hybrid control method for APF based on PI and FRC," in *The JOE*, vol. 2019, no. 16, pp. 3002-3006, 3 2019.

[6] K. Tan, F. Lin and J. Chen, "DC-Link Voltage Regulation Using RPFNN-AMF for Three-Phase Active Power Filter," in *IEEE Access*, vol. 6, pp. 37454-37463, 2018.

[7] T. Mannen and H. Fujita, "A DC Capacitor Voltage Control Method for Active Power Filters Using Modified Reference Including the Theoretically Derived Voltage Ripple," in *IEEE Trans. Ind. Appl.*, vol. 52, no. 5, pp. 4179-4187, Sept.-Oct. 2016.

[8] Wong, M.-C., Tang, J., Han, Y.-D.: 'Cylindrical coordinate control of three-dimensional PWM technique in three-phase four-wired trilevel inverter', *IEEE Trans. Power Electron.*, 2003, 18, pp. 208–220

[9] H. Vahedi, A. A. Shojaei, L. Dessaint and K. Al-Haddad, "Reduced DC-Link Voltage Active Power Filter Using Modified PUC5 Converter," in *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 943-947, Feb. 2018.

[10] S. Rahmani, A. Hamadi, K. Al-Haddad and L. A. Dessaint, "A Combination of Shunt Hybrid Power Filter and Thyristor-Controlled Reactor for Power Quality," in *IEEE Trans. Ind. Electron.*, vol. 61, no. 5, pp. 2152-2164, May 2014

[11] L. Asiminoaei, P. Rodriguez, F. Blaabjerg and M. Malinowski, "Reduction of Switching Losses in Active Power Filters With a New Generalized Discontinuous-PWM Strategy," *IEEE Trans. Power. Electron.*, vol. 55, no. 1, pp. 467-471, Jan. 2008.

[12] C. Lam, M. Wong, W.-H. Choi, X.-X. Cui, H.-M. Mei, and J.-Z. Liu, "Design and performance of an adaptive low-dc-voltage-controlled LC-hybrid active power filter with a neutral inductor in three-phase four-wire power systems," IEEE Trans. Ind. Electron., vol. 61, no. 6, pp. 2635-2647, Jun. 2014.

[13] C. Lam, M. Wong, N. Dai, W. Choi, X. Cui and C. Chung, "Switching-loss reduction technique in active power filters without auxiliary circuits," in *IET Power Electron.*, vol. 9, no. 4, pp. 728-742, 30 3 2016.

[14] Xie, B. , et al. "Optimization control of DC link voltage for shunt activepowerfilter." *Proceedings of the CSEE*, vol. 31, no. 9, pp. 23-29, 2011.

[15] Subhas Chandra Das, G. Narayanan, Arvind Tiwari, "Experimental study on the dependence of IGBT switching energy loss on DC link voltage," in *IEEE Int. Conf. Power Electronics, Drives and Energy Systems.* Mumbai, 2014, pp. 1-5.

[16] C. Lam, L. Wang, S. Ho and M. Wong, "Adaptive Thyristor-Controlled LC-Hybrid Active Power Filter for Reactive Power and Current Harmonics Compensation With Switching Loss Reduction," in *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7577-7590, Oct. 2017.

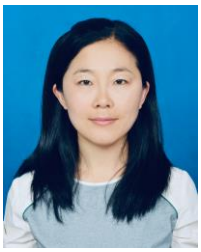
[17] J. Rodriguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortes, and U. Ammann, "Predictive Current Control of a Voltage Source Inverter," *IEEE. Trans. Ind. Electron*, vol. 54, no. 1, pp. 495-503, 2007

[18] S. Khadem, M. Basu, and M. Conlon, "Harmonic power compensation capacity of shunt active power filter and its relationship with design parameters," *IET Power Electron*., vol. 7, no. 2, pp. 418–430, Feb. 2014.

[19] Rodriguez J, Cortes P. "Prediction of Future References," in Predictive Control of Power Converters and Electrical Drives. Wiley-IEEE Press, 2012, ch. 12, sec. 4, pp. 181-188.

[20] R. W. Erickson, D. Maksimovic, "Line-commutated Rectifiers," in *Fundamentals of power electronics*. New York, America: Kluwer Academic Publishers, 2004, pp.615-617.

[21] D. Kucherenko and P. Safronov, "A comparison of time domain harmonic detection methods for compensating currents of shunt active power filter," 2014 IEEE International Conference on Intelligent Energy and Power Systems (IEPS), Kiev, 2014, pp. 40-45, doi: 10.1109/IEPS.2014.6874198.



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