ADAPTIVE PATTERNING FOR PANELIZED PACKAGING

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ABSTRACT

Fan-Out Wafer-Level Packaging (FOWLP) or fan-out technology has held promise for a number of years; primarily as a means of packaging semiconductor devices with interconnect densities exceeding the capabilities of standard Wafer Level Chip Scale Packaging (WLCSP). With FOWLP technology, die are embedded in a molded panel, and I/Os are then redistributed over the larger effective surface area using conventional WLCSP techniques. The packages are then singulated and attached directly to a printed circuit board (PCB) or low-cost substrate. This technology provides one of the smallest and lightest possible package form factors; enables more I/Os for a given pitch with excellent electrical properties; and eliminates the need for custom substrates used in flip chip or wirebond Ball Grid Array (BGA) packages. Despite its promise, widespread adoption of FOWLP packaging has been limited largely by cost and yield issues. The requirement for high die placement accuracy when forming the molded panel restricts throughput at the die pick-and-place operation, leading to high process costs. Die drift, or movement during panel molding, limits via and RDL design rules and ultimately can result in yield loss when the drift is excessive. Managing or overcoming die offset is one of the keys to making FOWLP competitive with other package formats.

This paper describes an approach to FOWLP that allows die offset to increase by an order of magnitude compared with conventional methods. Using a novel Adaptive Patterning* technology, real-time designs are created for each package within each panel during the manufacturing process. After panelization, the position of each die within each molded panel is precisely measured. Information is fed into a proprietary auto-routing design tool on a per panel basis. The resulting pattern layers are then issued to a lithography system which dynamically implements the unique design on a per panel basis. Dynamic layers include various design features such as vias or redistribution layers (RDL). The ability of adaptive patterning to correct for deviations in die location can result in both improved yield and higher panelization throughput, thereby enabling the industry to finally realize the cost, flexibility, and form factor benefits of FOWLP. In the paper, adaptive patterning examples will be presented and the benefits and limitations of the technology will be discussed.

Key words: adaptive patterning, fan-out wafer-level packaging (FOWLP), panelized packaging, WLP

INTRODUCTION

The handheld consumer electronics space, where portability and increasing functionality are strong drivers, continues to motivate the transition to packaging approaches that provide small size, high performance, and low cost. Wafer Level Chip Scale Packaging (WLCSP), which offers the smallest packaging form factor, has often been a preferred option for addressing the handheld market. In WLCSP, chip I/Os are generally fanned-in across the die surface using polymer and redistribution line (RDL) buildup layers to produce an area array, and large solder bumps are formed at the terminals by ball drop or plating. These additive processes allow the chip to be attached directly to a PCB with high reliability. However, two progressions in front-end chip manufacturing offer challenges to packaging in a WLCSP format: (1) die shrink, enabled by advancing semiconductor technology nodes, makes it increasingly difficult to fit all of the large solder ball I/Os on the die surface; and (2) increasing chip functionality produces a need for more I/Os, also making WLCSP packaging more difficult. One approach to extending WLCSP is to shrink the size of the I/Os or solder bumps on the chip surface so that more can fit within the chip area. However, this approach is generally limited by a lack of assembly infrastructure and higher assembly costs for dealing with the smaller or tighter pitch I/Os. [1]

Fan-out, or FOWLP has been offered for a number of years as an alternative for addressing constraints to WLCSP [2,3]. In this technology, chips are singulated

and then embedded in a panel. A common method for forming this panel is to place the chips face-down on a carrier at a desired pitch and then mold over them using compression or print molding. The molded panel is subsequently separated from the carrier. The panel is often formed in the shape of a wafer, so that standard wafer processing techniques can be used to create buildup layers on the panel surface. The extra panel surface around the chip allows I/Os to be both fanned in over the chip and fanned out across the mold compound, thus accommodating a larger number of I/Os. After buildup layer processing and solder ball attachment, the packages undergo backgrinding, laser marking, and singulation, just like WLCSPs. The resulting package is often just slightly larger than the chip and just large enough to accommodate the I/Os. Like WLCSPs, the package is ready to be mounted directly to a PCB.

The potential benefits of FOWLP are numerous. This technology provides the smallest and lightest possible form factor for packaging small, high I/O chips that cannot be packaged as WLCSPs. As with WLCSPs, the device-to-board connections through thick copper routing layers and large solder balls offer excellent electrical properties and performance. When hitting acceptable cost targets, FOWLP can potentially displace other forms of packaging, such as flip chip or wirebond BGAs. In those cases, it generally brings a size advantage and eliminates the need for custom substrates, significantly simplifying the supply chain. Finally, FOWLP enables the connection of two or more chips in the fan-out routing layer, facilitating multichip and system-in-package (SIP) applications [4-7].

Cost, yield and reliability issues have effectively limited the widespread adoption of FOWLP despite its promise. Placing singulated chips on the carrier to form the molded panel requires high placement accuracy. Any misplacements can lead to pattern overlay difficulties in the buildup process on the reconstituted panel. The requirement for high placement accuracy restricts throughput at the pick-and-place operation, leading to high process costs. During the molding operation and mold cure, die drift or movement can occur. This die drift can further complicate pattern overlay matching in the buildup process on the panel and can result in yield loss when the drift is excessive. In addition to die offset issues, several other challenges must be addressed for successful FOWLP packaging. The molded panels tend to warp during the buildup process; limiting or minimizing this warpage is important to enabling the use of standard wafer processing equipment. A low-cure polymer is required for the buildup layers over the mold compound. Identifying a low-cure polymer with good mechanical properties is important to ensuring package reliability. Finally, the coefficient of thermal expansion (CTE) mismatch between the mold compound and the silicon can lead to reliability issues and must be carefully managed.

Addressing or overcoming die offset and resulting overlay issues is one of the keys to making FOWLP competitive with other package formats. This paper discusses a novel approach called Adaptive Patterning, which allows die offset to increase by an order of magnitude compared with conventional methods. The ability of adaptive patterning to correct for deviations in die location can result in both improved yield and higher panelization throughput, thereby enabling cost-effective FOWLP packaging.

BACKGROUND

To illustrate the challenges in die position control, bond pads at a 45µm pitch, representative of an advanced technology node, are shown in Fig.1. A 20µm via is shown centered in the bond pad opening (BPO), representing the first layer in the fan-out buildup. The bond pad is assumed to be 40µm, with a BPO of 38µm. At these dimensions, a die shift of no more than 9µm in X and 9µm in Y can be tolerated before the via is no longer making full contact to the bond pad, as shown in Fig. 2.

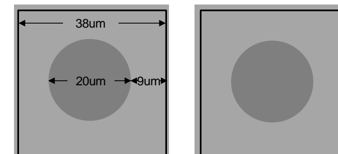

Fig. 1. Illustration of perfect die placement for an advanced technology node: 20µm via centered in bond pad openings (BPO) of 38µm on a 45µm pitch.

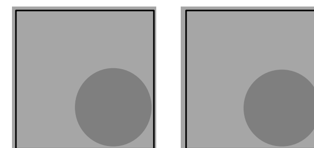

Fig. 2. Die shift by -9µm in X and 9µm in Y: 20µm via just makes full contact with BPO

Die rotation errors also present a challenge, as is illustrated in Fig. 3. For a 2mm x 2mm die, rotation placement errors as small as 0.5 degrees can result in a 9mm offset in the die corners, essentially using up the maximum 9mm shift budget of the previous example. As

shown in Fig. 3, the situation gets significantly worse with larger die sizes.

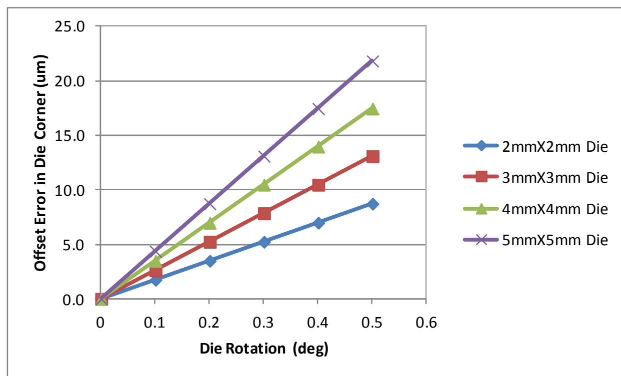

Fig. 3. Contribution of die rotation error to offset error in die corner vs. die rotation placement errors.

This demands excellent die placement and rotation control in the pick-and-place operation used to form the panel. Generally, die placement accuracy of < 10µm and rotational accuracy of < 0.1deg are required. Thus, relatively slow speeds must be utilized at the pick-and-place operation, adding significantly to the overall cost of FOWLP packages.

Die location can be further adversely affected by the panel molding operation. Die drift or shifts in position are commonly encountered during panel molding. Expected shifts can be modeled and compensated for in the pitch used at die placement. However, random shifts can result in yield loss, when the die placement error plus the random shift error exceeds the maximum shift budget for successful overlay of the buildup layers.

One strategy for dealing with die mislocation is to utilize design rules that accommodate substantial shifts and still result in yielding parts. An example would be limiting FOWLP to devices with large bond pad pitch and bond pad openings, so that the via and RDL layers in the buildup have a good chance of making contact to the BPOs. This approach, however, severely limits the number and types of chips to which FOWLP can be applied.

An alternative approach, possibly utilizing stepper technology, is to use local alignment schemes to better align the buildup layers to the die pads [8]. This has been demonstrated to result in improved alignment to mislocated die, and thus improved overall yield. However, this approach still requires a high degree of die placement and die drift control. In the extreme case, steppers can be used to perform die-by-die alignment but with a significant throughput penalty, making this approach impractical for a production environment.

ADAPTIVE PATTERNING METHOD

A new manufacturing method called adaptive patterning has been developed to correct for die shifts inherent in any chips-first, panelized packaging process. The first application of this technique is FOWLP, but it can also be applied to embedded die in substrate or other chips-first processes. The adaptive patterning method draws from techniques used in traditional wirebond packaging. In standard wirebond package assembly processes, die are placed using a high-speed die placement machine and rigidly attached to a package substrate, typically a strip containing an array of units. Subsequently, a wire bonder inspects the strip to measure the actual location of the die and dynamically adapts the wirebond program for each individual chip, allowing the wire bonder to accurately connect the bond pads on the chip to the corresponding bond fingers on the substrate or leadframe. This process of dynamically adapting the chip-to-package interconnect pattern has previously not been technically feasible and economically viable for fan-out or embedded die processes wherein the die is placed prior to forming the routing layers on the package.

The adaptive patterning process developed for FOWLP works by dynamically adjusting a portion of the interconnect structure to accurately connect to the bond pads or other structures on each individual die in the molded panel. The process is summarized in Fig. 4. First the die are thinned and singulated from the native wafer. Die are placed onto a temporary carrier and a compression molding process is used to encapsulate the die, forming a panel. While the initial implementation uses a form factor similar to a 300mm semiconductor wafer, the method can be readily extended to larger panel formats of any shape. Next, an optical scanner inspects features on each die to determine actual position and rotation of every die on the panel with respect to a panel frame of reference. Using the actual die position data for each die on the panel, a proprietary design tool adjusts the fan-out unit design for each package on the panel so that the first via layer and RDL pattern are properly aligned to bond pad features on the die. The individual package designs are combined to form a drawing of the full panel for each of the layers that need to be adjusted, typically including the first via layer on the panel and the first RDL layer. The design files for each panel are imported to a lithography machine, which uses the design data to

dynamically apply a custom, adaptive pattern to each panel.

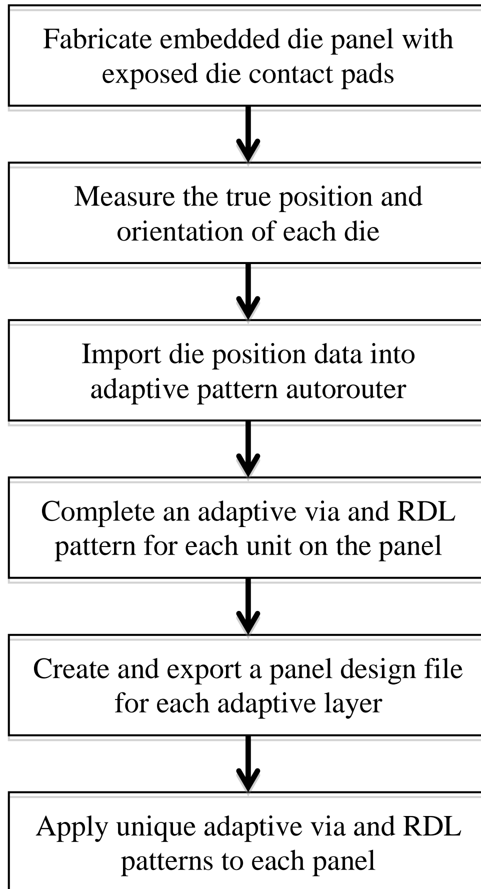

Fig. 4. Adaptive Patterning flow.

Multiple strategies for adapting the pattern were considered. The simplest method would be to adjust only the first dielectric via layer to the corresponding contact pads on the panel. The RDL capture pad overlying the via can be enlarged to accommodate shifts in the via position with respect to a static RDL pattern. This approach is limited to larger pad pitch applications and is therefore not extendable to advanced technology semiconductor nodes.

An alternate approach is to adjust the position of the first via layer and the entire RDL pattern for each unit in order to align to the actual position of the die on the panel. This technique eliminates the via-to-RDL capture pad offset issue described above, so it has the potential to support designs with finer pad pitch. However, for a package with a single fan-out routing layer, the overlay problem is moved to the next via layer underlying the UBM. It is not desirable to allow the position of the UBM pattern to shift with respect to the edge of the package – it must be held constant. Therefore, if the entire RDL pattern shifts with respect to the fixed UBM pattern, the shift must be accommodated either by increasing the size of the underlying capture pad on the RDL layer or by reducing the diameter of the via connecting the UBM to the RDL layer. In addition, this technique will not work for multi-chip modules wherein die will shift with respect to each other within the same unit design. This technique is therefore limited to smaller, low routing density, single chip packages.

A variation on this technique has been considered. It is possible to create a discrete number of fixed RDL patterns during the initial design process, each pattern being applicable to a subset of the possible die shifts defined by the process capability of the panelization process. In this case, the best fit design is selected for each unit on the panel, and a minor offset in x-y and theta is applied.

The ultimate flexibility could be achieved by calculating a complete custom RDL pattern for each unit on the panel. This method has the potential to address both die-to-RDL and RDL-to-UBM alignment without compromising on overlay design rules. Although we have demonstrated feasibility of this approach, there are some potential disadvantages. The algorithms required to complete a full package auto route are quite complex and less capable for reliably replicating complex patterns such as inductors and large power and ground planes.

ADAPTIVE PATTERNING USING PRESTRATUM

The most flexible and consistent adaptive patterning method is a hybrid approach, in which a portion of the first RDL remains fixed with respect to the package outline and BGA array. This fixed partial pattern, or prestratum, includes capture pads for subsequent pattern layers including dielectric vias and UBM structures. However, a small portion of the RDL layer in close proximity to the die contact pads is omitted from the prestratum pattern. After scanning the panel to measure the actual position and orientation of each unit, the design of each unit on the panel is completed to connect the prestratum pattern to the die contact pads and their corresponding dielectric vias. The adaptive region in which the RDL traces are allowed to dynamically change is typically on the order of 100μm to 200μm surrounding the contact pads on the chip.

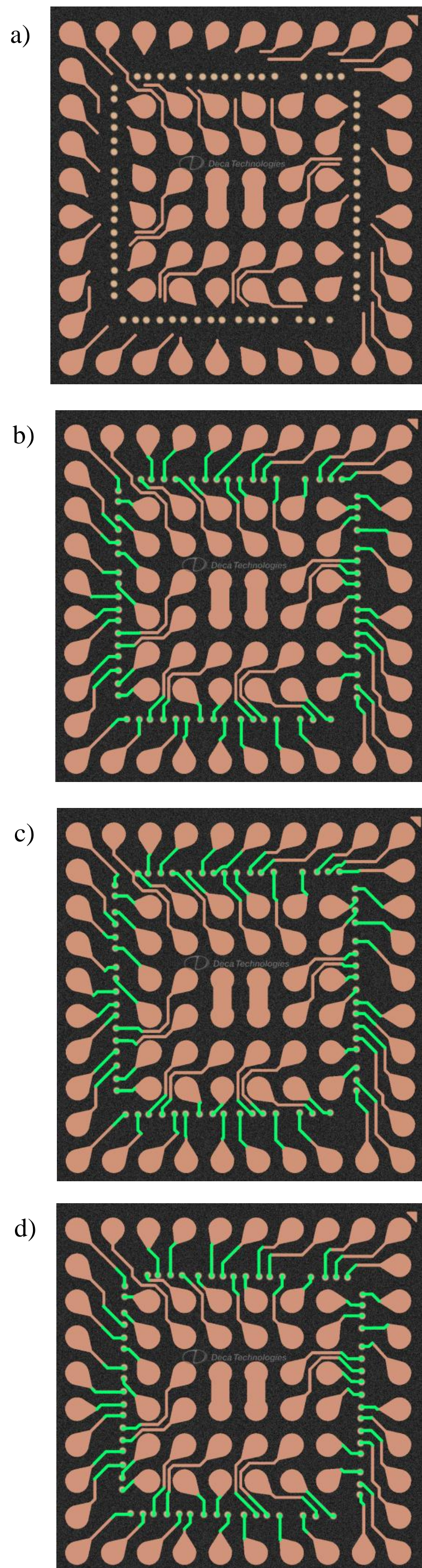

Fig. 5. Adaptive pattern design using prestratum. a) prestratum design with nominal position of die contact pads b) completed design for the nominal die position c) completed design with die shift (x, y, theta) of –50µm, -50µm, 0.5º d) completed design with die shift (x, y, theta) of 50µm, 50µm, -0.5º

Figure 5a shows an example of a fan-out RDL layer with only the prestratum pattern routed. This portion of the design is created in a traditional layout tool, such as Cadence. In order to determine the optimum prestratum design and to ensure routability of the design for all possible die shifts, a Monte Carlo analysis is performed. This is done using a proprietary design tool by applying an array of die shifts in x, y, and theta that represents the expected range of die shift resulting from the panelization process. Any design rule violations or routing errors can be characterized quickly in the design environment and corrected by adjusting the prestratum design prior to prototyping.

Figure 5b shows the completed RDL design wherein the prestratum pattern has been connected to the die bond positions on the chip. The portion of the routing is highlighted. This figure represents the nominal design, i.e. the case wherein the die shift and rotation is nil.

Figure 5c shows the completed RDL design for the case where the die is shifted from the nominal position by 50µm in x, 50µm in y and -0.5º in theta. Note that the prestatum pattern remains constant, but the autorouter changes the adaptive region of the RDL layer to ensure contact is made with the die contact pads. Figure 5d shows a completed design for the case where die shift is -50µm in x, -50µm in y and 0.5º in theta with respect to nominal. Again, the prestratum is held constant and the adaptive region of the RDL pattern is adjusted by the autorouter to make contact with the die contact pads. Monte Carlo analysis was completed to validate that routing is feasible with shifts in X and Y of up to +/-80µm and rotation up to 0.5 degrees.

Note that in all of the adaptive patterning methods described above, the first dielectric via patterns are adapted to align precisely with the contact pads on each chip in the panel.

FUNCTIONAL DEVICE EXAMPLE

The adaptive patterning method has been demonstrated on a FOWLP containing a functional mixed signal IC with die size of 2.9mm x 4.47mm. The package has a body size of 4.65mm x 4.9mm and a 92 ball BGA at 0.4mm pitch. The package contains a single fan-out RDL layer, and an in-line arrangement of die contact pads at 102µm pitch. The RDL prestratum design for the package is shown in Fig. 6. Note that the prestratum design contains a fixed ground pattern at the center of the package.

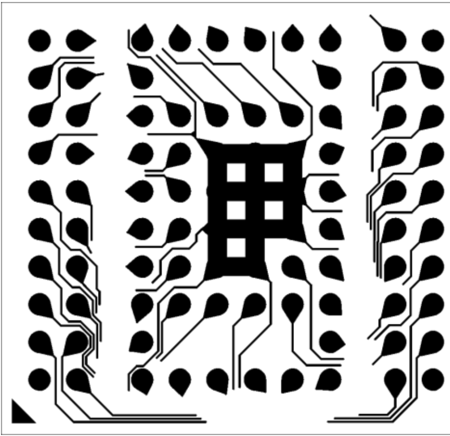

Fig. 6: RDL prestratum design containing a fixed ground plane structure.

The FOWLP was constructed on a 300mm diameter molded panel using the method described in Fig. 4. A first photopolymer layer was applied using adaptive patterning to align the via pattern to the contact pads on each unit. A unique RDL pattern was created for each unit on the panel to connect the prestratum traces shown in Fig. 6 to the associated polymer via overlying the die contact pads. An example of a finished package is shown in Fig. 7. The device shown exhibits die offset of 10µm in X, 20µm in Y, with rotation error of 0.3 deg, adding effectively 7µm of error to X and 11µm of error to Y in the corner region. Total misplacement in the corner region is ~ 17µm in X and 31µm in Y. The adaptive RDL traces effectively align to the vias resulting in an electrically functional unit.

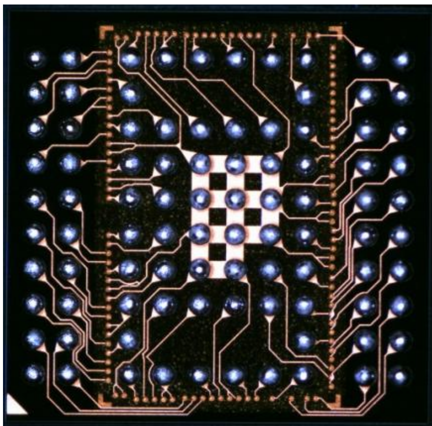

Fig. 7: Fan-out package with adaptive pattern: 2.9mm X 4.47mm die in a fully molded 4.65mmX4.9mm package; 92 balls, 0.4mm pitch.

CONCLUSIONS

Chips-first panelized packaging technologies have been in development for more than 2 decades, but have been limited by the ability of traditional patterning methods to accurately align to the die, which tend to shift within the panel. A method of adaptive patterning for FOWLP and embedded die packages has been demonstrated that solves this problem. Adaptive patterning allows die offset from the panelization process to increase by an order of magnitude compared with conventional methods. The prestratum design methodology described in this paper offers the flexibility to adapt to die position shifts in assembly while maintaining a mostly constant, deterministic routing pattern. The ability of adaptive patterning to correct for deviations in die location can result in both improved yield and higher die placement throughput, removing the key barriers to broad adoption of FOWLP and embedded die packaging.

*Adaptive Patterning™ by Deca Technologies, Inc.

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