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Adaptive Test with Test Escape Estimation for Mixed-Signal ICs

Haralampos-G. Stratigopoulos, *Member, IEEE,* and Christian Streitwieser

***Abstract*— The standard approach in industry for post-manufacturing testing of mixed-signal circuits is to measure the performances that are included in the data sheet. Despite being accurate and straightforward, this approach involves a high test time since there are numerous performances that need to be measured sequentially by switching the circuit into different test configurations. Adaptive test is a new test paradigm that still adheres to the standard approach, but it adjusts it on-the-fly to the particularities of the circuit under test so as to better control test time and to achieve robust outlier detection. In this paper, we present an adaptive test flow for mixed-signal circuits that has comprehensive user-defined parameters to span the trade-off between test time savings and fault coverage so as to select an advantageous point on the curve based on test economics. The flow also provides robust test escape risk estimation so as to add confidence to the test process. The proposed idea is demonstrated on a sizable production dataset from a large mixed-signal circuit.**

***Index Terms*— Mixed analog digital integrated circuit testing, adaptive testing, test metrics estimation, dynamic part average testing.**

I. Introduction

The standard manufacturing test approach for mixed-signal circuits consists of measuring the performances promised in the data sheet and comparing them to the specifications to make a pass or fail decision. Some performances in the data sheet are measured directly, while others require a dedicated design-for-test on-chip infrastructure to be measured. This standard test approach is straightforward to put in place and results in high test quality, typically expressed in terms of test escapes (i.e. faulty circuits that are undetected) and yield loss (i.e. functional circuits that are inadvertently discarded). However, it incurs a very high test cost since it requires sophisticated automatic test equipment (ATE) and long test times. The test cost keeps increasing as technology nodes advance, as systems become more complex and heterogeneous and deliver more functionalities, as the frequency of operation increases, etc.

In recent years, there has been an intense effort to develop alternative test approaches that can replace effectively the standard test approach. Alternative test approaches include defect-oriented test that improves test quality and can replace the standard test approach in the case of robust designs that are very well centered and never fail due to process variations [1]–[4], design-for-test and built-in self-test that aim to speedup the test by alleviating also the ATE requirements [5]–[8], and alternate test (or machine learning-based test) that aims to infer the performances implicitly based solely on low-cost measurements [9]–[13]. Such alternative test approaches have a high potential, yet they have not yet fully materialize either because they require design modifications which often finds designers very reluctant or because it is difficult to prove their equivalence to the standard test approach before a large volume of production data is collected for analysis [14], [15]. In general, any approach that is less direct and conceptually different than the easily interpretable standard approach has been hardly convincing so far.

In the standard test approach, the test process is fixed and identical for every circuit and is only occasionally revised, typically every few months, when extensive test data have been collected and confident decisions can be made as to how the test process could be improved to lower the test cost.

A recently proposed alternative test paradigm is adaptive test which still adheres to the standard test approach, but dynamically adjusts it to the particularities of each wafer or die instead of having a fixed test process [16]. In this way, significant test time savings and test quality improvements can be achieved. In the extreme, each wafer or die can be tested using a unique test process.

Adjusting the test process may involve adjusting: (a) The test limits so as to improve outlier detection and quality control; (b) The test content, i.e. given a test suite certain ineffective tests are dropped so as to save test time; and (c) The test order, i.e., assuming stop-at-first-fail and single-site testing, tests with higher fail rate are moved forward and applied first so as to save test time.

The dynamic adjustment is decided based on historical, near-time, and real-time data. Historical data include data from previously tested wafers or lots at various levels (i.e. e-tests, wafer-probe test, burn-in test, final package test, card/system test, etc.), as well as data on faulty devices that are customer returns. Near-time data include data of previously tested dies from the wafer that is currently under test or from wafers in the same lot that have been tested so far. Real-time data include data of previously performed tests on the die that is currently under test.

Despite the clear benefits of adaptive test, several challenges need to be addressed, including: (a) The development of decision-making algorithms to adjust the test process in real-time towards reducing the average test time per wafer or die. It is clear that any such real-time adjustment should either have no impact on test application time, i.e. it happens in the background in the idle time between testing two consecutive wafers or dies within the same wafer, or, if test application is delayed, then any such delay is counterbalanced and recompensed by

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an overall or average test time reduction per wafer or die; (b) The development of a test infrastructure that is flexible to simplify integration of new adaptive test techniques as they become available. The test infrastructure should support feed-forward and feed-backward real-time data communication flow interfaces between the die that is under test, the ATE, and the memory where multiple large databases are stored, and should also be capable of tracing and linking stored data in real-time. In addition, it should offer test engineers a convenient means of obtaining deep visibility into the inner workings of an adaptive test system [17]; and (c) The real-time monitoring of the probability of test escapes which may inadvertently result from performing a reduced test suite.

In this work, we present a novel adaptive test algorithm for mixed-signal circuits. We consider wafer test, but the algorithm is directly extensible for final test as well. The algorithm starts with a pre-processing step where, based on a sample set of dies that is collected across the wafer, a first guess is made as to which tests can be skipped without sacrificing appreciably the fault coverage. The rest of the dies go through the adaptive test cycle where only the kept tests are applied. During the adaptive test cycle, optionally the test process can be tuned on a die-to-die basis. In particular: (a) Periodically a die can be sampled to be subjected to a full test for quality control purposes; (b) Dynamic part average testing (DPAT) can be embedded within the adaptive test cycle so as to apply tighter test limits and screen out outliers; and (c) If a test that was skipped initially in the pre-processing step is found to fail, then it can be switched on for the rest of the dies of the wafer that will go through the adaptive test cycle with the aim to reduce prospective test escape. In the final post-processing step, the test escape probability is estimated, thus monitoring in real-time the practical equivalence of the adaptive test approach with respect to the standard test approach and reporting any alarming situations. The proposed adaptive test algorithm considers multi-site testing and fully complies to the capabilities and restrictions of an existing adaptive test infrastructure implemented in ATE [18]. The algorithm is demonstrated on a sizable production dataset from a large mixed-signal circuit. It is shown that various trade-offs between test escape and test time savings can be achieved by varying comprehensive user-defined parameters.

The rest of the paper is structured as follows. In Section II, we provide a concise overview of previous works on adaptive test. In Section III, we present the proposed adaptive test algorithm in details. In Section IV, we discuss metrics to assess the adaptive test flow. In Section V, we present the case study and the available dataset. The results are presented in Section VI and the conclusions are drawn in Section VII.

II. Previous Work on Adaptive Test

There are several adaptive test ideas that have been explored to date. Approaches for purely digital and mixed-signal circuits present some conceptual similarities, but their practical implementation is different due to the different type of underlying data that are processed for making adaptive test decisions. In particular, in the case of purely digital circuits the underlying data are binary pass/fail data, whereas in the case of mixed-signal circuits the underlying data are continuous parametric measurements. The only approaches that are virtually applicable to both purely digital and mixed-signal circuits are those related to outlier detection since for this purpose it is typically required to extract parametric measurements from the digital circuit, i.e. IDDQ tests, minimum operating voltage, etc.

Ideas for purely digital circuits include: (a) Per-die test pattern re-ordering and elimination by scoring test patterns based on their fail rate probability which is updated on a die-to-die basis [19], i.e. test patterns with high fail rate are forwarded to the beginning of the list while test patterns that appear steadily in the end of the list are dropped. The scores of test patterns can be weighted based on test time, i.e. test patterns with lower test time are given a higher score, and based also on the position of the test pattern in the order, i.e. test patterns that appear late in the order are given a higher score because they are likely to uniquely detect defects [20]; (b) Per-wafer scoring of test patterns based on a control sample of dies collected across the wafer and subsequent application of only the highest score test patterns for the rest of the dies in the wafer, i.e. test patterns that uniquely detect a faulty die in the control sample are given the highest score considering that the majority of faulty dies are detected by a large number of test patterns [21]; (c) Per-wafer measurement of the global process parameters using on-chip sensors (i.e. ring oscillators) and selection of the corresponding test pattern set to be applied according to the process condition that is identified, where test pattern sets for different process conditions (i.e. fast-fast, typical, slow-slow, etc.) are generated in an off-line step [22]; (d) Robust outlier detection by adapting the pass/fail threshold of IDDQ tests [23]–[25] or other parametric tests, such as the minimum operating voltage [25] and the clock frequency at which the delay test patterns fail [26]; (e) Periodical customization of the set of test patterns based on fault diagnosis results with the aim to minimize test escape for a given constraint on test costs, or alternatively, ensure that test escape does not exceed some predetermined threshold [27].

Ideas for mixed-signal circuits include: (a) Skipping tests on a wafer-by-wafer basis based on fail statistics of the wafer [18], [28]–[30]; (b) Skipping tests that have a high pass probability on a die-to-die basis [31]–[33]; (c) Tightening on-the-fly test limits so as to improve quality control and outlier detection [34]–[37]; (d) Changing the order of tests so as to move forward tests that have proven to achieve higher fault coverage [38]; (e) Assessing on-the-fly the confidence of low-cost machine learning-based test solutions so as to perform a standard test if confidence is low [10], [11] or stop testing if the device is deemed functional with high confidence [39]; and (f) Re-learning periodically the statistical mappings in low-cost machine learning-based tests so as to account for manufacturing process drifts [40].

III. Proposed Adaptive Test Flow

We consider multi-site testing with N_{sites} sites, where in a single touchdown N_{sites} dies are tested in parallel. Adaptive test flow and test content decisions can only be done per

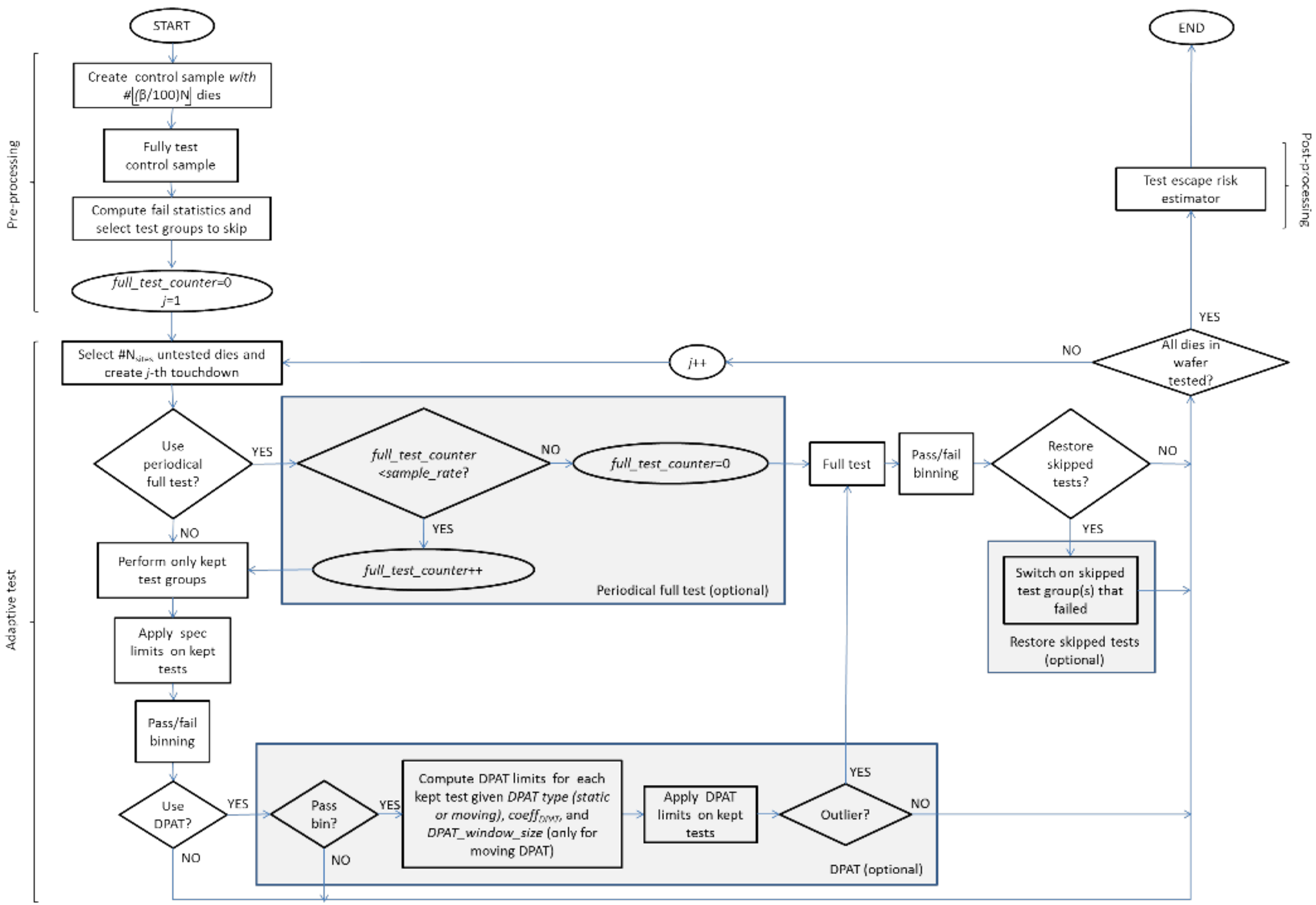


Fig. 1: Adaptive test flow.

touchdown. This means that the test program execution is identical for all dies occupying the sites within one touchdown. Statistical analysis on tests takes into account site-to-site variations due to the different tester hardware and instruments per site.

We also consider that tests are arranged into test groups. A test group refers to the group of individual tests that are performed sequentially on the same test configuration. Since the switching time to a new test configuration is considerably higher than the test times of the individual tests that will be performed on this test configuration, it would make little sense to skip individual tests after having spent already the time to set up the test configuration. Furthermore, individual tests within a test configuration are often interdependent, that is, one test is needed for computing the value of another test. For these two reasons, it makes sense to skip or execute the whole group of tests corresponding to a test configuration.

The proposed adaptive test flow per wafer is shown in Fig. 1. It consists of a pre-processing step, the adaptive test cycle itself, and a post-processing step. These steps will be described next in more details.

A. Pre-processing step

In the pre-processing step, a *control sample* containing $\beta\%$ of dies of the wafer (or approximately $\lfloor \frac{\beta}{100} N \rfloor$ dies, where N is the total number of dies contained in the wafer) is selected randomly across the wafer. The dies in the *control sample* are fully tested and, based on the test results, the fail statistics are computed, in order to make a quick decision as to which test groups can be skipped without jeopardizing considerably the fault coverage. A test group is not skipped if any of the following conditions is met: (a) it contains permanent tests that are demanded by the end customer; (b) it contains tests with negligible test time and proven fault coverage, such as continuity and leakage tests; (c) it contains tests with low C_{pk} values, where $C_{pk} = \min \left[\frac{\text{USL}-\mu}{3\sigma}, \frac{\mu-\text{LSL}}{3\sigma} \right]$, USL and LSL denote the upper and lower specification limits of the test, respectively, and μ and σ denote the mean and standard deviation of the test, respectively; (d) one or more dies in the *control sample* fail the test group, where, by definition, a test group fails when at least one test within this test group fails.

Condition (d) considers the typical scenario where stop-at-first-fail is employed. Stop-at-first-fail means that the test procedure terminates after all tests within the test group where the test that failed belongs to are executed. As a result, the values for the tests in the remaining dropped out test groups are missing from the data set. Stop-at-first-fail is not used to save test time, since in the context of multi-site testing it is unlikely that the dies on all sites will fail simultaneously, but to protect the ATE hardware. For example, after having detected a short on a high voltage pin, continuing testing is not wise as this may damage the ATE hardware. If stop-at-first-fail is not

used and full test data from all failed dies are available, then we could potentially skip some test groups that present a non-zero failure rate on the *control sample*. For example, if two test groups always fail simultaneously, then the one incurring the largest test time could be skipped.

B. Adaptive test cycle step

In the adaptive test cycle, we go through the rest of the $N - \lfloor \frac{\beta}{100} N \rfloor$ dies of the wafer that are not included in the *control sample*. N_{sites} dies are sampled each time and tested in the exact same way in a single touchdown.

In its simplest form, the adaptive test cycle consists of performing only the test groups that are kept based on the analysis in the pre-processing step and subsequently assigning pass or fail labels by comparing the recorded test values to the corresponding specifications. Several other options can be enabled during the adaptive test cycle so as to improve test quality at the expense, however, of increased test time. These options include applying periodical full test, applying DPAT, and restoring skipped tests and are discussed below. If none of the test groups is skipped, then the adaptive test cycle becomes equivalent to the standard test approach. In this case, all these options are meaningless and are automatically turned off. According to the conditions set above for skipping test groups, if there exist non-permanent test groups and finally none of such test groups is skipped, then it implies that the device under test likely has high failure probability and a low yield, thus performing adaptive test is too risky since it entails a high test escape probability.

The periodical full test option is used to generate useful data for (a) reevaluating the skipped tests and restoring those that could help minimizing test escape and for (b) estimating the test escape probability in the post-processing step. Specifically, in every *sample_rate*-th touchdown the dies undergo a full test. For this purpose, a *full_test_counter* is maintained and is reset to 0 after *sample_rate* touchdowns.

The DPAT option aims at applying tighter test limits so as to perform outlier screening [41]. In addition, it generates the same useful data as the periodical full test. DPAT is applied only to those dies in a touchdown that have been classified in the pass bin based on the kept test groups. First, the DPAT limits are computed for all kept tests. The computation is done per site so as to take into consideration site-to-site variations. The user can choose between two different DPAT approaches, namely *static* DPAT and *moving* DPAT. In the static DPAT approach, DPAT limits per site for a test are computed using the recorded values of the test on the dies in the *control sample* that occupied the corresponding site. Specifically, the DPAT limits are set to $[\tilde{\mu} \pm coeff_{DPAT}\tilde{\sigma}]$, where $\tilde{\mu} = Q_2$, $\tilde{\sigma} = \frac{Q_3 - Q_1}{1{,}35}$, and Q_1, Q_2, Q_3 are the 25-th, 50-th, and 75-th percentile, respectively, of the ordered test values [41]. In the calculation of the mean and standard deviation we consider only the main part of the distribution between the 25-th and 75-th percentile, in order to make the calculation insensitive to outliers. The parameter $coeff_{DPAT}$ defines the sensitivity to outliers. Typically, $coeff_{DPAT} = 6$ is used for robust outlier detection. Static DPAT limits need to be computed in fact only once before the adaptive test cycle starts and stay constant across all touchdowns. In the moving DPAT approach, DPAT limits are set using the above formula, but are recomputed and updated in each touchdown based on the last $DPAT_window_size$ recorded values of the test from previous touchdowns. Potentially they can provide more robust outlier detection since they take into consideration the test equipment drift per site. In both approaches, DPAT limits for a test are defined only if at least 30 test values are available, otherwise they are set equal to the specification limits [41]. Once the DPAT limits are computed, they are applied to all kept tests. If one or more of the performed tests violates its DPAT limits, then the die is declared to be an outlier. An outlier die is not summarily discarded, but it is fully tested by switching-on and performing all the skipped tests, in order to assign it a pass or fail label with confidence. Inevitably, in this case, all other dies in the same touchdown are fully tested as well even if they are not outliers since the same test program applies to all dies in a touchdown.

Finally, if for any of the fully tested dies there is a test that was skipped and is found now to fail its specification limits, then the test group where this test belongs to could be optionally switched-on for all the following touchdowns so as to reduce test escape in future test insertions. Note that restoring skipped test groups requires full test data, thus this option requires that one or both other options, e.g. periodical full test and DPAT, are enabled.

C. Post-processing step

The post-processing step starts when all dies in the wafer have been tested. It consists of estimating the test escape risk for the dies that have gone through adaptive test and they have not been fully tested, that is, their pass or fail label has been assigned by comparing the values of the kept tests to their specifications. The test escape risk estimation is used to monitor the quality of the adaptive test program and guarantee its practical equivalence to a full test program. Essentially, whenever the test escape risk becomes prohibitively high beyond a specific threshold, then it triggers an alert signal that in the extreme could prompt a re-test of the whole wafer using the standard, non-adaptive, full test program. The test escape risk estimation method is detailed in Section IV-B.

D. Tuning the adaptive test flow

The proposed adaptive test flow offers several options (i.e. periodically performing full test, applying outlier screening based on DPAT, applying static or moving DPAT limits, restoring skipped tests) and several parameters (i.e. β, $coeff_{DPAT}$, $sample_rate$, $DPAT_window_size$). Each adaptive test flow and selection of corresponding parameters results, in general, in a different trade-off between fault coverage (or, equivalently, test escape) and test time savings. Selecting the most appropriate adaptive test flow and corresponding parameter depends on test economics, the target application, and the required outgoing quality levels.

In the most conservative scenario, the adaptive test flow and corresponding parameters are decided on a lot-to-lot basis by

performing the standard test approach on one wafer in the lot. Thereafter, the selected adaptive test flow and corresponding parameters are employed for the rest of the wafers in the lot substituting the standard test approach. If the lot-to-lot variance due to equipment drift, operating procedures, etc., is insignificant, then this tuning could be done less regularly. In contrast, the *control sample* is selected on a wafer-by-wafer basis so as to capture individual wafer characteristics.

IV. Adaptive test metrics

A. Test time savings

If the wafer comprises N dies, then these N dies can be tested into

$$N_{\text{t}} = \left\lceil \frac{N}{N_{sites}} \right\rceil, \tag{1}$$

touchdowns. If the *control sample* comprises $\beta\%$ of the N dies, then the dies in the *control sample* are tested into

$$N_{\text{t-cs}} = \left\lceil \frac{\lfloor \frac{\beta}{100} N \rfloor}{N_{sites}} \right\rceil, \tag{2}$$

touchdowns. The rest $N - \lfloor \frac{\beta}{100} N \rfloor$ dies are forwarded to adaptive test and are tested into

$$N_{\text{t-ada-test}} = \left\lceil \frac{N - \lfloor \frac{\beta}{100} N \rfloor}{N_{sites}} \right\rceil, \tag{3}$$

touchdowns. During adaptive test, the number of touchdowns that are periodically sampled to subject the dies into a full test is given by

$$N_{\text{t-ps}} = \left\lfloor \frac{N_{\text{t-ada-test}}}{sample_rate} \right\rfloor. \tag{4}$$

Regarding the rest of the touchdowns where the dies undergo a reduced test and outlier screening using DPAT limits, the number of touchdowns for which a full test will be performed because one or more dies within the touchdown is found to be an outlier is given by

$$N_{\text{t-outliers}} = \sum_{\substack{i=1 \\ i \neq k \cdot sample_rate \\ k \in \mathbb{Z}^+}}^{N_{\text{t-ada-test}}} \min(1, N^{(i)}_{\text{outliers}}), \tag{5}$$

where $N^{(i)}_{\text{outliers}}$ is the number of dies that are screened out as outliers in the i-th touchdown.

Combining equations (2)-(5), during the adaptive test cycle, the number of touchdowns for which dies undergo a full test is given by

$$N_{\text{t-fulltest}} = N_{\text{t-cs}} + N_{\text{t-ps}} + N_{\text{t-outliers}}. \tag{6}$$

and the number of touchdowns for which dies undergo a reduced test is given by

$$N_{\text{t-red-test}} = \sum_{\substack{i=1 \\ i \neq k \cdot sample_rate \\ k \in \mathbb{Z}^+}}^{N_{\text{t-ada-test}}} \left(1 - \min(1, N^{(i)}_{\text{outliers}})\right). \tag{7}$$

Since tests that were previously skipped can be switched on during the adaptive test cycle based on the full test results of outliers and every $sample_rate$-th touchdown, the kept test groups may change from touchdown to touchdown. Let T denote the sum of test times of all test groups and let $T^{(i)}_{\text{kept}}$ denote the sum of test times of kept test groups for the i-th touchdown.

The test time per wafer of the standard, non-adaptive test program is given by

$$T_{\text{sta-test}} = N_{\text{t}} \cdot T. \tag{8}$$

The test time of the adaptive test program is given by

$$T_{\text{ada-test}} = N_{\text{t-fulltest}} \cdot T + \sum_{\substack{i=1 \\ i \neq k \cdot sample_rate \\ k \in \mathbb{Z}^+}}^{N_{\text{t-ada-test}}} \left(1 - \min(1, N^{(i)}_{\text{outliers}})\right) T^{(i)}_{\text{kept}}. \tag{9}$$

The test time savings per wafer can be expressed in % as

$$\Delta T = 100 \left(1 - \frac{T_{\text{ada-test}}}{T_{\text{sta-test}}}\right). \tag{10}$$

B. Test escape

A test escape is the event where a die goes through the adaptive test cycle (i.e. it is not included in the *control sample*), ends up being tested using only the kept tests (i.e. if the full periodical full test option is used, then the die is not selected for full periodical test, and if DPAT is used, then the die is not screened out as an outlier), it passes all kept tests, but fails one or more tests that were skipped in the pre-processing step.

Let $p^j_{T_E}$ denote the probability of test escape for the j-th die that is candidate for test escape. Let also the j-th die be tested with a specific kept test suite, denoted by t_j, and specific DPAT limits, denoted by ℓ_j.

The set of n dies that are fully tested is used for the computation of probability of test escape for all dies that are candidate for test escape. This set includes the dies in the *control sample*, the dies in the touchdowns that are periodically sampled to be subjected to a full test, and the dies in the touchdowns that end up being subjected to a full test because one or more dies within the touchdown are screened out as outliers based on the DPAT limits.

Let us consider the i-die in this set and assume that it is tested with the kept test suite t_j and DPAT limits ℓ_j. We define the indicator function

$$I^{ij} = \begin{cases} 1 & : & i\text{-th die is a test escape} \\ 0 & : & \text{otherwise} \end{cases}. \tag{11}$$

The indicator function I^{ij} is a random variable which follows a Bernouli distribution with mean and variance

$$\mu_j = p^j_{T_E} \tag{12}$$

$$\sigma^2_j = p^j_{T_E}(1 - p^j_{T_E}). \tag{13}$$

An estimate of the test escape probability $p^j_{T_E}$ is given by

$$\hat{p}^j_{T_E} = \frac{\sum_{i=1}^n I^{ij}}{n}. \tag{14}$$

Using the central limit theorem, for $n \to \infty$

$$\frac{\sum_{i=1}^n \left(I^{ij} - \mu_j\right)}{\sqrt{\sum_{i=1}^n \sigma_j^2}} \sim \mathcal{N}(0,1). \tag{15}$$

Equivalently, substituting (12)-(14) into (15) we have

$$\frac{\hat{p}^j_{T_E} - p^j_{T_E}}{\sqrt{p^j_{T_E}(1-p^j_{T_E})/n}} \sim \mathcal{N}(0,1). \tag{16}$$

From (16) we have

$$\Pr\{-z_{\frac{\alpha}{2}} \le \frac{\hat{p}^j_{T_E} - p^j_{T_E}}{\sqrt{p^j_{T_E}(1-p^j_{T_E})/n}} \le z_{\frac{\alpha}{2}}\} = 1-\alpha, \tag{17}$$

where $z_{\frac{\alpha}{2}}$ is the $(1-\frac{\alpha}{2})$ quantile of the standard normal distribution. Therefore, the $100\cdot(1-\alpha)\%$ confidence interval for $p^j_{T_E}$ is given by

$$\hat{p}^j_{T_E} \pm z_{\frac{\alpha}{2}}\sqrt{\frac{p^j_{T_E}(1-p^j_{T_E})}{n}}. \tag{18}$$

Replacing $p^j_{T_E}$ with $\hat{p}^j_{T_E}$ into (18) we obtain

$$\hat{p}^j_{T_E} \pm z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n}}. \tag{19}$$

To account for small n and extreme probabilities $p^j_{T_E}$, we use the Wilson interval that implements a correction factor

$$\frac{1}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}}\left[\hat{p}^j_{T_E} + \frac{z^2_{\frac{\alpha}{2}}}{2n} \pm z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n} + \frac{z^2_{\frac{\alpha}{2}}}{4n^2}}\right], \tag{20}$$

which can be rewritten as

$$\left[\hat{p}^{j'}_{T_E} \pm \frac{z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n} + \frac{z^2_{\frac{\alpha}{2}}}{4n^2}}}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}}\right], \tag{21}$$

where

$$\hat{p}^{j'}_{T_E} = \frac{\hat{p}^j_{T_E} + \frac{z^2_{\frac{\alpha}{2}}}{2n}}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}} \tag{22}$$

is the corrected estimate of test escape probability $p^j_{T_E}$. Since $p^j_{T_E} \ge 0$, the lower bound of the confidence interval is set at

$$\max\left(\hat{p}^{j'}_{T_E} - \frac{z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n} + \frac{z^2_{\frac{\alpha}{2}}}{4n^2}}}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}}, 0\right). \tag{23}$$

The absolute test escape per wafer, denoted by N_{T_E}, is defined as the number of dies per wafer that are given a pass label while they are faulty. Using (22), an estimate can be expressed as

$$\hat{N}_{T_E} = \sum_j \hat{p}^{j'}_{T_E}, \tag{24}$$

where the summation is over all dies that go through the adaptive test cycle and are only tested with a reduced test suite. Using (21) and (23), the lower and upper bounds of the $100\cdot(1-\alpha)\%$ confidence interval for N_{T_E} are given by

$$\sum_j \max\left(\hat{p}^{j'}_{T_E} - \frac{z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n} + \frac{z^2_{\frac{\alpha}{2}}}{4n^2}}}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}}, 0\right) \tag{25}$$

and

$$\sum_j \left(\hat{p}^{j'}_{T_E} + \frac{z_{\frac{\alpha}{2}}\sqrt{\frac{\hat{p}^j_{T_E}(1-\hat{p}^j_{T_E})}{n} + \frac{z^2_{\frac{\alpha}{2}}}{4n^2}}}{1+\frac{z^2_{\frac{\alpha}{2}}}{n}}\right), \tag{26}$$

respectively, where, again, the summation is over all dies that go through the adaptive test cycle and are only tested with a reduced test suite.

As test escape risk metric we can use either the absolute test escape per wafer estimate in (24) or the upper bound of the confidence interval in (26).

By definition, only faulty dies can be a test escape. Intuitively, DPAT may have tendency to screen out faulty dies and subject them to a full test. Thus, in the set that is used for the computation of test escape there are more dies candidate for test escapes compared to a random selection of dies and this may introduce some bias. The *control sample*, however, adds an opposite bias since it has zero dies candidate for test escapes. Indeed, given the conditions for skipping tests in Section III-A, the dies in the *control sample* do not fail any skipped test. Only the full periodical test option does a strictly random selection of dies.

C. Fault coverage

Let D_l denote the defect level of the wafer, defined as the total number of faulty dies contained in the wafer. The fault coverage can be expressed in % as

$$FC = 100\left(1 - \frac{N_{T_E}}{D_l}\right). \tag{27}$$

V. Case Study

Our case study is a mixed-signal application specific integrated circuit (ASIC) designed by ams AG. The ASIC is an inductive high speed off-axis motion sensor[1]. The standard test suite consists of 338 tests that are assorted into 69 different test groups each requiring a specific test configuration. As shown in Fig. 2, the number of tests per test group ranges from 1 to 40. The total test time is 7.8726s and is distributed per test group as shown in Fig. 3. The test group with the largest number of tests does not necessarily incur the largest test time. For example, test group 41 is the most populous

[1]More details regarding the ASIC may not be released due to a binding NDA.

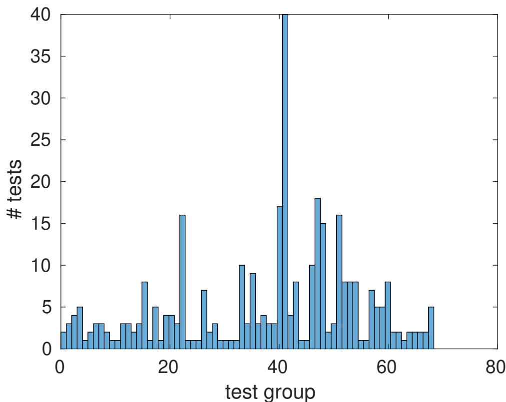


Fig. 2: Number of tests per test group.

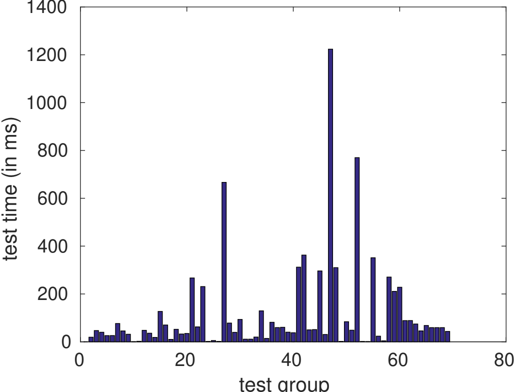


Fig. 3: Test time per test group.

test group with 40 tests incurring 312.1ms, while test group 47 is the most time-consuming test group with test time 1.233s including just 10 tests.

We have at hand a data set that contains the test results from 2 lots. Each lot contains 25 wafers and each wafer contains about 4370 dies. For the first lot, the yield per wafer varies between 80.74% and 93.75% with an average value of 92.01% and the defect level per wafer varies between 273 and 843 with an average value of 349.44. For the second lot, the yield per wafer varies between 95.47% and 96.61% with an average value of 96.10% and the defect level per wafer varies between 143 and 191 with an average value of 164.28.

The multi-site test environment allows testing concurrently $N_{sites} = 4$ dies and implements stop-at-first-fail.

VI. Experimental Results

A. Adaptive test flows study and comparisons

We will study and compare three adaptive test flow scenarios, ranging from simplest to most elaborate, namely (a) The flow "no DPAT, no periodical full test" where during the adaptive test cycle no outlier screening and no periodical full test are allowed, that is, all dies are tested with a fixed reduced test suite defined based on the fail statistics from the *control sample*. In this scenario, the parameters $coeff_{DPAT}$, $sample_rate$, and $DPAT_window_size$ are irrelevant; (b) The flow "static DPAT, periodical full test" where during the adaptive test cycle outlier screening based on static DPAT limits and periodical full test are enabled. This scenario is enabled by setting $coeff_{DPAT} = 6$ and $sample_rate = 20$, whereas the parameter $DPAT_window_size$ is irrelevant; (c) The flow "moving DPAT, periodical full test" where during the adaptive test cycle outlier screening based on moving DPAT limits and periodical full test are enabled. This scenario is enabled by setting $coeff_{DPAT} = 6$, $sample_rate = 20$, and $DPAT_window_size = 30$. Restoring skipped tests is enabled in all flows, but for the flow "no DPAT, no periodical full test" this has no effect since no full test data are collected for reevaluating and eventually switching-on skipped tests if necessary.

In this experiment, we employ the first wafer from the first lot and we study the trade-off between fault coverage (or, equivalently, test escape) and test time savings for the three aforementioned adaptive test flows by varying the *control sample* size β. For a given value of β, the resultant trade-off depends on the particular subset of dies from the wafer that are included in the *control sample*. Therefore, to report trustworthy metrics, for each value of β we perform many trials, where in each trial we randomly populate the *control sample* from the available dies of the wafer. In the end, we report minimum, maximum, and average metrics values observed across the trials.

Fig. 4 shows the minimum, maximum, and average fault coverage and test time savings observed across 50 trials as a function of β for the three aforementioned adaptive test flows. The markers correspond to the average numbers, whereas the lower and upper ends of the intervals correspond to the minimum and maximum numbers, respectively.

Fig. 5(a) plots the data in Fig. 4 from a different perspective. In particular, it shows using average values the trade-off between FC and ΔT that is achieved by each adaptive test flow scenario pointing also to the direction of change of β. In Fig. 5(b), the absolute test escape N_{T_E} is used instead of FC. The relationship between N_{T_E} and FC is given by (27) considering that for this particular wafer $D_l = 303$.

We observe that every adaptive test flow has specific capabilities regarding the trade-offs $FC - \Delta T$ and $N_{T_E} - \Delta T$ that can be achieved. This is illustrated by the vertical and horizontal lines in Figs. 5(a) and 5(b). For a given adaptive test flow, as the *control sample* size β increases, the fault coverage FC increases since the fail statistics are computed on more dies and, thereby, they become more representative of the underlying failure modes. The improvement of FC, however, is at the expense of reduced test time savings ΔT since, as the *control sample* size β increases, more dies are fully tested and also the kept test suite is likely to be larger. For a given *control sample* size β, by enabling the periodical full test and DPAT options within the adaptive test cycle, we allow dies to be fully tested during the adaptive test cycle, which increases fault coverage at the expense of deceasing test time savings. In short, enabling the options within the adaptive test cycle, or keeping the options disabled and using a large *control sample* size β, results in a high FC-low ΔT or,

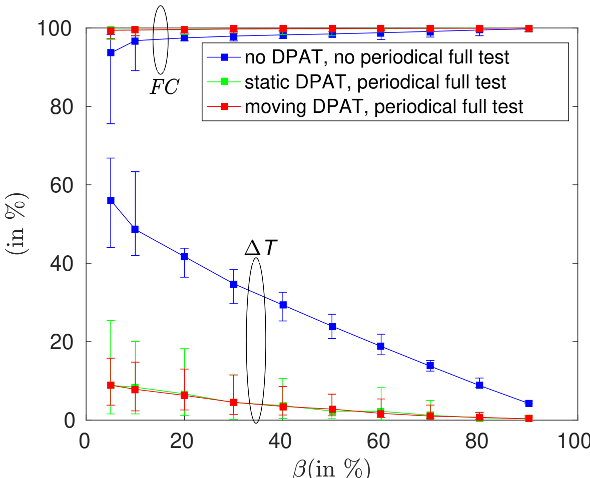
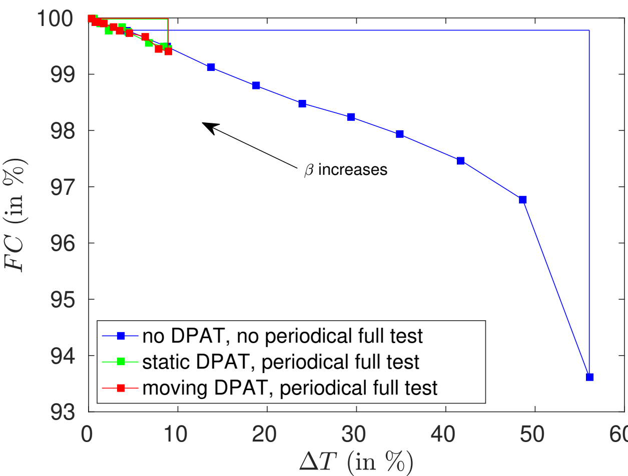
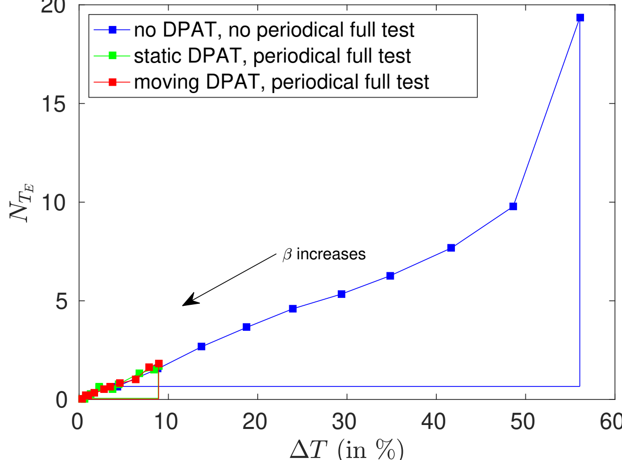


Fig. 4: Fault coverage and test savings as a function of the *control sample* size β for different adaptive test flow scenarios.



(a) Trade-off between fault coverage and test time savings achieved by different adaptive test flows.



(b) Trade-off between test escape and test time savings achieved by different adaptive test flows.

Fig. 5: Selecting adaptive test flow and relevant parameters based on test economics.

equivalently, low N_{T_E}-low ΔT trade-off. Keeping the options disabled and using a low *control sample* size β results in a low FC-high ΔT or, equivalently, high N_{T_E}-high ΔT trade-off.

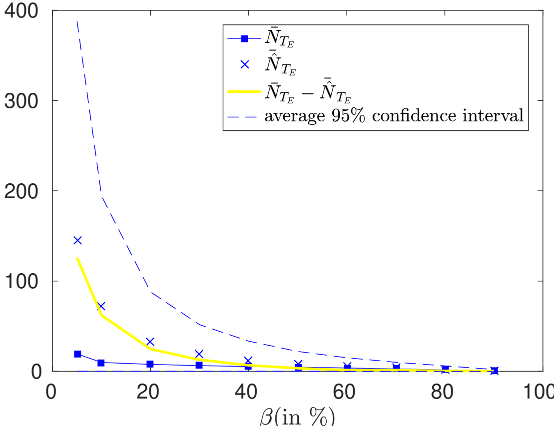
Specifically, for the simplest flow "no DPAT, no periodical full test", FC lies in the range $[93.62\%, 99.78\%]$, N_{T_E} lies in the range $[0.66, 19.34]$, and ΔT lies in the range $[4.27\%, 56.01\%]$. For the most elaborate flow "moving DPAT, periodical full test", FC lies in the range $[99.40\%, 99.99\%]$, N_{T_E} lies in the range $[0.02, 1.82]$, and ΔT lies in the range $[0.31\%, 8.91\%]$. The flow "static DPAT, periodical full test" achieves similar range of values with the flow "moving DPAT, periodical full test". The difference is that for the flow "moving DPAT, periodical full test", in general, ΔT presents a much smaller variance across the different trials for a given β, as can be observed in Fig. 4. This points to a smaller variation in the number of outliers across the different trials, that is, a more robust outlier detection, and also reveals overall a smaller dependence on the composition of the control sample. In short, comparing the flows "static DPAT, periodical full test" and "moving DPAT, periodical full test", they achieve practically the same trade-offs $FC - \Delta T$ and $N_{T_E} - \Delta T$, but it is recommended to use the flow "moving DPAT, periodical full test" since it offers test time savings with smaller variance.

For small β, many tests are expected to be skipped and this is likely to give rise to smaller fault coverage or, equivalently, higher test escape rate. Furthermore, as shown in Fig. 4, the variance of fault coverage is expected to be higher. This is due to the fact that as β decreases the defect level of the set of dies that go through adaptive test and end up being tested with a reduced test suite increases proportionally, thus increasing the upper bound of test escape across the trials. This elucidates that estimating the fault coverage or, equivalently, the test escape rate, is indispensable so as to monitor the test quality and identify alarming situations.

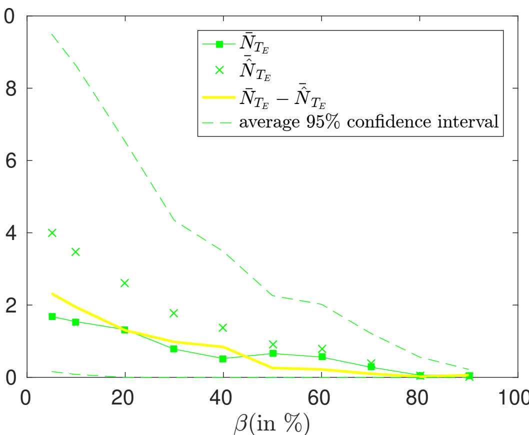
Figs. 6(a)-(c) show the average true and estimated test escape, denoted by $\bar{N}_{T_E}$ and $\hat{\bar{N}}_{T_E}$, respectively, computed across the 50 trials, as well as their difference, as a function of β for the three aforementioned adaptive test flows. Figs. 6(a)-(c) also show the average 95% confidence interval as a function of β, which is computed by averaging the lower and upper bounds of the 95% confidence interval that are obtained across the 50 trials.

For a given flow, as β increases, the number of dies that are fully tested increases and, thereby, the true test escape drops, as is also illustrated in Fig. 5(b). At the same time, as the number of dies that are fully tested increases, more data become available for estimating the test escape, resulting in more robust and accurate estimates and more confined confidence intervals. For a given value of β, the more reactive the adaptive test flow is in screening out dies for a full test, either periodically for quality control or because they are deemed to be outliers, the smaller the true test escape is and the more data are typically available for estimating it, resulting in more robust and accurate estimates and more confined confidence intervals.

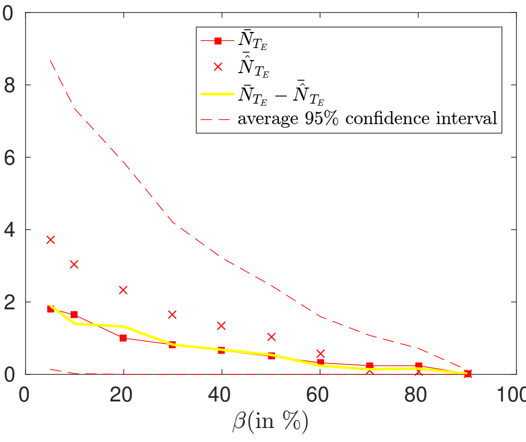
For the flow "no DPAT, no periodical full test", only the *control sample* is used for estimating the test escape since



(a) No DPAT, no periodical full test.



(b) Static DPAT limits, periodical full test.



(c) Moving DPAT limits, periodical full test.

Fig. 6: Average true and estimated test escape as a function of the *control sample* size β for different adaptive test flow scenarios showing also the average 95% confidence intervals.

there is no outlier detection or periodical quality control. By construction, all tests that fail for one or more dies contained in the *control sample* are kept and are carried out during the adaptive test cycle. In other words, in the *control sample* there is no die that passes the kept tests and fails a skipped test. Returning to (22), this means that $\hat{p}^j_{T_E} = 0$ and $\hat{p}^{j'}_{T_E} \approx \frac{z^2_{\frac{\alpha}{2}}}{2n}$,

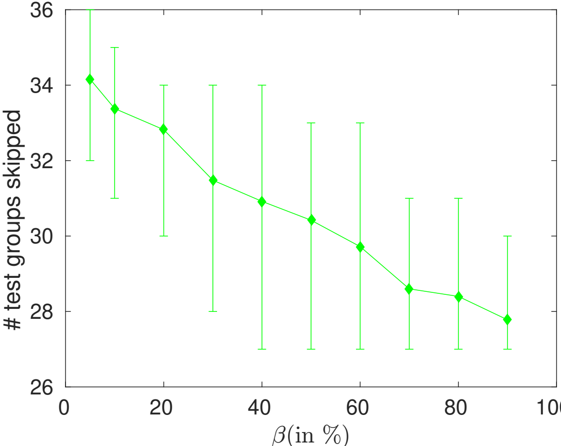


Fig. 7: Number of test groups that are skipped across the 50 trials as a function of the *control sample* size.

where $n = \lfloor \frac{\beta}{100} N \rfloor$. The 95% confidence interval becomes $\left[0, \frac{z^2_{\frac{\alpha}{2}}}{n}\right]$. Therefore, for the flow "no DPAT, no periodical full test", the test escape estimate and the width of the confidence interval simply drop inversely proportional to β, as is also illustrated in 6(a). For the other two flows "static DPAT, periodical full test" and "moving DPAT, periodical full test", in general, $\hat{p}^j_{T_E} \neq 0$ and $n > \lfloor \frac{\beta}{100} N \rfloor$.

As it can be observed, for every flow and for every value of β, the average true test escape always lies within the 95% confidence interval. For the flow "no DPAT, no periodical full test", average test escape is largely overestimated for small values of β, but estimates improve as β increases. For the other two flows "static DPAT, periodical full test" and "moving DPAT, periodical full test", the average test escape estimates are very accurate even for low values of β and the 95% confidence interval is sufficiently narrow. In particular, for the flow "static DPAT, periodical full test", the maximum estimation error is 2.32 test escapes for $\beta = 5\%$ and drops below 0.5 test escapes for $\beta = 50\%$. For the flow "moving DPAT, periodical full test", the maximum estimation error is 1.90 test escapes for $\beta = 5\%$ and drops below 1 test escape for $\beta = 30\%$. Yet, similar to the flow "no DPAT, no periodical full test", we observe that for the two flows "static DPAT, periodical full test" and "moving DPAT, periodical full test" the test escape estimates are overestimated, but only slightly compared to the flow "no DPAT, no periodical full test".

B. In-depth analysis for a specific adaptive test flow

In this experiment, we consider without loss of generality the flow "moving DPAT, periodical full test" and we perform a more in-depth analysis. Similarly to Section VI-A, we employ the first wafer from the first lot.

Fig. 7 shows the minimum, maximum, and average number of test groups that are skipped during the pre-processing step across 50 trials as a function of β. As it can observed, the average number of test groups that are skipped drops from around 34 to around 28 as β increases from 5% to 90%.

Fig. 8 shows the percentage of trials for which each test group is skipped for β=10%. As it can be observed, there are

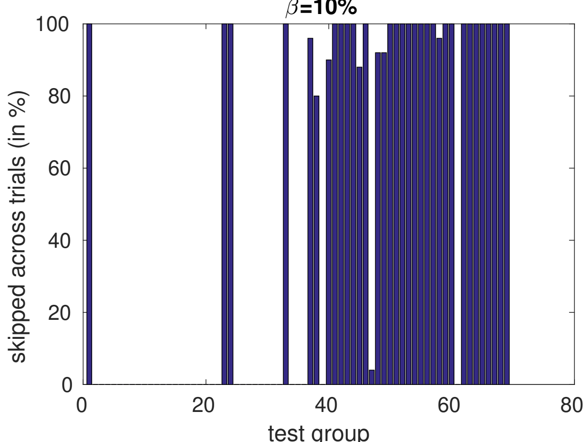


Fig. 8: Percentage of trials for which each test group is skipped.

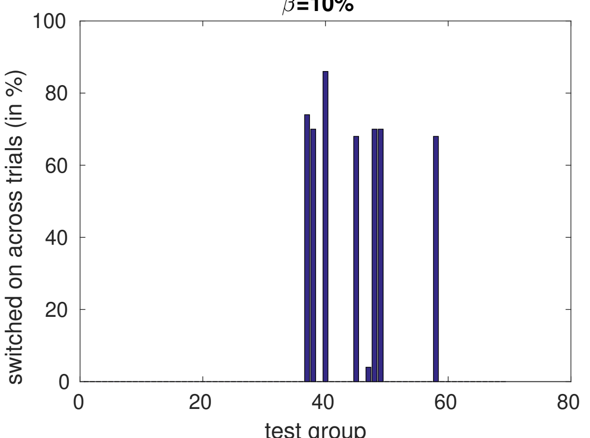


Fig. 9: Percentage of trials for which each test group is switched on.

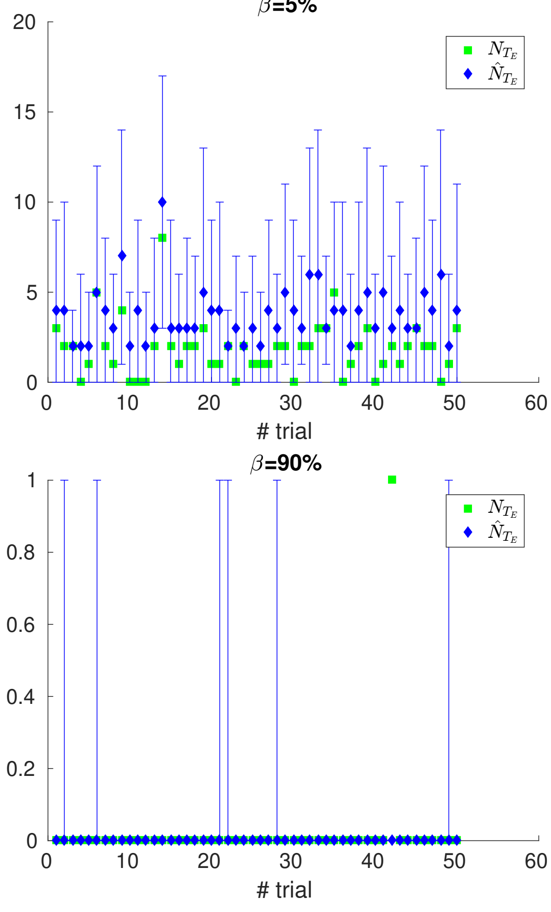


Fig. 10: True and estimated absolute test escape across the 50 trials for two "extreme" values of β, showing also the 95% confidence interval.

three categories of test groups. The two largest categories are those corresponding to test groups that are always skipped or never skipped. In total, there are 34 test groups that are never skipped and 27 test groups that are always skipped. The third smaller category contains 8 test groups that are skipped only in certain trials. Among these 8 test groups, the extreme cases are test group 47 which is skipped only 4% of the trials and test groups 37 and 58 which are skipped 96% of the trials. The height of the bars in Fig. 8 essentially point to the frequency with which a test group fails. A test group that is skipped for all 50 trials seems to never fail or, considering stop-on-first-fail, whenever it fails, another test group earlier in the test group sequence fails at the same time and is not skipped. A test group that is never skipped for any of the 50 trials is either a permanent test group or it fails very often, that is, any random *control sample* would contain a die that fails this test group.

Fig. 9 shows the percentage of trials for which each test group is switched on during the adaptive test cycle for β=10%. As it can be observed, the skipped test groups that have a non-zero probability of being switched on are the same aforementioned 8 test groups shown in Fig. 8 that are skipped only in certain trials. In other words, a test group that is skipped for all 50 trials has a zero probability of being switched on during the adaptive test cycle.

The aforementioned 8 test groups give rise to the intervals in Figs. 4 and 7. For example, for β=10%, across the 50 trials, the number of test groups that are skipped varies from 31 to 35, while the corresponding test time savings vary from 2.36% to 14.78%. As it can be observed, although the number of test groups that are skipped varies very little, the test time savings can vary by more than 10%. This is due to the fact that these 8 test groups include test group 47 with test time 1.23s, which is by far the most time-consuming test group, as well as test groups 45, 48, and 58 with high test times 296.3ms, 310ms and 270.6ms, respectively.

Fig. 10 shows the true and estimated absolute test escape, as well as the 95% confidence interval, across the 50 trials considering the two extreme values for β, i.e. 5% and 90%, which correspond to highest and lowest test escape risk, respectively. Fig. 10 sheds more light in the result in Fig. 6(c) showing the accuracy of test escape estimation across trials. As it can be observed, the true and estimated test escape values are close to each other, for all except one trial (e.g. trial 42 for β=90%) the true test escape value lies within the 95% confidence interval, and the 95% confidence interval is sufficiently narrow. In trial 42 for β=90% where the true

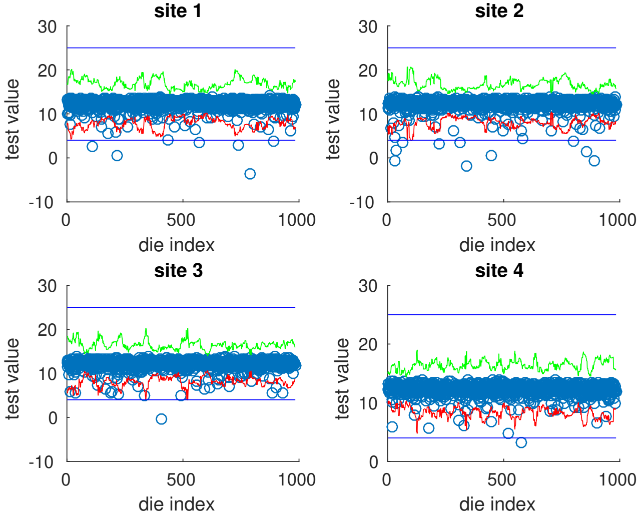


Fig. 11: Moving DPAT limits per site as dies go through the adaptive test cycle.

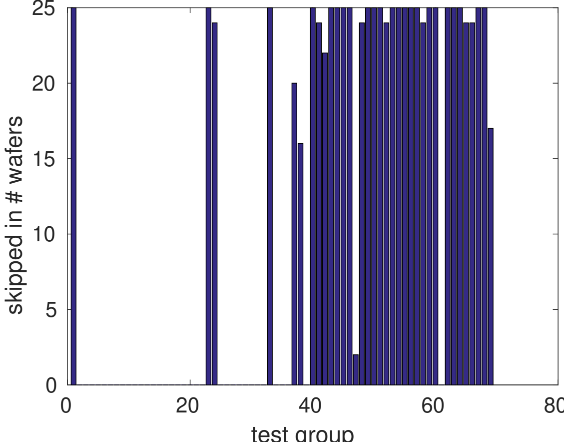


Fig. 12: Adaptive test flow "moving DPAT, periodical full test": number of wafers in the first lot for which each test group is skipped.

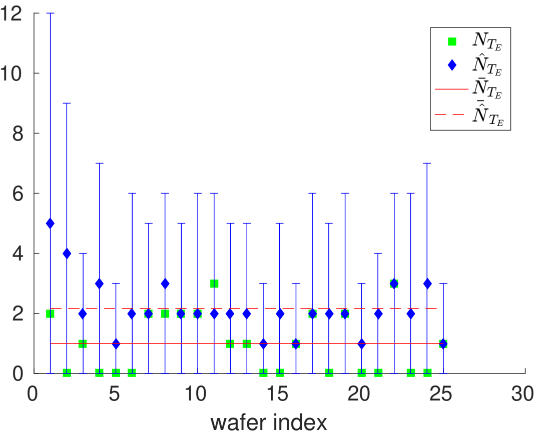


Fig. 13: Adaptive test flow "moving DPAT, periodical full test": true and estimated test escape across wafers in the first lot, showing also the 95% confidence interval.

test escape values lie outside the 95% confidence interval, the distance between the closest bound of the confidence interval and the true test escape is 1. Therefore, we conclude that test escape risk is well estimated, regardless whether it is high or low, providing large confidence in the adaptive test decisions.

Finally, Fig. 11 shows for a specific test the moving DPAT limits per site as dies go through the adaptive test cycle. The moving DPAT limits are at any point in time tighter compared to the standard specifications, which are represented with the horizontal lines. As it can be observed, for this specific test there are tens of dies which do not violate the test specifications, but are clear outliers and are forwarded to a full test during the adaptive test cycle to investigate whether they fail one of the skipped tests.

C. Adaptive test in action

Since in our experiment adaptive test is applied during wafer test, any point in the curves in Fig. 5 is valid and potentially interesting from a test economics perspective. For example, if we are interested in performing a fast wafer test while discarding the majority of faulty dies but still affording packaging a non-negligible number of faulty dies, then using the simple flow "no DPAT, no periodical full test" and a low value for β is probably the best option. If, in contrast, we are very much concerned about saving the considerable cost of packaging faulty devices, then we may opt for the more elaborate flow "moving DPAT, periodical full test".

In this experiment, we consider without loss of generality the flows "moving DPAT, periodical full test" and "no DPAT, no periodical full test", and we apply them separately on all available wafers from the two lots imitating a real implementation scenario. For the flow "moving DPAT, periodical full test" we use $\beta = 5\%$, while for the flow "no DPAT, no periodical full test" we use $\beta = 30\%$.

Let us consider first the flow "moving DPAT, periodical full test". Fig. 12 shows the number of wafers in the first lot for which each test group is skipped during the pre-processing step. We observe three categories of test groups, namely test groups that are skipped for every wafer, test groups that are not skipped for any of the wafers, and test groups that are skipped only for a certain number of wafers. Comparing Fig. 12 to Fig. 8 that corresponds to a single wafer from the first lot, we observe that the same test groups that are kept for all trials for the single wafer are always kept for every other wafer too. These test groups are permanent and/or are very effective in detecting failures. In contrast, test groups that were skipped for all trials for the single wafer may be switched on for other wafers. This observation points to the fact that there are some defect types that do not manifest themselves on every wafer and are uniquely detected by specific test groups. Furthermore, in the set of test groups that are skipped only for a certain number of wafers, we observe that there are 7 test groups that are skipped for 24 wafers, that is, they are kept only for 1 wafer. These test groups seem to detect a rather rare fault that is not manifested in any of the other wafers.

Fig. 13 shows the true and estimated test escape across all wafers in the first lot, as well as the 95% confidence interval

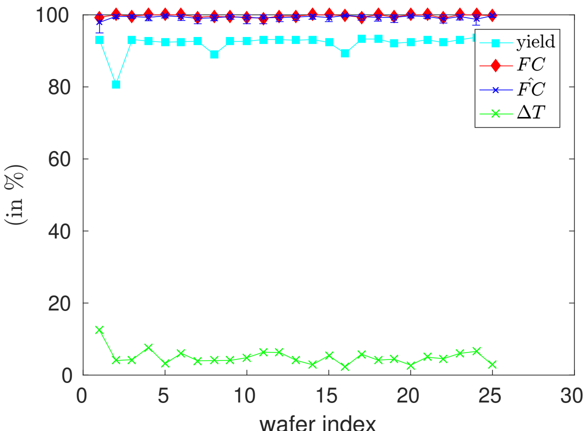


Fig. 14: Adaptive test flow "moving DPAT, periodical full test": trade-off between yield, true and estimated fault coverage values, and test time savings across wafers in the first lot, showing also the 95% confidence interval for fault coverage.

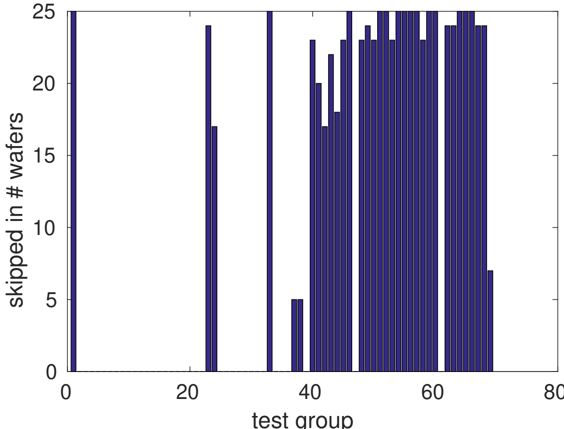


Fig. 15: Adaptive test flow "no DPAT, no periodical full test": number of wafers in the first lot for which each test group is skipped.

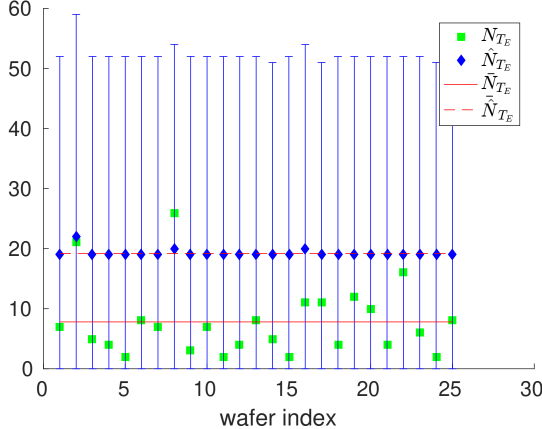


Fig. 16: Adaptive test flow "no DPAT, no periodical full test": true and estimated test escape across wafers in the first lot, showing also the 95% confidence interval.

for the estimated test escape. We recall that the defect level varies across wafers in the first lot between 273 and 842 with an average value of 349.44. As it can be seen, the true test escape varies between 0 and 3 and lies always within the 95% confidence interval. The mean estimation error is 1.24. Fig. 13 also shows the average true and estimated test escape, denoted by $\bar{N}_{T_E}$ and $\bar{\hat{N}}_{T_E}$, respectively, defined as the mean true and estimated test escape, respectively, computed over all wafers in the lot. The average true and estimated test escape values are 1 and 2.16, respectively, that is, the true value is overestimated by 1.16. We conclude that the test escape risk is very well estimated for all wafers providing confidence in the decisions.

Fig. 14 shows the trade-off between yield, true and estimated fault coverage values, and test time savings across all wafers in the first lot. The plot also shows the 95% confidence interval for the estimated fault coverage. We recall that in the first lot the wafer yield varies between 80.74% and 93.75% with an average value of 92.01%. It is practically constant at around 92% across all wafers except for the second wafer that presents a much lower value of 80.74%. To estimate fault coverage from (27), an estimate of the defect level is derived from the dies in the *control sample* that are fully tested during the pre-processing step. The 95% confidence interval for the fault coverage is derived by using the 95% confidence interval for the absolute test escape. The true fault coverage varies between 99% and 100% with an average value of 99.70%. The estimated fault coverage is very accurate for all wafers in the lot with a mean estimation error of 0.42%, and the true fault coverage always lies within the 95% confidence interval which is very tight and hardly legible in the plot. The test time savings vary between 2.29% and 12.46% with an average value of 4.97%. We recall that this particular adaptive test flow targets a steadily high fault coverage, while achieving the maximum possible test time savings given this constraint. This flow is appropriate when the goal is to screen out all faulty dies at wafer-level so as to avoid packaging faulty dies, while still achieving some test time savings, which when projected to high volume are very significant.

Figs. 15-17 show the results for the flow "no DPAT, no periodical full test" using the wafers in the first lot. Comparing Fig. 15 to Fig. 12, we observe that on average test groups are skipped with a lower rate in the flow "no DPAT, no periodical full test" compared to the flow "moving DPAT, periodical full test". This is due to the fact that the value of β is higher for the flow "no DPAT, no periodical full test" than for the flow "moving DPAT, periodical full test". The true fault coverage varies between 94.60% and 99.40% with an average value of 97.87%, and the test time savings vary between 28.97% and 37.83% with an average value of 34.56%. Thus, the flow "no DPAT, no periodical full test" achieves on average about 2% less fault coverage and about 30% more test time savings than the flow "moving DPAT, periodical full test". This is expected since the flow "no DPAT, no periodical full test" is more appropriate when the goal is to maximize test time savings at wafer test, while detecting the vast majority of faulty dies and allowing a small percentage of faulty dies to be packaged. The estimates of the test escape and fault coverage are less accurate than in the flow "moving DPAT, periodical full test" and also pessimistic since, as explained in Section VI-A, in the absence

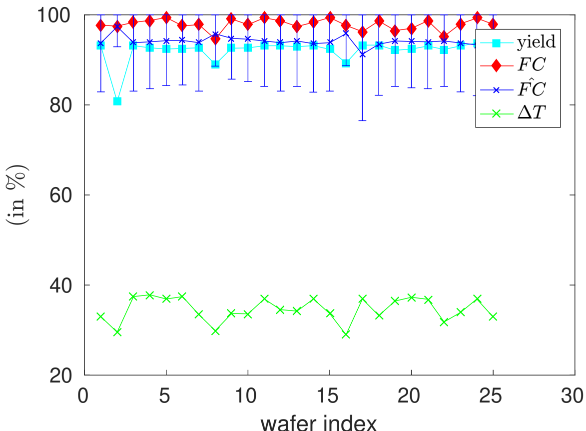


Fig. 17: Adaptive test flow "no DPAT, no periodical full test": trade-off between yield, true and estimated fault coverage values, and test time savings across wafers in the first lot, showing also the 95% confidence interval for fault coverage.

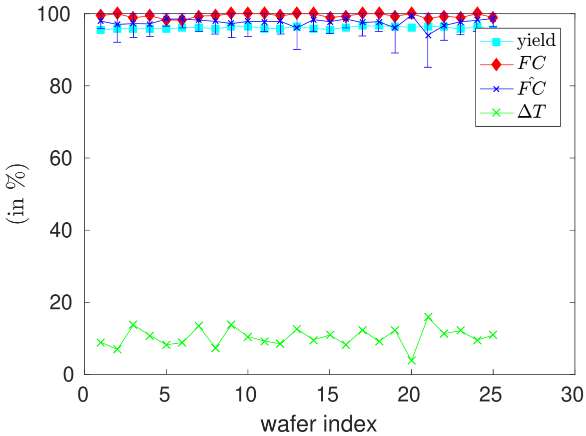


Fig. 18: Adaptive test flow "moving DPAT, periodical full test": trade-off between yield, true and estimated fault coverage values, and test time savings across wafers in the second lot, showing also the 95% confidence interval for fault coverage.

of full test data during the adaptive cycle, they rely solely on the correction factor in the Wilson interval. Nevertheless, the estimates are deemed to be reasonable and always lie within the 95% confidence interval.

Finally, from Fig. 17 we observe that the lowest test time savings are observed for the wafers that incur the lowest yield. To shed more light into this observation, we repeat the experiment for the wafers in the second lot using the exact same parameter values as for the first lot. We recall that the average wafer yield for the first and second lot is 92.01% and 96.10%, respectively. Fig. 18, which shows the result of applying the flow "moving DPAT, periodical full test" for the wafers in the second lot. The test time savings end up being on average 10.33% across all wafers, while we recall that for the first lot the test time savings are on average 4.97% across all wafers, that is, an increase of more than 5%. When applying the flow "no DPAT, no periodical full test" the test time savings are on average 36.01%, while for the first lot the test time savings are on average 34.56%, that is, an increase of about 1.5%. This proves that there is a correlation between yield and test time savings for a target fault coverage, that is, the lower the yield is, the lower the test time savings are. This is expected since, in general, the lower the yield is, the smaller the number of test groups that is skipped in the pre-processing step is, and the larger the number of test groups that is switched on during the adaptive test cycle is. Moreover, in general, lower yield implies more outliers, thus the number of dies that end up being fully tested during the adaptive test cycle is higher.

VII. Conclusions

We presented an adaptive test algorithm for mixed-signal circuits. The algorithm is specifically designed for wafer test, but it can be extended for final test as well. It includes a number of comprehensive options and user-defined parameters such that it can be tuned to achieve the desired advantageous trade-off between test escapes and test time savings as dictated by the test economics of the target application. The algorithm considers the standard test suite and saves test time on average by judiciously selecting tests to skip. The set of tests that is skipped is adapted to the particularities of each wafer. It is selected based on automated criteria that include the fail statistics of a fraction of dies from the wafer that are fully tested and real-time outlier detection. In its last step, the algorithm quickly calculates an estimate of the test escape risk and a corresponding confidence interval, in order to add confidence to the adaptive test flow and report any alarming event. The algorithm is demonstrated using a sizable production test data set from a large mixed-signal circuit. It is shown that the algorithm can be tuned to achieve a large range of trade-offs between test escapes and test time savings and that test escapes can be estimated very accurately. It is also shown that the algorithm adapts to the wafer yield, resulting in significantly less test effort for wafers that present high yield.

References

[1] D. Mannath, D. Webster, V. Montano-Martinez, D. Cohen, S. Kush, T. Ganesan, and A. Sontakke, "Structural approach for built-in tests in RF devices," in *Proc. IEEE International Test Conference*, 2010, Paper 14.1.

[2] H. Hashempour, J. Dohmen, B. Tasic, B. Kruseman, C. Hora, M.Van Beurden, and Y. Xing, "Test time reduction in Analogue/Mixed-signal devices by defect oriented testing: An industrial example," in *Proc. Design, Automation & Test in Europe Conference*, 2011.

[3] S. Sunter, K. Jurga, P. Dingenen, and R. Vanhooren, "Practical random sampling of potential defects for analog fault simulation," in *Proc. IEEE International Test Conference*, 2014, Paper 2.3.

[4] A. Coyette, B. Esen, W. Dobbelaere, R. Vanhooren, and G. G. E. Gielen, "Automatic test signal generation for mixed-signal integrated circuits using circuit partitioning and interval analysis," in *Proc. IEEE International Test Conference*, 2016.

[5] H.-G. D. Stratigopoulos and Y. Makris, "Concurrent detection of erroneous responses in linear analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 878–891, 2006.

[6] A. Valdes-Garcia, R. Venkatasubramanian, J. Silva-Martinez, and E. Sanchez-Sinencio, "A broadband CMOS amplitude detector for on-chip RF measurements," *IEEE Transactions on Instrumentation and Measurement*, vol. 57, no. 7, pp. 1470–1477, 2008.

[7] E. S. Erdogan and S. Ozev, "Detailed characterization of transceiver parameters through loop-back-based BiST," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 6, pp. 901–911, 2010.

[8] M. Barragan, R. Alhakim, H.-G. Stratigopoulos, M. Dubois, S. Mir, H. Le Gall, N. Bhargava, and A. Bal, "A fully-digital BIST wrapper based on ternary test stimuli for the dynamic test of a 40nm CMOS 18-bit stereo audio $\Sigma\Delta$ ADC," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1876–1888, 2016.

[9] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, 2002.

[10] H.-G. Stratigopoulos and Y. Makris, "Error moderation in low-cost machine-learning-based Analog/RF testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 2, pp. 339–351, 2008.

[11] H.-G. Stratigopoulos and S. Mir, "Adaptive alternate analog test," *IEEE Design & Test of Computers*, vol. 29, no. 4, pp. 71–79, 2012.

[12] H. Ayari, F. Azais, S. Bernard, M. Compte, V. Kerzerho, O. Potin, and M. Renovell, "Making predictive analog/RF alternate test strategy independent of training set size," in *Proc. IEEE International Test Conference*, 2012, Paper 10.1.

[13] M. J. Barragan and G. Léger, "A procedure for alternate test feature design and selection," *IEEE Design & Test*, vol. 32, no. 1, pp. 18–25, 2015.

[14] H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-based estimation of analog parametric test metrics," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 12, pp. 1977–1990, 2014.

[15] J. Sequeira, S. Natarajan, P. Goteti, and N. Chaudhary, "Fault simulation for analog test coverage," in *Proc. IEEE International Test Conference*, 2016.

[16] P. Maxwell, "Adaptive testing: Dealing with process variability," *IEEE Design & Test of Computers*, vol. 28, no. 6, pp. 41–49, 2011.

[17] N. Kupp and Y. Makris, "Applying the model-view-controller paradigm to adaptive test," *IEEE Design & Test*, vol. 29, no. 1, pp. 28–35, 2011.

[18] C. Streitwieser, "Real-time test data acquisition and data processing enabling closed loop control systems for adaptive test," in *Proc. IEEE International Symposium on Circuits and Systems*, 2016, pp. 902–905.

[19] K. R. Gotkhindikar, W. R. Daasch, K. M. Butler, J. M. Carulli Jr., and A. Nahar, "Die-level adaptive test: Real-time test reordering and elimination," in *Proc. IEEE International Test Conference*, 2011.

[20] B. Aslan and A. Orailoglu, "Aggressive test cost reductions through continuous test effectiveness assessment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 12, pp. 2093–2103, 2016.

[21] M. Grady, B. Pepper, J. Patch, M. Degregorio, and P. Nigh, "Adaptive testing - cost reduction through test pattern sampling," in *Proc. IEEE International Test Conference*, 2013.

[22] M. Shintani, T. Uezono, T. Takahashi, K. Hatayama, T. Aikyo, K. Masu, and T. Sato, "A variability-aware adaptive test flow for test quality improvement," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 7, pp. 1056–1066, 2014.

[23] W. R. Daasch, J. McNames, R. Madge, and K. Cotar, "Neighborhood selection for i_{DDQ} outlier screening at wafer sort," *IEEE Design & Test of Computers*, vol. 19, no. 5, pp. 74– 81, 2002.

[24] S. S. Sabade and D. M. Walker, "IC outlier identification using multiple test metrics," *IEEE Design & Test of Computers*, vol. 22, no. 6, pp. 586–595, 2005.

[25] W. R. Daasch and R. Madge, "Variance reduction and outliers: statistical analysis of semiconductor test data," in *Proc. IEEE International Test Conference*, 2005, Paper 13.1.

[26] S. H. Wu, B. N. Lee, L.-C. Wang, and M. S. Abadir, "Statistical analysis and optimization of parametric delay test," in *Proc. IEEE International Test Conference*, 2007, Paper 23.1.

[27] X. Yu and R. D. Blanton, "Diagnosis-assisted adaptive test," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 9, pp. 1405–1416, 2012.

[28] S. Benner and O. Boroffice, "Optimal production test times through adaptive test programming," in *Proc. IEEE International Test Conference*, 2001, pp. 908–915.

[29] C. Streitwieser, "Real-time adaptive test algorithm including test escape estimation method," in *Proc. International Mixed-Signal Testing Workshop*, 2015.

[30] A. Ahmadi, A. Nahar, B. Orr, M. Pas, and Y. Makris, "Wafer-level process variation-driven probe-test flow selection for test cost reduction in analog/RF ICs," in *Proc. IEEE VLSI Test Symposium*, 2016.

[31] E. Yilmaz and S. Ozev, "Adaptive test elimination for Analog/RF circuits," in *Proc. ACM/IEEE Design Automation Conference*, 2009, pp. 720–725.

[32] E. Yilmaz and S. Ozev, "Test application for analog/rf circuits with low computational burden," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 6, pp. 968–979, 2012.

[33] E. Yilmaz, S. Ozev, and K. Buttler, "Per-device adaptive test for analog/rf circuits using entropy-based process monitoring," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 6, pp. 1116–1128, 2013.

[34] L. Fang, M. Lemnawar, and Y. Xing, "Cost effective outliers screening with moving limits and correlation testing for analogue ICs," in *Proc. IEEE International Test Conference*, 2006, Paper 31.2.

[35] D. Drmanac, N. Sumikawa, L. Winemberg, L.-C. Wang, and M. S. Abadir, "Multidimensional parametric test set optimization of wafer probe data for predicting in field failures and setting tighter test limits," in *Proc. Design, Automation & Test in Europe Conference*, 2011.

[36] S. Krishnan and H. Kerkhoff, "Exploiting multiple mahalanobis distance metrics to screen outliers from analog product manufacturing test responses," *IEEE Design & Test*, vol. 30, no. 3, pp. 18–24, 2013.

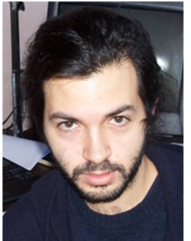
[37] W. Dobbelaere, R. Vanhooren, W. De Man, K. Matthijs, A. Coyette, B. Esen, and G. G. E. Gielen, "Analog fault coverage improvement using final-test dynamic part average testing," in *Proc. IEEE International Test Conference*, 2016.

[38] M. Chen and A. Orailoglu, "Test cost minimization through adaptive test development," in *Proc. IEEE International Conference on Computer Design*, 2008, pp. 234–239.

[39] G. Léger, "Combining adaptive alternate test and multi-site," in *Proc. Design, Automation & Test in Europe Conference & Exhibition*, 2015, pp. 1389–1394.

[40] S. Biswas and R. D. (Shawn) Blanton, "Maintaining accuracy of test compaction through adaptive re-learning," in *Proc. IEEE VLSI Test Symposium*, 2009, pp. 257–263.

[41] Automotive Electronics Council (AEC), *Guidelines for Part Averaging Testing, AEC-Q001 Rev-D*, 2011.



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