# Adaptive Voltage Position Design for Voltage Regulators

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*Abstract*—**This paper proposes a general design guideline for the voltage regulator (VR) to achieve adaptive voltage position (AVP). All existing control methods are covered for different kinds of output filter capacitors. Based on the small-signal model analysis, the output impedance and system control bandwidth are discussed. Following the proposed design guidelines, simulation and experimental results demonstrate very good VR transient response.**

***Keywords-voltage regulator; output impedance; AVP***

## I. INTRODUCTION

It is perceived that Moore's Law will prevail at least for the next decade with the continuous advancement of processing technologies for integrated circuits. According to Intel's roadmap, over one billion transistors will be integrated in one processor by the year 2010; the processor's clock speed will approach 15 GHz; the core static currents will increase up to 150A; the dynamic current slew rate will rise up to 120A/ns; and the core voltage will reduce to 0.8V [1-2]. The rapid advancement of processor technology has posed stringent challenges to power management and power delivery.

One pressing issue is the dynamic voltage regulation of the voltage regulator (VR). Many output capacitors have already been used to reduce the voltage spikes that occur during the transient period. Increasing the number of capacitors to meet the even higher transient requirement in the future is no longer a suitable solution because of size and cost issues. One way to alleviate this problem is based on adaptive voltage position (AVP) control [3-4]. The basic idea is to control the output voltage level so that it is slightly higher than the minimum value at full load, and a little lower than the maximum value at light load. As a result, the entire voltage tolerance window can be used for the voltage jump or drop during the transient period. Fig. 1 shows the transient comparison between non-AVP and AVP designs. It is very clear that the AVP design allows the use of fewer output capacitors, and hence reduces the VR cost. A side benefit of the AVP control is that the VRM output power at full load is degraded, which greatly facilitates the thermal design. Also, the AVP design is indispensable for meeting the processor load line specifications [3].

The AVP is related to the steady-state operation of the VRM. If the transients between the two steady-state stages have no spikes and no oscillations, as is the situation shown in Fig. 2 (a), the AVP design is optimal. The transient can take advantage of the entire voltage tolerance window. The comparison between the current and the related output voltage waveforms reveals that the VRM equals an ideal voltage source in series with a resistor $R_O$.

$$R_o = \Delta v_o / \Delta i_o . \tag{1}$$

Fig. 2 (b) shows the equivalent circuit of the VRM.

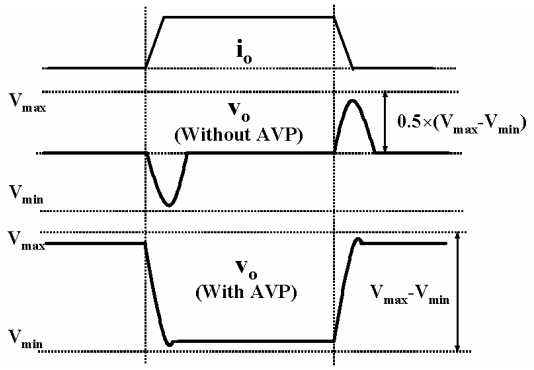


Figure 1. Transient without and with AVP designs.

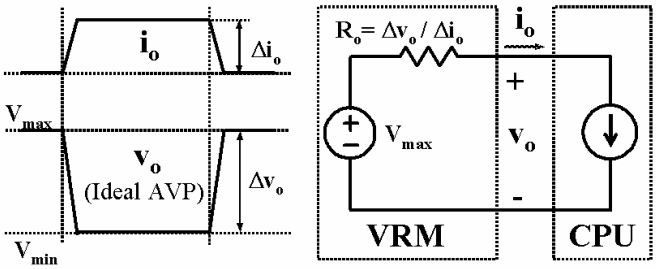


Figure 2. (a) The ideal AVP design and (b) the equivalent circuit of the VRM.

Now it is very clear that the constant resistive output impedance design for the VRM is an optimal design for the transient response. Actually, improving the dynamic regulation of a converter based on the output impedance consideration is

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an old concept [5-8]. However, not every converter can achieve constant resistive output impedance. How to apply this concept to VR for AVP design is not clear. This paper clarifies these issues for all kinds of existing control methods. Section II classifies the existing control methods into two. By comparing their small signal models, a general way is derived to design the AVP. Section III discusses the compensator design for different control methods with different kinds of output capacitors. Simulation and experimental results demonstrate very good AVP transient response.

## II. A General Design Guideline

The multiphase buck converter is widely adopted for the VR design. The small-signal model of the multiphase buck converter can be simplified as a single-phase buck converter in continuous-current mode (CCM) [9]. As a result, a simple synchronous buck converter is used here for analysis.

### A. Existing Control Methods

Power management IC companies have developed many controllers to achieve AVP function. Basically, all the control methods can be classified as current-mode control or active-droop control. Fig. 3(a) shows the current-mode control scheme, and Fig. 3(b) shows the active-droop control scheme. The equivalent series inductor (ESL) of the output capacitor is ignored here since the high-frequency ceramic capacitors in parallel greatly reduce its effect. In the current-mode control, a finite DC gain is designed for the voltage-loop compensator $G_{cv}$ to achieve AVP by introducing a steady-state output voltage error. In the active-droop control, the current information is injected into the feedback voltage information, so that the AVP can be realized with an infinite DC gain compensator design for $A_v$. That is why this control method is also referred to as current-injection control. The design methods to achieve AVP for these two kinds of controls have already been discussed by the authors [10-11]. However, the designs are based only on electrolytic capacitors (the Oscon capacitor). This paper develops a general way to analyze the two kinds of control methods, and this approach can be extended to all kinds of output filter capacitors.

Based on the multi-loop analysis method [12], Fig. 4 shows the small-signal block of the two control schemes with the power stage. $Z_o$ is the power stage open-loop output impedance. $G_{vd}$ is the transfer function of output voltage $v_o$ to the duty cycle d. $G_{ii}$ is the transfer function of inductor current $i_L$ to load current $i_o$. $G_{id}$ is the transfer function of the inductor current to the duty cycle. $F_m$ represents the comparator effect. In Fig. 3(a), $G_{ci}$ is the current-loop compensator transfer function, and $G_{cv}$ is the voltage-loop compensator transfer function. In Fig. 3(b), $A_i$ represents the current-sensing function. $A_v$ is the feedback compensator transfer function.

$$Z_o(s) = R_L \cdot \frac{(1+s/\omega_{ESR})\cdot(1+s/\omega_L)}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \tag{2}$$

$$G_{vd}(s) = V_{in} \cdot \frac{1+s/\omega_{ESR}}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \tag{3}$$

$$G_{ii}(s) = \frac{1+s/\omega_{ESR}}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \tag{4}$$

$$G_{id}(s) = V_{in} \cdot \frac{s\cdot C_o}{1+s/(Q\cdot\omega_o)+s^2/\omega_o^2} \tag{5}$$

$$F_M = \frac{1}{V_{p-p}} \tag{6}$$

$$\omega_o \approx \frac{1}{\sqrt{C_o\cdot L_o}},\ Q \approx \frac{\sqrt{L_o/C_o}}{R_L + ESR_C}, \tag{7}$$

$$\omega_{ESR} = \frac{1}{ESR_C\cdot C_o},\ \omega_L = \frac{L_o}{R_L}. \tag{8}$$

$R_L$ includes the DC resistance of the inductor $L_o$, the conduction resistance $R_{ds\text{-}on}$ of the MOSFETs, and the parasitic resistance of the traces.

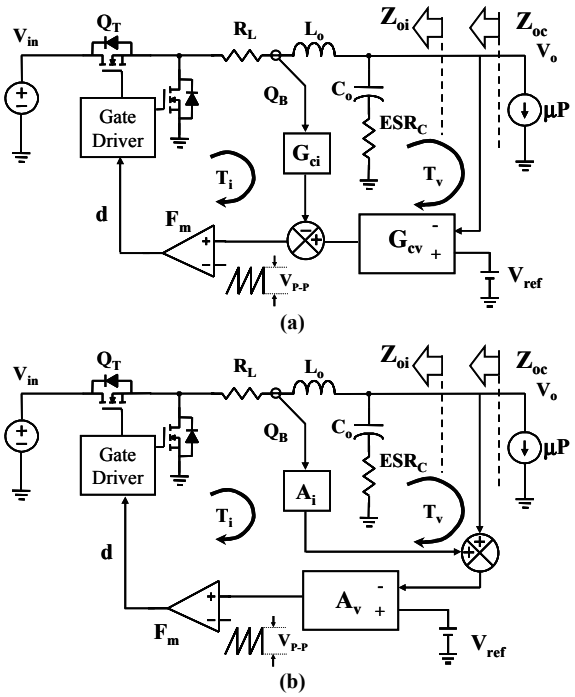



Figure 3. Output impedance analysis using a buck converter: (a) current-mode control and (b) active-droop control.

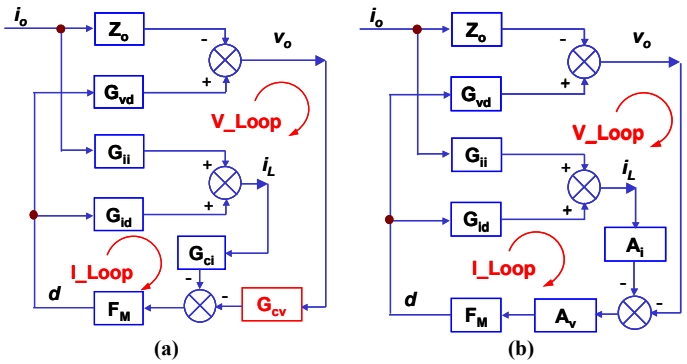



Figure 4. The small-signal blocks: (a) current-mode control and (b) active-droop control.

From Fig. 4, it is very clear that both controls are two-loop feedback systems. Table I lists the system current loop $T_i$ and voltage loop $T_v$. In the expression of $T_i$, $H_e(s)$ models the current sampling effect:

$$H_e(s) = 1 - \frac{s}{2 \cdot f_s} + \frac{s^2}{(\pi \cdot f_s)^2} \cdot \tag{9}$$

In current-mode control, the current loop is inside the voltage loop. The voltage-loop compensator requires a finite DC gain to achieve AVP control, and the designs of $G_{ci}$ and $G_{cv}$ can be separated. In active-droop control, the current and voltage are fed back, and then the two are added together. The compensator design of $A_v$ influences both the current and voltage loops, and it needs an infinite DC gain. Thus, the design for the active-droop control seems more complex. However, a comparison between Figs. 4 (a) and (b) shows that the two control methods are very similar. When $G_{cv}=A_v$ and $G_{ci}=A_i \times A_v$, these two small-signal blocks are equivalent. As a result, the active-droop control is a special case of current-mode control. The AVP design for these two control methods should follow the same principle.

TABLE I. THE CURRENT LOOP AND VOLTAGE LOOP FOR THE TWO CONTROL METHODS.

| | Current-Mode Control | Active-Droop Control |
|---|---|---|
| Current Loop | $T_i = G_{ci} \cdot F_M \cdot G_{id} \cdot H_e(s)$ | $T_i = A_i \cdot A_v \cdot F_M \cdot G_{id} \cdot H_e(s)$ |
| Voltage Loop | $T_v = G_{cv} \cdot F_M \cdot G_{vd}$ | $T_v = A_v \cdot F_M \cdot G_{vd}$ |

### B. *The Basic Design Idea*

The design for the current-mode control has already been discussed before to realize a stable system [13-15]. A high-bandwidth current-loop design can simplify the buck converter from a two-order system to a one-order system. When the current loop is closed and the voltage loop is open, the buck converter operates as an ideal current source, as shown in Fig. 5. Its output impedance can be approximately represented as:

$$Z_{oi} = \frac{1}{s \cdot C_o} + ESR_C = \frac{1 + s/\omega_{ESR}}{s \cdot C_o} \cdot \tag{10}$$

When the voltage loop is closed, the closed-loop output impedance is:

$$Z_{oc} = \frac{Z_{oi}}{1 + T_2}, \tag{11}$$

where $$T_2 = \frac{T_v}{1 + T_i} \cdot \tag{12}$$

$T_2$ is defined as the system control loop in a multi-loop controlled system [12].

With a logarithm union, the closed-loop output impedance is:

$$Z_{oc}(dB) \cong \begin{cases} Z_{oi}(dB) - T_2(dB) & (T_2 >> 1) \\ Z_{oi}(dB) & (T_2 << 1) \end{cases} \cdot \tag{13}$$

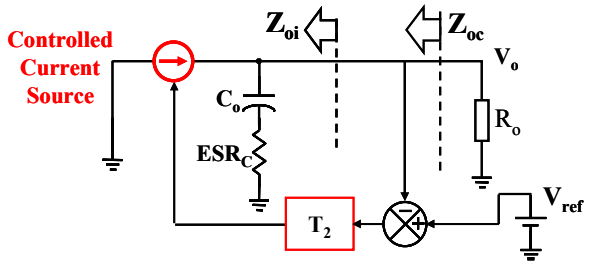



Figure 5. The simplified small-signal model with current-mode control.

For the output impedance $Z_{oi}$, the corner frequency is just at the capacitor ESR zero $\omega_{ESR}$. Following the constant output impedance design concept [10], it is easy to derive that the system loop $T_2$ should be designed with a -20dB/dec slope and a bandwidth ($\omega_c$) at $\omega_{ESR}$. Fig. 6 shows this clearly.

However, for different kinds of output capacitors, the ESR zeros is different. Table II lists three major kinds of output capacitors in the practical VR applications. For the design with Oscon capacitors, 200~300KHz switching frequencies are sufficient to achieve the 16 KHz bandwidth. Further increasing the bandwidth cannot help the transient response, because the impedance beyond $\omega_c$ determines the transient voltage spikes. Fig. 7 (a) shows this condition. This is the critical control bandwidth concept proposed before by the authors [16]. The design with ESRE capacitors can still achieve constant output impedance, but it needs higher switching frequencies to realize the 40 KHz control bandwidth so that to take advantage of the small capacitor size. For the ceramic capacitor, it is impossible to push the bandwidth to 1.1 MHz with a reasonable efficiency. However, as long as the output impedance is constant within the control bandwidth, and the impedance beyond the bandwidth is smaller than that in the lower frequency range, AVP can still be achieved. Fig. 7 (b) shows this condition, and the simulation results in Fig. 8 show a good AVP design with the ceramic capacitors. In this case, the output impedance within the control bandwidth determines the AVP.

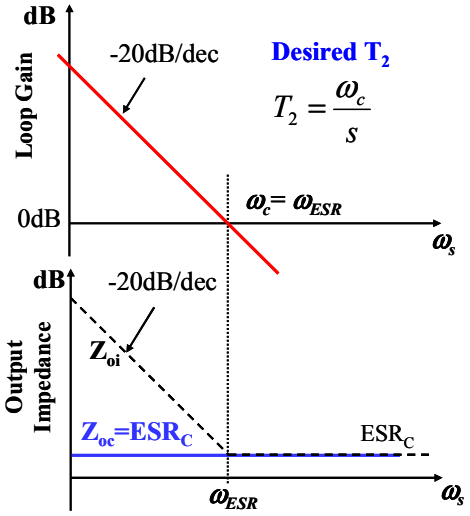



Figure 6. Constant output impedance design with $\omega_c=\omega_{ESR}$.

At the bandwidth frequency point ($\omega_c$), $T_2 = 1\angle(-180° + \theta)$, where θ is the phase margin. In order to make sure the above analysis is still effective at $\omega_c$, the following relationship should be satisfied:

$$|1 + T_2| > 1.$$

It is easy to derive that the phase margin θ must be larger than 60° based on the vector analysis in Fig. 9. Otherwise, there will be a bump at $\omega_c$ in the closed-loop impedance curve, which will cause extra transient voltage spikes. For a system loop $T_2$ designed with a -20dB/dec, there is no such problem because the phase margin is about 90°.

Consequently, for all kinds of output capacitors, the desired system loop $T_2$ is:

TABLE II. THE ESR ZERO OF DIFFERENT KINDS OF OUTPUT CAPACITORS.

| VR Output Capacitors | Size ($mm^3$) | ESR Zero ($\omega_{ESR}$) |
|---|---|---|
| Oscon (820μF/12Ω) | $\phi 10^2 \times 10.5$ | 16KHz |
| ESRE (270μF/15Ω) | 7.3×4.3×4.2 | 40KHz |
| Ceramic (100μF/1.5Ω) | 4.5×3.2×3.1 | 1.1MHz |

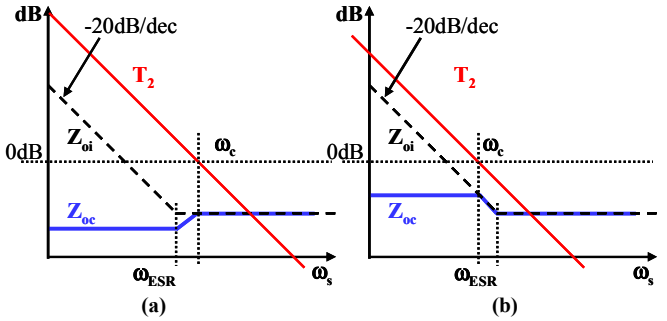



Figure 7. Output impedance with: (a) $\omega_c > \omega_{ESR}$ and (b) $\omega_c < \omega_{ESR}$.

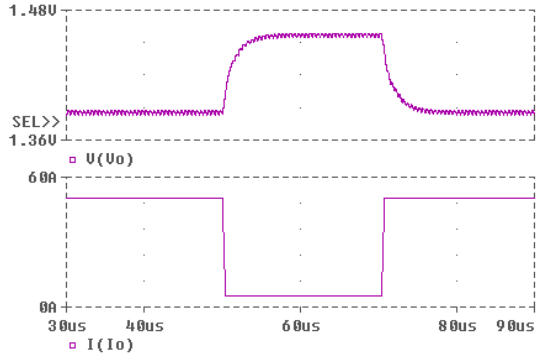



Figure 8. Simulation result for AVP design with ceramic capacitors.

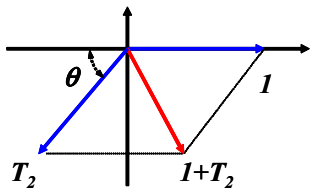



Figure 9. θ>60° for $|1+T_2|>1$.

$$T_2(s) = \frac{\omega_c}{s}. \tag{14}$$

The following items summarize the AVP design guidelines:

- A stable current-loop design with a high bandwidth simplifies the buck converter into a one-order system.
- A system loop $T_2$ deigned with -20dB/dec slope, a bandwidth equal to or smaller than the capacitor ESR zero, and a phase margin over 60°. This is necessary to achieve a constant output impedance design within the control bandwidth.
- $Z_{oc} \le \Delta V_o / \Delta i_o$ is needed to meet the transient response requirement.

Based on these guidelines, it is easy to design the compensators for different control methods with different kinds of output capacitors.

## III. COMPONSATOR DESIGN

If the current loop bandwidth $\omega_{ci}$ is much larger than the system bandwidth $\omega_c$, (12) can be simplified as:

$$T_2 = \frac{T_v}{1 + T_i} \approx \frac{T_v}{T_i}. \tag{15}$$

Table I shows the relationship between the compensator transfer function between the current-loop and voltage-loop transfer functions. Then from (14) and (15), the required compensator design can be derived to achieve the desired system loop $T_2$. Consequently, AVP design can be realized based on the constant output impedance design within the control bandwidth.

The following analysis and modeling are based on a 12V-to-1.5V/25A VR design with both Oscon and ceramic output capacitors in Table II. Both cases the capacitor numbers are four. The output chock follows the critical inductance design in [9, 10].

### A. *Current-Mode Control*

For current-mode control, (15) becomes

$$T_2(s) \approx \frac{T_v(s)}{T_i(s)} = \frac{G_{vd}(s) \cdot G_{con}(s)}{R_i \cdot G_{id}(s) \cdot H_e(s)}. \tag{16}$$

From (14) and (16), we can derive the desired compensator design as:

$$G_{con}(s) = \frac{R_i}{ESR_C} \cdot \frac{H_e(s)}{1 + s/\omega_{ESR}}. \tag{17}$$

Approximately, we can put a zero at half of the switching frequency to simplify the compensator design.

$$G_{con}(s) \approx \frac{R_i}{ESR_C} \cdot \frac{1 + s/(\pi \cdot f_s)}{1 + s/\omega_{ESR}} \tag{18}$$

There is some physical meaning for the compensator design. A pole compensates the output capacitor ESR zero, and a zero compensates the double right-half-plane zero introduced by the current sample and hold effect. The finite DC gain design is to adjust the steady-stage output error to achieve the AVP.

Fig. 10 shows the outer-loop $T_2$ and output impedance with the proposed compensator design for the current-mode control. They approximate very well to the desired designs for both applications with Oscon and ceramic capacitors.

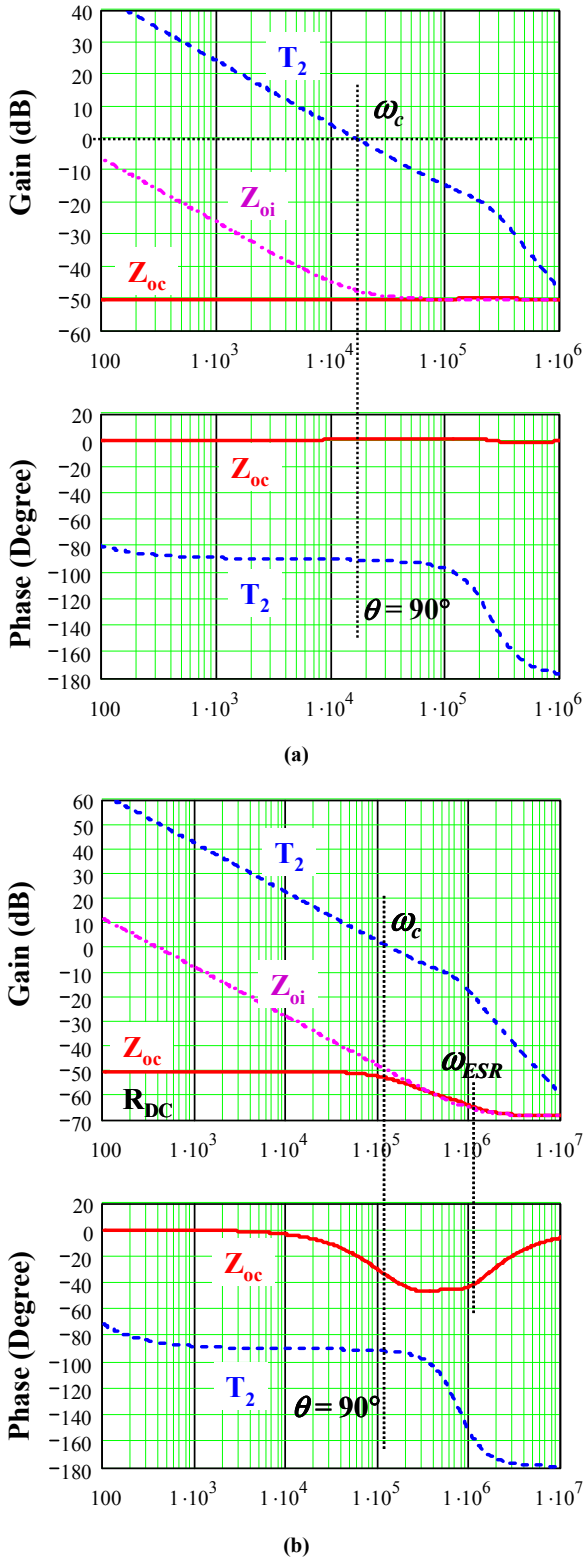



Figure 10. Outer-loop $T_2$ and output impedance in the current-mode control: (a) with Oscon output capacitors, and (b) with ceramic output capacitors.

### B. *Active-Droop Control*

For active-droop control, (15) becomes

$$T_2(s) \approx \frac{T_v(s)}{T_i(s)} \approx \frac{1 + s/\omega_{ESR}}{A_i \cdot C_o \cdot s}. \tag{19}$$

Normally, $A_i$ is designed with the specified $R_{droop}$, which is the DC output impedance. If the control bandwidth is lower than the ESR zero, (19) can be further simplified as:

$$T_2(s) \approx \frac{1}{R_{droop} \cdot C_o \cdot s} = \frac{\omega_c}{s}, \tag{20}$$

which is exactly the desired outer-loop design. And the compensator design $A_v(s)$ has no impact as long as it can meet the design assumption: a current loop with high control bandwidths.

Then the compensator design for the active-droop control is relative simple. The current-loop design guideline in the average current-mode control can be applied here:

$$A_v = K \cdot \frac{1 + s/\omega_o}{s \cdot (1 + s/\omega_p)}. \tag{21}$$

An integrator is used to eliminate the steady-state error. A zero is put to compensate the system double pole. A pole at high frequency range can be used to further attenuate the switching noise, but it can be omitted to simplify the compensator design. The K is designed to achieve a high current loop bandwidth $\omega_{ci}$.

For $\omega_c << \omega_{ESR}$, the K can be expressed as:

$$K = \frac{\Delta(\omega_{ci}) \cdot \omega_c}{F_M \cdot V_{in} \cdot (1 + \omega_{ci}/\omega_o)}, \tag{22}$$

where $\Delta(s) = \dfrac{1}{1 + s/(Q \cdot \omega_o) + s^2/\omega_o^2}$. (23)

Fig. 11 shows the outer-loop $T_2$ with the proposed compensator design for the active-droop control. They approximate very well to the desired design in (14) for both designs with Oscon and ceramic capacitors. The deviation at very high frequencies has little impact for the system performance.

For the design with Oscon capacitors, it is very interesting that all the three loops ($T_i$, $T_v$ and $T_2$) have almost the same control bandwidths at the capacitor ESR zero. Fig. 11(b) shows this clearly.

## IV. Experimental Results

A two-phase interleaved buck converter is designed for a 12V-to-1.5V/25A VR to verify the theoretical analysis for the current-mode control. The controller ISL6560 from Intersil is used. Fig. 12 shows the output current and voltage during a transient response. Fig. 12(a) is for the Oscon capacitor design. Four Oscon capacitors (in Table II) are used in parallel as the bulk output filter capacitor $C_o$. A switching frequency of 300 KHz is good enough to achieve the 16KHz bandwidth, and in the same time the VRM can achieve high efficiency. The output filter inductor in each phase is set as 1 µH. Fig. 12(b) is for the ceramic capacitor design. Six ceramic capacitors (in

Table II) are used in parallel as the bulk output filter capacitor $C_o$. A switching frequency of 650 KHz is selected to achieve a bandwidth of 96 KHz. The output filter inductor in each phase is set as 150 nH. Also, 16 decoupling capacitors (22µF) are used in the output to attenuate the high di/dt effect.

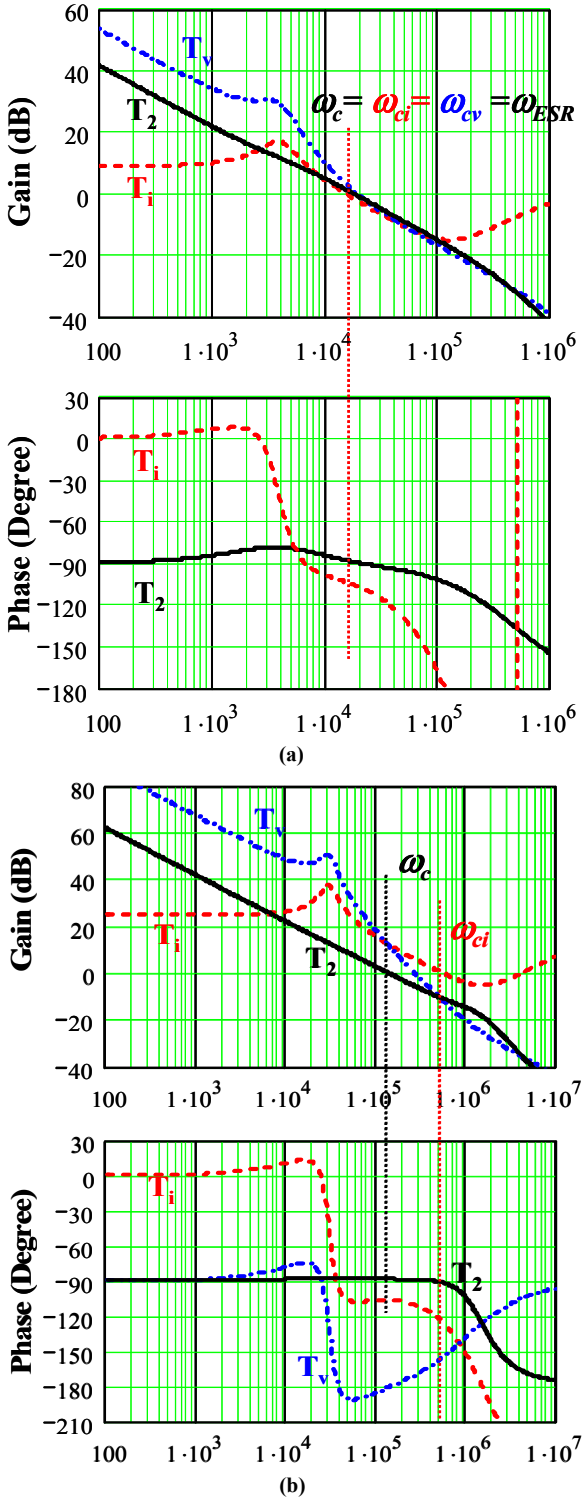



Figure 11. Outer-loop $T_2$ in the active-droop control: (a) with Oscon output capacitors, and (b) with ceramic output capacitors.

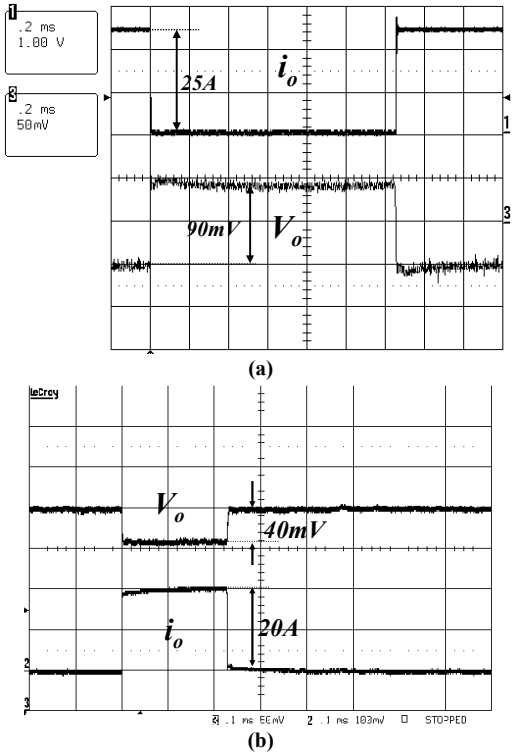



Figure 12. The transient response with current-mode control: (a) with Oscon capacitors and (c) with ceramic capacitors.

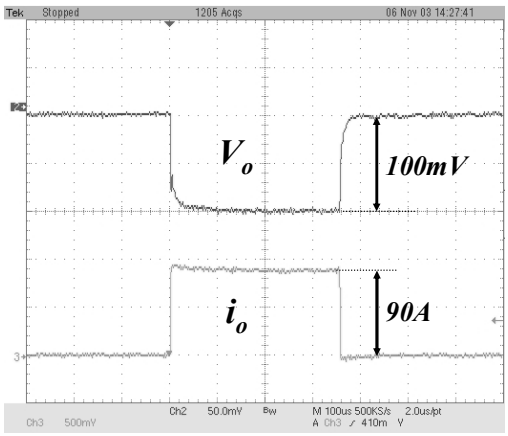
A four-phase interleaved buck converter is designed for a 12V-to-1.5V/90A VR to verify the theoretical analysis for the active-droop control. The controller ISL6561 from Intersil is used. Fig. 13 shows the output current and voltage during a transient response. Fig. 13(a) is for the Oscon capacitor design. Ten Oscon capacitors (560µF/7mΩ for each one) are used in parallel as the bulk output filter capacitor $C_o$. The switching frequency is 300 KHz. The output filter inductor in each phase is set as 300 nH. Fig. 12(b) is for the ceramic capacitor design. Four ceramic capacitors (in Table II) are used in parallel as the bulk output filter capacitor $C_o$. A switching frequency of 1 MHz is selected to achieve a bandwidth of 220 KHz. The output filter inductor in each phase is set as 100 nH. Also, the decoupling capacitors use 10×22µF and 23×10µF to attenuate the high di/dt effect.

Fig. 14 shows the tested outer-loop bandwidth in the current-mode control with Oscon capacitors. It shows that the crossover frequency is exactly on the ESR zero of the output capacitors. Fig. 15 is the case for the ceramic capacitor design with the active-droop control. It agrees very well with the theoretical analysis.

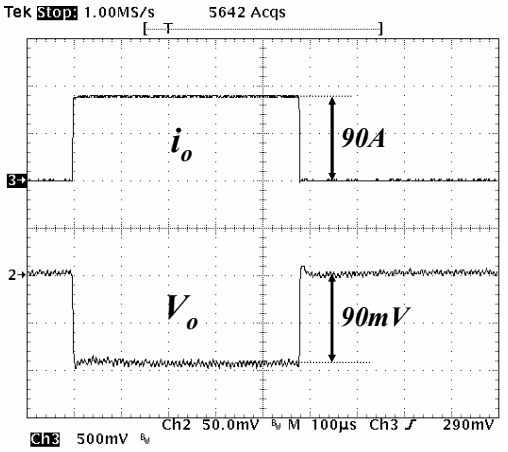
## VI. Conclusion

The AVP design based on the output impedance consideration is discussed in this paper. Small-signal model analysis shows that all the existing control methods for VR follow the same dual-loop structure. By designing a high bandwidth current loop, the system is very easy to achieve

constant output impedance within the control bandwidth. Experimental results show very good AVP control for different kinds of output capacitors.




(a)




(b)

Figure 13. The transient response with active-droop control: (a) with Oscon capacitors and (c) with ceramic capacitors.

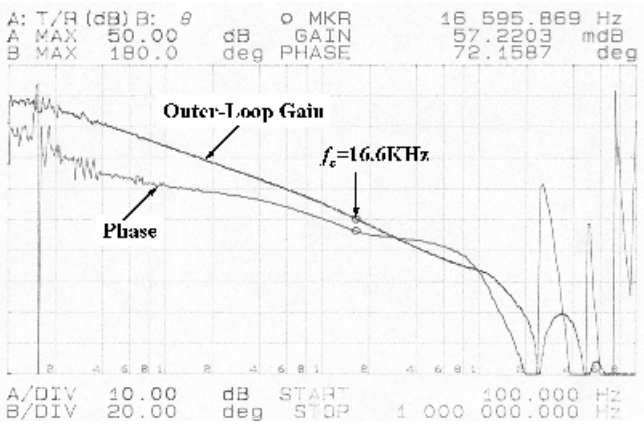



Figure 14. The measured outer-loop gain and phase for the current-mode control with Oscon capacitor design.

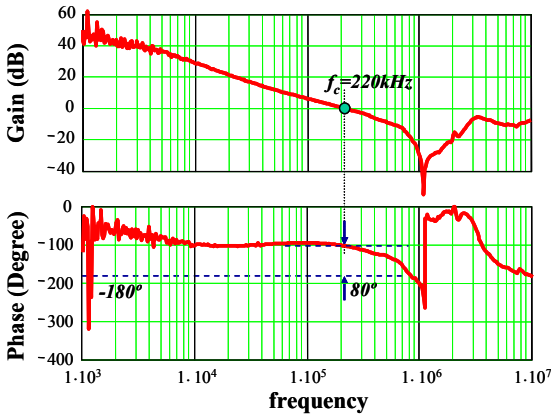



Figure 15. The measured outer-loop gain and phase for the active-droop control with ceramic capacitor design.

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