Adiabatic Logic versus CMOS for Low Power Applications

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***Abstract*—This paper presents a new quasi adiabatic logic family that uses a pair of complementary split-level sinusoidal power supply clocks for digital low power applications such as sensors. The proposed two phase clocked adiabatic static CMOS logic (2PASCL) circuit utilizes the principle of adiabatic switching and energy recovery. By removing the diode at the charging path, higher output amplitude is achieved and the power consumption of the diode is eliminated. We design and simulate NOT, NAND, NOR and Exclusive-OR logic gates based on 2PASCL with SPICE implemented using 0.18 μm CMOS technology. A driving pulse with the height equal to V_{dd} is supplied to the gates. From the simulation results, 2PASCL inverter logic can save up to 97% of energy dissipation compared with static CMOS logic at transition frequencies of 10 to 100 MHz. It also shows the lowest in energy dissipation compared with other proposed simple adiabatic logic inverters.**

I. Introduction

With the widespread use of mobile, hand-held and wireless electronics devices, the demands for the innovations of low-power VLSI arise. For most of the digital circuits today, CMOS logic scheme has been the technology of choice for implementing low-power systems. As the clock and logic speeds increase to meet the new performance requirements, the energy requirement of CMOS circuits are becoming a major concern in the design of these devices.

Power dissipation in conventional CMOS primarily occurs during device switching. When the system is set into a logical "1" level; in other words, when the pull up network is switched on, current starts flowing suddenly through R. Charge of $Q = C_L V_{dd}$ is pulled out of the positive power supply rail to charge the load capacitance C_L up to V_{dd}. The energy taken from the power supply is $Q \cdot V_{dd} = C_L V_{dd}^2$ [1]. By assuming that the energy taken equals the energy supplied to the load capacitor, the energy stored into the load C_L is half of the supplied energy: $E_{stored} = (\frac{1}{2}) C_L V_{dd}^2$. The other half is dissipated in R. The same amount of energy is dissipated during the discharge process in the nMOS pull-down network when the logic level is "0". Therefore the total dissipation as heat during charging and discharging is

$$E_{charge} + E_{discharge} = \frac{1}{2} C_L V_{dd}^2 + \frac{1}{2} C_L V_{dd}^2 = C_L V_{dd}^2. \quad (1)$$

From the above equation, the energy consumption in conventional CMOS can be reduced by reducing the supply voltage V_{dd} and/or the load capacitance C_L. If we focus on the power consumption of the circuit, $(P = \frac{dE}{dt})$, the switching activity can be reduced as well.

In recent years, studies on adiabatic computing have been utilized for low-power systems and several adiabatic logic families have been proposed [2]–[8]. However, the diode based logics have several weaknesses such as low output amplitude and power dissipation of diodes at the charging path are observed.

In this paper, we propose a Two-Phase Clocked Adiabatic Static CMOS Logic (2PASCL) circuit. The innovation to reduce energy dissipation is by excluding diodes at the charging path. Therefore, during charging, the current only flows through the transistor. This makes our proposed circuit differ from other diode based adiabatic circuits [6]–[8] in which charging occurs through diode and transistor. Besides achieving higher amplitude, we can also reduce the energy dissipation by this approach. In addition, to minimize the dynamic power consumption, split level sinusoidal driving voltage is applied.

The remainder of this paper has four sections. In Section II we present the structure, operation and simulation results of the performance of our proposed circuit compared to some representative adiabatic inverter logics which are easily converted from CMOS [4]–[8]. Following that, in Section III we propose a new scheme of NAND, NOR and Exclusive-OR gates based on 2PASCL. Discussion on the strength and weakness of 2PASCL is given in Section IV, followed by conclusion in Section V.

II. Two Phase clocked Adiabatic Static CMOS Logic

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter. It resembles the static CMOS logic inverter but operates in a nearly adiabatic fashion. The first difference between 2PASCL and static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the nMOS logic to another power clock. Both MOSFET-diodes are used to recycle the charges from the output node, to improve discharging speed of internal signal nodes. This is especially advantageous for signal nodes with a long chain of switches before them.

The other difference is that split-level sinusoidal power clock supplies, ϕ and $\overline{\phi}$ are used to replace the V_{dd} and the V_{ss}. Substrate of pMOS is connected to ϕ whereas for nMOS, it is connected to $\overline{\phi}$. From the simulation, we found that split-level sinusoidal gives a lower energy dissipation compared to trapezoidal power clock supply even if we set the T_{rise} and T_{fall} of the trapezoidal waveforms to maximum values. By using two split-level sinusoidal waveforms where each peak-to-peak is 0.9 V, we can reduce the voltage difference, thus reducing the charging and discharging activities. Sinusoidal waveforms can also be generated with higher energy efficiency than trapezoidal waveforms [6].

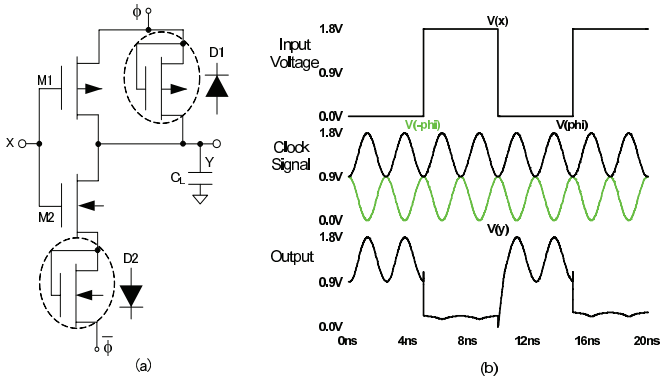

Fig. 1. (a) 2PASCL inverter circuit and (b) the simulated waveforms; (top) input signal X=100 MHz, (center) $V_\phi = V\overline{\phi}$ = 400 MHz, (bottom) the output waveforms.

The operation of 2PASCL is as follows. Let us consider the inverter logic circuit demonstrated in Fig. 1. The circuit operation phase is divided into *evaluation* and *hold* phase as shown in Fig. 2. *Evaluation* phase is when the voltage driver ϕ swings up and $\overline{\phi}$ swings down The opposite, *hold* is when $\overline{\phi}$ swings up and ϕ swings down.

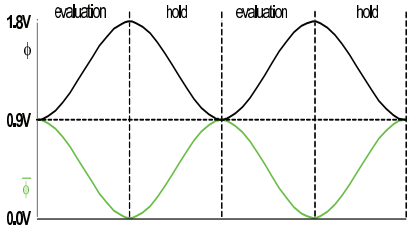

Fig. 2. Clocked voltage driver showing the *evaluation* and *hold* phase.

In *evaluation* phase, when the output node Y is LOW and pMOS tree is turned ON, C_L is charged through pMOS transistor resulting in the HIGH state at the output. When Y is LOW and nMOS is ON, no transition occurs. The same result is gained when the output node is HIGH and pMOS is ON. Finally, when Y node is HIGH and nMOS is ON, discharging via nMOS and D2 resulting in the decrease of output voltage to V_t value where the logical state is "0" [8].

At *hold* phase, due to the diodes, the state of Y when preliminary state is LOW remains unchanged. When the preliminary state of the output node is HIGH, it will change to V_t, the threshold voltage of the diode. At this point, discharging via diode D1 occurs.

From the operation of 2PASCL as explained in *evaluation* and *hold* phase, less dynamic switchings are observed as circuit nodes are not necessarily charging and discharging every clock cycle which reduces the node switching activities significantly. The lower the switching activity the lower its energy dissipation will be.

A. Adiabatic logic inverter circuits comparison

The paper starts by examining the functional and energy dissipation of a simple logic gate, an inverter of 2PASCL as shown in Fig. 1. Then, we evaluate by simulation the functional and energy dissipation results of basic adiabatic logic inverters which are easily converted from CMOS. The representative circuits are 1n1p [4], 1n1p with split-level driving pulse [5], Quasi-Static Energy Recovery Logic (QSERL) [6], Adiabatic Dynamic CMOS Logic (ADCL) [7] and 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL) [8]. We also include conventional static CMOS in the simulation. All the circuits are simulated for their energy dissipation at transition frequencies varying from 10 to 100 MHz.

1) Condition of simulation: We use SPICE simulation with a 0.18 μm, 1.8 V standard CMOS process. The W/L of nMOS and pMOS logic gates used is 0.6 μm/0.18 μm. A capacitive load C_L, of 0.01 pF is placed at output node Y. The power supply clock frequencies are set to be 4 times higher than the transition frequency after considering energy dissipation results. Using a pair of split-level sinusoidal power clock driving voltages of 0.9 V peak-to-peak, the result at 100 MHz transition frequency of 2PASCL inverter is shown in Fig. 1. For other adiabatic inverters, the results are shown in Figs. 3–7. On the right side of each inverter schemes, the top graph shows the input signals which are CMOS-compatible rectangular pulses. The second graph demonstrates the voltage driver supply clock. The third graph shows the output waveform of a correctly functioning inverter which is simulated using SPICE.

The energy dissipation is calculated by integrating the voltage and current product value as follows:

$$E = \int_0^{T.} \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt, \qquad (2)$$

where T_s is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current and n is the number of power supply [8]. The energy in joule is then converted to watt by multiplying it with the input frequency.

2) Simulation results: From the simulation results, the inverter function of the adiabatic circuits and conventional static CMOS has been confirmed. All the input waveforms, clocked driving voltages and the output graphs are shown in Figs. 3–7.

The energy dissipation of our proposed 2PASCL, other adiabatic circuits and static CMOS at transition frequencies

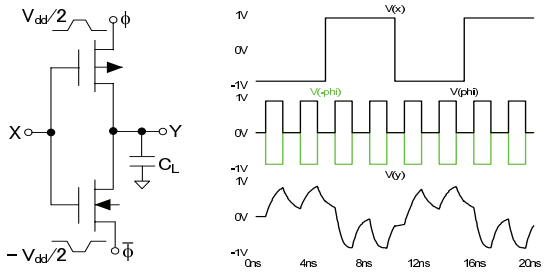

Fig. 3. 1n1p Split Level Pulse (SLP) inverter and waveforms from the simulation.

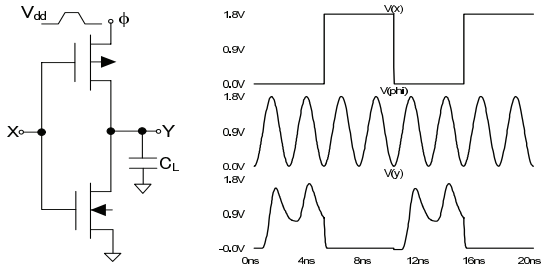

Fig. 4. 1n1p quasi inverter and waveforms from the simulation.

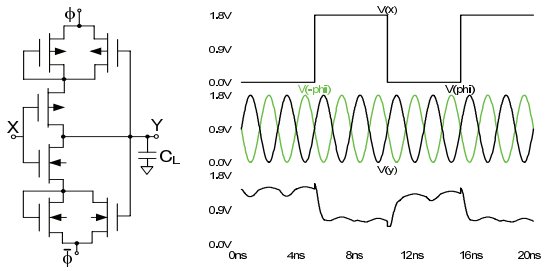

Fig. 5. QSERL inverter and waveforms from the simulation.

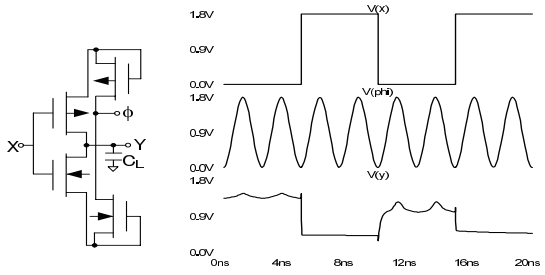

Fig. 6. ADCL inverter and waveforms from the simulation.

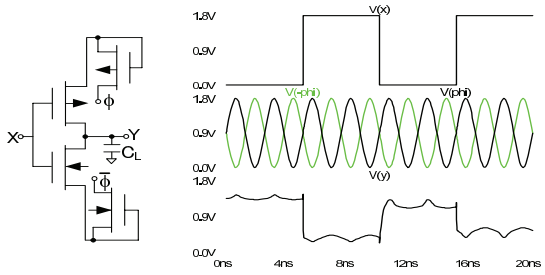

Fig. 7. 2PADCL inverter and waveforms from the simulation.

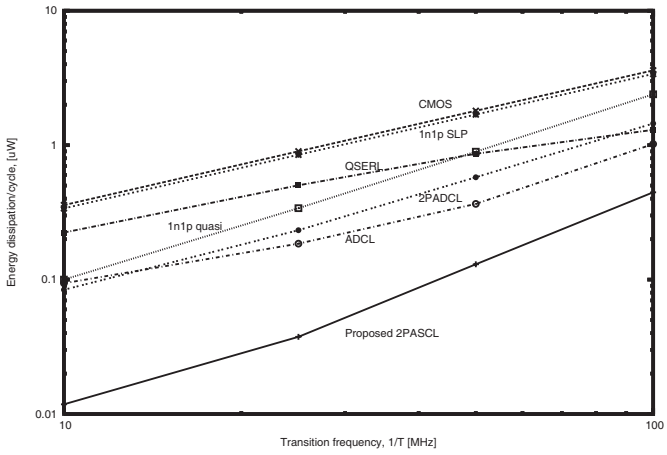

Fig. 8. Energy dissipation comparison for inverter logics.

of 10 to 100 MHz are shown in Fig. 8. From the results, 2PASCL based inverter gives the lowest energy dissipation per cycle. It can save up to 97% of the power dissipated from CMOS inverter. The nearest adiabatic circuit in terms of power dissipation to 2PASCL inverter is ADCL which dissipates 28% more than 2PASCL.

III. Application of Combination Circuits

A. Simulation condition

Next, we simulate the other logic gates implemented with 2PASCL. The schematic for NAND, NOR and exclusive-OR logic circuits are shown in Figs. 9, 10 and 11 respectively. Input signals values of a/b of (0101)/(0110) are applied. Two-phase split-level sinusoidal voltage drivers power clock of ϕ and $\overline{\phi}$ are utilized for the simulation. The output of the proposed logic gates are recorded from Y.

B. Simulation results

The logic functions of these fundamental logics based on 2PASCL have been observed where the circuits are confirmed to operate accordingly as shown on the right side of each figures.

IV. Discussion

All substrate voltages of 2PASCL based circuits simulated in this paper are as follows. For pMOS, the bulks are connected to ϕ. The substrates of nMOS are connected to $\overline{\phi}$. From our simulation result, only 1.6% lower energy achieved in 2PASCL inverter compared to the bulks connected to V_{dd} and V_{ss}. Since the difference is low, we are suggesting that both ϕ, $\overline{\phi}$ and V_{dd}, V_{ss} can be used for the substrate voltage connection. However, for application such as register, the bulks need to be connected to only V_{dd} and V_{ss}.

By taking lower power dissipation as its strength, the weakness of 2PASCL is related to output floating associated with the alternate hold phases in operation. Further analysis will be carried out in the future to solve these two phase clocking related problems.

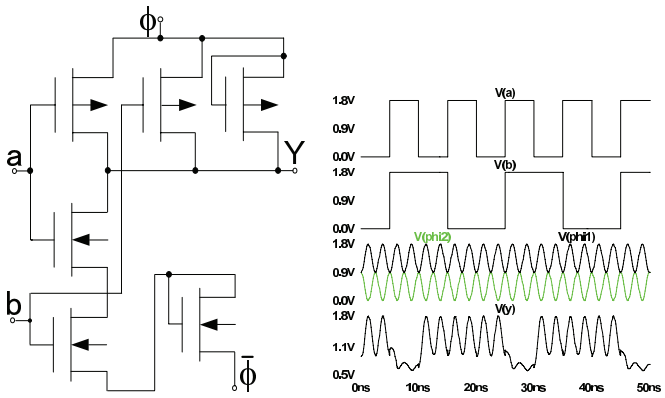

Fig. 9. Scheme for 2PASCL based NAND logic (left), waveforms from the simulation where the output $Y = \overline{a \cdot b}$ (right).

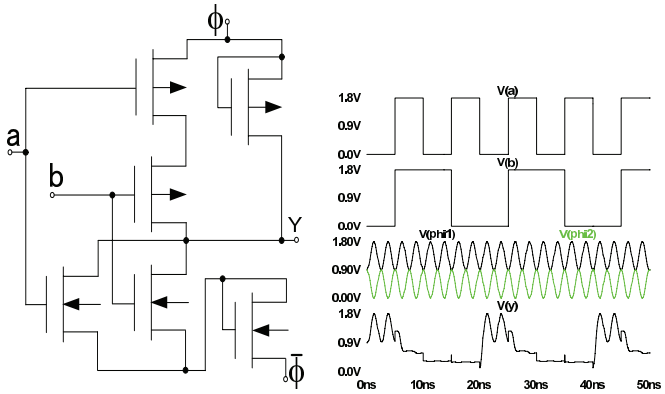

Fig. 10. Scheme for 2PASCL based NOR logic (left), waveforms from the simulation where the output $Y = \overline{a + b}$ (right).

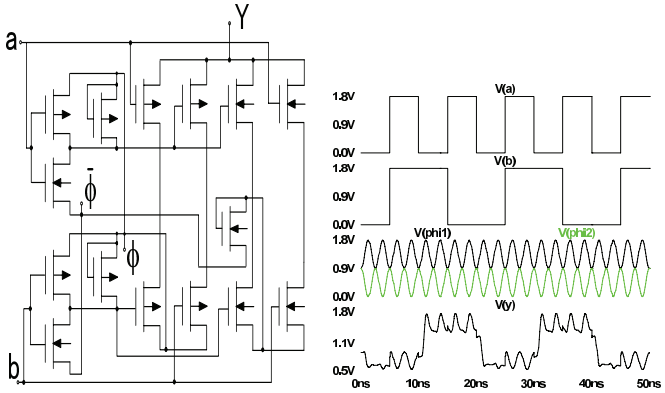

Fig. 11. Scheme for 2PASCL based ExOR logic (left), waveforms from the simulation where the output $Y = a \oplus b$ (right).

V. Conclusion

This paper has described a simulation of Two-Phase clocked Adiabatic Static CMOS Logic (2PASCL). By implementing the adiabatic charging and energy recovery theory, 2PASCL inverter gives the lowest result in energy dissipation of all the simulated adiabatic inverters and CMOS. The enery dissipation measurement by SPICE program for other logic gate such as inverter chain [9] has also proved that this approach lowers the energy dissipation. The design principle can also be used for designing more complicated adiabatic CMOS circuits and its logic schemes can be a viable candidate for ultra-low energy computing.

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