Aleš Chvála[1]
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic
e-mail: ales.chvala@stuba.sk

Robert Szobolovszký
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Jaroslav Kováč, Jr.
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Martin Florovič
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Juraj Marek
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Ľuboš Černaj
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Daniel Donoval
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Jaroslav Kováč
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava,
Ilkovičova 3,
Bratislava 812 19, Slovak Republic

Christian Dua
III-V Lab,
1 Avenue Augustin Fresnel,
Palaiseau 91767, France

Sylvain L. Delage
III-V Lab,
1 Avenue Augustin Fresnel,
Palaiseau 91767, France

Jean-Claude Jacquet
III-V Lab,
1 Avenue Augustin Fresnel,
Palaiseau 91767, France

Advanced Characterization Techniques and Analysis of Thermal Properties of AlGaN/GaN Multifinger Power HEMTs on SiC Substrate Supported by Three-Dimensional Simulation

In this paper, several methods suitable for real time on-chip temperature measurements of power AlGaN/GaN-based high-electron mobility transistor (HEMT) grown on a SiC substrate are presented. The measurement of temperature distribution on HEMT surface using Raman spectroscopy is presented. The second approach utilizes electrical I–V characteristics of the Schottky diode neighboring to the heat source of the active transistor under different dissipated power for temperature measurement. These methods are further verified by measurements with microthermistors. The features and limitations of the proposed methods are discussed. The thermal parameters of materials used in the device are extracted from the temperature distribution in the structure with the support of three-dimensional thermal simulation of the device. Thermal analysis of the multifinger power HEMT is performed. The effects of the structure design and fabrication processes from semiconductor layers, metallization, and packaging up to cooling solutions are investigated. The influence of individual layer properties on the thermal performance of different HEMT structures under different operating conditions is presented. The results show that the proposed experimental methods supported by simulation have a potential for the design, analysis, and thermal management of HEMT. [DOI: 10.1115/1.4043477]

[1]Corresponding author.
Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received October 26, 2018; final manuscript received March 1, 2019; published online May 17, 2019. Assoc. Editor: Przemyslaw Gromala.

1 Introduction

Recent progress in GaN-based high-electron mobility transistors (HEMTs) has confirmed them to be the main transistor technology for upcoming high-power devices at high-frequency operation because of their excellent electronic properties, especially high-electron saturation velocity, and high breakdown voltage [1–6]. Multifinger devices with a compact layout are required for high-power operation. However, self-heating-induced thermal crosstalk between individual gate fingers can become a significant issue that degrades device performance or can even result in an irreversible damage. Therefore, thermal management is crucially important to the viability of power HEMTs [7–11]. Lower structure temperature improves the power efficiency and increases the reliability of the device.

In the past, a lot of work was carried out to reduce the device self-heating by improving device geometry and material thermal properties. The GaN-based heterostructure is usually grown on sapphire, Si or SiC substrates [12]. However, low-thermal conductance is a major disadvantage for sapphire and Si substrates. The high-thermal conductivity of SiC provides the favorable performance for power HEMTs. Another promising material is isotope-enriched SiC with at least 18% higher thermal conductivity than natural SiC. However, the high-production cost and scaling problems cause that there are still a lot of areas to be investigated [13]. In Ref. [14], the authors focused on the analysis of different types of buffers and SiC substrate implantations to improve the thermal performance of HEMTs.

Experimental temperature measurements are essential for complex characterization of these devices. Temperature is one of the dominant drivers of device degradation and has a substantial influence on the device. Therefore, accurate device temperature characterization is very important to reach reliability and good performance of the device. Among all techniques, micro-Raman thermometry is one of the most popular for this purpose [15–17], along with the electrical parameter-based thermometry [18]. Compared to an infrared technique with low-spatial resolution of about 5–10 μm, micro-Raman thermometry has a spatial resolution better than 1 μm [19]. It can be convenient to profile micrometer-sized source/drain openings in HEMTs. However, the micro-Raman technique can only be used for open or window-packaged devices without metal air bridges between the source/drain fingers or source/gate field plates.

Another common approach to determine the chip temperature is by integration of on-chip sensors. The well-known temperature-dependent characteristics of a pn junction are used in many works for Si devices, e.g., see Refs. [20–23]. The electrothermal dependence of the pn junction is very sensitive and mostly linear. Therefore, the pn junction is often utilized as a temperature sensor. For the GaN-based devices the Schottky diode can be used instead of the pn junction [24,25].

In this paper, we present several methods for temperature measurements of power HEMTs. The investigation uses micro-Raman spectroscopy and neighboring Schottky diode electrical measurement. The Raman shift and Schottky voltage at a constant forward current are directly proportional to the temperature. The results are validated by microthermistor measurements. These methods are used for extraction and calibration of the material thermal coefficients for the three-dimensional (3D) thermal simulation. Subsequently, the thermal analysis of multifinger power HEMTs at stationary and pulse operating modes is performed. The analysis is supported by 3D device simulations as a highly useful and effective tool for the analysis and characterization of the electrothermal behavior of power HEMTs. The effects of the structure design and fabrication processes from semiconductor layers, metallization, and packaging up to cooling assemblies are studied.

2 Structure Description

The structure under investigation is a 1.5 nm GaN-cap/14.5 nm $Al_{0.29}Ga_{0.71}N$-barrier/50 nm GaN-spacer/1650 nm GaN-doped heterostructure grown on 500 μm 4H-SiC substrate. Figure 1 depicts the two-dimensional (2D) cross section of the structure. The backside 5-μm thick Au substrate contact is soldered to a 1000-μm thick CuMo leadframe by a 25-μm thick AuSn solder. Top ohmic drain/source and gate contacts are created by Au-based metallization layers with thicknesses of 0.5 μm and 0.6 μm, respectively. The structure is set in an open package placed on a cooler (Fig. 2).

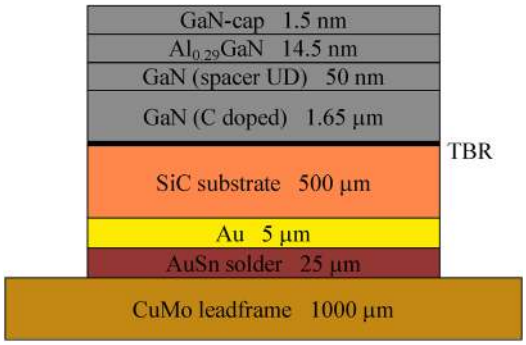

Fig. 1 Two-dimensional cross section of the analyzed AlGaN/GaN heterostructure grown on SiC substrate and soldered to CuMo leadframe

3 Methods for Temperature Extraction

A gated transmission line method (GTLM) topology (Fig. 2) is used for electrothermal characterization. The first transistor (D1-G1-S1) in GTLM topology is used as a heat source. Several

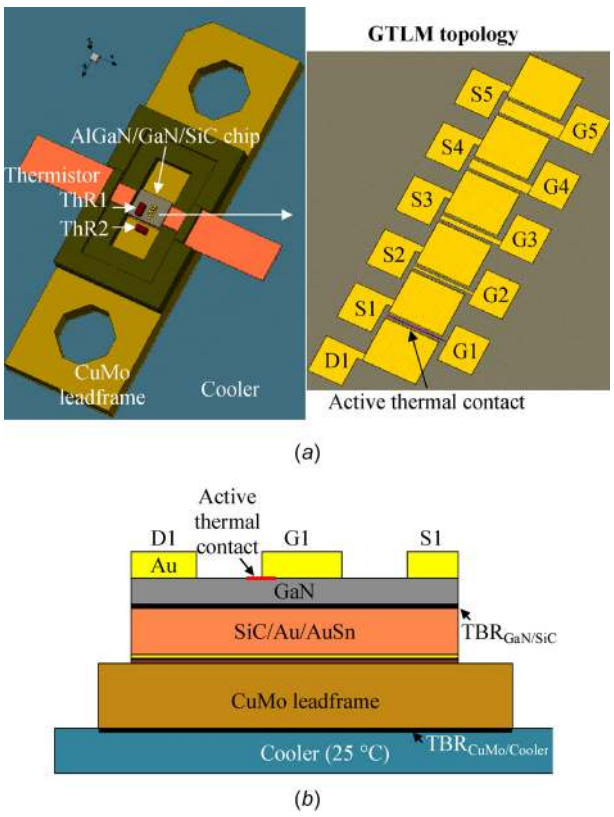

Fig. 2 (*a*) Three-dimensional thermal model of the structure with GTLM topology set in open package. Micro thermistors ThR1 and ThR2 are attached on the chip and the leadframe, respectively. (*b*) Schematic (not to scale) of 2D cross section of the model with depicted thermal interfaces and boundary conditions.

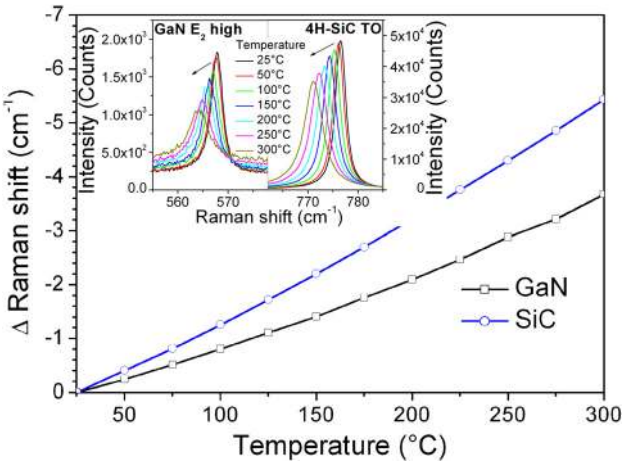

Fig. 3 Raman spectra at different temperatures and GaN E_2 high and 4H-SiC to phonon peak shift dependence on the temperature

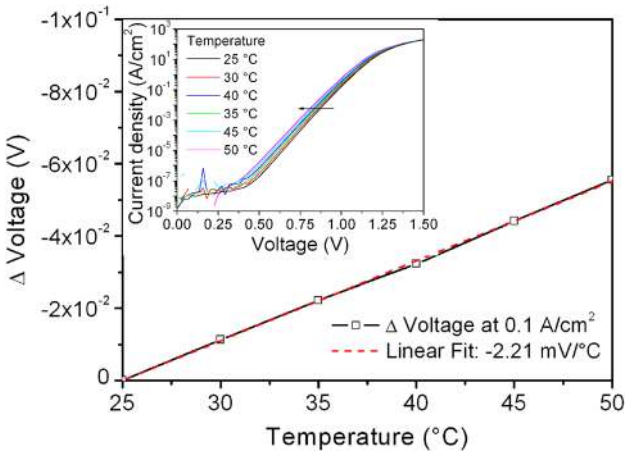

Fig. 4 Static *I–V* characteristics of the Schottky diode at different temperatures and calibration curve of voltage deviation as a function of temperature

experimental methods are proposed and evaluated for extraction of structure temperature at different positions.

3.1 Micro-Raman Thermometry. The MonoVista 750 CRS system with laser excitation wavelength of 514 nm was used for Raman spectra recording. In the first step, calibration measurements were carried out to obtain the Raman shift of GaN and SiC phonons as a function of absolute temperature. These measurements were performed on a temperature-controlled chuck in a chamber. The measured GaN E_2 high and 4H-SiC TO phonon locations are $\sim 568\,cm^{-1}$ and $\sim 776\,cm^{-1}$ at room temperature, respectively [26]. The obvious exponential relation between the Raman shift and the temperature of the device is plotted in Fig. 3. This measurement was used as a calibration for determining the absolute temperature at specific locations of the device under operation. Subsequently, the measurements were performed at various locations for different dissipated power of the active HEMT device. The piezoelectric stress which can be present due to the applied biases is neglected because it is not strong enough to exhibit a measurable difference [27].

3.2 Schottky Diode. This proposed method is based on temperature sensitive parameters of neighboring Schottky diodes to determine the device temperature at various positions. The first transistor (D1-G1-S1) in GTLM topology is used as a heat source. The rest of the transistors use only gates and sources to utilize the Schottky diodes (G2-S2, G3-S3, G4-S4, and G5-S5). In the first step, a calibration measurement of Schottky diodes at defined temperatures was performed. The voltage difference for a constant current density of $0.1\,A/cm^2$ at forward bias is directly proportional to the temperature (Fig. 4). Subsequently, the first transistor was connected to the power supply to generate heat. The temperature of particular diodes at distinctive positions as a function of dissipated power at the first transistor is obtained by temperature calibration of the Schottky diodes. The applied current ($0.1\,A/cm^2$) is low on the sensing diodes to prevent their self-heating.

3.3 Thermistor. MURATA NCP03WB473J05RL [28] microthermistor was used for direct temperature evaluation of the device. The thermistor has a very high accuracy ($\sim$3%). However, the thermistor dimension is large compared to the GTLM topology. Therefore, only one thermistor (ThR1) was placed on the chip near the active HEMT using thermal glue. A second thermistor (ThR2) was attached to the leadframe near the chip. These thermistors were used to validate the previously described methods and determine the heat transfer from the chip to leadframe through the solder interface.

4 Three-Dimensional Model Description and Experimental Validation

The 3D model of the structure for thermal simulation based on the physical and geometrical description of all semiconductors, metallization layers, and package corresponding to the real device is created in Sentaurus Device Editor [29] (Fig. 2). Three-dimensional thermal simulations are performed in Sentaurus Device tool [29]. A few nm thick GaN-cap and AlGaN barrier layer are neglected in the model due to their minimal impact on the thermal simulations. The dissipated electrical power that results in thermal heating is modeled by a heat source placed under the gate electrode edge at the drain side, where the heat generation occurs during the on-state operation of the device [30,31]. Boundary condition with a constant temperature of 25 °C is set on the structure backside. This represents an ideal heat transfer to the Peltier-cooled aluminum plate. The material thermal coefficients for the structure model and thermal boundary resistance (TBR) of the interfaces are taken from the literature and subsequently calibrated and validated using the above described methods. The values are evaluated from the measured temperature distribution on the chip. The thermal coefficients for the materials in the structure are listed in Table 1. The thermal boundary resistance is set to $1 \times 10^{-4}\,cm^2\,KW^{-1}$ at the GaN/SiC interface [40]. TBR value of $2\,cm^2\,KW^{-1}$ is set at the CuMo leadframe/cooler interface.

Figure 5 shows the simulated structure temperature distribution for applied power 2 W in the active D1-G1-S1 HEMT. Comparison of the measured and simulated temperatures of Raman G1-D1 position, Schottky contacts G2-S2—G4-S4, and thermistors ThR1 and ThR2 at different powers of the active D1-G1-S1 HEMT is shown in Fig. 6(*a*). Figure 6(*b*) shows the temperature distribution

Table 1 Thermal conductivity values calibrated and used in the simulation

Material		Thermal conductivity ($W\,m^{-1}\,K^{-1}$)
Au		310 [32]
AlGaN		$40 \times (T/298)^{-1.37}$ [33]
GaN (C doped)		$190 \times (T/298)^{-1.37}$ [34]
4H-SiC	*xy*-axis	$430 \times (T/298)^{-1.5}$ [35–37]
	z-axis	$370 \times (T/298)^{-1.5}$
AuSn		57 [38]
CuMo		160 [39]

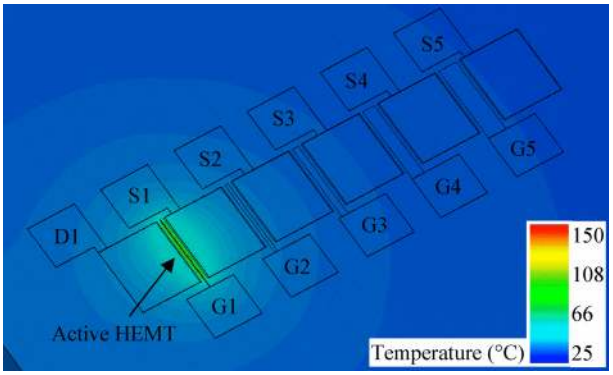

Fig. 5 Simulated temperature distribution in the structure for dissipated power of 2 W at the active D1-G1-S1 HEMT

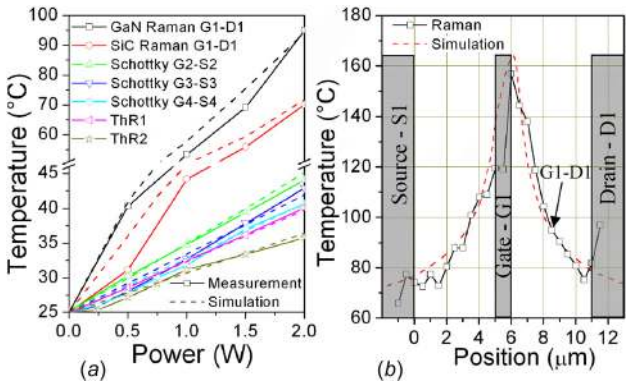

Fig. 6 Comparison of the measured and simulated (*a*) temperatures of Raman G1-D1 position, Schottky contacts G2-S2—G4-S4, and thermistors ThR1 and ThR2 at different powers of the active D1-G1-S1 HEMT and (*b*) temperature distributions across the active D1-G1-S1 HEMT for 2 W

across the active HEMT. Very good agreement between simulations and experimental results confirms the validity of the proposed methodologies and model parameters.

5 Thermal Analysis of Power High-Electron Mobility Transistors

After calibrating the thermal properties, the analysis of power multifinger HEMTs was performed. The previously described structure with different thicknesses of SiC substrate and CuMo leadframe is used. The SiC substrate is usually grinded and polished to a lower thickness for the final assembly. Moreover, the chip is soldered to a package with a thinner leadframe to improve heat transfer to the heat sink. Therefore, a 100 μm-thick SiC substrate and a 300 μm-thick CuMo leadframe are used for the analysis. Two different HEMT topologies with 2 and 50 gate fingers were investigated (Fig. 7). It has to be noted that the gate pitches and elementary widths are different for the two topologies (Table 2). Simulations were focused on the thermal characterization of both HEMT structures behavior under different operating conditions. Subsequently, these results were exploited for explaining the structure design impact on the thermal properties of HEMTs.

Figure 8(*a*) shows the temperature distribution under gate at stationary (CW) and pulse (5 ms and 5 μs) operating modes for dissipated power 15 W/mm and 4 W/mm for 2- and 50-gate HEMT, respectively. In the case of the larger structure with 50 gate fingers, thermal crosstalk between the gate fingers and higher active area dimensions reduce the lateral heat spreading and power dissipation capability [41]. Moreover, the reduced lateral

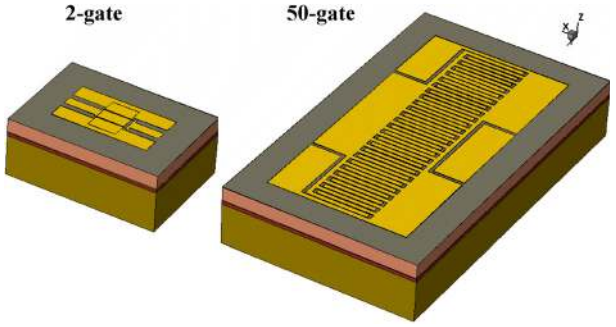

Fig. 7 Layout and structure of investigated 2- and 50-gate HEMT

Table 2 Device geometry of 2- and 50-gate fingers HEMT

Topology	2-gate	50-gate
Number of elementary gates	2	50
Gate length	0.5 μm	0.7 μm
Elementary gate width	200 μm	400 μm
Total gate width	400 μm	20 mm
Gate pitch	100 μm	40 μm

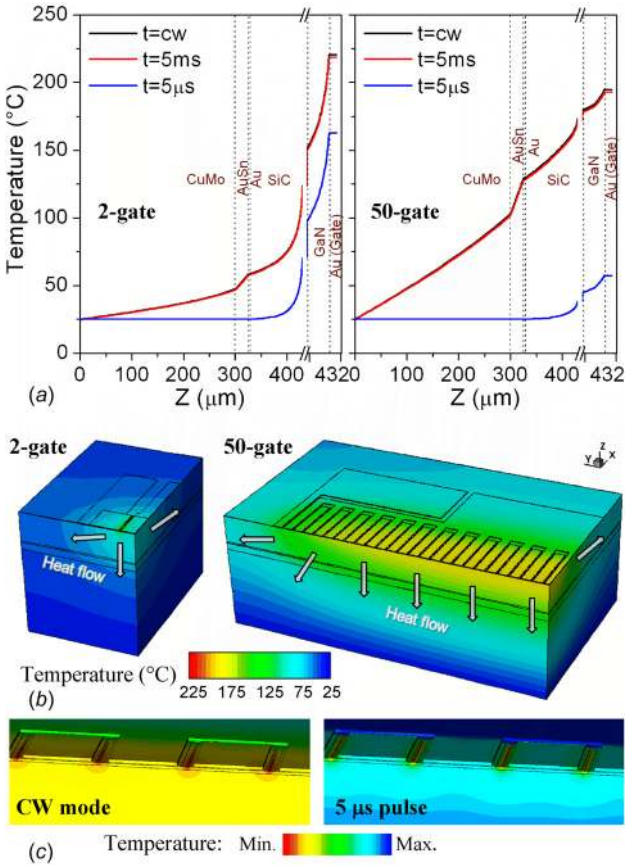

Fig. 8 (*a*) Temperature distribution under gate at CW, 5 ms, and 5 μs for dissipated power 15 W/mm and 4 W/mm for 2- and 50-gate HEMT, respectively. (*b*) Temperature distribution inside HEMT structures at steady-state. Reduced lateral heat flow increases temperature in the vertical direction for 50-gate structure compared to the 2-gate structure. (*c*) Temperature distribution inside HEMT structures at CW and time 5 μs.

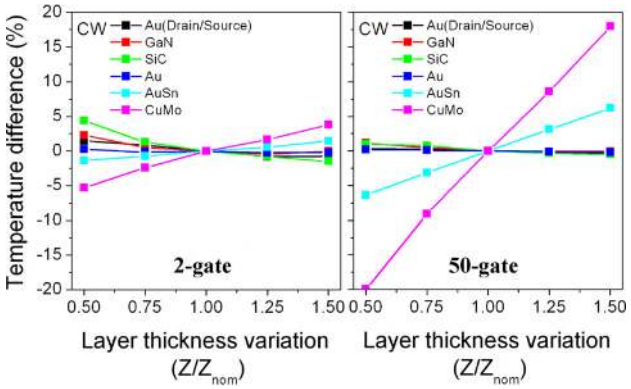

Fig. 9 Influence of layers thickness on HEMT temperature at steady-state

heat flow increases the temperature in the vertical direction compared to the 2-gate structure (Fig. 8(*b*)). For the CW and 5 ms pulse, it is visible that the highest temperature gradient and resulting highest heat dissipation occurs in the top layers (GaN and SiC) for the 2-gate structure while the temperature gradient is more uniformly distributed for the 50-gate device. The highest dissipated heat is mainly distributed in the bottom layers (MoCu and AuSn) for the 50-gate structure. Thermal crosstalk between the gate fingers is lower for short pulses (5 μs), and temperature is much more reduced mainly for the 50-gate HEMT (Fig. 8(*c*)).

After characterization of both HEMTs behavior, the analysis of influence of particular layers geometry and their thermal parameters on HEMTs thermal properties and behavior at different pulse widths was performed. The investigated variables are the thickness of layers Z and their thermal conductivities κ. Figures 9 and 10 show the influence of layers thickness and thermal conductivity on HEMT temperature difference at a steady-state, respectively. The temperature difference is calculated as a percentage ratio of the maximum temperature for the investigated structure and a structure with nominal parameters (Z_{nom} and κ_{nom}).

Lowering the higher thermal resistive CuMo and AuSn layer thickness decreases the HEMT temperature due to a better heat transfer to the bottom heat sink. Because of the dominant vertical heat flow in the 50-gate HEMT, the impact of these layers on temperature is more significant compared to the 2-gate HEMT. Thinner SiC and GaN layers reduce the lateral heat flow, increase the vertical heat flow through low conductive AuSn and TBR layers (Fig. 11), and consequently increase the HEMT temperature. As observed for the 50-gate HEMT, the reduced lateral heat flow diminishes the impact of SiC and GaN layer thickness on the temperature compared to 2-gate HEMT. Increasing the thickness of Au drain/source layers allows better cooling of the HEMT

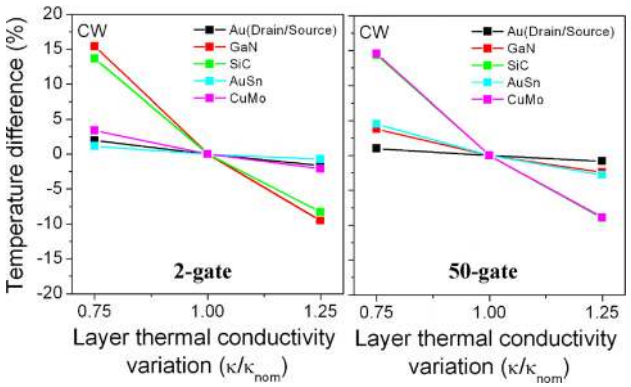

Fig. 10 Influence of layers thermal conductivity on HEMT temperature at steady-state

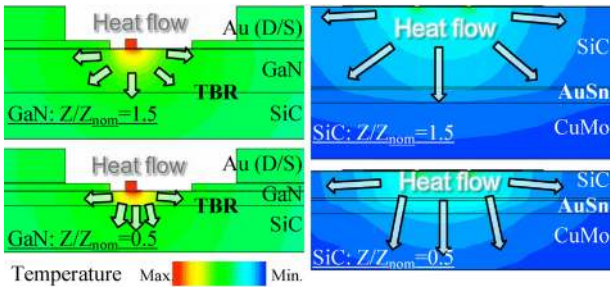

Fig. 11 Temperature distribution and heat flow inside HEMT structures for various thicknesses of SiC and GaN layers

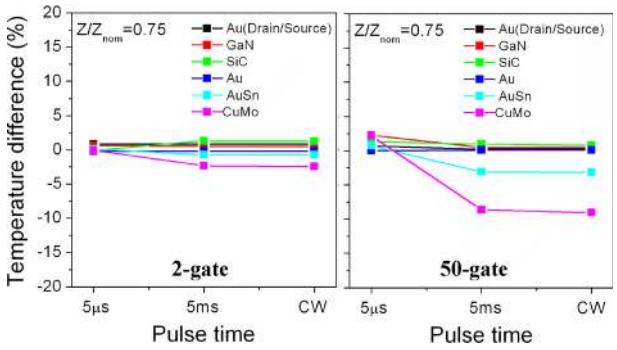

Fig. 12 Influence of layers thickness on HEMT temperature at different pulse time

through the top metallization, and therefore, slightly decreases the HEMT temperature.

Higher thermal conductivity of all layers decreases HEMTs temperature (Fig. 10) due to the better heat transfer to the bottom heat sink. For example, isotopic SiC with 18% higher thermal conductivity than natural SiC reaches about 6% and 6.5% lower temperature for 2- and 50-gate HEMT, respectively. GaN thermal conductivity has a dominant impact in the 2-gate HEMT due to a higher lateral heat flow in the top layers. For 50-gate HEMT, the influence of the GaN thermal conductivity on the temperature is significantly lower due to its higher vertical heat flow. For the same reason, the impact of the AuSn solder thermal conductivity is slightly higher and the thermal conductivity of the CuMo leadframe becomes the most dominant. Influence of the SiC substrate is similar for both structures.

Figures 12 and 13 show the influence of layers thickness and layers thermal conductivity on the HEMT temperature difference at different pulse times. As shown in Fig. 8, the heat flow is dissipated in a short distance from the thermal source (gate) for short

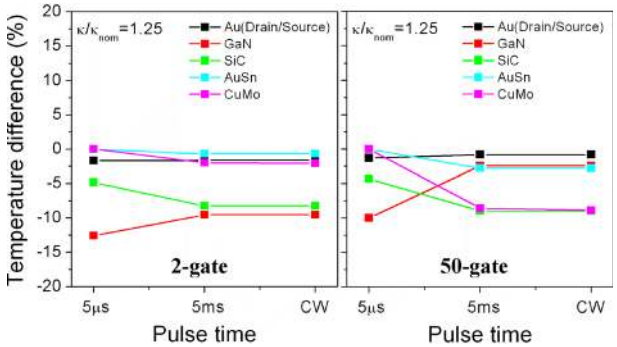

Fig. 13 Influence of layers thermal conductivity on HEMT temperature at different pulse time

pulses. This reduces the influence of the thickness of deeper layers (mainly CuMo, AuSn, and SiC) on the device temperature (Fig. 12, 5 μs pulse). Similarly, thermal conductivity of these layers has a weaker impact on the temperature difference (Fig. 13, 5 μs pulse). Conversely, thermal conductivity of the top GaN layer has significant impact on temperature difference for short pulses (5 μs).

6 Conclusions

Several methods for on-chip temperature measurements of power AlGaN/GaN HEMTs grown on SiC substrate were presented. The device material thermal coefficients have been extracted from structure temperature distribution measured by micro-Raman spectroscopy, neighboring Schottky diode electrical measurement, and microthermistor measurement with the support of 3D simulation. Very good agreement between simulations and experimental results confirms the validity of the proposed methodologies and the model parameters. The well calibrated 3D device model was used for thermal analysis of the multifinger power HEMT. Different behavior has been observed, discussed, and explained for two HEMT structures. The influence of layers properties on the structure behavior was investigated as well. The simulation results of well-calibrated model show particular impacts of individual layer properties on the thermal performance of different HEMT structures at different operating conditions. For example, the isotopic SiC substrate can reduce the structure temperature by about 6%. GaN buffer thermal conductivity is important only for low power HEMTs or short power pulses. Soldering and packaging also play a key role. The thermal analysis can help during design and optimization of power HEMTs. These observations contribute to the on-going optimization of power transistor structures in respect to the geometry of layers design and their thermal parameters.

Acknowledgment

The research leading to these results has received funding from the Electronic Component Systems for European Leadership (ECSEL) Joint Undertaking (JU) under grant agreement No 662322, project OSIRIS. This Joint Undertaking receives support from the European Union's Horizon 2020 Research and Innovation Program and France, Norway, Slovakia, and Sweden. This work has also received funding from the ECSEL JU under grant agreement No 783274, project 5G_GaN2. The JU receives support from the European Union's Horizon 2020 Research and Innovation Program and France, Germany, Slovakia, Netherlands, Sweden, Italy, Luxembourg, Ireland. This work was also supported by Grant VEGA 1/0630/19 supported by Ministry of Education, Science, Research and Sport of Slovakia.

Funding Data

- Electronic Components and Systems for European Leadership (Grant No. 662322; Funder ID: 10.13039/501100011688).
- European Union (Funder ID: 10.13039/501100000780).
- Ministry of Education, Science, Research and Sport of Slovakia (Grant No. VEGA 1/0630/19; Funder ID: 10.13039/5011100003193).

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