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978-0-521-86581-4 - Advanced Model Order Reduction Techniques in VLSI Design

Sheldon X. - D. Tan and Lei He

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Advanced Model Order Reduction Techniques in VLSI Design

Model order reduction (MOR) techniques are important in reducing the complexity of nanometer VLSI designs, and consequently controlling “parasitic” electromagnetic effects, so that higher operating speeds and smaller feature sizes can be achieved. This book presents a systematic introduction to, and treatment of, the key MOR methods used in general linear circuits, using real-world examples to illustrate the advantages and disadvantages of each algorithm.

Starting with a review of traditional projection-based techniques and proofs of some fundamental theories, coverage progresses to advanced “state-of-the-art” MOR methods for VLSI design. These include HMOR, passive truncated balanced realization (TBR) methods, efficient inductance modeling via the VPEC model, general model optimization and passivity enforcement methods, passive model realization techniques, and structure-preserving MOR techniques. Numerical methods have been used throughout and, where possible, approached from the CAD engineer’s perspective. This avoids complex mathematics, and allows the reader to take on real design problems and develop more effective tools.

With practical examples and over 100 illustrations, this book is suitable for researchers and graduate students of electrical and computer engineering, as well as for practitioners working in the VLSI design and design automation industries.

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Contents

<i>Contents</i>	<i>page</i>	<i>v</i>
<i>Figures</i>		<i>viii</i>
<i>Tables</i>		<i>xiv</i>
<i>Foreword</i>		<i>xv</i>
<i>Acknowledgments</i>		<i>xvii</i>
1 Introduction		1
1.1 The need for compact modeling of interconnects		1
1.2 Interconnect analysis and modeling methods in a nutshell		2
1.3 Book outline		4
1.4 Summary		7
2 Projection-based model order reduction algorithms		8
2.1 Moments and moment-matching methods		8
2.2 Moment computation in MNA formulation		11
2.3 Asymptotic waveform evaluation		13
2.4 Projection-based model order reduction methods		20
2.5 Numerical examples		32
2.6 Historical notes		32
2.7 Summary		34
2.8 Appendices		34
3 Truncated balanced realization methods for MOR		37
3.1 Introduction		37
3.2 The singular value decomposition (SVD)		38
3.3 Proper orthogonal decomposition (POD)		38
3.4 Classic truncated balanced realization methods		39
3.5 Passive-preserving truncated balanced realization methods		43
3.6 Hybrid TBR and combined TBR-Krylov subspace methods		45
3.7 Empirical TBR and poor man's TBR		45
3.8 Computational complexities of TBR methods		47
3.9 Practical implementation and numerical issues		48
3.10 Numerical examples		53
3.11 Summary		54

4	Passive balanced truncation of linear systems in descriptor form	56
4.1	Introduction	56
4.2	The passive balanced truncation algorithm: PriTBR	57
4.3	Structure-preserved balanced truncation	60
4.4	Numerical examples	62
4.5	Summary	64
5	Passive hierarchical model order reduction	67
5.1	Overview of hierarchical MOR algorithm	68
5.2	DDD-based hierarchical decomposition	70
5.3	Hierarchical reduction versus moment-matching	76
5.4	Preservation of reciprocity	80
5.5	Multi-point expansion hierarchical reduction	81
5.6	Numerical examples	84
5.7	Summary	91
5.8	Historical notes on node-elimination-based reduction methods	91
6	Terminal reduction of linear dynamic circuits	93
6.1	Review of the SVD MOR method	95
6.2	Input and output moment matrices	96
6.3	The extended-SVD MOR (ESVD MOR) method	99
6.4	Determination of cluster number by SVD	102
6.5	K-means clustering algorithm	104
6.6	TermMerg algorithm	106
6.7	Numerical examples	111
6.8	Summary	116
7	Vector-potential equivalent circuit for inductance modeling	118
7.1	Vector-potential equivalent circuit	119
7.2	VPEC via PEEC inversion	124
7.3	Numerical examples	128
7.4	Inductance models in hierarchical reduction	131
7.5	Summary	136
8	Structure-preserving model order reduction	137
8.1	Introduction	137
8.2	Chapter overview	138
8.3	Background	139
8.4	Block-structure-preserving model reduction	141
8.5	TBS method	144
8.6	Two-level analysis	149
8.7	Numerical examples	151
8.8	Summary	157
9	Block structure-preserving reduction for RLCK circuits	158

Cambridge University Press

978-0-521-86581-4 - Advanced Model Order Reduction Techniques in VLSI Design

Sheldon X. - D. Tan and Lei He

Frontmatter

[More information](#)

Contents	vii
9.1 Introduction	158
9.2 Block structure-preserving model reduction	159
9.3 Structure preservation for admittance transfer-function matrices	161
9.4 General block structure-preserving MOR method	163
9.5 Numerical examples	167
9.6 Summary	169
9.7 Appendix	170
10 Model optimization and passivity enforcement	172
10.1 Passivity enforcement	172
10.2 Model optimization for active circuits	176
10.3 Optimization for magnitude and phase responses	178
10.4 Numerical examples	181
10.5 Summary	185
11 General multi-port circuit realization	187
11.1 Review of existing circuit-realization methods	187
11.2 General multi-port network realization	195
11.3 Multi-port non-reciprocal circuit realization	197
11.4 Numerical examples	199
11.5 Summary	203
12 Reduction for multi-terminal interconnect circuits	204
12.1 Introduction	204
12.2 Problems of subspace projection-based MOR methods	205
12.3 Model order reduction for multiple-terminal circuits: MTermMOR	208
12.4 Numerical examples	212
12.5 Summary	214
13 Passive modeling by signal waveform shaping	215
13.1 Introduction	215
13.2 Passivity and positive-realness	217
13.3 Conditional passivity and positive-realness	218
13.4 Passivity enforcement by waveform shaping	221
13.5 Numerical examples	225
13.6 Summary	226
<i>References</i>	<i>229</i>
<i>Index</i>	<i>238</i>

Figures

2.1	The network of an ideal delay of T .	9
2.2	The unit impulse and unit step responses.	11
2.3	Block diagram of (2.54).	21
2.4	Arnoldi method based on modified Gram–Schmidt orthonormalization for SISO systems.	25
2.5	Non-symmetric Lanczos method for SISO systems.	26
2.6	Transient response of a non-passive circuit.	29
2.7	Block Arnoldi method for MIMO systems.	31
2.8	A two-port large lumped RCL circuit.	32
2.9	Comparison of the magnitudes of $Y(11)$ for different reduction orders for the lumped RLC circuit.	33
2.10	Comparison of the magnitudes of $Y(12)$ for different reduction orders for the lumped RLC circuit.	33
3.1	Frequency responses of a reduced model and its original system.	54
3.2	Frequency response of the input impedance of a reduced model and its original system.	55
4.1	Frequency responses of TBR, PriTBR, and PRIMA reduced models and the original circuit.	63
4.2	Nyquist plots of the TBR reduced model and the PriTBR reduced model.	64
4.3	Pole zero map of system before mapping.	65
4.4	Frequency responses of PRIMA and combined PRIMA and PriTBR reduced models and the original circuit.	65
4.5	Frequency responses of SPRIM and SP-PriTBR reduced models and the original circuit.	66
5.1	A hierarchical circuit. Reprinted with permission from [126] (c) 2000 IEEE.	68
5.2	A simple RC circuit.	71
5.3	A matrix determinant and its DDD.	71

FIGURES

ix

5.4	Illustration of Theorem 5.1. Reprinted with permission from [122] (c) 2005 IEEE.	72
5.5	A determinant and its YDDD. Reprinted with permission from [122] (c) 2005 IEEE.	73
5.6	Y-expanded DDD construction. Reprinted with permission from [122] (c) 2005 IEEE.	74
5.7	The general hierarchical model order algorithm flow.	76
5.8	Frequency responses of $\mu A741$ circuit under different reduction orders. Reprinted with permission from [94] (c) 2006 IEEE.	78
5.9	Frequency responses of an RC tree circuit under different reduction orders. Reprinted with permission from [94] (c) 2006 IEEE.	79
5.10	Responses of a typical $k_i/(s - p_i)$. Reprinted with permission from [94] (c) 2006 IEEE.	83
5.11	Frequency responses of the three-turn spiral inductor and its reduced model by using waveform matching and the common-pole method. Reprinted with permission from [94] (c) 2006 IEEE.	85
5.12	Colpitts LC oscillator with spiral inductors. Reprinted with permission from [94] (c) 2006 IEEE.	86
5.13	Time-domain comparison between original and synthesized models for a Colpitts LC oscillator with a three-turn spiral inductor. Reprinted with permission from [94] (c) 2006 IEEE.	86
5.14	Frequency responses of Y_{11} of a two-bit transmission line. Reprinted with permission from [94] (c) 2006 IEEE.	87
5.15	Frequency responses of Y_{12} of a two-bit transmission line. Reprinted with permission from [94] (c) 2006 IEEE.	88
5.16	Transient responses of a two-bit transmission line. Reprinted with permission from [94] (c) 2006 IEEE.	89
5.17	Frequency responses of a two-bit transmission line at two ports. Reprinted with permission from [94] (c) 2006 IEEE.	89
6.1	Terminal reduction versus traditional model order reduction.	94
6.2	Frequency responses from SVDMOR and ESVDMOR for <i>net27</i> circuit.	102
6.3	Frequency response from SVDMOR and ESVDMOR with different terminals for <i>net27</i> circuit.	103
6.4	K-means clustering algorithm. Reprinted with permission from [75] (c) 2005 IEEE.	105
6.5	The reduction flow of combined terminal and model order reductions.	107
6.6	Simple interface circuit.	108
6.7	Frequency impedance responses from the SVDMOR method for <i>net1026</i> circuit.	112
6.8	Output terminal distribution for each cluster for <i>net1026</i> circuit. Reprinted with permission from [75] (c) 2005 IEEE.	113
6.9	Step responses of representative output terminals. Reprinted with permission from [75] (c) 2005 IEEE.	114

x FIGURES

6.10	Comparison of 50% delay time among representative output terminals. Reprinted with permission from [75] (c) 2005 IEEE.	114
6.11	Step responses of representative output terminals and two suppressed outputs. Reprinted with permission from [75] (c) 2005 IEEE.	115
6.12	Comparison of 50% delay time among representative output terminals and two suppressed outputs. Reprinted with permission from [75] (c) 2005 IEEE.	115
6.13	Output terminal distribution for each cluster for <i>net27</i> circuit. Reprinted with permission from [75] (c) 2005 IEEE.	116
6.14	Input terminal distribution for each cluster for circuit <i>net38</i> .	117
6.15	Output terminal distribution for each cluster for circuit <i>net38</i> .	117
7.1	(a) Electronic current-controlled vector-potential current source; (b) The Kirchoff current law for vector potential circuit. An invoking vector potential current source is employed at a_i , and the responding vector potential at a_j is A_j^k , determined by the full effective resistance network. Reprinted with permission from [135] (c) 2005 IEEE.	121
7.2	Vector potential equivalent circuit model for three filaments. Reprinted with permission from [135] (c) 2005 IEEE.	123
7.3	For five-bit bus, (a) a 1-V step voltage with 10 ps rising time and (b) a 1-V <i>ac</i> voltage are applied to the first bit and all other bits are quiet. The responses of the PEEC model, full VPEC model, and localized VPEC model are measured at the far end of the second bit. Reprinted with permission from [135] (c) 2005 IEEE.	129
7.4	For 128-bit bus by numerical truncation, a 1-V step voltage with 10 ps rising time is applied to the first bit, and all other bits are quiet. The responses of the PEEC model, the full VPEC model, and the <i>t</i> VPEC model are measured at the far end of the second bit. Reprinted with permission from [135] (c) 2005 IEEE.	130
7.5	Example of a coupled two-bit RLCM circuit under the PEEC model. Reprinted with permission from [135] (c) 2005 IEEE.	132
7.6	Example of a coupled two-bit RLCM circuit under the nodal susceptance model. Reprinted with permission from [135] (c) 2005 IEEE.	133
7.7	Frequency responses of PEEC model in SPICE, susceptance under NA and VPEC models for the two-bit bus. Reprinted with permission from [135] (c) 2005 IEEE.	133
7.8	Stamp of the second-order admittance in the NA matrix, where (a), (b) and (c) represent for G , Γ , C and B . G (rank=4) and Γ (rank=4) are both singular for 6×6 matrices. Reprinted with permission from [135] (c) 2005 IEEE.	134
7.9	Example of a coupled two-bit RLCM circuit under the VPEC model. Reprinted with permission from [135] (c) 2005 IEEE.	135

FIGURES

xi

8.1	Pole matching comparison: m poles matched by TBS and BSMOR, and q poles matched by HiPRIME. Reprinted with permission from [138] (c) 2006 ACM.	150
8.2	Non-zero (nz) pattern of conductance matrices: (a) original system, (b) triangular system, (c) reduced system by TBS. (a)–(c) have different dimensions, but (b)–(c) have the same triangular structure and the same diagonal block structure. Reprinted with permission from [138] (c) 2006 ACM.	151
8.3	Comparison of time-domain responses between HiPRIME, BSMOR, [139], TBS and the original. TBS is identical to the original. Reprinted with permission from [138] (c) 2006 ACM.	152
8.4	Comparison of frequency-domain responses between HiPRIME, BSMOR, TBS, and the original. TBS is identical to the original. Reprinted with permission from [138] (c) 2006 ACM.	153
8.5	Comparison of runtime under similar accuracy. (a) macro-model building time (log scale) comparison; (b) macro-model time-domain simulation time (log scale) comparison. Reprinted with permission from [138] (c) 2006 ACM.	154
8.6	A P/G voltage bounce map without decoupling capacitor allocations. Reprinted with permission from [138] (c) 2006 ACM.	155
8.7	A P/G voltage bounce map with decoupling capacitors allocated at the centers of four blocks. Reprinted with permission from [138] (c) 2006 ACM.	156
9.1	Comparison between SPRIM, PRIMA, and BSPRIM for impedance form.	167
9.2	Sparsity preservation of BSPRIM.	168
9.3	Comparison between PRIMA and structure-preserving algorithm (BSPRIM) for admittance form.	168
9.4	Comparison between PRIMA and BSPRIM with and without re-orthonormalization for admittance form.	169
10.1	Admittance Y_{21} response of the μ A725 opamp without considering phase. Reprinted with permission from [73] (c) 2005 IEEE.	178
10.2	Frequency response of Y_{12} of opamp model. Reprinted with permission from [73] (c) 2005 IEEE.	182
10.3	Active Sallen–Key topology low-pass filter. Reprinted with permission from [73] (c) 2005 IEEE.	182
10.4	Frequency response of Y_{21} of the Sallen–Key topology low-pass filter. Reprinted with permission from [73] (c) 2005 IEEE.	183
10.5	Frequency response of Y_{21} of the Sallen–Key topology low-pass filter without considering phase. Reprinted with permission from [73] (c) 2005 IEEE.	183

xii FIGURES

10.6	Frequency response of the transfer function of the Sallen–Key topology low-pass filter. Reprinted with permission from [73] (c) 2005 IEEE.	184
10.7	Transient response of the Sallen–Key topology low-pass filter with different excitations. Reprinted with permission from [73] (c) 2005 IEEE.	184
10.8	Active low-pass FDNR filter. Reprinted with permission from [73] (c) 2005 IEEE.	185
10.9	Frequency response of the transfer function of the low-pass FDNR filter. Reprinted with permission from [73] (c) 2005 IEEE.	185
10.10	Transient response of the FDNR filter with different excitations. Reprinted with permission from [73] (c) 2005 IEEE.	186
11.1	Realization of $Z(s)$ in (11.2) and $Y(s)$ in (11.3).	189
11.2	Realization of $Z(s)$ in (11.4) and $Y(s)$ in (11.5).	190
11.3	Realization of $Z(s)$ in (11.6).	190
11.4	Real-part responses of $Z(s)$ and the remainder $Z_1(s) = Z(s) - R_{\min}$.	191
11.5	Brune’s driving point synthesis by multiple-stage RLCM ladders (Brune’s cycle).	193
11.6	Brune’s multiple level ladder macromodel synthesis.	193
11.7	Example of Brune’s synthesis with passivity-preserved transformation: the non-passive T circuit is transformed to a passive coupled-inductor circuit.	194
11.8	One-port Foster admittance realization. Reprinted with permission from [94] (c) 2006 IEEE.	196
11.9	General two-port realization II model. Reprinted with permission from [94] (c) 2006 IEEE.	197
11.10	Six-port realization based on II-structure. Reprinted with permission from [94] (c) 2006 IEEE.	198
11.11	General two-port non-reciprocal active realization. Reprinted with permission from [73] (c) 2005 IEEE.	199
11.12	Comparison between the transfer function $Y_{1-port}(s)$ and its circuit realization.	200
11.13	Comparison between the transfer function $Y_{12}(s)$ and its circuit realization.	202
11.14	Comparison between the transfer function $Y_{22}(s)$ and its circuit realization.	202
12.1	Frequency response of the three-input circuit. Reprinted with permission from [76] (c) 2006 IEEE.	207
12.2	Frequency response of the three-input circuit with different approximation. Reprinted with permission from [76] (c) 2006 IEEE.	210
12.3	Comparison of computation cost for admittance. Reprinted with permission from [76] (c) 2006 IEEE.	212

FIGURES

xiii

12.4	Frequency response comparison among the original circuit, PRIMA model, and MTermMOR model of the circuit <i>clktree50</i> . Reprinted with permission from [76] (c) 2006 IEEE.	213
12.5	Frequency response comparison among the original circuit, PRIMA model, and MTermMOR model of the circuit <i>sram1026</i> . Reprinted with permission from [76] (c) 2006 IEEE.	213
13.1	Transient response of a non-passive circuit.	217
13.2	Frequency responses of a reduced model and its original RC circuit.	218
13.3	Transient responses of a reduced model and its original RC circuit for a 10 GHz input.	219
13.4	Transient responses of a reduced model and its original RC circuit for a 60 GHz input.	220
13.5	Algorithm flow of FFT-IFFT-based waveform shaping.	221
13.6	Algorithm of FFT-IFFT-based waveform shaping.	222
13.7	Ramp signal shaped at different frequencies.	223
13.8	Low-pass-filter-based waveform shaping.	224
13.9	Group-delay characteristic and magnitude response for different order Bessel filters (normalized frequency).	224
13.10	Comparison of responses of different models in time domain for the first example.	227
13.11	Comparison in time domain between reduced models based on Bessel filters and ellipse filters.	228
13.12	Comparison of responses of different models in time domain for second example.	228

Tables

3.1	The Hankel singular values for a six-port linear interconnect circuit.	53
5.1	Simulation efficiency comparison between original and synthesized model (part I). Reprinted with permission from [94] (c) 2006 IEEE.	88
5.2	Simulation efficiency comparison between original and synthesized model (part-II). Reprinted with permission from [94] (c) 2006 IEEE.	90
5.3	Comparison of reduction CPU times. Reprinted with permission from [94] (c) 2006 IEEE.	90
6.1	Singular values of DC moment, input moment matrix and output moment matrix of the circuit <i>net27</i> .	101
6.2	Singular values of the DC admittance moment, 1st order admittance moment matrices of the circuit <i>net1026</i> when all the terminals are treated as bidirectional.	110
6.3	Singular values of DC admittance moment, input moment matrix and output moment matrix of the circuit <i>net1026</i> .	112
6.4	Output clustering results for the one-bit lines circuit <i>net1026</i> . Reprinted with permission from [75] (c) 2005 IEEE.	113
7.1	Table of notations. Reprinted with permission from [135] (c) 2005 IEEE.	119
7.2	Settings and results of geometrical <i>tVPEC</i> models. Reprinted with permission from [135] (c) 2005 IEEE.	130
7.3	Settings and results of numerical <i>tVPEC</i> models. Reprinted with permission from [135] (c) 2005 IEEE.	131
8.1	Time-domain waveform error of reduced models by HiPRIME, BSMOR, and TBS under the same order (number of matched moments). Reprinted with permission from [138] (c) 2006 ACM.	155

Foreword

Interconnect model reduction has emerged as one crucial operation for circuit analysis in the last decade as a result of the phenomenon of interconnect dominance of advanced VLSI technologies. Because interconnect contributes to a significant portion of the system performance, we have to take into account the coupling effects between subcircuit modules. However, the extraction of the coupling renders many small fragments of parasitics. While the values of the parasitics are small, the number of fragments is huge and this makes the accumulated effect non-negligible. If left untreated, the amount of parasitics can gobble up the memory capacity and consume long CPU time during circuit analysis.

Model reduction transforms a system into a circuit of much smaller size to approximate the behavior of the original description. Many researchers have contributed to the advancement of the techniques and demonstrated drastic reduction of the circuit sizes with satisfactory output responses in published reports. Many of these techniques have also been implemented in software tools for applications. However, it is important for the users to understand the techniques in order to use the package properly. To adopt these approaches, we need to inspect the following features.

1. Efficiency of the reduction: the complexity of the reduction algorithm determines the CPU time of the model reduction. The size of the reduced circuit affects the simulation time.

2. Reduction of both model order and terminals of circuits: reduction of terminals was investigated less in the past and combined terminal and model order reduction leads to more compact models.

3. Robustness of the algorithms: the numerical stability of the reduction algorithm ensures the robustness of the operation.

4. Structure of the reduced systems: the reduced systems may or may not preserve important characteristics like symmetry, reciprocity, etc. Those structure characteristics are important for reduction itself and for systems using the models.

5. Realizability of the reduced system: the reduced system is realizable if it is passive and we can implement it using electrical elements with positive or negative values. We can simulate a realizable system with general simulation tools. Otherwise, we need to check if the reduced system satisfies the constraints of the simulation package.

6. Passivity of the reduced circuits: the passivity ensures that the simulation

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Frontmatter

[More information](#)

outputs are bounded for bounded inputs even if the reduced circuit is combined with other passive subcircuits.

7. Error bounds: The error bounds of the output responses provide users with confidence in the results.

In this book, Professors Sheldon X.-D. Tan and Lei He presented a comprehensive description of the reduction techniques. They have provided motivations for the approaches and insights into the algorithms as active researchers in the field. I found that the treatment of the subject is innovative and the general description is pleasant to read. The book covers the contemporary results and opens windows on future research directions in the field.

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Frontmatter

[More information](#)

xviii Acknowledgments
