Advanced solid-phase crystallization for high-hole mobility (450 cm^2/Vs) Ge thin film on an insulator

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The hole mobility of the solid-phase-crystallized Ge layer is significantly improved by controlling the deposition temperature of Ge (50–200 °C) and the Ge thickness (50–500 nm) and by applying post annealing at 500 °C. The resulting hole mobility, 450 cm^2/Vs, is the highest value to date among that of semiconductor layers directly formed on glass. The mechanism of the mobility enhancement is discussed from the perspective of three carrier scattering factors: grain boundary scattering, interface scattering, and impurity scattering. The high-hole mobility Ge layer formed by the simple fabrication process will be useful for high-speed thin-film transistors.

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Ge has attracted attention as the most promising candidate for post-Si material because it has higher carrier mobility than Si and is compatible with conventional Si process. Effective mobilities in Ge metal-oxide-semiconductor field-effect-transistors (MOSFETs) have exceeded those in Si-MOSFETs thanks to the development of device technologies including gate stacks.[1–6] Ge on insulator (GOI) technology has been widely studied for lowering the fabrication cost and improving the device performance of Ge-MOSFETs. Researchers have developed many techniques for GOIs, such as mechanical transfer,[7] oxidation-induced condensation,[8–10] epitaxial growth on Si on insulator,[11,12] and rapid-melting growth.[13–16] Although these techniques are attractive for achieving high quality GOIs, the direct low-temperature formation (< 600 °C) of Ge on arbitrary substrates is desired for lowering the process costs and expanding the device application. Polycrystalline Ge (poly-Ge) thin films have been directly formed on glass or plastic substrates at low temperatures using solid-phase crystallization (SPC),[17–22] laser annealing,[23–26] chemical vapor deposition,[27,28] flash lamp annealing,[29] and metal-induced crystallization.[30–34] The performance of the Ge thin film transistors (TFTs), however, has been no match for that of Si-MOSFETs.[20,21,26,29,34] This is attributed to the fact that the carrier mobilities of the Ge layers are still low (≤ 200 cm^2/Vs). In addition, the Ge layers are highly p-doped (> 10^{17} cm^{-3}) because of point defects generating holes,[35] which restricts device application. To further improve Ge-TFTs, one needs to study not only device technology but also crystallization techniques.

Toko *et al*. reported that post annealing (PA) at 500 °C is effective to reduce the point defects and then the hole concentration of SPC-Ge,[17] which allows for the hole mobility of 140 cm^2/Vs. On the other hand, Sadoh *et al*. reported that a thicker film allows for the higher hole mobility in SPC-GeSn.[36] Very recently, we improved the hole mobility of SPC-Ge from 140 cm^2/Vs to 340 cm^2/Vs by preparing an amorphous Ge (a-Ge) precursor with heating the substrate.[37] This hole mobility was the highest ever recorded for a thin film formed on

45 insulators at temperatures below the melting point of Ge (937 °C). In this study, we investigated
46 the effects of both film thickness and PA on the SPC-Ge and broke the record with a hole
47 mobility of 450 cm^2/Vs. The process temperature was 500 °C, making it possible to fabricate
48 devices on glass substrates.

49 In the experiment, the Ge precursors were deposited on SiO_2 glass substrates using the
50 Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The
51 deposition rate was 1.0 nm/min where the sample substrate was not heated. The thickness of
52 the a-Ge layer, t, ranged from 50 to 500 nm. The substrate temperature during the deposition,
53 T_d, ranged from 50 to 200 °C. We note that T_d spontaneously rises from room temperature to
54 50 °C without heating the substrate because of the heat radiation from the Knudsen cell. The
55 samples were then loaded into a conventional tube furnace in a N_2 (99.9%) atmosphere and
56 annealed at 450 °C for 5 h to induce SPC. After that, we performed PA at 500 °C for 5 h to
57 enhance the electrical properties. To avoid sublimation of Ge by reaction with oxygen,[17] PA
58 was performed in a lamp heating furnace in a high-purity Ar (99.9999%) atmosphere.

59 The as-deposited Ge layers, precursors for SPC, were evaluated using X-ray reflectivity
60 (XRR) and Raman spectroscopy (spot size 20 µm, wavelength 532 nm). Figure 1(a) shows that
61 the relationship between the film density of the precursor and T_d is different for different t. This
62 behavior can be explained as follows. As the migration of Ge atoms reaching the substrate
63 becomes more active, the film density increases and approaches the crystal. Since Ge is difficult
64 to adhere to SiO_2,[28] migration is active on the SiO_2 substrate. In contrast, because Ge easily
65 adhere to each other, migration is not active on the Ge film. Reflecting these phenomena, the
66 film density becomes higher as the film becomes thinner for T_d = 50 °C (Fig. 1(a)). The higher
67 T_d, the more the migration is promoted and the film density approaches the crystal, as seen for
68 t = 100 and 200 nm. Meanwhile, for t = 50 nm, the film density does not approach that of
69 crystalline Ge. This behavior is not completely understood, but possibly due to residual strain

70 in a thin film. In the case of the a-Ge film on a SiO_2 substrate, the tensile strain due to the film
71 formation is more remarkable in the thinner film.[38,39] We speculate that the effect of tensile
72 strain is dominant for t = 50 nm, resulting in a constant density with respect to T_d. Figure 1(b)
73 shows broad peaks near 275 cm^{-1} corresponding to a-Ge, while Fig. 1(c) shows the sharp peaks
74 near 300 cm^{-1} corresponding to crystalline Ge for all samples. These results indicate that the
75 crystalline Ge nuclei start to form in the a-Ge layer for $T_d > 150$ °C.

76 After annealing for SPC, the grown Ge layers were evaluated using electron
77 backscattering diffraction (EBSD) analysis. The EBSD images in Fig. 2(a) show that the grains
78 are randomly oriented and the grain size strongly depends on both T_d and t. Figure 2(b) shows
79 that there are optimum values for both T_d and t. For each t, the grain size expands with the
80 increase of T_d, then turns to shrink. As a result, the grain size reaches the highest value at around
81 $100 \leq T_d \leq 150$ °C. The behavior at $T_d \geq 150$ °C can be explained by nucleation during
82 deposition of the precursor.[37] On the other hand, the cause of the behavior at $T_d \leq 100$ °C is not
83 yet clear, but the process of nucleation and growth may depend on the atomic density of the a-
84 Ge precursor. In order to verify the speculation, further studies to quantitatively determine the
85 activation energies and frequency factors for nucleation and growth are strongly needed. For t
86 = 50 nm, the grain size is relatively low over the whole T_d. For $t \geq 100$ nm, the T_d for achieving
87 the maximum grain size value shifted to higher T_d with thicker t. Assuming that the grain size
88 depends on the precursor density, these behaviors are consistent with the results in Fig. 1(a).
89 For $t \geq 100$ nm, the grain size became smaller with increasing t. This result likely reflects the
90 increase of bulk nucleation with the increasing t.[36,40] As a result of these phenomena, the
91 maximum grain size value is 3.8 μm for the sample with T_d = 100 °C and t = 100 nm.

92 The electrical properties of the SPC-Ge layers before PA were evaluated using Hall effect
93 measurements. All samples showed p-type conduction, similar to conventional non-doped poly-
94 Ge.[17,27,29,34] This is because point defects in Ge provide shallow acceptor levels and then

95 generate holes at room temperature.[35] There are three possible locations of point defects: the
96 interface between Ge and SiO_2, Ge grain boundaries, and within Ge grains. Figure 3(a) shows
97 that hole concentration decreases with increasing t for T_d = 50 °C. This behavior is the same as
98 the previous study on the SPC of GeSn[36] and considered to arise from point defects located at
99 the interface between Ge and SiO_2. For t = 50 and 100 nm, the hole concentrations are reduced
100 for T_d > 50 °C. These make the t dependence of the hole concentration small for T_d > 50 °C.
101 These behaviors suggest that the point defects located at the interface between Ge and SiO_2 are
102 reduced by the heating deposition of the precursor. For T_d > 50 °C, the hole concentration
103 increases as T_d increases for each t. This behavior can be explained from the perspective of the
104 point defects located at grain boundaries and within grains. Since the grain boundary decreases
105 as the grain size increases, point defects due to grain boundaries decrease. Reflecting the change
106 in grain size with respect to T_d (Fig. 2(b)), point defects due to grain boundaries are the lowest
107 at around T_d = 125 °C. On the other hand, in crystal growth, as the growth rate increases,
108 vacancies are more easily taken into the grain. Since the growth rate increases with increasing
109 T_d,[37] higher T_d likely provides more vacancies in the Ge grains. As a result of the balance
110 between the defects in the grain boundary and grain, the hole concentration behaves as shown
111 in Fig. 3(a) with respect to T_d (> 50 °C).

112 Figure 3(b) shows that the hole mobility of the SPC-Ge layer strongly depends on T_d,
113 except t = 50 nm. For $t \geq 100$ nm, the high hole mobilities (> 250 cm^2/Vs) at the high-density
114 amorphous regime (100 ≤ T_d ≤ 150 °C) are attributed to both the large grain size and low
115 potential barrier height of grain boundaries.[37] The thicker t tends to provide the higher hole
116 mobility despite the grain becoming smaller (Fig. 2(b)). These results suggest that the higher
117 hole mobility with the thicker Ge layer arises from the reduction of the interface scattering. The
118 highest hole mobility of the SPC-Ge layer before PA is 380 cm^2/Vs obtained for T_d = 150 °C
119 and t = 300 nm. For this sample, the limiting factors of hole mobility were discussed as follows.

120 From the Matthiessen's rule, the hole mobility of the Ge layer μ (= 380 cm^2/Vs) is expressed
121 by the following equation:

$$\frac{1}{\mu}=\frac{1}{\mu_{\mathrm{P}}}+\frac{1}{\mu_{\mathrm{I}}}+\frac{1}{\mu_{\mathrm{others}}}\ , \quad (1)$$

122
123
124 where μ_{P}, μ_{I}, and μ_{others} are the hole mobilities limited by phonon scattering, impurity scattering,
125 and the other scattering factors, respectively. According to the Irvin's curve,[41] μ_{P} and μ_{I} are
126 determined to be 1900 cm^2/Vs and 770 cm^2/Vs, respectively. Therefore, from the equation (1),
127 μ_{others} is determined to be 1230 cm^2/Vs. These results indicate that the hole mobility in this
128 sample is dominantly limited by impurity scattering. Therefore, the reduction of the hole
129 concertation is necessary to further improve the hole mobility.

130 PA was performed for the samples of the highest hole mobility with each t. Figure 4(a)
131 shows that the hole concentration decreases by approximately 30% for all samples. This result
132 suggests that Ge atoms migrated by thermal diffusion and passivated point defects, generating
133 holes, in the Ge layers. Figure 4(b) shows that the hole mobility increases for all samples. The
134 improvement of the hole mobility is up to 100 cm^2/Vs, though the improvement rate is relatively
135 small for t = 50 nm. The effect of PA on the electrical properties of 50-nm-thick SPC-Ge agrees
136 with the previous study.[17] Considering the Irvin's curve and the equation (1), the hole mobility
137 for t = 50 nm is limited by grain boundary and/or interface scattering, whereas it is dominantly
138 limited by impurity scattering for t > 50 nm. These facts account for the t dependence of the PA
139 effect (Fig. 4(b)). Thus, the reduction of the hole concentration by PA led to the hole mobility
140 of as high as 450 cm^2/Vs for t = 400 nm. This Ge layer will be suitable for application to
141 junctionless type multiple gate FETs including FinFETs.[6,29]

142 In conclusion, we further improved the hole mobility of the SPC-Ge layer by controlling
143 T_{d} (50–200 °C) and t (50–500 nm) and applying PA (500 °C, 5 h). The resulting hole mobility,
144 450 cm^2/Vs, is the highest value to date among that of semiconductor layers directly formed on

145 glass. This achievement is likely attributed to the reduction of the carrier scattering factors: (i)
146 the interface scattering was reduced by thickening SPC-Ge; (ii) the impurity scattering was
147 reduced by PA passivating vacancy defects. These results open up the possibility for developing
148 high-speed complimentary metal-oxide-semiconductor transistors leading to advanced system-
149 in-displays and three-dimensional integrated circuits.

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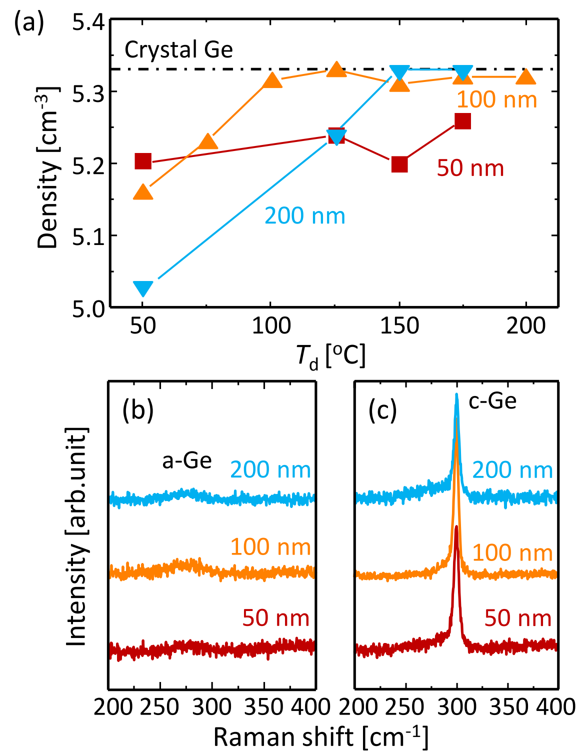

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221 **FIG. 1.** Characteristics of the as-deposited Ge layers before SPC obtained by XRR and Raman

222 measurement. (a) Density of precursor Ge as a function of T_d for t = 50, 100, and 200 nm. The

223 data for crystalline Ge are shown by the dotted line. (b),(c) Raman spectra for the samples with

224 T_d = (b) 150 °C and (c) 200 °C.

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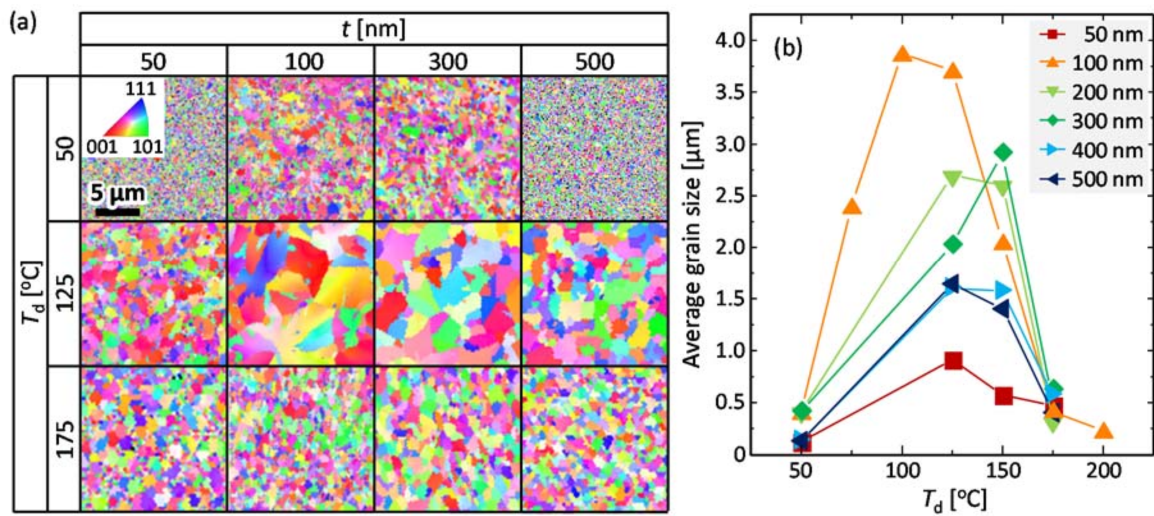

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234 **FIG. 2.** Grain size of the SPC-Ge layers. (a) EBSD images of SPC-Ge summarized as the

235 matrix composed of T_d (50, 125, and 175 °C) and t (50, 100, 300, and 500 nm). The colors

236 indicate the crystal orientation, according to the inserted color key. (b) T_d dependence of the

237 average grain size calculated from the EBSD images for t = 50–500 nm.

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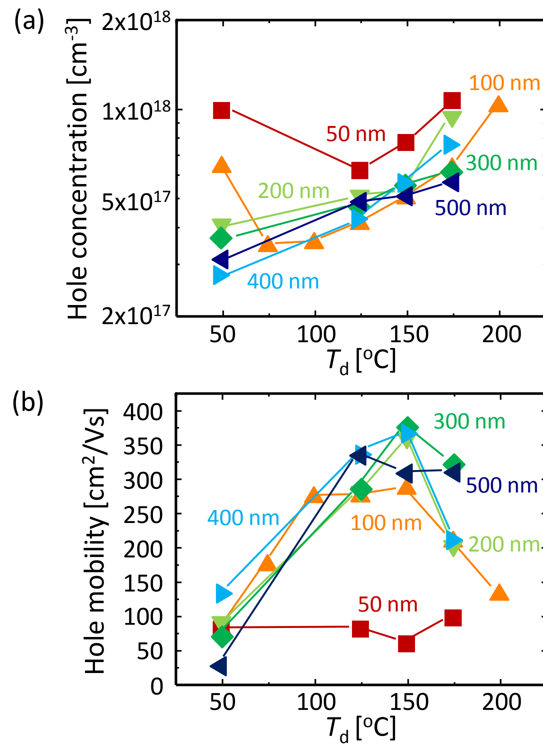

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245 **FIG. 3.** Electrical properties of the SPC-Ge layers before PA for t = 50–500 nm, obtained by

246 Hall effect measurement with the van der Pauw method. (a) Hole mobility and (b) hole

247 concentration as a function of T_d.

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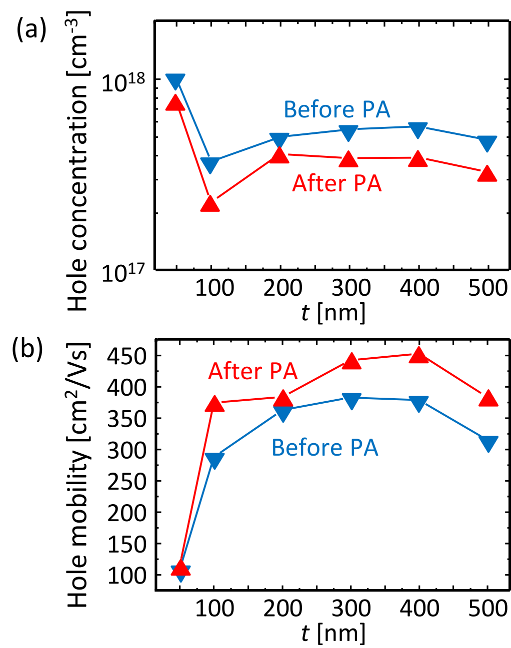

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259 **FIG. 4.** Electrical properties of the SPC-Ge layers for t = 50–500 nm before and after PA at

260 500 °C for 5 h. (a) Hole mobility and (b) hole concentration as a function of t.